



**THE DATASHEET OF  
9DBL0841BKILFT**



## Description

The 9DBL02x2/9DBL04x2/ 9DBL06x1/9DBL08x1 buffers are low-power, high-performance members of Renesas' full featured PCIe family. The buffers support PCIe Gen1 through Gen5.

## PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

## Typical Applications

- PCIe Riser Cards
- nVME Storage
- Networking
- Accelerators
- Industrial Control/Embedded

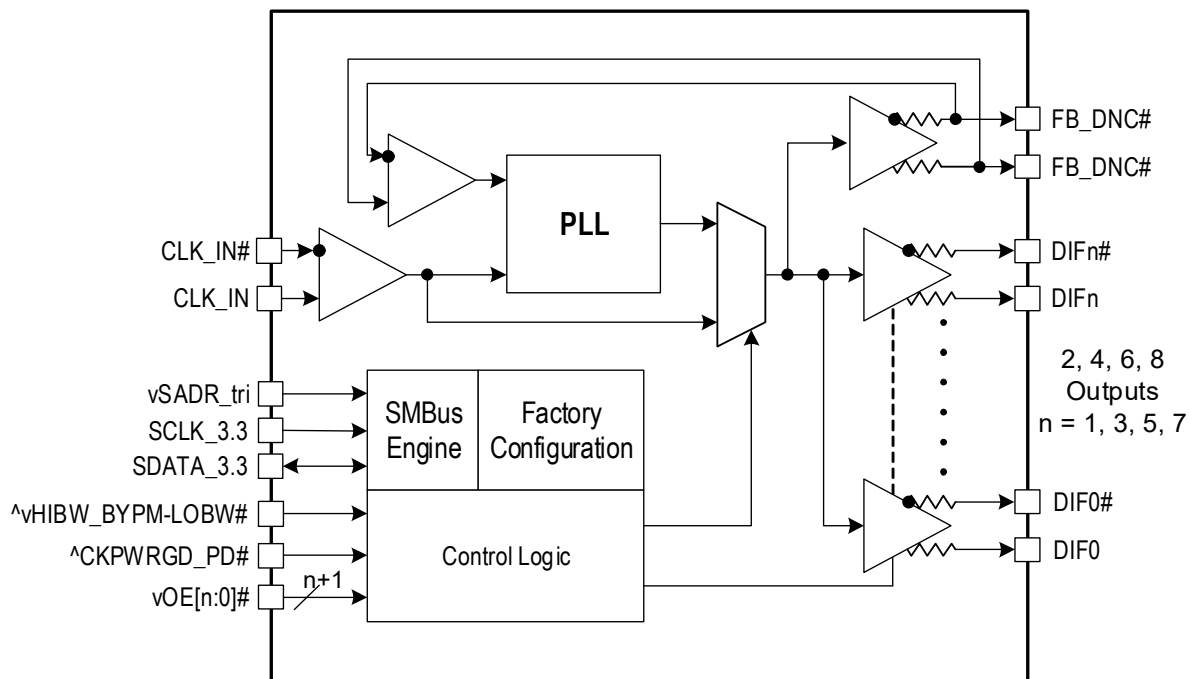
## Key Specifications

- Additive PCIe Gen5 CC jitter < 60fs RMS (fan-out mode)
- PCIe Gen5 CC jitter < 150fs RMS (High-BW ZDB Mode)

## Features

- 2 to 8 Low-Power HCSSL (LP-HCSSL) outputs eliminate 4 resistors per output pair
- 9DBLxx4x devices provide integrated 100Ω terminations
- 9DBLxx5x devices provide integrated 85Ω terminations
- See [AN-891](#) for easy coupling to other logic families
- Spread-spectrum compatible
- Dedicated OE# pin for each output
- 1MHz to 200MHz operation in fan-out mode
- 3 selectable SMBus addresses
- Extensive SMBus-selectable features allow optimization to customer requirements
- SMBus interface not required for device operation
- -40°C to +85°C operating temperature range
- Space-saving 4 × 4 mm 24-VFQFPN to 6 × 6 mm 48-VFQFPN packages (see [Ordering Information](#) table for details)

## Block Diagram



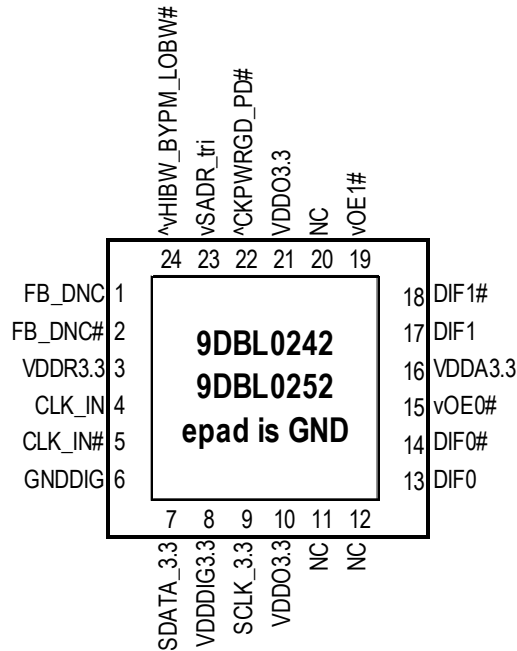
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## Pin Assignments

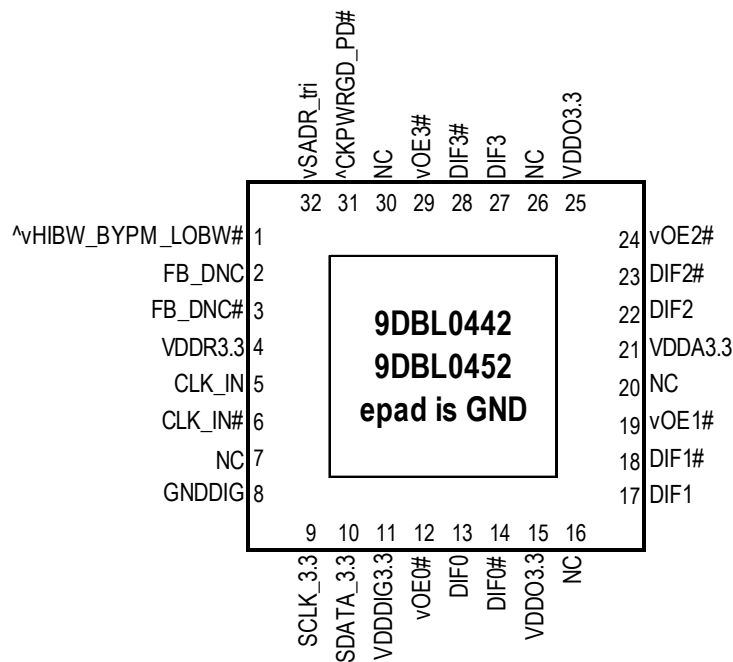
### 9DBL02x2 Pin Assignment

Figure 1. Pin Assignment for 4 × 4 mm 24-VFQFPN Package – Top View



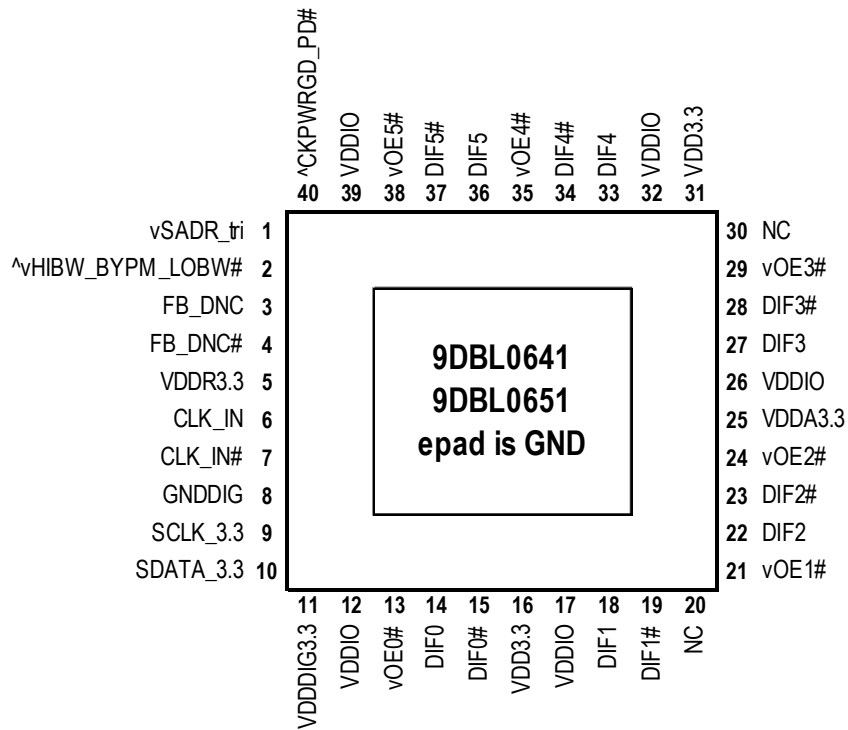
### 9DBL04x2 Pin Assignment

Figure 2. Pin Assignment for 5 × 5 mm 32-VFQFPN Package – Top View



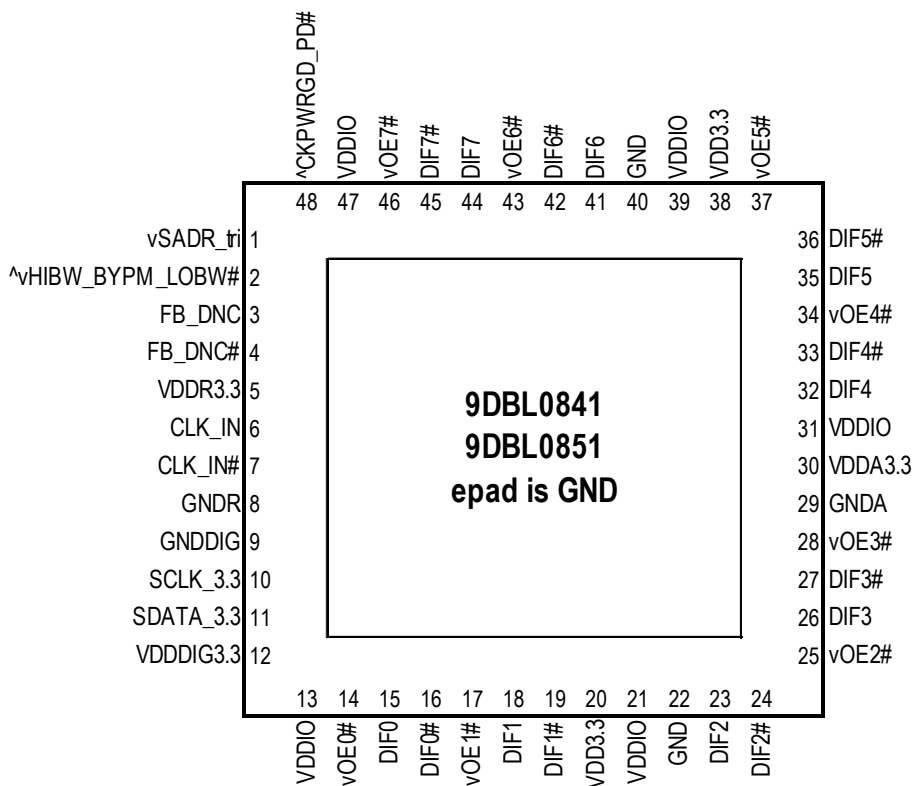
### 9DBL06x1 Pin Assignment

Figure 3. Pin Assignment for 5 × 5 mm 40-VFQFPN Package – Top View



### 9DBL08x1 Pin Assignment

Figure 4. Pin Assignment for 6 × 6 mm 48-VFQFPN Package – Top View



## Pin Descriptions

**Table 1. Pin Descriptions**

| Pin Name [a] [b] [c] | Type       | Description   | 08x1 Pin No. | 06x1 Pin No. | 04x2 Pin No. | 02x2 Pin No. |
|----------------------|------------|---|--------------|--------------|--------------|--------------|
| ^CKPWRGD_PD#         | Input      | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kΩ pull-up resistor. | 48           | 40           | 31           | 22           |
| ^vHIBW_BYPM_LOBW#    | Latched In | Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull-up/pull-down resistors.  | 2            | 2            | 1            | 24           |
| CLK_IN               | Input      | True input of differential input clock.   | 6            | 6            | 5            | 4            |
| CLK_IN#              | Input      | Complementary input if differential input clock.  | 7            | 7            | 6            | 5            |
| DIF0                 | Output     | Differential true clock output.   | 15           | 14           | 13           | 13           |
| DIF0#                | Output     | Differential complementary clock output.  | 16           | 15           | 14           | 14           |
| DIF1                 | Output     | Differential true clock output.   | 18           | 18           | 17           | 17           |
| DIF1#                | Output     | Differential complementary clock output.  | 19           | 19           | 18           | 18           |
| DIF2                 | Output     | Differential true clock output.   | 23           | 22           | 22           | –            |
| DIF2#                | Output     | Differential complementary clock output.  | 24           | 23           | 23           | –            |
| DIF3                 | Output     | Differential true clock output.   | 26           | 27           | 27           | –            |
| DIF3#                | Output     | Differential complementary clock output.  | 27           | 28           | 28           | –            |
| DIF4                 | Output     | Differential true clock output.   | 32           | 33           | –            | –            |
| DIF4#                | Output     | Differential complementary clock output.  | 33           | 34           | –            | –            |
| DIF5                 | Output     | Differential true clock output.   | 35           | 36           | –            | –            |
| DIF5#                | Output     | Differential complementary clock output.  | 36           | 37           | –            | –            |
| DIF6                 | Output     | Differential true clock output.   | 41           | –            | –            | –            |
| DIF6#                | Output     | Differential complementary clock output.  | 42           | –            | –            | –            |
| DIF7                 | Output     | Differential true clock output.   | 44           | –            | –            | –            |
| DIF7#                | Output     | Differential complementary clock output.  | 45           | –            | –            | –            |
| EPAD                 | GND        | Connect to ground.  | 49           | 41           | 33           | 25           |
| FB_DNC               | DNC        | True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.  | 3            | 3            | 2            | 1            |
| FB_DNC#              | DNC        | Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.  | 4            | 4            | 3            | 2            |
| GND                  | GND        | Ground pin.   | 22, 40       | –            | –            | –            |
| GND A                | GND        | Ground pin for the PLL core.  | 29           | –            | –            | –            |

**Table 1. Pin Descriptions (Cont.)**

| Pin Name [a] [b] [c] | Type  | Description  | 08x1 Pin No.       | 06x1 Pin No.       | 04x2 Pin No.      | 02x2 Pin No. |
|----------------------|-------|--|--------------------|--------------------|-------------------|--------------|
| GNDDIG               | GND   | Ground pin for digital circuitry.  | 9                  | 8                  | 8                 | 6            |
| GNDR                 | GND   | Analog ground pin for the differential input (receiver).   | 8                  | –                  | –                 | –            |
| NC                   | –     | No connection.   | –                  | 20, 30             | 7, 16, 20, 26, 30 | 11, 12, 20   |
| SCLK_3.3             | Input | Clock pin of SMBus circuitry, 3.3V tolerant.   | 10                 | 9                  | 9                 | 9            |
| SDATA_3.3            | I/O   | Data pin for SMBus circuitry, 3.3V tolerant.   | 11                 | 10                 | 10                | 7            |
| VDD3.3               | Power | Power supply, nominal 3.3V.  | 20, 38             | 16, 31             | –                 | –            |
| VDDA3.3              | Power | 3.3V power for the PLL core.   | 30                 | 25                 | 21                | 16           |
| VDDDIG3.3            | Power | 3.3V digital power (dirty power).  | 12                 | 11                 | 11                | 8            |
| VDDIO                | Power | Power supply for differential outputs.   | 13, 21, 31, 39, 47 | 12, 17, 26, 32, 39 | –                 | –            |
| VDDO3.3              | Power | Power supply for outputs. Nominally 3.3V.  | –                  | –                  | 15, 25            | 10, 21       |
| VDDR3.3              | Power | 3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. | 5                  | 5                  | 4                 | 3            |
| vOE0#                | Input | Active low input for enabling output 0. This pin has an internal 120kohm pull-down.<br>1 =disable outputs, 0 = enable outputs      | 14                 | 13                 | 12                | 15           |
| vOE1#                | Input | Active low input for enabling output 1. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs        | 17                 | 21                 | 19                | 19           |
| vOE2#                | Input | Active low input for enabling output 2. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs        | 25                 | 24                 | 24                | –            |
| vOE3#                | Input | Active low input for enabling output 3. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs        | 28                 | 29                 | 29                | –            |
| vOE4#                | Input | Active low input for enabling output 4. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs        | 34                 | 35                 | –                 | –            |
| vOE5#                | Input | Active low input for enabling output 5. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs        | 37                 | 38                 | –                 | –            |

**Table 1. Pin Descriptions (Cont.)**

| Pin Name [a] [b] [c] | Type       | Description  | 08x1 Pin No. | 06x1 Pin No. | 04x2 Pin No. | 02x2 Pin No. |
|----------------------|------------|--|--------------|--------------|--------------|--------------|
| vOE6#                | Input      | Active low input for enabling output 6. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs            | 43           | –            | –            | –            |
| vOE7#                | Input      | Active low input for enabling output 7. This pin has an internal 120kΩ pull-down.<br>1 =disable outputs, 0 = enable outputs            | 46           | –            | –            | –            |
| vSADR_tri            | Latched In | Tri-level latch to select SMBus Address. It has an internal pull-down resistor. See the <a href="#">SMBus Address Selection</a> table. | 1            | 1            | 32           | 23           |

[a] A ‘^’ prefix indicates internal 120kΩ pull-up resistor.

[b] A ‘^v’ prefix indicates internal 120kΩ pull-up and pull-down resistor (biased to VDD/2).

[c] A ‘v’ prefix indicates internal 120kΩ pull-down resistor.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBL02x2/9DBL04x2/ 9DBL06x1/9DBL08x1. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

**Table 2. Absolute Maximum Ratings<sup>[a]</sup>**

| Symbol             | Parameter                     | Conditions  | Minimum | Typical | Maximum               | Units |
|--------------------|-------------------------------|---|---------|---------|-----------------------|-------|
| V <sub>DDx</sub>   | Supply Voltage <sup>[b]</sup> | Applies to V <sub>DD</sub> , V <sub>DDA</sub> and V <sub>DDIO</sub> . | -0.5    |         | 3.9                   | V     |
| V <sub>IN</sub>    | Input Voltage <sup>[c]</sup>  |   | -0.5    |         | V <sub>DD</sub> + 0.5 | V     |
| V <sub>IHSMB</sub> | Input High Voltage, SMBus     | SMBus clock and data pins.  |         |         | 3.9                   | V     |
| T <sub>s</sub>     | Storage Temperature           |   | -65     |         | 150                   | °C    |
| T <sub>j</sub>     | Junction Temperature          |   |         |         | 125                   | °C    |
| ESD prot           | Input ESD Protection          | Human Body Model.   | 2000    |         |                       | V     |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] Operation under these conditions is neither implied nor guaranteed.

[c] Not to exceed 3.9V.

## Electrical Characteristics

**Table 3. Additive PCIe Phase Jitter (Fan-out Buffer Mode) [a] [b]**

| Symbol               | Parameter   | Conditions  | Minimum | Typical | Maximum | Industry Limit | Units         |
|----------------------|---|---|---------|---------|---------|----------------|---------------|
| $t_{jphPCIeG1-CC}$   | Additive PCIe Phase Jitter<br>(Common Clocked Architecture) | PCIe Gen1 (2.5 GT/s)<br>SSC $\leq$ -0.5%          | –       | 2.6     | 5.0     | 86             | ps<br>(pk-pk) |
| $t_{jphPCIeG2-CC}$   |   | PCIe Gen2 Hi Band (5.0 GT/s)<br>SSC $\leq$ -0.5%  | –       | 0.357   | 0.428   | 3.1            | ps<br>(RMS)   |
|                      |   | PCIe Gen2 Lo Band (5.0 GT/s)<br>SSC $\leq$ -0.5%  | –       | 0.023   | 0.033   | 3              | ps<br>(RMS)   |
| $t_{jphPCIeG3-CC}$   |   | PCIe Gen3 (8.0 GT/s)<br>SSC $\leq$ -0.5%          | –       | 0.091   | 0.149   | 1              | ps<br>(RMS)   |
| $t_{jphPCIeG4-CC}$   |   | PCIe Gen4 (16.0 GT/s) [c] [d]<br>SSC $\leq$ -0.5% | –       | 0.092   | 0.156   | 0.5            | ps<br>(RMS)   |
| $t_{jphPCIeG5-CC}$   |   | PCIe Gen5 (32.0 GT/s) [c] [e]<br>SSC $\leq$ -0.5% | –       | 0.031   | 0.059   | 0.15           | ps<br>(RMS)   |
| $t_{jphPCIeG1-SRIS}$ | Additive PCIe Phase Jitter<br>(SRIS Architecture) [f]       | PCIe Gen1 (2.5 GT/s)<br>SSC $\leq$ -0.3%          | –       | N/A     | N/A     | N/A            | ps<br>(pk-pk) |
| $t_{jphPCIeG2-SRIS}$ |   | PCIe Gen2 Band (5.0 GT/s)<br>SSC $\leq$ -0.3%     | –       | 0.455   | 0.524   | N/A            | ps<br>(RMS)   |
| $t_{jphPCIeG3-SRIS}$ |   | PCIe Gen3 (8.0 GT/s)<br>SSC $\leq$ -0.3%          | –       | 0.131   | 0.150   | N/A            | ps<br>(RMS)   |
| $t_{jphPCIeG4-SRIS}$ |   | PCIe Gen4 (16.0 GT/s) [c] [d]<br>SSC $\leq$ -0.3% | –       | 0.111   | 0.128   | N/A            | ps<br>(RMS)   |
| $t_{jphPCIeG5-SRIS}$ |   | PCIe Gen5 (32.0 GT/s) [c] [e]<br>SSC $\leq$ -0.3% | –       | 0.040   | 0.045   | N/A            | ps<br>(RMS)   |

**Table 4. PCIe Phase Jitter (Zero-Delay Buffer Mode)<sup>[a] [b]</sup>**

| Symbol               | Parameter   | Conditions   | Minimum | Typical | Maximum | Industry Limit | Units         |
|----------------------|---|--|---------|---------|---------|----------------|---------------|
| $t_{jphPCleG1-CC}$   | PCIe Phase Jitter<br>(Common Clocked<br>Architecture)   | PCIe Gen1 (2.5 GT/s), SSC $\leq$ -0.5%<br>Any BW ZDB Mode                        | –       | 23      | 33      | 86             | ps<br>(pk-pk) |
| $t_{jphPCleG2-CC}$   |   | PCIe Gen2 Hi Band (5.0 GT/s),<br>SSC $\leq$ -0.5%, Any BW ZDB Mode               | –       | 1.4     | 1.9     | 3.1            | ps<br>(RMS)   |
| $t_{jphPCleG3-CC}$   |   | PCIe Gen2 Lo Band (5.0 GT/s),<br>SSC $\leq$ -0.5%, Any BW ZDB Mode               | –       | 0.5     | 0.81    | 3              | ps<br>(RMS)   |
| $t_{jphPCleG4-CC}$   |   | PCIe Gen3 (8.0 GT/s),<br>SSC $\leq$ -0.5%, High BW ZDB Mode                      | –       | 0.28    | 0.53    | 1              | ps<br>(RMS)   |
| $t_{jphPCleG5-CC}$   |   | PCIe Gen4 (16.0 GT/s) <sup>[c] [d]</sup><br>SSC $\leq$ -0.5%, High BW ZDB Mode   | –       | 0.26    | 0.48    | 0.5            | ps<br>(RMS)   |
| $t_{jphPCleG5-CC}$   |   | PCIe Gen5 (32.0 GT/s) <sup>[c] [e]</sup> ,<br>SSC $\leq$ -0.5%, High BW ZDB Mode | –       | 0.07    | 0.149   | 0.15           | ps<br>(RMS)   |
| $t_{jphPCleG1-SRIS}$ | PCIe Phase Jitter<br>(SRIS Architecture) <sup>[f]</sup> | PCIe Gen1 (2.5 GT/s), SSC $\leq$ -0.5%<br>High BW ZDB Mode                       | –       | N/A     | N/A     | N/A            | ps<br>(pk-pk) |
| $t_{jphPCleG2-SRIS}$ |   | PCIe Gen2 (5.0 GT/s), SSC $\leq$ -0.5%<br>High BW ZDB Mode                       | –       | 0.99    | 1.23    | N/A            | ps<br>(RMS)   |
| $t_{jphPCleG3-SRIS}$ |   | PCIe Gen3 (8.0 GT/s), SSC $\leq$ -0.5%<br>High BW ZDB Mode                       | –       | 0.61    | 0.69    | N/A            | ps<br>(RMS)   |

[a] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. Jitter may be subtracted from the limit using RSS subtraction to determine remaining margin. Guaranteed by design and characterization, not 100% tested in production.

[b] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

[c] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[d] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[e] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[f] While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the N/A in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by  $\sqrt{2}$ . It is up to the user to divide the clock output budget or the clock input budget by  $\sqrt{2}$  to arrive at a target limit.

**Table 5. 12kHz to 20MHz Phase Jitter [a] [b]**

| Symbol              | Parameter                          | Conditions                 | Minimum | Typical | Maximum | Units    |
|---------------------|------------------------------------|----------------------------|---------|---------|---------|----------|
| $t_{jph156M12k-20}$ | Additive Phase Jitter, Fanout Mode | 156.25MHz, 12kHz to 20MHz. | –       | 363     | –       | fs (rms) |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] Additive jitter is calculated using Root-Sum-Square (RSS) subtraction.

**Table 6. Clock Input Parameters**

| Symbol      | Parameter                         | Conditions                           | Minimum | Typical | Maximum | Units   |
|-------------|-----------------------------------|--------------------------------------|---------|---------|---------|---------|
| $V_{CROSS}$ | Input Crossover Voltage [a]       | Crossover voltage.                   | 150     | –       | 900     | mV      |
| $V_{SWING}$ | Input Swing [a]                   | Differential value.                  | 300     | –       |         | mV      |
| $dv/dt$     | Input Slew Rate [a] [b]           | Measured differentially.             | 0.4     | –       | 8       | V/ns    |
| $I_{IN}$    | Input Leakage Current             | $V_{IN} = V_{DD}$ , $V_{IN} = GND$ . | -5      | –       | 5       | $\mu A$ |
| $d_{tin}$   | Input Duty Cycle [a]              | Differential measurement.            | 45      | –       | 55      | %       |
| $J_{DIFIn}$ | Input Jitter – Cycle to Cycle [a] |                                      | 0       | –       | 125     | ps      |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] Slew rate measured through  $\pm 75mV$  window centered around differential zero.

**Table 7. Output Duty Cycle, Skew and PLL Characteristics [a]**

| Symbol          | Parameter                     | Conditions                            | Minimum | Typical | Maximum | Units |
|-----------------|-------------------------------|---------------------------------------|---------|---------|---------|-------|
| BW              | PLL BW [b]                    | -3dB point in High BW Mode (100MHz).  | 2       | 3.3     | 4       | MHz   |
|                 |                               | -3dB point in Low BW Mode (100MHz).   | 1       | 1.5     | 2       | MHz   |
| $t_{JPEAK}$     | PLL Jitter Peaking            | Peak Pass band gain (100MHz).         |         | 0.8     | 2       | dB    |
| $t_{DC}$        | Duty Cycle [c]                | Measured differentially, PLL Mode.    | 45      | 50      | 55      | %     |
| $t_{DCD}$       | Duty Cycle Distortion [c] [d] | Measured differentially, Bypass Mode. | -1      | 0.0     | 1       | %     |
| $t_{pdBYP}$     | Skew, Input to Output [e]     | Bypass Mode, $V_T = 50\%$ .           | 2500    | 3406    | 4500    | ps    |
| $t_{pdPLL}$     |                               | PLL Mode $V_T = 50\%$ .               | -100    | 8       | 100     | ps    |
| $t_{sk3}$       | Skew, Output to Output [e]    | $V_T = 50\%$ .                        |         | 21      | 55      | ps    |
| $t_{jycyc-cyc}$ | Jitter, Cycle to Cycle        | PLL Mode.                             |         | 15      | 50      | ps    |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] The Minimum/Typical/Maximum values of each BW setting track each other, i.e., maximum low BW will never occur with minimum high BW.

[c] Measured from differential waveform.

[d] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[e] All outputs at default slew rate.

**Table 8. LP-HCSL (DIF) Output Characteristics**

| Symbol                       | Parameter  | Conditions  | Minimum | Typical | Maximum | Units |
|------------------------------|--|---|---------|---------|---------|-------|
| dV/dt                        | Slew Rate <sup>[a]</sup> <sup>[b]</sup> <sup>[c]</sup> | Scope averaging on, fast setting.   | 2       | 2.8     | 4       | V/ns  |
|                              |  | Scope averaging on, slow setting.   | 1.2     | 1.9     | 3.1     |       |
| $\Delta tR/tF$               | Rise/Fall Matching <sup>[a]</sup> <sup>[d]</sup>       | Single-ended measurement.   |         | 7       | 20      | %     |
| V <sub>HIGH</sub>            | Voltage High <sup>[e]</sup>                            | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 660     | 768     | 850     | mV    |
| V <sub>LOW</sub>             | Voltage Low <sup>[e]</sup>                             |   | -150    | -11     | 150     |       |
| V <sub>max</sub>             | Max Voltage <sup>[e]</sup>                             | Measurement on single ended signal using absolute value (scope averaging off).                        |         | 811     | 1150    |       |
| V <sub>min</sub>             | Min Voltage <sup>[e]</sup>                             |   | -300    | -49     |         |       |
| V <sub>cross_abs</sub>       | Crossing Voltage (abs) <sup>[a]</sup> <sup>[f]</sup>   | Scope averaging off.  | 250     | 357     | 550     |       |
| $\Delta$ -V <sub>cross</sub> | Crossing Voltage (var) <sup>[a]</sup> <sup>[g]</sup>   | Scope averaging off.  |         | 14      | 140     |       |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] Measured from differential waveform.

[c] Slew rate is measured through the V<sub>swing</sub> voltage range centered around differential 0V. This results in a  $\pm 150$ mV window around differential 0V.

[d] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a  $\pm 75$ mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[e] At default SMBus settings.

[f] V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[g] The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting  $\Delta$ -V<sub>cross</sub> to be smaller than V<sub>cross</sub> absolute.

**Table 9. Current Consumption – 9DBL02xx**

| Symbol               | Parameter                        | Conditions                                  | Minimum | Typical | Maximum | Units |
|----------------------|----------------------------------|---|---------|---------|---------|-------|
| I <sub>DDA</sub>     | Operating Supply Current         | VDDA, PLL Mode at 100MHz.                   | –       | 7       | 10      | mA    |
| I <sub>DDDIG</sub>   |                                  | VDDDIG, PLL Mode at 100MHz.                 | –       | 3.4     | 5       | mA    |
| I <sub>DDO+R</sub>   |                                  | VDDO+VDDR, PLL Mode, all outputs at 100MHz. | –       | 20      | 25      | mA    |
| I <sub>DDRPD</sub>   | Powerdown Current <sup>[a]</sup> | VDDA, CKPWRGD_PD# = 0.                      | –       | 0.6     | 1.0     | mA    |
| I <sub>DDDIGPD</sub> |                                  | VDDDIG, CKPWRGD_PD# = 0.                    | –       | 3.0     | 4.3     | mA    |
| I <sub>DDAOPD</sub>  |                                  | VDDO+VDDR, CKPWRGD_PD# = 0.                 | –       | 0.9     | 1.3     | mA    |

**Table 10. Current Consumption – 9DBL04xx**

| Symbol        | Parameter                        | Conditions                                  | Minimum | Typical | Maximum | Units |
|---------------|----------------------------------|---|---------|---------|---------|-------|
| $I_{DDA}$     | Operating Supply Current         | VDDA, PLL Mode at 100MHz.                   | –       | 7       | 10      | mA    |
| $I_{DDDIG}$   |                                  | VDDDIG, PLL Mode at 100MHz.                 | –       | 3.4     | 5       | mA    |
| $I_{DDO+R}$   |                                  | VDDO+VDDR, PLL Mode, all outputs at 100MHz. | –       | 30      | 37      | mA    |
| $I_{DDRPD}$   | Powerdown Current <sup>[a]</sup> | VDDA, CKPWRGD_PD# = 0.                      | –       | 0.6     | 1.0     | mA    |
| $I_{DDDIGPD}$ |                                  | VDDDIG, CKPWRGD_PD# = 0.                    | –       | 3.1     | 4.3     | mA    |
| $I_{DDAOPD}$  |                                  | VDDO+VDDR, CKPWRGD_PD# = 0.                 | –       | 0.9     | 1.3     | mA    |

**Table 11. Current Consumption – 9DBL06xx**

| Symbol       | Parameter                        | Conditions                           | Minimum | Typical | Maximum | Units |
|--------------|----------------------------------|--------------------------------------|---------|---------|---------|-------|
| $I_{DDA}$    | Operating Supply Current         | VDDA, PLL Mode, at 100MHz.           | –       | 7       | 10      | mA    |
| $I_{DD}$     |                                  | VDDx, all outputs active at 100MHz.  | –       | 17      | 22      | mA    |
| $I_{DDIO}$   |                                  | VDDIO, all outputs active at 100MHz. | –       | 20      | 25      | mA    |
| $I_{DDAPD}$  | Powerdown Current <sup>[a]</sup> | VDDA, CKPWRGD_PD# = 0.               | –       | 0.6     | 1       | mA    |
| $I_{DDPD}$   |                                  | VDDx, CKPWRGD_PD# = 0.               | –       | 3.8     | 6       | mA    |
| $I_{DDIOPD}$ |                                  | VDDIO, CKPWRGD_PD# = 0.              | –       | 0.04    | 0.10    | mA    |

**Table 12. Current Consumption – 9DBL08xx**

| Symbol       | Parameter                        | Conditions                           | Minimum | Typical | Maximum | Units |
|--------------|----------------------------------|--------------------------------------|---------|---------|---------|-------|
| $I_{DDA}$    | Operating Supply Current         | VDDA, PLL Mode, at 100MHz.           | –       | 7       | 10      | mA    |
| $I_{DD}$     |                                  | VDDx, all outputs active at 100MHz.  | –       | 22      | 32      | mA    |
| $I_{DDIO}$   |                                  | VDDIO, all outputs active at 100MHz. | –       | 35      | 45      | mA    |
| $I_{DDAPD}$  | Powerdown Current <sup>[a]</sup> | VDDA, CKPWRGD_PD# = 0.               | –       | 0.6     | 1       | mA    |
| $I_{DDPD}$   |                                  | VDDx, CKPWRGD_PD# = 0.               | –       | 4.9     | 7       | mA    |
| $I_{DDIOPD}$ |                                  | VDDIO, CKPWRGD_PD# = 0.              | –       | 0.04    | 0.10    | mA    |

[a] Input clock stopped.

**Table 13. Input/Supply/Common Parameters – Normal Operating Conditions**

| Symbol                | Parameter                            | Conditions  | Minimum  | Typical              | Maximum                | Units  |
|-----------------------|--------------------------------------|---|--|----------------------|------------------------|--------|
| VDDx                  | Supply Voltage                       | Supply voltage for core and analog.   | 3.135  | 3.3                  | 3.465                  | V      |
| VDDIO                 | Output Supply Voltage <sup>[a]</sup> | Supply voltage for Low Power HCSL outputs.  | 0.95   | 1.05-3.3             | 3.465                  | V      |
| T <sub>AMB</sub>      | Ambient Operating Temperature        | Industrial range.   | -40  | 25                   | 85                     | °C     |
| V <sub>IH</sub>       | Input High Voltage                   | Single-ended inputs, except SMBus.  | 0.75 V <sub>DDx</sub>  |                      | V <sub>DDx</sub> + 0.3 | V      |
| V <sub>IL</sub>       | Input Low Voltage                    |   | -0.3   |                      | 0.25 V <sub>DDx</sub>  | V      |
| V <sub>IHtri</sub>    | Input High Voltage                   | Single-ended tri-level inputs ('_tri' suffix).  | 0.75 V <sub>DDx</sub>  |                      | V <sub>DD</sub> + 0.3  | V      |
| V <sub>IMtri</sub>    | Input Mid Voltage                    |   | 0.4 V <sub>DDx</sub>   | 0.5 V <sub>DDx</sub> | 0.6 V <sub>DDx</sub>   | V      |
| V <sub>ILtri</sub>    | Input Low Voltage                    |   | -0.3   |                      | 0.25 V <sub>DDx</sub>  | V      |
| I <sub>IN</sub>       | Single-ended Input Current           |   | Inputs without internal pull-up/pull-down resistors<br>V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD. | -5                   |                        | 5      |
| I <sub>INP</sub>      |                                      | Inputs with internal pull-up resistors, V <sub>IN</sub> = 0V.<br>Inputs with internal pull-down resistors, V <sub>IN</sub> = VDD. | -50  |                      | 50                     | μA     |
| F <sub>IN</sub>       | Input Frequency                      | Bypass Mode.  | 1  |                      | 200                    | MHz    |
|                       |                                      | 100MHz PLL Mode.  | 60   | 100.00               | 140                    | MHz    |
|                       |                                      | 50MHz PLL Mode.   | 30   | 50.00                | 65                     | MHz    |
|                       |                                      | 125MHz PLL Mode.  | 75   | 125.00               | 175                    | MHz    |
| L <sub>pin</sub>      | Pin Inductance <sup>[b]</sup>        |   |  | 7                    | nH                     |        |
| C <sub>IN</sub>       | Capacitance <sup>[b]</sup>           | Logic Inputs, except DIF_IN.  | 1.5  |                      | 5                      | pF     |
| C <sub>INDIF_IN</sub> |                                      | DIF_IN differential clock inputs.   | 1.5  |                      | 2.7                    | pF     |
| C <sub>OUT</sub>      |                                      | Output pin capacitance.   |  |                      | 6                      | pF     |
| T <sub>STAB</sub>     | Clk Stabilization <sup>[c]</sup>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or deassertion of PD# to 1st clock.                             |  |                      | 1                      | ms     |
| f <sub>SSCMODIN</sub> | Input SS Modulation Frequency        | PCIe applications.  | 30   |                      | 33                     | kHz    |
|                       |                                      | Non-PCIe applications.  | 0  |                      | 66                     | kHz    |
| t <sub>LATOE#</sub>   | OE# Latency <sup>[b] [c]</sup>       | DIF start after OE# assertion<br>DIF stop after OE# deassertion.  | 1  |                      | 3                      | clocks |
| t <sub>DRVPD</sub>    | Tdrive_PD# <sup>[b] [d]</sup>        | DIF output enable after PD# deassertion.  |  |                      | 300                    | μs     |
| t <sub>F</sub>        | Tfall <sup>[c]</sup>                 | Fall time of single-ended control inputs.   |  |                      | 5                      | ns     |
| t <sub>R</sub>        | Trise <sup>[c]</sup>                 | Rise time of single-ended control inputs.   |  |                      | 5                      | ns     |

[a] Only present on 9DBL06xx and 9DBL08xx devices.

[b] Guaranteed by design and characterization, not 100% tested in production.

[c] Control inputs must be monotonic from 20% to 80% of input swing.

[d] Time from deassertion until outputs are > 200 mV.

**Table 14. SMBus Parameters**

| Symbol              | Parameter                                    | Conditions                            | Minimum | Typical | Maximum | Units |
|---------------------|--|---------------------------------------|---------|---------|---------|-------|
| V <sub>ILSMB</sub>  | SMBus Input Low Voltage                      | V <sub>DDSMB</sub> = 3.3V.            |         |         | 0.8     | V     |
| V <sub>IHSMB</sub>  | SMBus Input High Voltage                     | V <sub>DDSMB</sub> = 3.3V.            | 2.1     |         | 3.6     | V     |
| V <sub>OLSMB</sub>  | SMBus Output Low Voltage                     | At I <sub>PULLUP</sub> .              |         |         | 0.4     | V     |
| I <sub>PULLUP</sub> | SMBus Sink Current                           | At V <sub>OL</sub> .                  | 4       |         |         | mA    |
| V <sub>DDSMB</sub>  | Nominal Bus Voltage                          |                                       | 2.7     |         | 3.6     | V     |
| t <sub>RSMB</sub>   | SCLK/SDATA Rise Time <sup>[a]</sup>          | (Max VIL - 0.15) to (Min VIH + 0.15). |         |         | 1000    | ns    |
| t <sub>FSMB</sub>   | SCLK/SDATA Fall Time <sup>[a]</sup>          | (Min VIH + 0.15) to (Max VIL - 0.15). |         |         | 300     | ns    |
| f <sub>SMB</sub>    | SMBus Operating Frequency <sup>[b] [c]</sup> | SMBus operating frequency.            |         |         | 500     | kHz   |

[a] Guaranteed by design and characterization, not 100% tested in production.

[b] The device must be powered up for the SMBus to function.

[c] The differential input clock must be running for the SMBus to be active.

## Power Management

**Table 15. Power Management**

| CKPWRGD_PD# | CLK_IN  | SMBus OEn bit | OEn# Pin | DIFn               | DIFn#              | PLL State (ZDB Mode) |
|-------------|---------|---------------|----------|--------------------|--------------------|----------------------|
| 0           | X       | X             | X        | Low <sup>[a]</sup> | Low <sup>[a]</sup> | Off                  |
| 1           | Running | 0             | X        | Low <sup>[a]</sup> | Low <sup>[a]</sup> | On <sup>[b]</sup>    |
| 1           | Running | 1             | 0        | Running            | Running            | On <sup>[b]</sup>    |
| 1           | Running | 1             | 1        | Low <sup>[a]</sup> | Low <sup>[a]</sup> | On <sup>[b]</sup>    |

[a] The output state is set by B11[1:0] (Low/Low default).

[b] If Bypass mode is selected, the PLL will always be off.

## ZDB Operating Mode

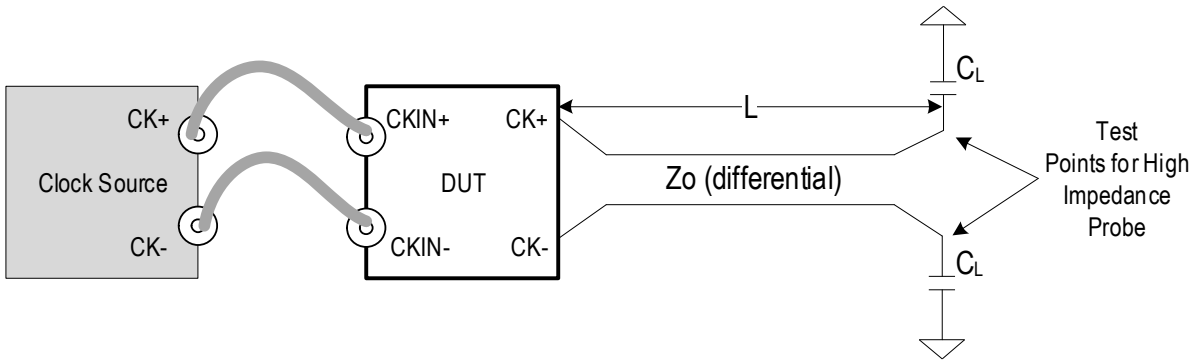
**Table 16. ZDB (PLL) Operating Mode<sup>[a]</sup>**

| HiBW_BypM_LoBW#   | Operating Mode                | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|-------------------|-------------------------------|----------------------|---------------------|
| 0                 | Low Bandwidth PLL (ZDB) Mode  | 00                   | 00                  |
| Mid-level (VDD/2) | Bypass Mode (Fanout buffer)   | 01                   | 01                  |
| 1                 | High Bandwidth PLL (ZDB) Mode | 11                   | 11                  |

[a] '10' value is reserved.

## Test Loads

**Figure 5. Test Load for AC/DC Measurements and ZDB Mode PCIe Jitter Measurements**

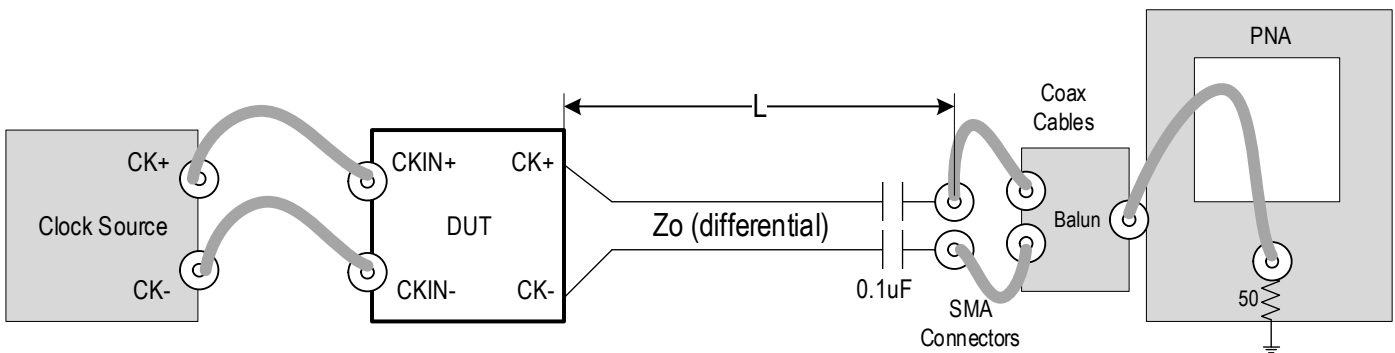


**Table 17. Parameters for Measurements Using Test Setup in Figure 5 [a]**

| Clock Source | Device Under Test (DUT) | Differential Zo ( $\Omega$ ) | L (cm) | C <sub>L</sub> (pF) | Parameters Measured  |
|--------------|-------------------------|------------------------------|--------|---------------------|----------------------|
| SMA100B      | 9DBLxx5x                | 85                           | 12.7   | 2                   | AC/DC parameters     |
| SMA100B      | 9DBLxx4x                | 100                          | 12.7   | 2                   |                      |
| 9FGL08x1C    | 9DBLxx5x                | 85                           | 12.7   | 2                   | ZDB-mode PCIe Jitter |
| 9FGL08x1C    | 9DBLxx4x                | 100                          | 12.7   | 2                   |                      |

[a] A DSO is used for all measurements in this table. Equipment noise is removed from all jitter measurements taken with this setup.

**Figure 6. Test Loads for Additive Phase Jitter Measurements**



**Table 18. Parameters for Measurements Using Test Setup in Figure 6**

| Clock Source | Device Under Test (DUT) | Differential Zo ( $\Omega$ ) | L (cm) | C <sub>L</sub> (pF) | Parameters Measured               |
|--------------|-------------------------|------------------------------|--------|---------------------|-----------------------------------|
| SMA100B      | 9DBLxx5x                | 85                           | 12.7   | 2                   | Fan-out Mode Additive PCIe Jitter |
| SMA100B      | 9DBLxx4x                | 100                          | 12.7   | 2                   |                                   |

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation |           |                          |
|-----------------------------|-----------|--------------------------|
| Controller (Host)           |           | Renesas (Slave/Receiver) |
| T                           | starT bit |                          |
| Slave Address               |           |                          |
| WR                          | WRite     |                          |
| Beginning Byte = N          |           | ACK                      |
| Data Byte Count = X         |           | ACK                      |
| Beginning Byte N            |           | ACK                      |
| O                           |           | O                        |
| O                           |           | O                        |
| O                           |           | O                        |
| Byte N + X - 1              |           | ACK                      |
| P                           | stoP bit  |                          |

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |         |
|----------------------------|-----------------|---------|
| Controller (Host)          |                 | Renesas |
| T                          | starT bit       |         |
| Slave Address              |                 |         |
| WR                         | WRite           |         |
| Beginning Byte = N         |                 | ACK     |
| Repeat starT               |                 | ACK     |
| Slave Address              |                 |         |
| RD                         | ReaD            |         |
| Data Byte Count=X          |                 | ACK     |
| Beginning Byte N           |                 | O       |
|                            |                 | O       |
|                            |                 | O       |
| Byte N + X - 1             |                 | ACK     |
| N                          | Not acknowledge |         |
| P                          | stoP bit        |         |

**Table 19. SMBus Address Selection**

| State of SADR_tri pin on first high assertion of CKPWRGD_PD# | Address <sup>[a]</sup> |
|--|------------------------|
| 0  | 1101011x               |
| M  | 1101100x               |
| 1  | 1101101x               |

[a] 'x' is the Read/Write bit.

**Table 20. Byte 0: Output Enable Control**

| Byte 0   | Bit        | 7  | 6      | 5        | 4      | 3      | 2        | 1        | 0        |
|----------|------------|--|--------|----------|--------|--------|----------|----------|----------|
|          | Function   | Output Enable  |        |          |        |        |          |          |          |
|          | Type       | RW   | RW     | RW       | RW     | RW     | RW       | RW       | RW       |
| Device   | Definition | 0 = Output is disabled <sup>[a]</sup><br>1 = OE# Pin Controls Output |        |          |        |        |          |          |          |
| 9DBL08xx | Name       | DIF7oe   | DIF6oe | DIF5oe   | DIF4oe | DIF3oe | DIF2oe   | DIF1oe   | DIF0oe   |
|          | Default    | 1  | 1      | 1        | 1      | 1      | 1        | 1        | 1        |
| 9DBL06xx | Name       | DIF5oe   | DIF4oe | Reserved | DIF3oe | DIF2oe | DIF1oe   | Reserved | DIF0oe   |
|          | Default    | 1  | 1      | -        | 1      | 1      | 1        | -        | 1        |
| 9DBL04xx | Name       | Reserved   | DIF3oe | Reserved | DIF2oe | DIF1oe | Reserved | DIF0oe   | Reserved |
|          | Default    | -  | 1      | -        | 1      | 1      | -        | 1        | -        |
| 9DBL02xx | Name       | Reserved   |        |          | DIF1oe | DIF0oe | Reserved |          |          |
|          | Default    | -  | -      | -        | 1      | 1      | -        | -        | -        |

[a] See Byte11[1:0] for disabled state.

**Table 21. Byte 1: PLL Operating Mode and Output Amplitude Control**

| Byte 1      | Bit        | 7   | 6       | 5  | 4   | 3      | 2        | 1  | 0    |
|-------------|------------|---|---------|--|---|--------|----------|--|------|
|             | Function   | PLL Mode Readback                                 |         | Enable software PLL Mode control                       | Software PLL Mode Control <sup>[a]</sup>          |        | -        | Output Amplitude                                     |      |
|             | Type       | R   | R       | RW   | RW  | RW     | -        | RW   | RW   |
|             | Definition | See <a href="#">Table 16</a> (ZDB Operating Mode) |         | 0 = B1[7:6] sets PLL Mode<br>1 = B1[4:3] sets PLL Mode | See <a href="#">Table 16</a> (ZDB Operating Mode) |        | Reserved | 00 = 0.60V<br>01 = 0.68V<br>10 = 0.75V<br>11 = 0.85V |      |
| All Devices | Name       | PLLrbk1   | PLLrbk0 | PLLmdctrl  | PLLmd1  | PLLmd0 | -        | Amp1   | Amp0 |
|             | Default    | Latch   | Latch   | 0  | 0   | 0      | 1        | 1  | 0    |

[a] B1[5] must be set to a 1 for these bits to have any effect on the part.

**Table 22. Byte 2: Slew Rate Control 0**

| Byte 2   | Bit        | 7   | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|------------|---|----------|----------|----------|----------|----------|----------|----------|
|          | Function   | Slew Rate Selection   |          |          |          |          |          |          |          |
|          | Type       | RW  | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
| Device   | Definition | 0 = Slow Setting<br>1 = Fast Setting<br>See electrical characteristics for actual slew rates. |          |          |          |          |          |          |          |
| 9DBL08xx | Name       | DIF7slew  | DIF6slew | DIF5slew | DIF4slew | DIF3slew | DIF2slew | DIF1slew | DIF0slew |
|          | Default    | 1   | 1        | 1        | 1        | 1        | 1        | 1        | 1        |
| 9DBL06xx | Name       | DIF5slew  | DIF4slew | Reserved | DIF3slew | DIF2slew | DIF1slew | Reserved | DIF0slew |
|          | Default    | 1   | 1        | –        | 1        | 1        | 1        | –        | 1        |
| 9DBL04xx | Name       | Reserved  | DIF3slew | Reserved | DIF2slew | DIF1slew | Reserved | DIF0slew | Reserved |
|          | Default    | –   | 1        | –        | 1        | 1        | –        | 1        | –        |
| 9DBL02xx | Name       | Reserved  |          |          | DIF1slew | DIF0slew | Reserved |          |          |
|          | Default    | –   | –        | –        | 1        | 1        | –        | –        | –        |

**Table 23. Byte 3: ZDB Mode Frequency Select and Feedback Slew Rate Control**

| Byte 3      | Bit        | 7        | 6 | 5   | 4   | 3     | 2        | 1 | 0                                    |
|-------------|------------|----------|---|---|---|-------|----------|---|--------------------------------------|
|             | Function   | –        | – | Enable software (SW) selection of ZDB frequency                     | ZDB Frequency Select <sup>[a]</sup>                 |       | –        | – | Feedback Slew Rate                   |
|             | Type       | –        | – | RW  | RW  | RW    | –        | – | RW                                   |
|             | Definition | Reserved |   | 0 = SW frequency select disabled<br>1 = SW frequency select enabled | 00 = 100M<br>01 = 50M<br>10 = 125M<br>11 = Reserved |       | Reserved |   | 0 = Slow Setting<br>1 = Fast Setting |
| All Devices | Name       | –        | – | FSelEn  | FSel1   | Fsel0 | –        | – | FBKslew                              |
|             | Default    | 1        | 1 | 0   | 0   | 0     | 1        | 1 | 1                                    |

[a] B3[5] must be set to a 1 for these bits to have any effect on the part.

Byte 4 is Reserved.

**Table 24. Byte 5: Revision ID/Vendor ID**

| Byte 5      | Bit      | 7            | 6    | 5    | 4    | 3          | 2    | 1    | 0    |
|-------------|----------|--------------|------|------|------|------------|------|------|------|
|             | Function | Revision ID  |      |      |      | VENDOR ID  |      |      |      |
|             | Type     | R            | R    | R    | R    | R          | R    | R    | R    |
| All Devices | Name     | RID3         | RID2 | RID1 | RID0 | VID3       | VID2 | VID1 | VID0 |
|             | Default  | B rev = 0001 |      |      |      | 0001 = IDT |      |      |      |

**Table 25. Byte 6: Device Type/Device ID**

| Byte 6      | Bit      | 7                | 6        | 5  | 4       | 3       | 2       | 1       | 0       |
|-------------|----------|------------------|----------|--|---------|---------|---------|---------|---------|
|             | Function | Device Type      |          | Device ID  |         |         |         |         |         |
|             | Type     | R                | R        | R  | R       | R       | R       | R       | R       |
| All Devices | Name     | DevType 1        | DevType0 | Dev ID5  | Dev ID4 | Dev ID3 | Dev ID2 | Dev ID1 | Dev ID0 |
|             | Default  | 01 = DBx ZDB/FOB |          | 9DBL08x1 = 0b001000<br>9DBL06x1 = 0b000110<br>9DBL04x2 = 0b000100<br>9DBL02x2 = 0b000010 |         |         |         |         |         |

**Table 26. Byte 7: Byte Count**

| Byte 7 | Bit        | 7        | 6 | 5 | 4   | 3   | 2   | 1   | 0   |
|--------|------------|----------|---|---|---|-----|-----|-----|-----|
|        | Function   | -        | - | - | Byte Count Programming  |     |     |     |     |
|        | Type       | -        | - | - | RW  | RW  | RW  | RW  | RW  |
| Device | Definition | Reserved |   |   | Writing to this register will configure how many bytes will be read back on a block read. Default is = 8 bytes. |     |     |     |     |
| All    | Name       | -        | - | - | BC4   | BC3 | BC2 | BC1 | BC0 |
|        | Default    | 0        | 0 | 0 | 0   | 1   | 0   | 0   | 0   |

Bytes 8 and 9 are reserved.

**Table 27. Byte 10: Power-Down (PD) Restore**

| Byte 10     | Bit        | 7        | 6   | 5        | 4 | 3 | 2 | 1 | 0 |
|-------------|------------|----------|---|----------|---|---|---|---|---|
|             | Function   | -        | Restore Default Config in Power Down                              | -        | - | - | - | - | - |
|             | Type       | -        | RW  | -        | - | - | - | - | - |
|             | Definition | Reserved | 0 = Clear Config. in Power Down<br>1 = Keep Config. in Power Down | Reserved |   |   |   |   |   |
| All Devices | Name       | -        | PD_Restore  | -        | - | - | - | - | - |
|             | Default    | 1        | 1   | 0        | 0 | 0 | 0 | 0 | 0 |

**Table 28. Byte 11: Impedance Control 0 and Stop State**

| Byte 11 | Bit        | 7  | 6    | 5        | 4 | 3 | 2 | 1  | 0     |
|---------|------------|--|------|----------|---|---|---|--|-------|
|         | Function   | Output Impedance -Feedback                               |      | -        | - | - | - | DIF/DIF# Disable State   |       |
|         | Type       | RW   | RW   | -        | - | - | - | RW   | RW    |
| Device  | Definition | 00 = 33ohm<br>01 = 85ohm<br>10 = 100ohm<br>11 = Reserved |      | Reserved |   |   |   | 00 = Low/Low<br>01 = HiZ/HiZ<br>10 = High/Low<br>11 = Low/High |       |
| All     | Name       | FBz1   | FBz0 | -        | - | - | - | Stop1  | Stop0 |
|         | Default    | 10 = 9DBLxx4x<br>01 = 9DBLxx5x                           |      | 0        | 0 | 0 | 0 | 0  | 0     |

**Table 29. Byte 12: Impedance Control 1**

| Byte 12  | Bit        | 7  | 6      | 5        | 4      | 3        | 2      | 1        | 0      |
|----------|------------|--|--------|----------|--------|----------|--------|----------|--------|
|          | Function   | Output Impedance                                   |        |          |        |          |        |          |        |
|          | Type       | RW   | RW     | RW       | RW     | RW       | RW     | RW       | RW     |
| Device   | Definition | 00 = 33ohm, 01 = 85ohm, 10 = 100ohm, 11 = Reserved |        |          |        |          |        |          |        |
| 9DBL08xx | Name       | DIF3z1   | DIF3z0 | DIF2z1   | DIF2z0 | DIF1z1   | DIF1z0 | DIF0z1   | DIF0z0 |
|          | Default    | 9DBL084x = 0b10101010<br>9DBL085x = 0b01010101     |        |          |        |          |        |          |        |
| 9DBL06xx | Name       | DIF2z1   | DIF2z0 | DIF1z1   | DIF1z0 | Reserved |        | DIF0z1   | DIF0z0 |
|          | Default    | 9DBL064x = 0b1010xx10<br>9DBL065x = 0b0101xx01     |        |          |        |          |        |          |        |
| 9DBL04xx | Name       | DIF1z1   | DIF1z0 | Reserved |        | DIF0z1   | DIF0z0 | Reserved |        |
|          | Default    | 9DBL044x = 0b10xx10xx<br>9DBL045x = 0b01xx01xx     |        |          |        |          |        |          |        |
| 9DBL02xx | Name       | DIF0z1   | DIF0z0 | Reserved |        |          |        |          |        |
|          | Default    | 9DBL024x = 0b10xxxxxx<br>9DBL025x = 0b01xxxxxx     |        |          |        |          |        |          |        |

**Table 30. Byte 13: Impedance Control 2**

| Byte 13  | Bit        | 7  | 6      | 5      | 4      | 3        | 2      | 1      | 0      |
|----------|------------|--|--------|--------|--------|----------|--------|--------|--------|
|          | Function   | Output Impedance                                   |        |        |        |          |        |        |        |
|          | Type       | RW   | RW     | RW     | RW     | RW       | RW     | RW     | RW     |
| Device   | Definition | 00 = 33ohm, 01 = 85ohm, 10 = 100ohm, 11 = Reserved |        |        |        |          |        |        |        |
| 9DBL08xx | Name       | DIF7z1   | DIF7z0 | DIF6z1 | DIF6z0 | DIF5z1   | DIF5z0 | DIF4z1 | DIF4z0 |
|          | Default    | 9DBL084x = 0b10101010<br>9DBL085x = 0b01010101     |        |        |        |          |        |        |        |
| 9DBL06xx | Name       | DIF5z1   | DIF5z0 | DIF4z1 | DIF4z0 | Reserved |        | DIF3z1 | DIF3z0 |
|          | Default    | 9DBL064x = 0b1010xx10<br>9DBL065x = 0b0101xx01     |        |        |        |          |        |        |        |
| 9DBL04xx | Name       | Reserved   |        | DIF3z1 | DIF3z0 | Reserved |        | DIF2z1 | DIF2z0 |
|          | Default    | 9DBL044x = 0bxx10xx10<br>9DBL045x = 0bxx01xx01     |        |        |        |          |        |        |        |
| 9DBL02xx | Name       | Reserved   |        |        |        |          |        | DIF1z1 | DIF1z0 |
|          | Default    | 9DBL024x = 0bxxxxxx10<br>9DBL025x = 0bxxxxxx01     |        |        |        |          |        |        |        |

**Table 31. Byte 14: Pull-up/Pull-down Control 0**

| Byte 14  | Bit        | 7   | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------|------------|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|          | Function   | Pull-up (PuP)/Pull-down (Pdwn) control        |           |           |           |           |           |           |           |
|          | Type       | RW  | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
| Device   | Definition | 00 = None, 01 = Pdwn, 10 = Pup, 11 = Pup+Pdwn |           |           |           |           |           |           |           |
| 9DBL08xx | Name       | OE3pu/pd1                                     | OE3pu/pd0 | OE2pu/pd1 | OE2pu/pd0 | OE1pu/pd1 | OE1pu/pd0 | OE0pu/pd1 | OE0pu/pd0 |
|          | Default    | 0   | 1         | 0         | 1         | 0         | 1         | 0         | 1         |
| 9DBL06xx | Name       | OE2pu/pd1                                     | OE2pu/pd0 | OE1pu/pd1 | OE1pu/pd0 | Reserved  |           | OE0pu/pd1 | OE0pu/pd0 |
|          | Default    | 0   | 1         | 0         | 1         | -         | -         | 0         | 1         |
| 9DBL04xx | Name       | OE1pu/pd1                                     | OE1pu/pd0 | Reserved  |           | OE0pu/pd1 | OE0pu/pd0 | Reserved  |           |
|          | Default    | 0   | 1         | -         | -         | 0         | 1         | -         | -         |
| 9DBL02xx | Name       | OE0pu/pd1                                     | OE0pu/pd0 | Reserved  |           |           |           |           |           |
|          | Default    | 0   | 1         | -         | -         | -         | -         | -         | -         |

**Table 32. Byte 15: Pull-up/Pull-down Control 1**

| Byte 15  | Bit        | 7   | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------|------------|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|          | Function   | Pull-up (PuP)/Pull-down (Pdown) control         |           |           |           |           |           |           |           |
|          | Type       | RW  | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
| Device   | Definition | 00 = None, 01 = Pdown, 10 = Pup, 11 = Pup+Pdown |           |           |           |           |           |           |           |
| 9DBL08xx | Name       | OE7pu/pd1                                       | OE7pu/pd0 | OE6pu/pd1 | OE6pu/pd0 | OE5pu/pd1 | OE5pu/pd0 | OE4pu/pd1 | OE4pu/pd0 |
|          | Default    | 0   | 1         | 0         | 1         | 0         | 1         | 0         | 1         |
| 9DBL06xx | Name       | OE5pu/pd1                                       | OE5pu/pd0 | OE4pu/pd1 | OE4pu/pd0 | Reserved  |           | OE3pu/pd1 | OE3pu/pd0 |
|          | Default    | 0   | 1         | 0         | 1         | -         | -         | 0         | 1         |
| 9DBL04xx | Name       | Reserved  |           | OE3pu/pd1 | OE3pu/pd0 | Reserved  |           | OE2pu/pd1 | OE2pu/pd0 |
|          | Default    | -   | -         | 0         | 1         | -         | -         | 0         | 1         |
| 9DBL02xx | Name       | Reserved  |           |           |           |           |           | OE1pu/pd1 | OE1pu/pd0 |
|          | Default    | -   | -         | -         | -         | -         | -         | 0         | 1         |

**Table 33. Byte 16: Pull-up\_Pull-down Control 2**

| Byte 16 | Bit        | 7        | 6 | 5 | 4 | 3 | 2 | 1  | 0                     |  |
|---------|------------|----------|---|---|---|---|---|--|-----------------------|--|
|         | Function   | -        | - | - | - | - | - | Pull-up(PuP)/<br>Pull-down (Pdown) control         |                       |  |
|         | Type       | -        | - | - | - | - | - | RW   | RW                    |  |
| Device  | Definition | Reserved |   |   |   |   |   | 00 = None, 01 = Pdown,<br>10 = Pup, 11 = Pup+Pdown |                       |  |
| All     | Name       | -        | - | - | - | - | - | CKPWRGD_PD_<br>pu/pd1                              | CKPWRGD_PD_<br>pu/pd0 |  |
|         | Default    | 0        | 0 | 0 | 0 | 0 | 0 | 1  | 0                     |  |

Byte 17 is Reserved.

**Table 34. Byte 18: Polarity Control 0**

| Byte 18  | Bit        | 7   | 6      | 5        | 4      | 3      | 2        | 1        | 0        |
|----------|------------|---|--------|----------|--------|--------|----------|----------|----------|
|          | Function   | OE pin polarity   |        |          |        |        |          |          |          |
|          | Type       | RW  | RW     | RW       | RW     | RW     | RW       | RW       | RW       |
| Device   | Definition | 0 = Output enabled when OE pin is Low<br>1 = Output enabled when OE pin is High |        |          |        |        |          |          |          |
| 9DBL08xx | Name       | OE7pol  | OE6pol | OE5pol   | OE4pol | OE3pol | OE2pol   | OE1pol   | OE0pol   |
|          | Default    | 0   | 0      | 0        | 0      | 0      | 0        | 0        | 0        |
| 9DBL06xx | Name       | OE5pol  | OE4pol | Reserved | OE3pol | OE2pol | OE1pol   | Reserved | OE0pol   |
|          | Default    | 0   | 0      | 0        | 0      | 0      | 0        | 0        | 0        |
| 9DBL04xx | Name       | Reserved  | OE3pol | Reserved | OE2pol | OE1pol | Reserved | OE0pol   | Reserved |
|          | Default    | 0   | 0      | 0        | 0      | 0      | 0        | 0        | 0        |
| 9DBL02xx | Name       | Reserved  |        |          | OE1pol | OE0pol | Reserved |          |          |
|          | Default    | 0   | 0      | 0        | 0      | 0      | 0        | 0        | 0        |

**Table 35. Byte 19: Polarity Control 1**

| Byte 19     | Bit        | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0   |  |
|-------------|------------|----------|---|---|---|---|---|---|---|--|
|             | Function   | -        | - | - | - | - | - | - | CKPWRGD_PD pin polarity                             |  |
|             | Type       | -        | - | - | - | - | - | - | RW  |  |
|             | Definition | Reserved |   |   |   |   |   |   | 0 = Power Down when Low<br>1 = Power Down when High |  |
| All Devices | Name       | -        | - | - | - | - | - | - | CKPWRGD_Pdpol                                       |  |
|             | Default    | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0   |  |

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Thermal Characteristics

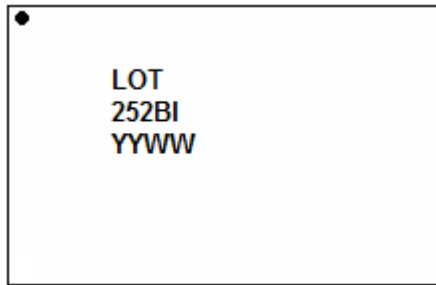
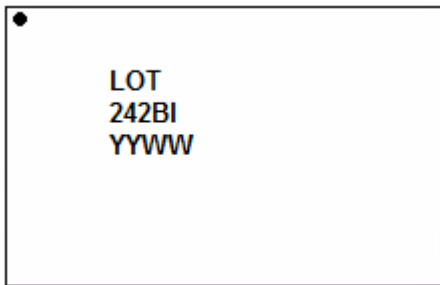
**Table 36. Thermal Characteristics [a]**

| Parameter                                     | Symbol         | Conditions                       | Package        | Typical Values | Units |
|---|----------------|----------------------------------|----------------|----------------|-------|
| 9DBL08xx<br>Thermal<br>Resistance             | $\theta_{JC}$  | Junction to case.                | NDG48          | 33             | °C/W  |
|   | $\theta_{Jb}$  | Junction to base.                |                | 2              | °C/W  |
|   | $\theta_{JA0}$ | Junction to air, still air.      |                | 37             | °C/W  |
|   | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. |                | 30             | °C/W  |
|   | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. |                | 27             | °C/W  |
|   | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. |                | 26             | °C/W  |
| 9DBL06xx<br>9DBL04xx<br>Thermal<br>Resistance | $\theta_{JC}$  | Junction to case.                | NDG40<br>NLG32 | 42             | °C/W  |
|   | $\theta_{Jb}$  | Junction to base.                |                | 2              | °C/W  |
|   | $\theta_{JA0}$ | Junction to air, still air.      |                | 39             | °C/W  |
|   | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. |                | 33             | °C/W  |
|   | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. |                | 28             | °C/W  |
|   | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. |                | 27             | °C/W  |
| 9DBL02xx<br>Thermal<br>Resistance             | $\theta_{JC}$  | Junction to case.                | NLG24          | 60             | °C/W  |
|   | $\theta_{Jb}$  | Junction to base.                |                | 5.4            | °C/W  |
|   | $\theta_{JA0}$ | Junction to air, still air.      |                | 50             | °C/W  |
|   | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. |                | 43             | °C/W  |
|   | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. |                | 39             | °C/W  |
|   | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. |                | 38             | °C/W  |

[a] epad soldered to ground

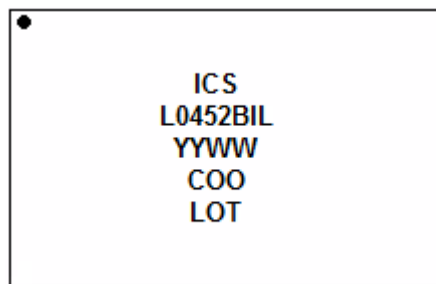
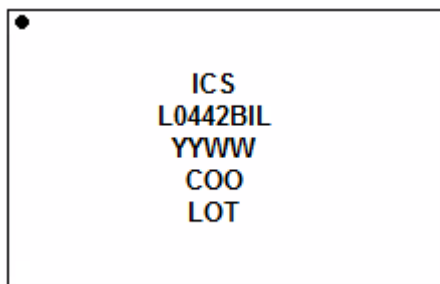
## Marking Diagrams

### 9DBL02x2



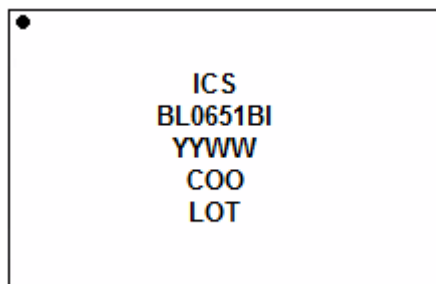
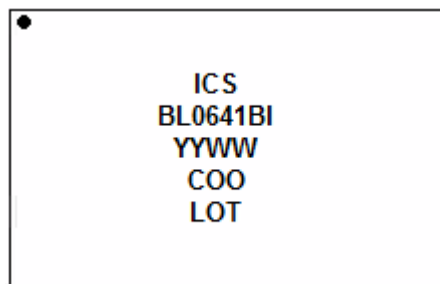
- Line 1: "LOT" is the lot sequence number.
- Line 2: truncated part number.
  - "I" denotes industrial temperature range device.
- Line 3: "YYWW" is the last two digits of the year and week that the part was assembled.

### 9DBL04x2



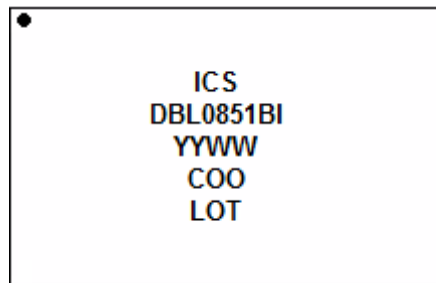
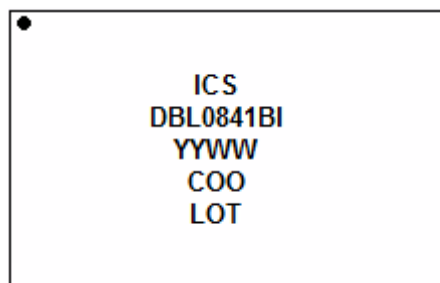
- Line 2: truncated part number.
  - "I" denotes industrial temperature range.
- Line 3: "YYWW" is the last two digits of the year and week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" is the lot sequence number.

### 9DBL06x1



- Line 2: truncated part number.
  - "I" denotes industrial temperature range.
- Line 3: "YYWW" is the last two digits of the year and week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" is the lot sequence number.

### 9DBL08x1



- Line 2: truncated part number.
  - "I" denotes industrial temperature range.
- Line 3: "YYWW" is the last two digits of the year and week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" is the lot sequence number.

## Ordering Information

**Table 37. Ordering Information** [a] [b] [c] [d]

| Output Impedance (ohms) | Number of Clock Outputs | Package                                  | Orderable Part Number | Shipment Packing    |
|-------------------------|-------------------------|--|-----------------------|---------------------|
| 85                      | 2                       | 24-VFQFPN - 4 × 4 × 0.9 mm, 0.50mm Pitch | 9DBL0252BKILF         | Trays               |
|                         |                         |  | 9DBL0252BKILFT        | "T" = Tape and Reel |
|                         | 4                       | 32-VFQFPN - 5 × 5 × 0.9 mm, 0.50mm Pitch | 9DBL0452BKILF         | Trays               |
|                         |                         |  | 9DBL0452BKILFT        | "T" = Tape and Reel |
|                         | 6                       | 40-VFQFPN - 5 × 5 × 0.9 mm, 0.40mm Pitch | 9DBL0651BKILF         | Trays               |
|                         |                         |  | 9DBL0651BKILFT        | "T" = Tape and Reel |
|                         | 8                       | 48-VFQFPN - 6 × 6 × 0.9 mm, 0.40mm Pitch | 9DBL0851BKILF         | Trays               |
|                         |                         |  | 9DBL0851BKILFT        | "T" = Tape and Reel |
| 100                     | 2                       | 24-VFQFPN - 4 × 4 × 0.9 mm, 0.50mm Pitch | 9DBL0242BKILF         | Trays               |
|                         |                         |  | 9DBL0242BKILFT        | "T" = Tape and Reel |
|                         | 4                       | 32-VFQFPN - 5 × 5 × 0.9 mm, 0.50mm Pitch | 9DBL0442BKILF         | Trays               |
|                         |                         |  | 9DBL0442BKILFT        | "T" = Tape and Reel |
|                         | 6                       | 40-VFQFPN - 5 × 5 × 0.9 mm, 0.40mm Pitch | 9DBL0641BKILF         | Trays               |
|                         |                         |  | 9DBL0641BKILFT        | "T" = Tape and Reel |
|                         | 8                       | 48-VFQFPN - 6 × 6 × 0.9 mm, 0.40mm Pitch | 9DBL0841BKILF         | Trays               |
|                         |                         |  | 9DBL0841BKILFT        | "T" = Tape and Reel |

[a] "B" is the device revision designator (will not correlate with the datasheet revision).

[b] "LF" denotes Pb-free configuration, RoHS compliant.

[c] "I" indicates that all devices are specified over the -40°C to +85°C (industrial) temperature range.

[d] "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 38 for more details)

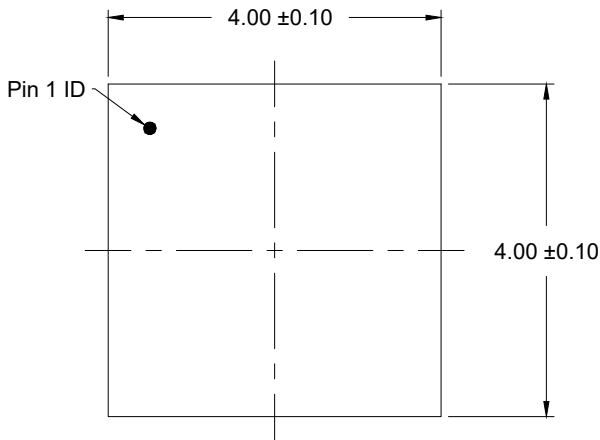
**Table 38. Pin 1 Orientation in Tape and Reel Packaging**

| Part Number Suffix | Pin 1 Orientation      | Illustration |
|--------------------|------------------------|--------------|
| T                  | Quadrant 1 (EIA-481-C) |              |

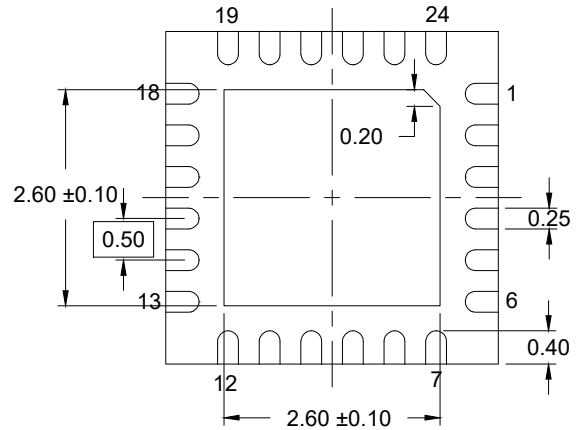
## Revision History

**Table 39. Revision History**

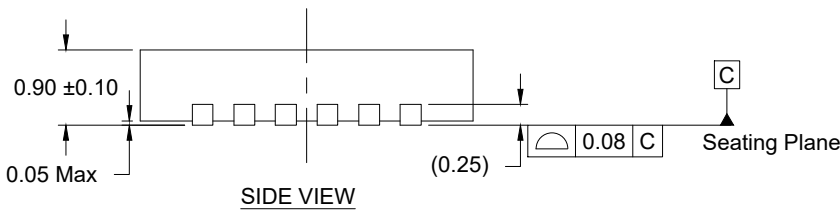
| Revision Date     | Description of Change   |
|-------------------|---|
| November 30, 2022 | Updated POD links in <a href="#">Ordering Information</a> table.  |
| March 18, 2022    | <ul style="list-style-type: none"> <li>▪ Updated <a href="#">Pin Descriptions</a>.</li> <li>▪ Updated <a href="#">Package Outline Drawings</a> section and <a href="#">Ordering Information</a> table.</li> </ul>   |
| January 24, 2022  | <ul style="list-style-type: none"> <li>▪ Added missing <a href="#">Table 16</a> ZDB (PLL) Operating Mode.</li> <li>▪ Added cross references to <a href="#">Table 16</a> in <a href="#">Table 21</a>.</li> </ul>   |
| April 1, 2021     | Corrected pin numbers on vSADR_tri pin for 04x2 and 02x2 in pin descriptions table.   |
| August 13, 2020   | <ul style="list-style-type: none"> <li>▪ Changed the shipment packing for the 9DBL0242B and 0252B from “Cut Tape” to “Trays” in the <a href="#">Ordering Information</a> table.</li> </ul>  |
| July 8, 2020      | <ul style="list-style-type: none"> <li>▪ Merged 9DBL02x2, 9DBL04x2, 9DBL06x1 and 9DBL08x1 into single document.</li> <li>▪ Updated PCIe jitter tables to show PCIe Gen5.</li> <li>▪ Updated Test Loads figures to indicate PCIe Jitter Test setup.</li> <li>▪ Updated package outline drawings link for the 9DBL08x1 devices to NDG48P2.</li> </ul> |
| February 8, 2017  | Last update of 9DBL0242/0252 data sheet.  |
| February 9, 2017  | Last update of 9DBL0442/0452 data sheet.  |
| February 8, 2017  | Last update of 9DBL0641/0651 data sheet.  |
| February 9, 2017  | Last update of 9DBL0841/0851 data sheet.  |



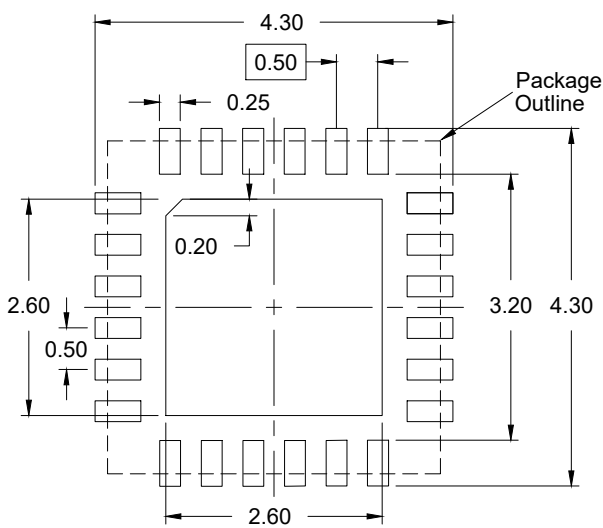
TOP VIEW



BOTTOM VIEW



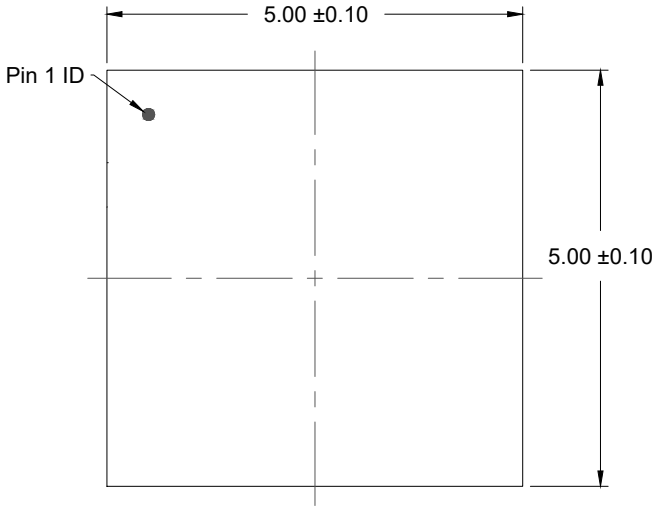
SIDE VIEW



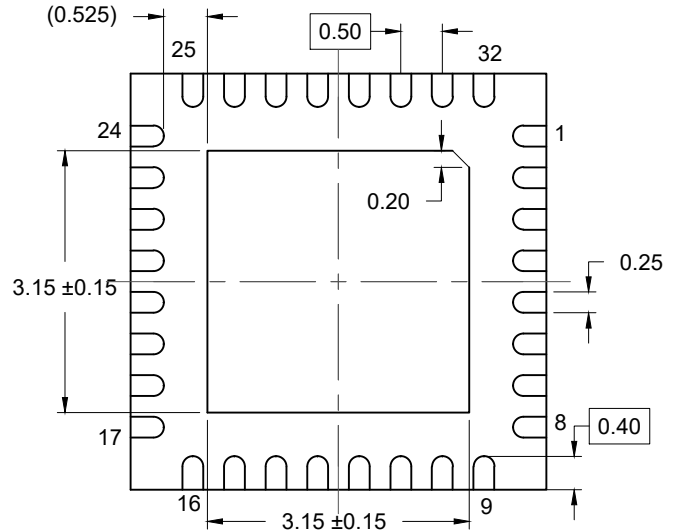
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

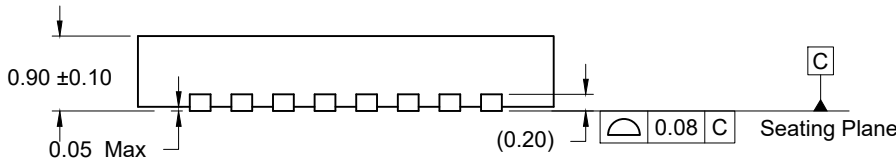
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



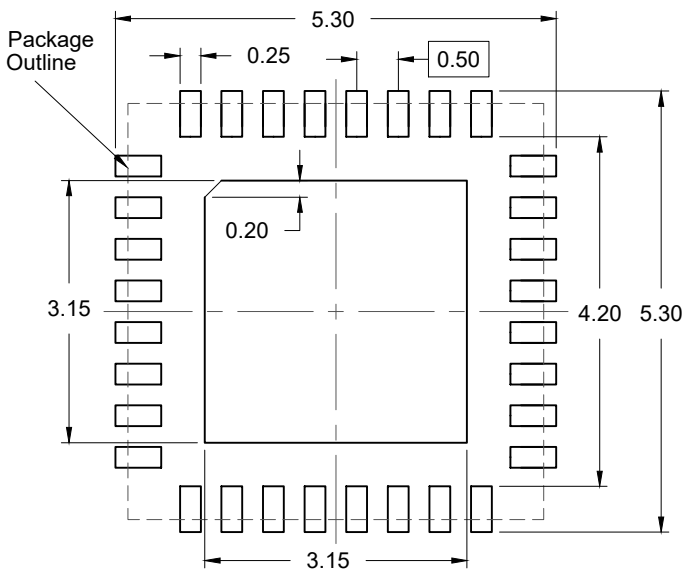
TOP VIEW



BOTTOM VIEW



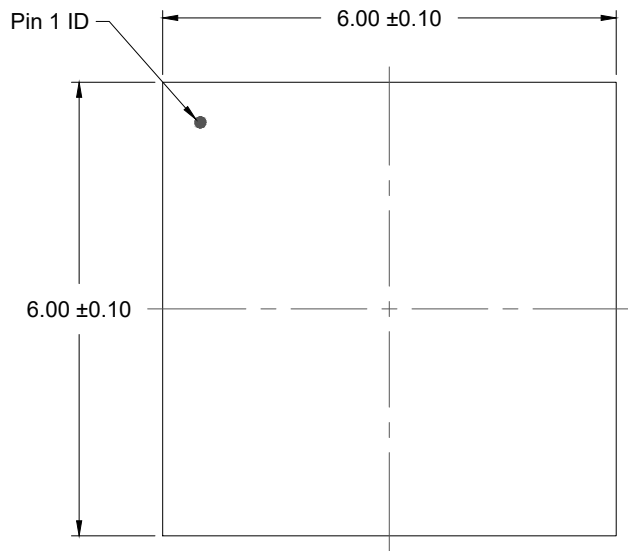
SIDE VIEW



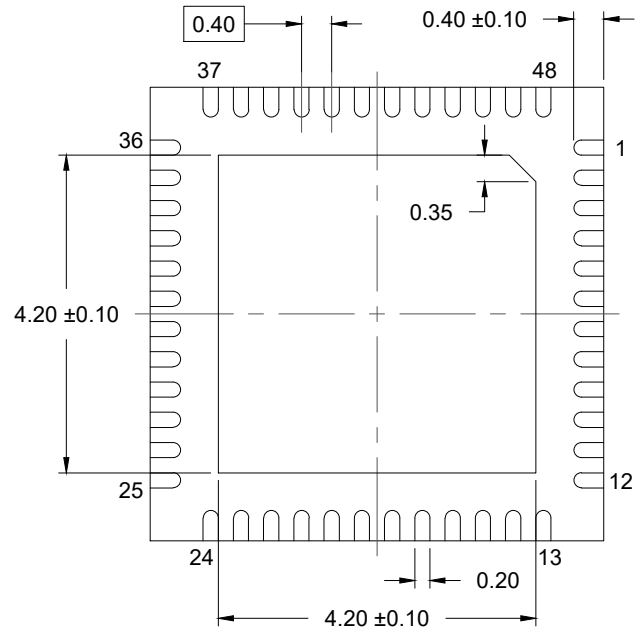
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

**NOTES:**

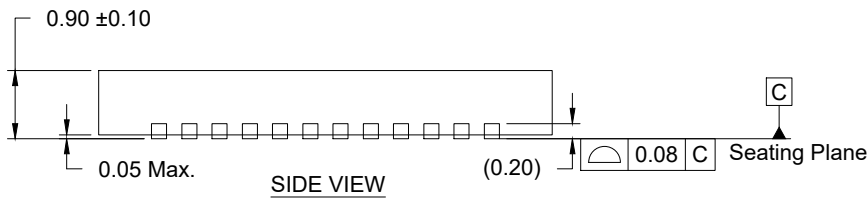
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



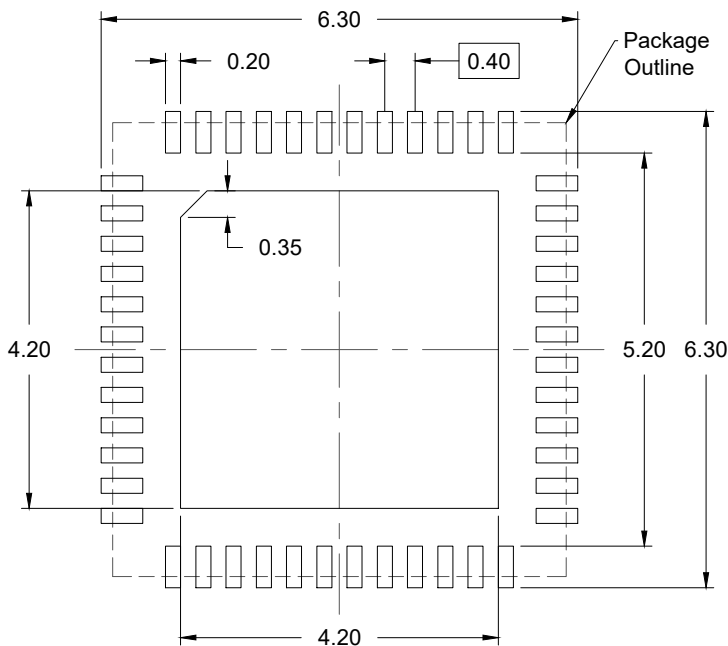
TOP VIEW



BOTTOM VIEW



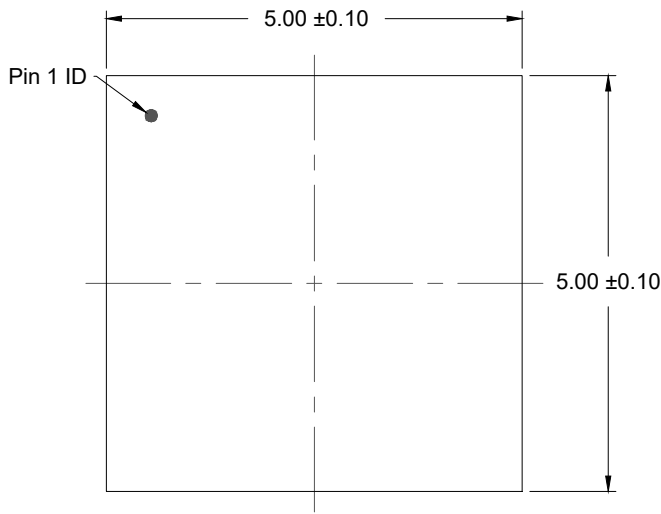
SIDE VIEW



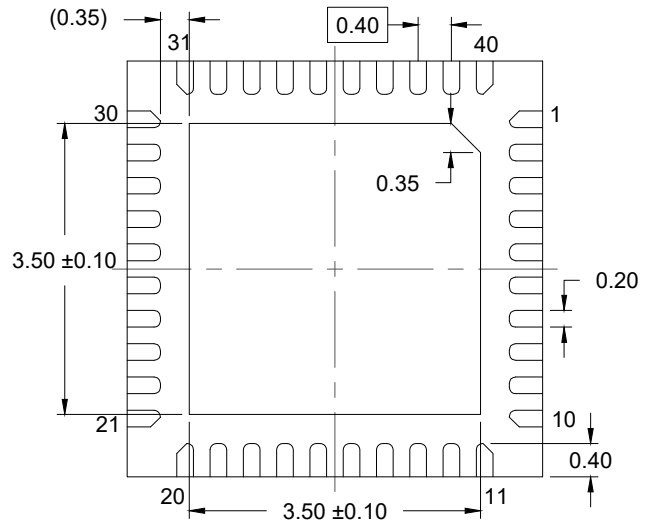
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



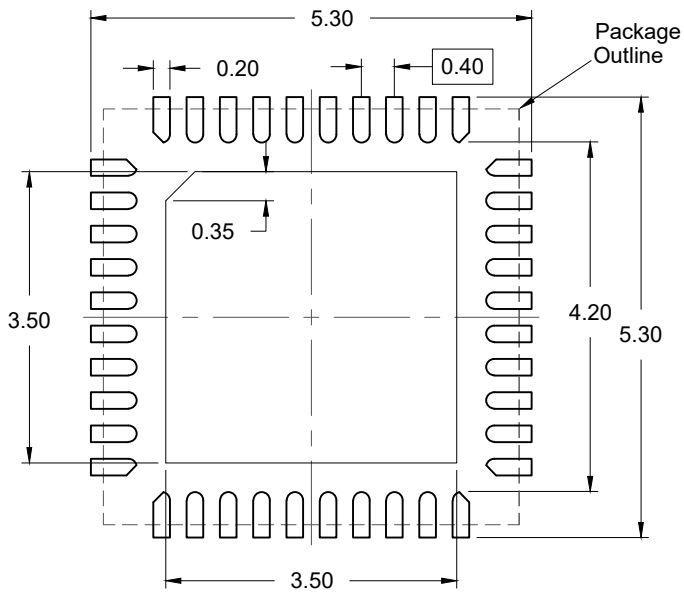
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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