



**THE DATASHEET OF
DZDH0401DW-7**



Description

The DZDH0401DW is intended to drive a P-channel enhancement MOSFET configured as an ideal diode. The device operates as a differential amplifier and PMOS controller to minimize forward current losses when $V_{IN} > V_{OUT}$ and provide high isolation when $V_{IN} < V_{OUT}$. The circuit compares the voltage between IN and OUT. If the differential is greater than $\sim 34\text{mV}$ (typ.) V_{BIAS} will fall and the PMOS will turn on. If the differential is less than $\sim 34\text{mV}$ V_{BIAS} will rise and the PMOS will turn off, isolating IN from OUT.

Applications


- High Side Gate Driving PMOS
- High Side Disconnect Switch
- Battery Discharge Protection
- Emergency Lighting
- Active OR'ing Redundant Power Supplies

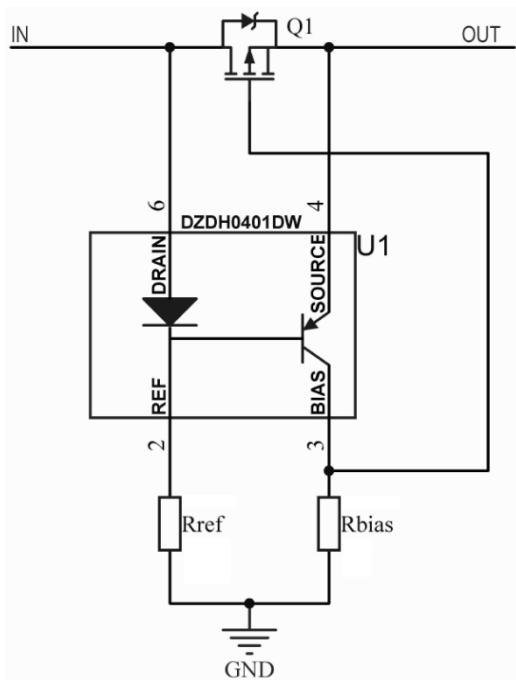
Features

- Max Input Voltage: 40V
- Peak Bias Current: -300mA
- Max Reverse Voltage Protection: 50V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.**

<https://www.diodes.com/quality/product-definitions/>

Mechanical Data

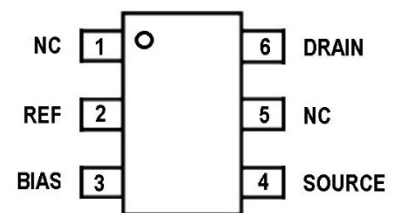
- Case: SOT363
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Finish. Solderable per MIL-STD-202, Method 208 
- Weight: 0.006 grams (Approximate)



Typical Configuration



SOT363 Top View



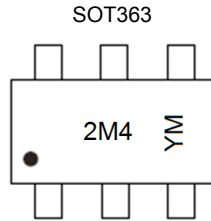
Pinout

Ordering Information (Note 4)

| Part Number | Marking | Reel Size (inches) | Tape Width (mm) | Quantity per Reel |
|--------------|---------|--------------------|-----------------|-------------------|
| DZDH0401DW-7 | 2M4 | 7 | 8 | 3,000 |

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



2M4 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: 1 = 2021)
 M = Month (ex: 3 = March)

Date Code Key

| Year | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 |
|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Code | H | I | J | K | L | M | N | O | P | R | S | T |

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | O | N | D |

Absolute Maximum Ratings (@ T_A = +25°C unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|----------------------|---------------------------|-------|------|
| DRAIN BIAS Voltage | V _{DRAIN-BIAS} | 40 | V |
| SOURCE DRAIN Voltage | V _{SOURCE-DRAIN} | 50 | V |
| BIAS Current | I _{BIAS} | -300 | mA |
| DRAIN Current | I _{DRAIN} | 300 | mA |

Thermal Characteristics – Total Device (@ T_A = +25°C unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|--------------------------------------------------|-----------------------------------|-------------|------|
| Power Dissipation (Note 5) | P _D | 300 | mW |
| Thermal Resistance, Junction to Ambient (Note 5) | R _{θJA} | 424 | °C/W |
| Thermal Resistance, Junction to Case (Note 5) | R _{θJC} | 111 | °C/W |
| Operating and Storage Temperature Range | T _J , T _{STG} | -65 to +150 | °C |

Note: 5. For a device mounted on minimum recommended pad layout with 1oz copper that is on a single-sided 1.6mm FR4 PCB; the device is measured under still air conditions whilst operating in a steady-state.

Thermal Characteristics – Total Device

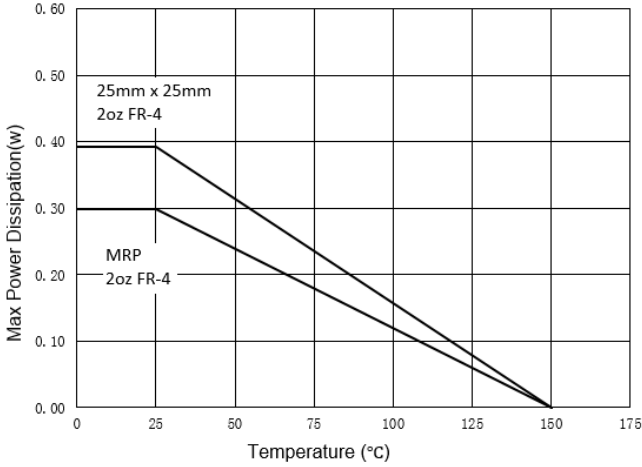


Fig.1 Derating Curve

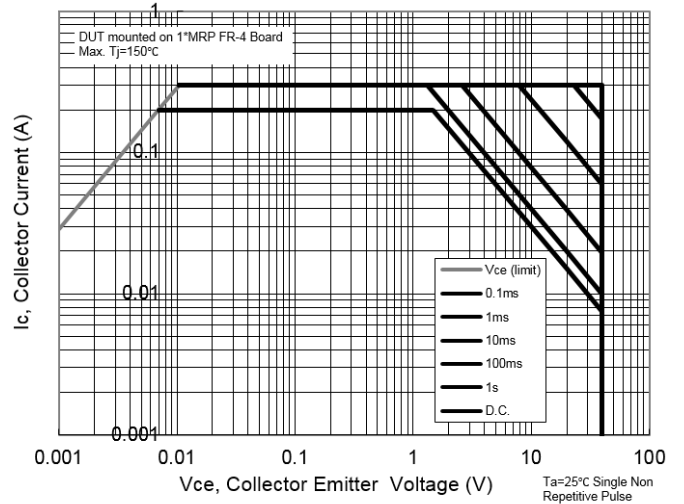


Fig.2 Safe Operation Area

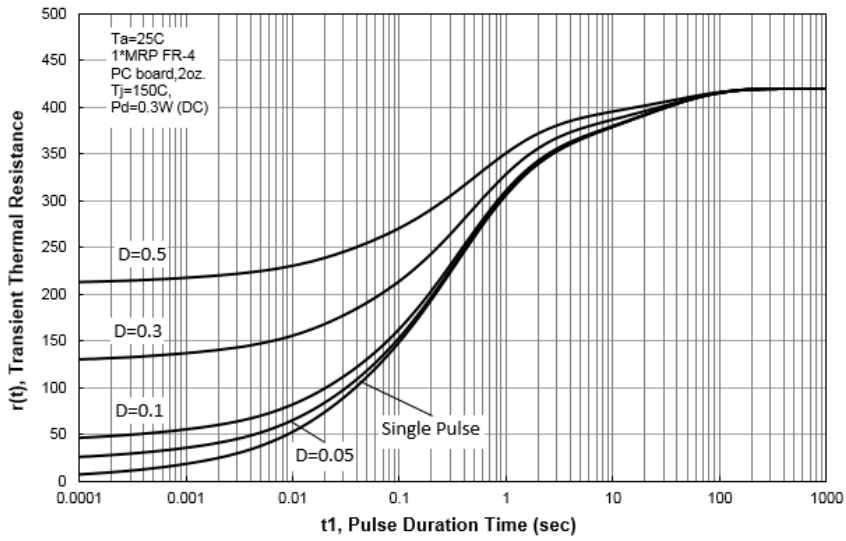


Fig.3 Transient Thermal Resistance

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$ unless otherwise specified)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|-----------------------------------------------|---------------------------|------|------|------|---------------|------------------------------------------------------------------------|
| DRAIN - BIAS Voltage | $V_{\text{DRAIN-BIAS}}$ | 40 | 78 | — | V | $I_{\text{DRAIN}}=100\mu\text{A}$ |
| SOURCE - DRAIN Voltage | $V_{\text{SOURCE-DRAIN}}$ | 50 | 84 | — | V | $I_{\text{SOURCE}}=100\mu\text{A}$ |
| DRAIN - REF Voltage | $V_{\text{DRAIN-REF}}$ | — | 588 | — | mV | $I_{\text{DRAIN}}=100\mu\text{A}$ |
| SOURCE Current | I_{SOURCE} | — | 11.6 | — | μA | $V_{\text{SOURCE-REF}}=0.56\text{V}$ |
| REF-SOURCE Voltage | $V_{\text{REF-SOURCE}}$ | — | -554 | — | mV | $I_{\text{REF}}=-10\mu\text{A}$ |
| Turn-Off Differential Voltage | V_T | 5 | 34 | 80 | mV | $I_{\text{DRAIN}}=100\mu\text{A}; I_{\text{SOURCE}}=10\mu\text{A}$ |
| REF-SOURCE Voltage ($V_{\text{BIAS low}}$) | $V_{\text{REF-SOURCE}}$ | -250 | -472 | — | mV | $V_{\text{BIAS-SOURCE}}=-5\text{V}; I_{\text{BIAS}}=-1\mu\text{A}$ |
| | | -300 | -541 | — | mV | $V_{\text{BIAS-SOURCE}}=-5\text{V}; I_{\text{BIAS}}=-10\mu\text{A}$ |
| REF-SOURCE Voltage ($V_{\text{BIAS high}}$) | $V_{\text{REF-SOURCE}}$ | — | -601 | -800 | mV | $V_{\text{BIAS-SOURCE}}=-0.5\text{V}; I_{\text{BIAS}}=-100\mu\text{A}$ |
| | | — | -663 | -850 | mV | $V_{\text{BIAS-SOURCE}}=-0.5\text{V}; I_{\text{BIAS}}=-1\text{mA}$ |

Typical Electrical Characteristics (@ $T_A = +25^\circ\text{C}$ unless otherwise specified.)

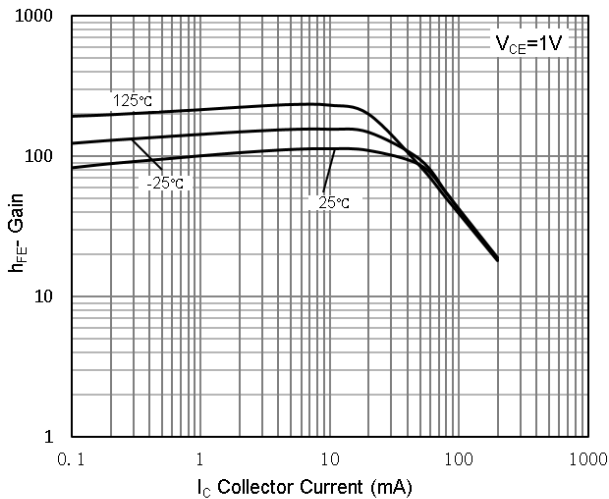


Fig.4 h_{FE} vs I_C

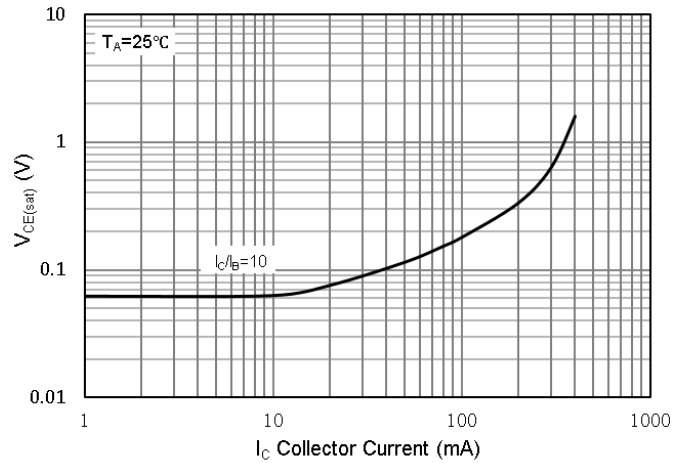


Fig.5 $V_{CE(sat)}$ vs I_C

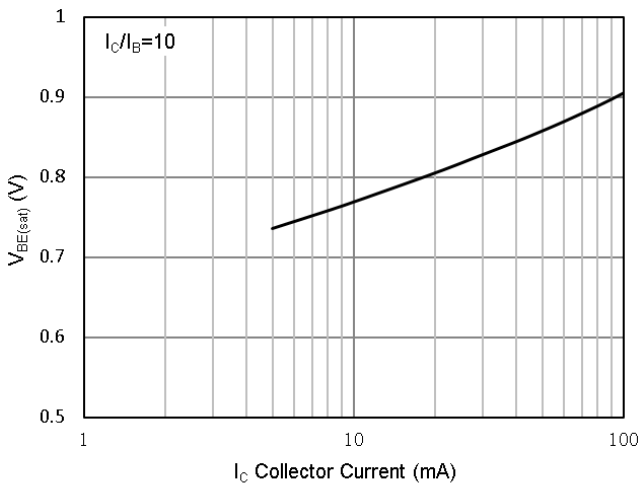


Fig.6 $V_{BE(sat)}$ vs I_C

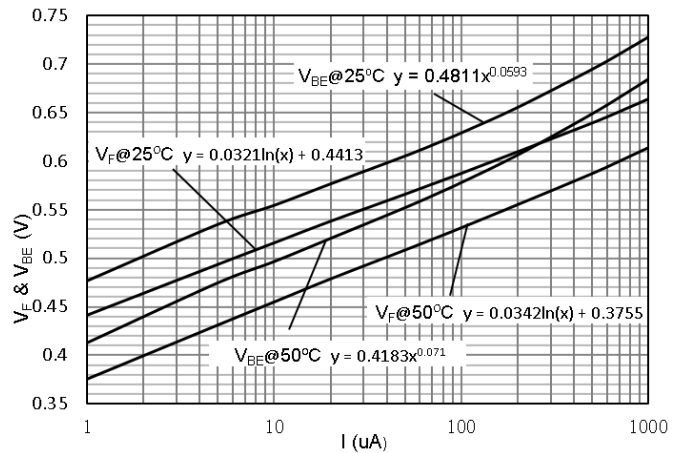
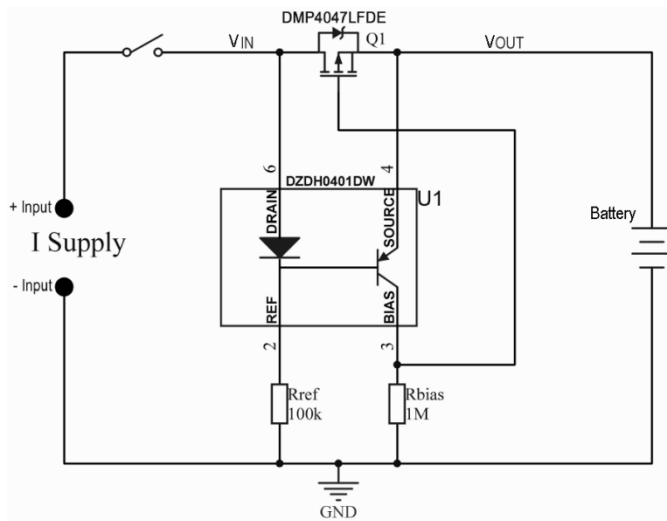


Fig.7 I vs V_F & V_{BE}

Typical Application Circuit/ Pin Out Details/ Functional Description



Typical Application Circuit

| Pin | Name | Function |
|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | NC | No internal connection |
| 2 | REF | Reference current to set V_F |
| 3 | BIAS | Reference current to set V_{BE} and control Gate |
| 4 | SOURCE | V_{OUT} sense voltage |
| 5 | NC | No internal connection |
| 6 | DRAIN | V_{IN} sense voltage |
| n/a | Rref | This resistor sets the turn off speed of the FET. The lower the resistance, the more base drive to the transistor, the faster the transistor shorts out the gate to turn off the FET. |
| n/a | Rbias | This resistor sets the turn on speed of the FET. When the ideal diode circuit is turning on the PNP is held off by the diode and FET voltage drops. It is Rbias that pulls the gate low and turns on the FET. |
| n/a | Rbias : Rref | Ideal diode Turn-Off threshold voltage $V_T \propto Rbias / Rref$ |
| n/a | Vref | Voltage across Rref |

Functional Description (Refer to typical application circuit above)

Supply Connect:

As a +Input is applied, the body drain diode of Q1 becomes forward biased. U1 diode holds U1 transistor base at $V_{IN} - V_F$, and so V_{BE} is too low to turn on U1 transistor. As Q1 gate capacitance charges through Rbias, Q1 turns on and R_{DS} decreases causing V_{DS} to decrease and V_{BE} to increase until U1 transistor starts to conduct. This process continues until Q1 R_{DS} reaches its minimum value and U1 transistor V_{BE} cannot increase and I_C reaches its maximum. V_{GS} should be high enough at this point to ensure linear operation.

Rref and Rbias set the currents through U1 diode and U1 collector respectively so that $V_{F(DIODE)}$ is greater than $V_{BE(on)}$.

Supply Disconnect:

As the +Input is removed, $V_{DS} < V_T$, Q1 is on and $V_{IN} = V_{OUT}$, causing V_{REF} to fall and U1 $V_{BE} > V_{BE(on)}$ so U1 transistor discharges Q1 gate capacitance and Q1 turns off causing V_{IN} to fall to 0V.

Quiescent Current and Isolation:

With a battery connected at Supply Out, there are two leakage paths back to the Supply In. One is straight through Q1 and the other is through U1 emitter-anode. The high reverse breakdown voltage of U1 diode provides a high isolation path. The Rref & Rbias currents bias U1 transistor on which keeps Q1 off. These resistors' values are chosen to minimize quiescent current operation of the circuit.

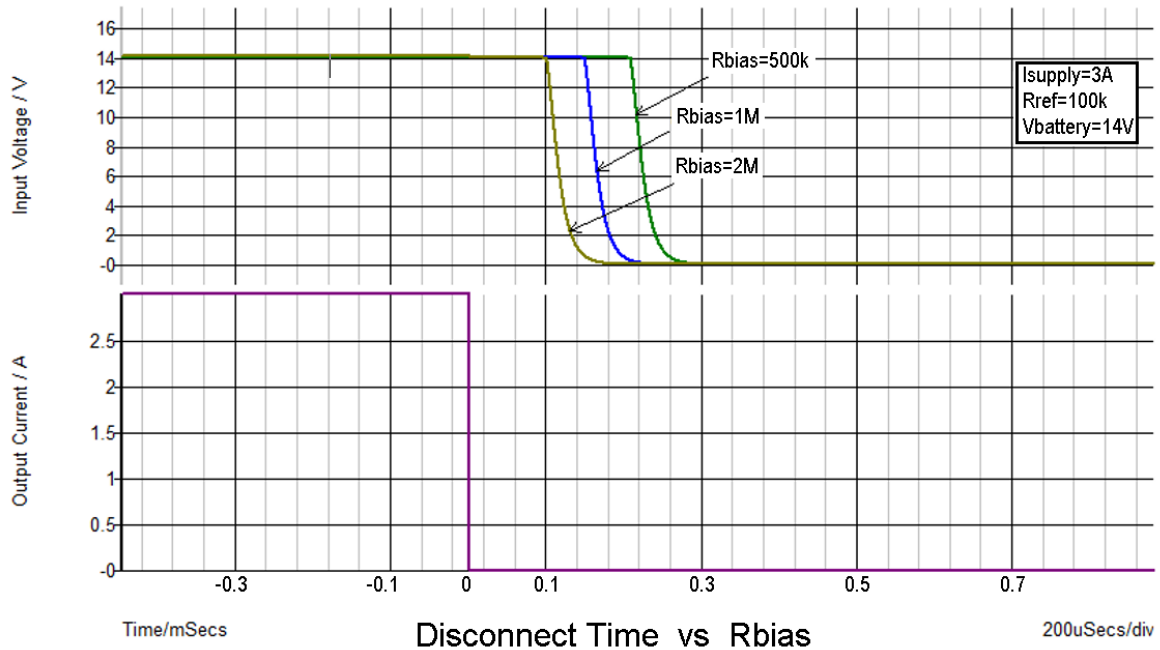
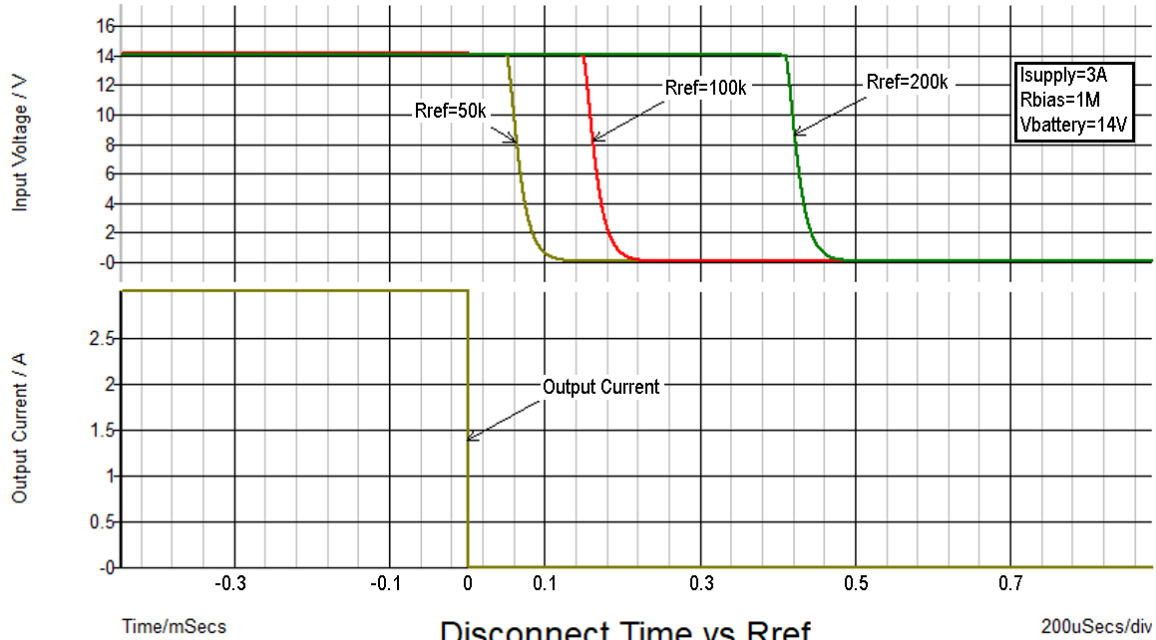
| Typical Charging Conditions. ($T_a=25^\circ\text{C}$ $V_{batt}=14\text{V}$ switch closed, $I_{supply}=3\text{A}$) | | | |
|---------------------------------------------------------------------------------------------------------------------|------------|-------|---------------|
| Parameter | Symbol | Typ | Unit |
| Input Voltage | V_{IN} | 14.1 | V |
| Input current | I_{IN} | 3 | A |
| Output Voltage | V_{OUT} | 14 | V |
| Output Current | I_{OUT} | 3.0 | A |
| Diode Forward Voltage | V_F | 0.6 | V |
| Diode forward current | I_F | 135 | μA |
| Reference Voltage | V_{REF} | 13.4 | V |
| Reference Current | I_{REF} | 136.6 | μA |
| Base Current | I_B | 1.6 | μA |
| Emitter Current | I_E | 12.1 | μA |
| Bias Voltage | V_{BIAS} | 10.5 | V |
| Collector Current | I_C | 10.5 | μA |
| Operating Current | I_{CC} | 147 | μA |

| Typical Non-Charging Conditions. ($T_a=25^\circ\text{C}$ $V_{batt}=14\text{V}$ switch open, $I_{supply}=3\text{A}$) | | | |
|-----------------------------------------------------------------------------------------------------------------------|------------|-------|---------------|
| Parameter | Symbol | Typ | Unit |
| Input Voltage | V_{IN} | - | μV |
| Input current | I_{IN} | -- | A |
| Output Voltage | V_{OUT} | 14 | V |
| Output Current | I_{OUT} | -- | A |
| Diode Forward Voltage | V_F | -- | V |
| Diode forward current | I_F | 0 | μA |
| Reference Voltage | V_{REF} | 13.3 | V |
| Reference Current | I_{REF} | 133 | μA |
| Base Current | I_B | 133 | μA |
| Emitter Current | I_E | 145 | μA |
| Bias Voltage | V_{BIAS} | 13.94 | V |
| Bias Current | I_{BIAS} | 13.94 | μA |
| Operating Current | I_{CC} | 147 | μA |

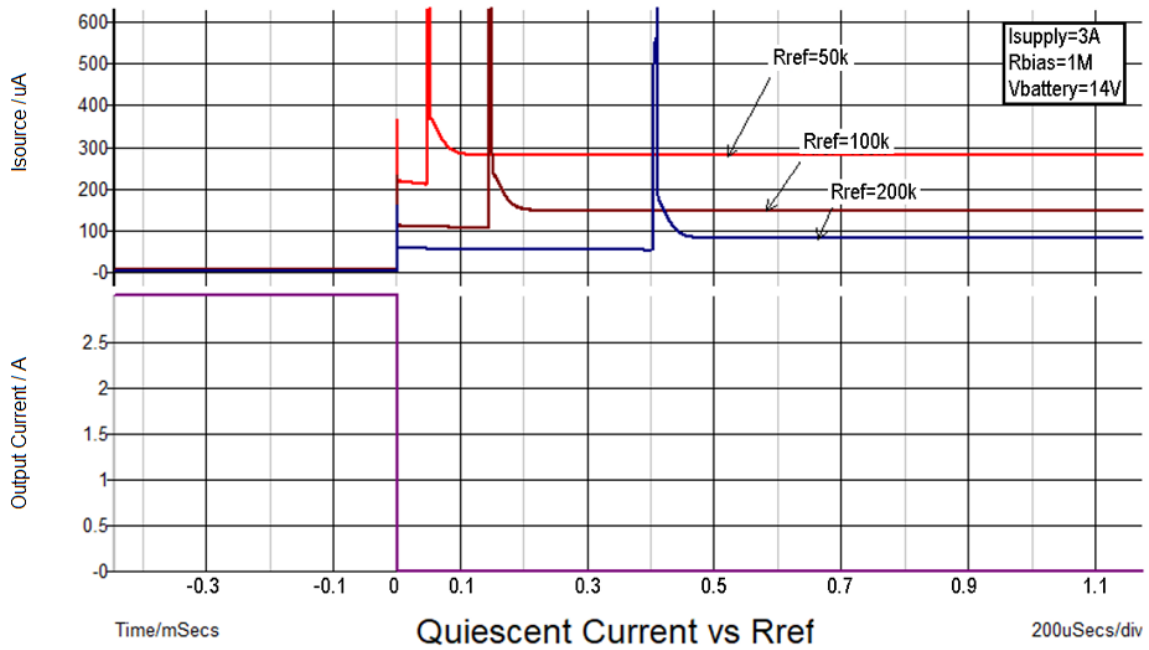
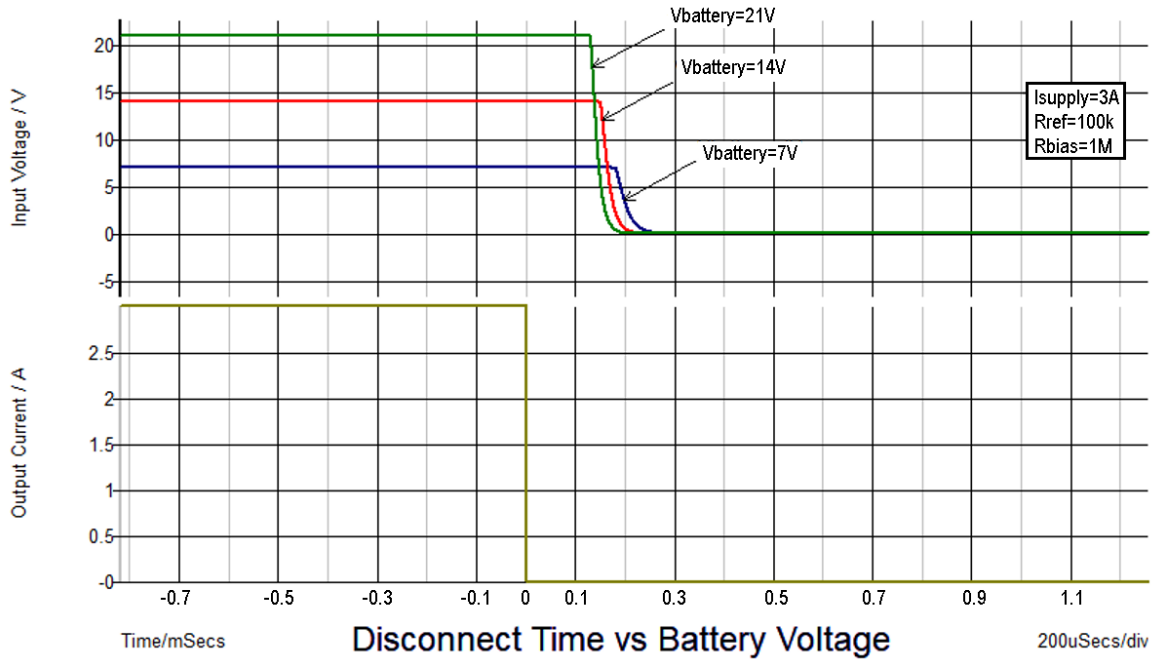
Typical Application Circuit/ Pin Out Details/ Functional Description (continued)

Timing

Switching speed is affected by PMOS characteristics, Rbias, Rref, and operating voltage. Using the typical application circuit, we can see how modifying values can affect the timing in the simulations below



Typical Application Circuit/ Pin Out Details/ Functional Description (continued)



Typical Application Circuit/ Pin Out Details/ Functional Description (continued)

Ideal Diode Power Saving

The typical voltage drop across a standard diode rectifier means higher power dissipation and more heat to manage. This both wastes power and significantly drops the potential on low voltage rails.

Example:

A diode rectifier with a typical forward voltage $V_F = 0.55V$ carrying 3A current would dissipate 1.65W ($I \times V_F$).

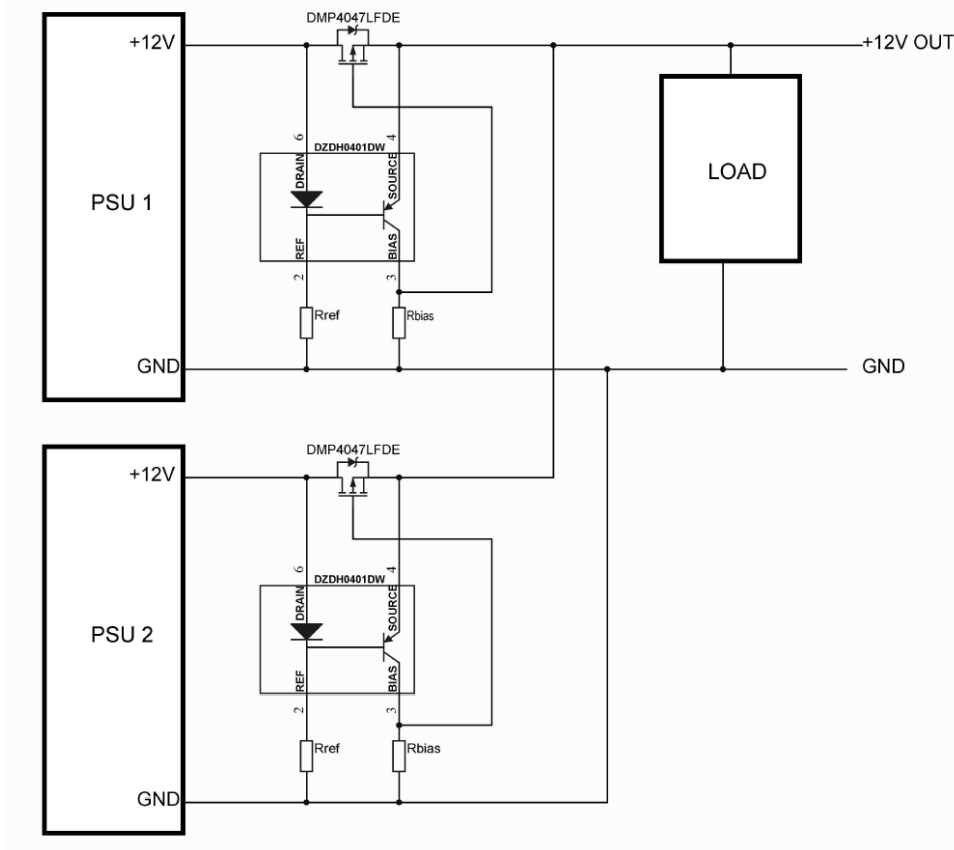
Whereas with P-MOSFET such as the DMP4047LFDE that has an $R_{DS(on)}$ of 33mΩ, the power dissipation reduces to only 0.29W ($I^2 \times R$).

Hence, very low $R_{DS(on)}$ Power MOSFETs can replace the standard rectifiers and the DZDH0401DW controls the MOSFET as an ideal diode.

N+1 redundancy OR'ing controller

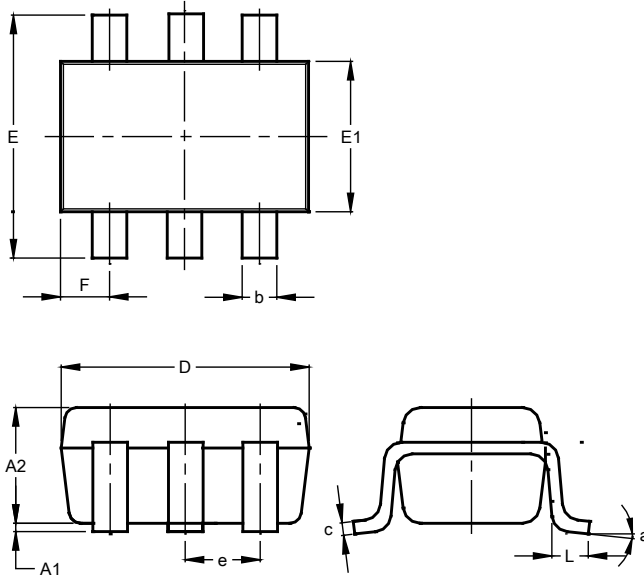
Critical systems require a fault-tolerant power supply that can be achieved by paralleling two or more PSUs into an (N+1) redundancy configuration.

During normal operation, usually all PSUs equally share the load for maximum reliability. If one of the PSUs is unplugged or fails, then the other PSUs fully support the load. To avoid the faulty PSU from affecting the common bus, an OR'ing rectifier blocks the reverse current flow into the faulty PSU. Likewise during hot-swapping, the OR'ing rectifiers isolate a PSU's discharged output capacitors from the common bus.



Package Outline Dimensions

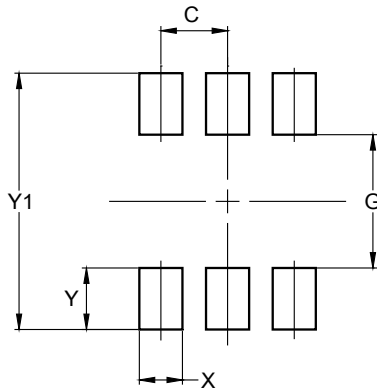
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



| SOT363 | | | |
|-----------------------------|-----------|------|-------|
| Dim | Min | Max | Typ |
| A1 | 0.00 | 0.10 | 0.05 |
| A2 | 0.90 | 1.00 | 1.00 |
| b | 0.10 | 0.30 | 0.25 |
| c | 0.10 | 0.22 | 0.11 |
| D | 1.80 | 2.20 | 2.15 |
| E | 2.00 | 2.20 | 2.10 |
| E1 | 1.15 | 1.35 | 1.30 |
| e | 0.650 BSC | | |
| F | 0.40 | 0.45 | 0.425 |
| L | 0.25 | 0.40 | 0.30 |
| a | 0° | 8° | -- |
| All Dimensions in mm | | | |

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.650 |
| G | 1.300 |
| X | 0.420 |
| Y | 0.600 |
| Y1 | 2.500 |

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