THE DATASHEET OF

BD39040MUF-CE2

Datasheet

Supervisor IC

System Power Good + Watchdog Timer + Reset for Automotive

BD39040MUF-C

General Description

BD39040MUF-C is a supervisor IC with quad power good, Watchdog timer and reset. This IC enables existing system to improve its ASIL level easily.
The BD39040MUF-C includes built-in self-test (BIST).

Features

- AEC-Q100 Qualified*(Note 1)*
- Quad Power Good for External Inputs
- Over Voltage Detection (OVD)
- Under Voltage Detection (UVD)
- Adjustable Window Watchdog Timer(WDT)
- Reset for VDD Input (POR)
- Built-in Self-test (BIST)

(Note 1) Grade 1

Applications

- Automotive for ADAS
- Camera Module
- Microwave Module
- Power Train ECU
- Other ECU

Key Specifications

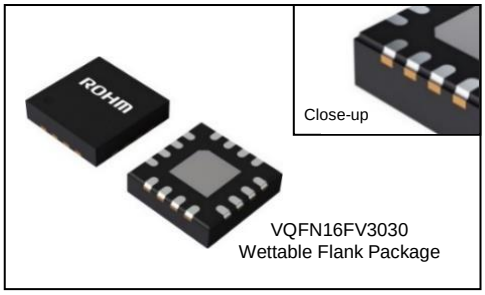
- VDD Input Voltage Range: 2.7 V to 5.5 V
  (VDD voltage level needs to be fixed within this range in 10% accuracy to avoid RSTIN reset detection)
- Detection Voltage (VDD POR/Power Good)
  Under Voltage Detection: -10 % (3 % accuracy)
  Over Voltage Detection: +10 % (3 % accuracy)
  Reset Off Time: 10 ms
- Operating Temperature Range: -40 °C to +125 °C

Special Characteristics

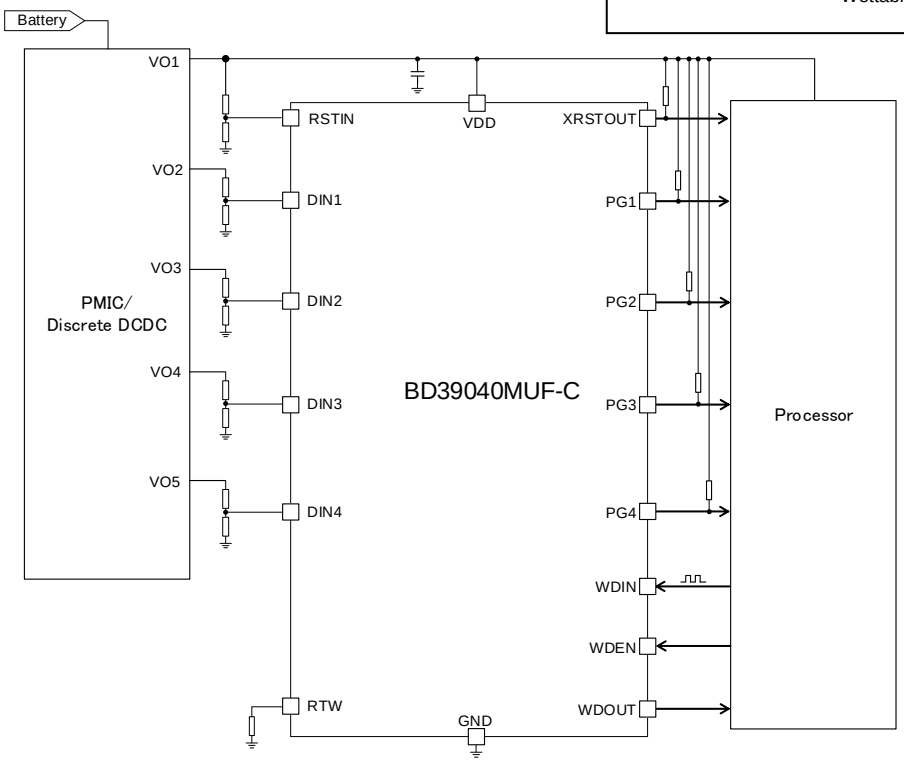
- Reference Voltage Accuracy
  Under Voltage Detection: ±3.0 %
  Over Voltage Detection: ±3.0 %

Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN16FV3030	3.00 mm x 3.00 mm x 1.00 mm



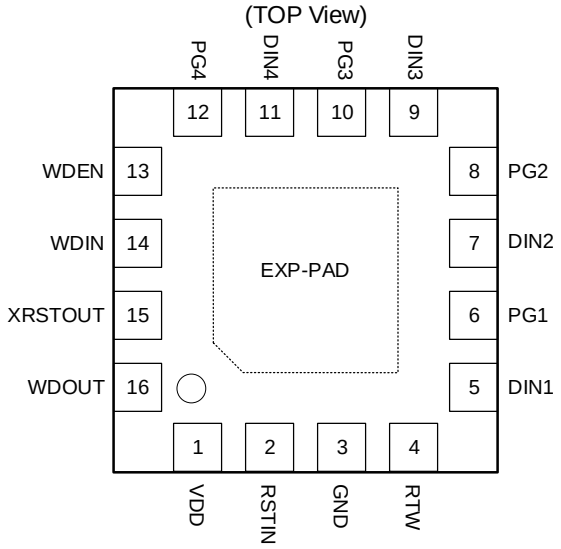
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

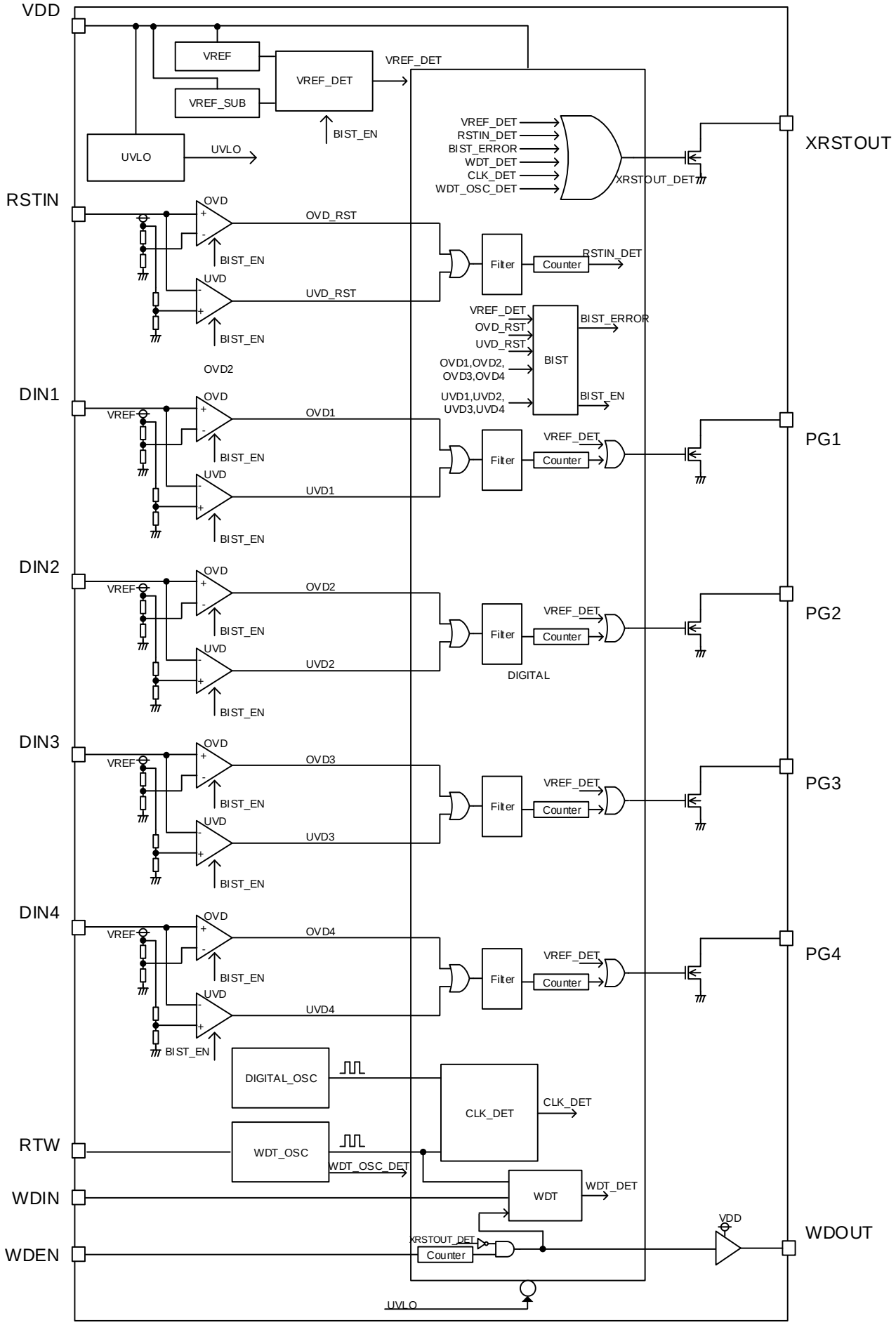
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	VDD	IC's Power Source
2	RSTIN	The VDD pin voltage divided by external resistor input pin. Nominal voltage level needs to be 0.8 V.
3	GND	IC's Power Ground
4	RTW	WDT frequency setting pin. FAST Timeout and SLOW Timeout is adjusted by the resistor value for this pin.
5	DIN1	Voltage for monitoring channel divided by external resistor input pin. Nominal voltage level needs to be 0.8 V.
6	PG1	POWER GOOD output pin for the DIN1 pin, and Nch Open Drain output. Hi-Z for assertion, and Low for de-assertion is its value. Please be pulled-up by external resistor. It can be pulled-up to any voltage source.
7	DIN2	Voltage for monitoring channel divided by external resistor input pin. Nominal voltage level needs to be 0.8 V.
8	PG2	POWER GOOD output pin for the DIN2 pin, and Nch Open Drain output. Hi-Z for assertion, and Low for de-assertion is its value. Please be pulled-up by external resistor. It can be pulled-up to any voltage source.
9	DIN3	Voltage for monitoring channel divided by external resistor input pin. Nominal voltage level needs to be 0.8 V.
10	PG3	POWER GOOD output pin for the DIN3 pin, and Nch Open Drain output. Hi-Z for assertion, and Low for de-assertion is its value. Please be pulled-up by external resistor. It can be pulled-up to any voltage source.
11	DIN4	Voltage for monitoring channel divided by external resistor input pin. Nominal voltage level needs to be 0.8 V.
12	PG4	POWER GOOD output pin for the DIN4 pin, and Nch Open Drain output. Hi-Z for assertion, and Low for de-assertion is its value. Please be pulled-up by external resistor. It can be pulled-up to any voltage source.
13	WDEN	Enable pin for WDT. High=Active, Low=Disable and WDT error is ignored.
14	WDIN	Clock input pin for WDT
15	XRSTOUT	Reset output pin. Nch Open Drain output. Hi-Z for normal, and Low for abnormal (reset) is its value. Please be pulled-up by external resistor. It can be pulled-up to any voltage source. Either error of OVD, UVD for RSTIN, reference voltage monitoring, internal OSC monitoring, WDT and BIST at power-up sequence causes this pin to drive low.
16	WDOUT	Buffer output pin for the WDEN pin input. Abnormal Power Source / the GND pin shortage for the WDEN pin can be recognized by monitoring this pin. This pin becomes Low when the XRSTOUT pin is low.
-	EXP-PAD	The EXP-PAD is connected to the PCB Ground plane.

Block Diagram



Block Diagrams - continued

Description of Blocks

Reference Voltage (VREF)
VREF is used for the reference voltage of monitoring each input voltage.

Reference Voltage (VREF_SUB)
VREF_SUB is used for the reference voltage of mutual monitoring VREF.

Reference Voltage (VREF_DET)
This is monitoring the 2 reference voltage, VREF and VREF_SUB.
This block contributes to the higher reliability by continuous, mutual monitoring each other if it turns on correctly.
Occurrence of error leads to Low output at the XRSTOUT pin and which is never de-asserted as long as abnormal status lasts. It becomes High at 10 ms (Typ) after the voltage returned to the normal range.

Under Voltage Lockout Circuit (UVLO)
Protection circuit to prevent internal circuit from malfunction at lower voltage (Power-up sequence or input power supply drop). This is monitoring the VDD pin voltage and UVLO works when it goes down to threshold level.
As UVLO is detected, the XRSTOUT, WDOUT, PG1, PG2, PG3 and PG4 pins output Low. Also Counter value in DIGITAL BLOCK is initialized and DIGITAL_OSC/WDT_OSC stop working.

Oscillator (DIGITAL_OSC)
This OSC generates the clock to control DIGITAL BLOCK. The frequency of DIGITAL_OSC is fixed at 2.2 MHz

Oscillator (WDT_OSC)
This OSC generates the clock to control WDT.
The frequency of WDT_OSC is possible to be adjusted by the resistor value, so that FAST Timeout / SLOW Timeout is changed by that.
WDT_OSC has the function to stop its working when the external resistor at the RTW pin is shorted or OPEN (WDT_OSC_DET). Once CLK_DET is detected, XRSTOUT becomes Low.

Oscillator (CLK_DET)
This block monitors both DIGITAL_OSC and WDT_OSC.
2 OSCs always monitor their frequency each other and it leads to the higher reliability.
When an error happened at the monitoring, XRSTOUT becomes Low.

Over Voltage Detection (OVD1, OVD2, OVD3, OVD4, OVD_RST)
When input voltage goes over the threshold level, OVD is detected and the PG1, PG2, PG3 and PG4 pins are driven by Low. Detecting pins are DIN1, DIN2, DIN3 and DIN4 and RSTIN. OVD detection for the DIN1, DIN2, DIN3 and DIN4 pins causes corresponding the PG1, PG2, PG3 and PG4 pins to become Low. OVD detection for RSTIN causes the XRSTOUT pin to become Low. These output signals become High at 10 ms (Typ) after each input pin returns within the nominal voltage range. And each input has a filter in DIGITAL BLOCK, then overshoot within 50 µs (Min) is ignored.

Under Voltage Detection (UVD1, UVD2, UVD3, UVD4, UVD_RST)
When input voltage goes below the threshold level, UVD is detected and the PG1, PG2, PG3 and PG4 pins are driven by Low. Detecting pins are DIN1, DIN2, DIN3, DIN4 and RSTIN. UVD detection for the DIN1, DIN2, DIN3 and DIN4 pins causes corresponding the PG1, PG2, PG3 and PG4 pins to become Low. UVD detection for RSTIN causes the XRSTOUT pin to become Low. These output signals become High at 10 ms (Typ) after each input pin returns within the nominal voltage range. And each input has a filter in DIGITAL BLOCK, then undershoot within 50 µs (Min) is ignored.

BIST
When VDD Power on Reset (monitoring the RSTIN pin) is released, BIST is performed and self-test for DIN1, DIN2, DIN3, DIN4, RSTIN and VREF_DET comparators are executed to see if each comparator correctly toggles their High/Low output based on input level change.
BIST time (t_{BIST}) is 2 ms (Max). Once BIST ends without any errors, XRSTOUT becomes High. If an error is found during BIST, XRSTOUT keeps Low and BIST is repeated until it passes.

Watchdog Timer (WDT)
Watchdog Timer (WDT) monitors microprocessor's operation by detecting the time from both rise and fall edge of WDIN. If BIST result is abnormality, WDT does not work and XRSTOUT is kept low. WDT is activated when WDOUT=High, and both WDEN and XRSTOUT have to be High in order to get WDOUT to be High.
As long as the duty of WDIN clock is kept within "Trigger open window" in Figure 1, WDT does not detect any errors and XRSTOUT stays at High.

Description of Blocks - continued

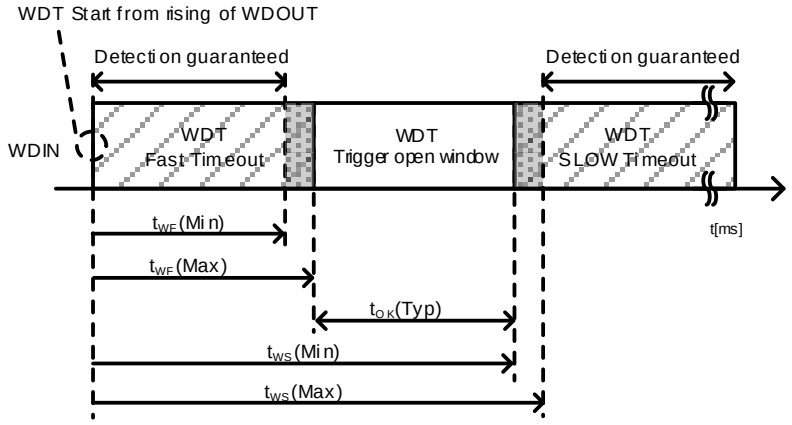


Figure 1. WDT Window Description

Sequence for FAST Timeout and SLOW Timeout are shown in Figure 2 and Figure 3.

WDT FAST Timeout Detection

1. WDIN input signal is ignored when WDOUT=Low. WDT is activated when WDOUT=High, and both WDEN and XRSTOUT have to be High in order to get WDOUT to be High.
2. For the initial duration just after WDOUT goes to High, only SLOW Timeout detection works and FAST Timeout does not work. Either Low or High input to the WDIN pin is acceptable as initial level. Once rising-up or falling-down edge of WDIN comes within SLOW Timeout, both FAST Timeout and SLOW Timeout detections start to work.
3. These time detection monitors the time until next edge and when it detects WDIN edge within FAST Timeout (t_{WF}), XRSTOUT and WDOUT becomes Low. XRSTOUT goes back to High after 10 ms (Typ) delay, while WDOUT goes back to High after t_{WDIM} (500 ms: Typ) in addition to t_{RSTL} (10 ms: Typ) as long as WDEN=High.
   t_{WDIM} is implemented as a time for microprocessor to be reset normally and stabilized.
   If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled like state 5 in the Figure 2.
   WDEN toggle during XRSTOUT=Low is ignored.
4. When WDOUT becomes High, WDT is activated again and operation resumes.
   Only SLOW Timeout detection works until the next first edge, and both SLOW Timeout and FAST Timeout starts at the first edge like state 1 in Figure 2.
5. If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled like in Figure 2. t_{WDIM} is canceled by toggling WDEN like High->Low->High and WDT is activated immediately even during t_{WDIM}.
   After WDT is enabled it works as same as state 2 in Figure 2.
6. When WDEN is Low, WDOUT becomes Low and WDT is disabled. During this period WDIN input signal is ignored and XRSTOUT output is not affected by that.

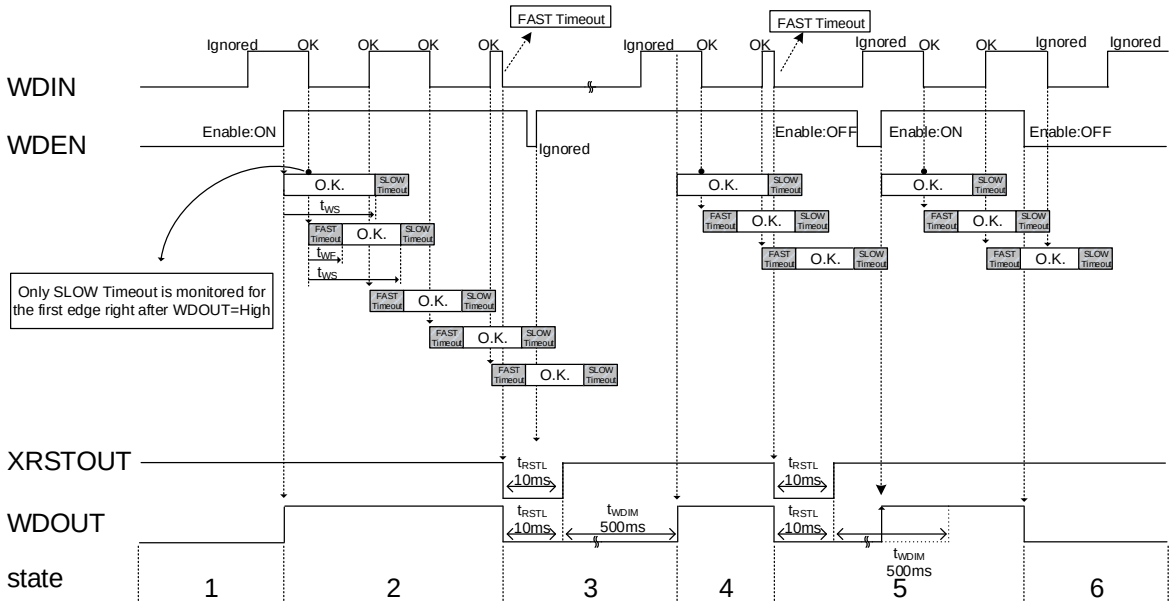


Figure 2. WDT FAST Timeout Detection

Block Diagrams - continued

WDT SLOW Timeout Detection

1. WDIN input signal is ignored when WDOUT=Low. WDT is activated when WDOUT=High, and both WDEN and XRSTOUT have to be High in order to get WDOUT to be High.
2. For the initial duration just after WDOUT goes to High, only SLOW Timeout detection works and FAST Timeout does not work. Either Low or High input to the WDIN pin is acceptable as initial level. Once rising-up or falling-down edge of WDIN comes within SLOW Timeout, both FAST Timeout and SLOW Timeout detections start to work.
3. These time detection monitors the time until next edge and when it can not detect WDIN edge within SLOW Timeout (t_{WS}), XRSTOUT and WDOUT becomes Low. XRSTOUT goes back to High after 10 ms (Typ) delay, while WDOUT goes back to High after t_{WDIM} (500 ms: Typ) in addition to t_{RSTL} (10 ms: Typ) as long as WDEN=High.
   t_{WDIM} is implemented as a time for microprocessor to be reset normally and stabilized.
   If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled like state 5 in the Figure 3.
   WDEN toggle during XRSTOUT=Low is ignored.
4. When WDOUT becomes High, WDT is activated again and operation resumes.
   Only SLOW Timeout detection works until the next first edge, and both SLOW Timeout and FAST Timeout starts at the first edge like state 1 in Figure 3.
5. If this time is unnecessary and WDT should be activated as soon as possible, WDEN may be controlled like the Figure 3.
   t_{WDIM} is canceled by toggling WDEN like High->Low->High and WDT is activated immediately even during t_{WDIM}.
   After WDT is enabled it works as same as state 2 in Figure3.
6. When WDEN is Low, WDOUT becomes Low and WDT is disabled. During this period WDIN input signal is ignored and XRSTOUT output is not affected by that.

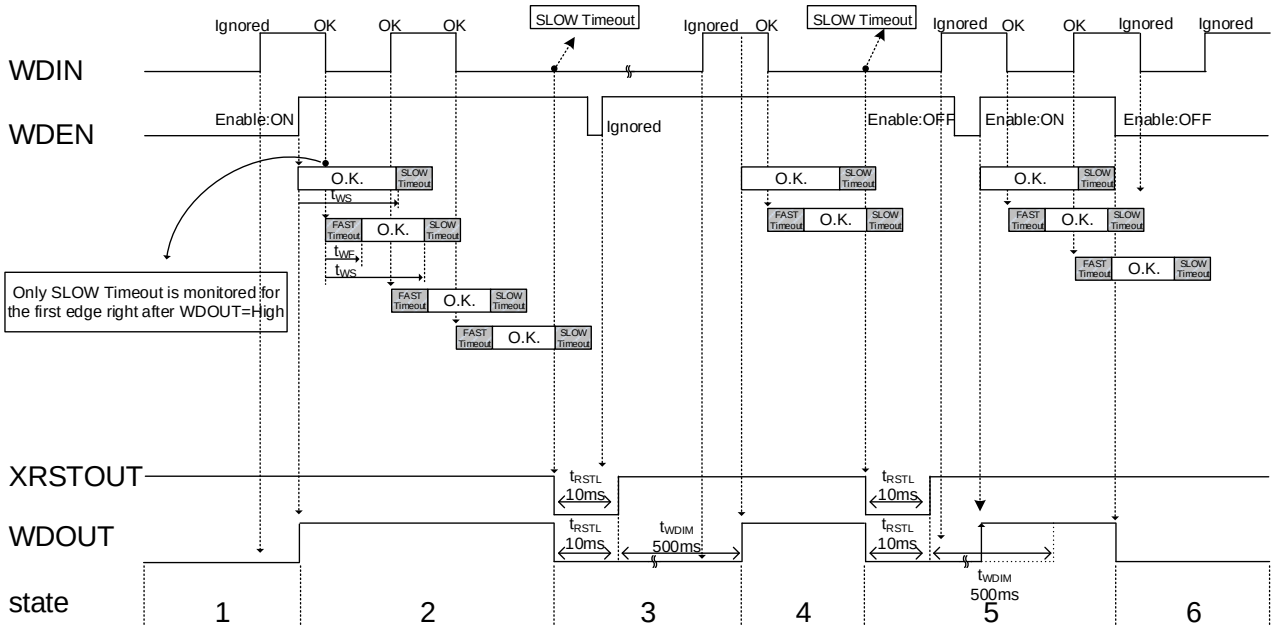


Figure 3. WDT SLOW Timeout Detection

WDT SLOW Timeout Detection - continued

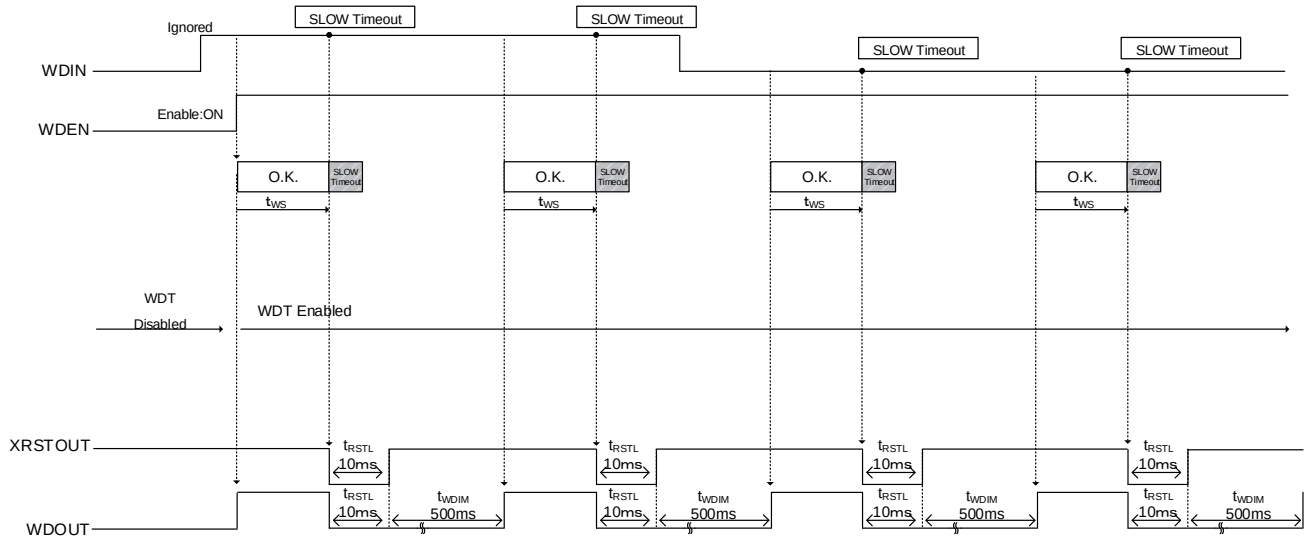


Figure 4. XRSTOUT Behavior with Continuous WDT Timeout Detected

The window time for detection can be changed by the resistor value between the RTW and GND pins. Following figure shows the detection time determined by R_{RTW} resistor value. Please refer to a table of electric characteristic regarding accuracy. Customer can choose the value ranging from 10 kΩ to 47 kΩ according to their clock frequency. The ratio for detection time is fixed and can be shown like this, FAST Timeout : SLOW Timeout = 1 : 2.

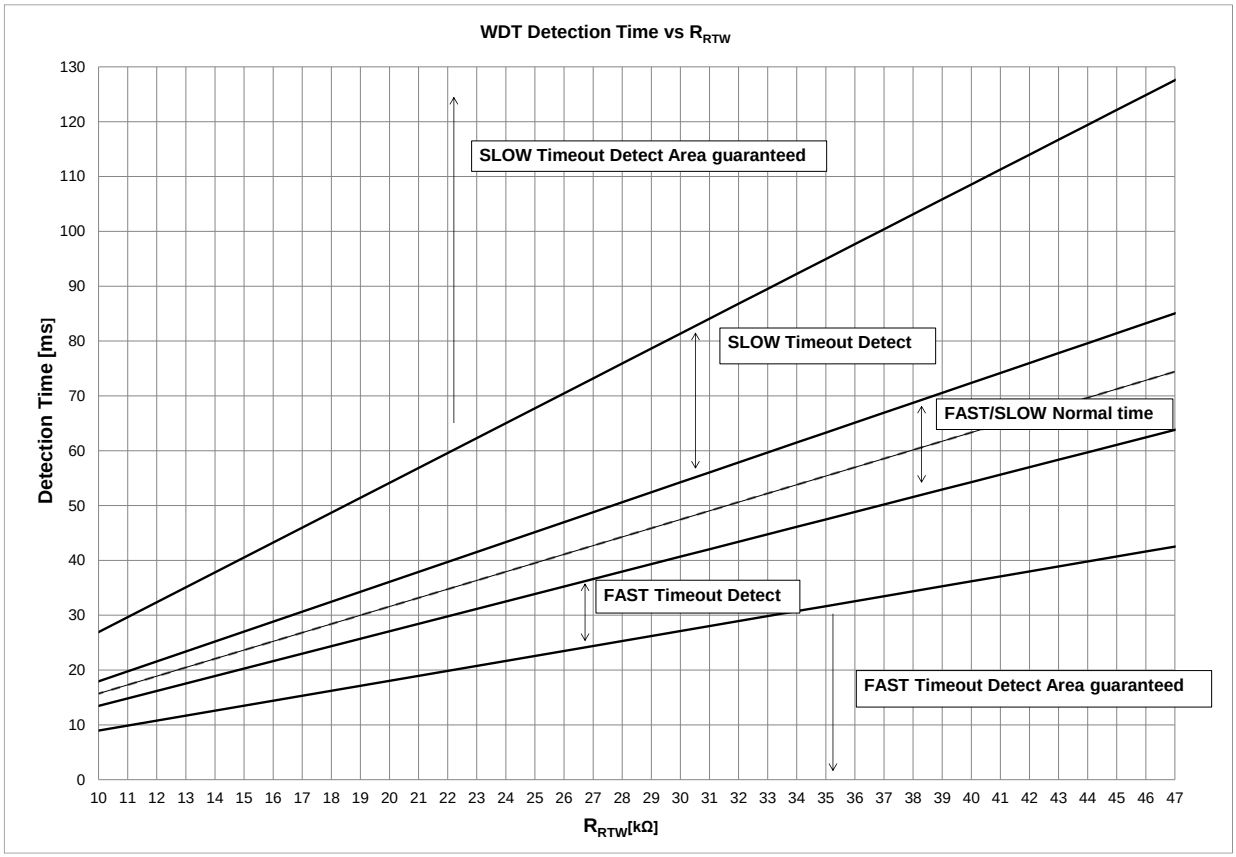


Figure 5. Detection Time vs R_{RTW}

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
VDD Voltage	V_{DD}	-0.3 to +7	V
RSTIN Voltage	V_{RSTIN}	-0.3 to +7	V
DIN1,DIN2,DIN3,DIN4 Voltage	V_{DIN1}, V_{DIN2}, V_{DIN3}, V_{DIN4}	-0.3 to +7	V
XRSTOUT Voltage	$V_{XRSTOUT}$	-0.3 to +7	V
PG1,PG2,PG3,PG4 Voltage	V_{PG1}, V_{PG2}, V_{PG3}, V_{PG4}	-0.3 to +7	V
WDIN Voltage	V_{WDIN}	-0.3 to +7	V
WDEN Voltage	V_{WDEN}	-0.3 to +7	V
WDOUT Voltage	V_{WDOUT}	-0.3 to V_{DD}+0.3	V
RTW Voltage	V_{RTW}	-0.3 to V_{DD}+0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN16FV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23	10	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	-	+125	°C
VDD Voltage	V_{DD}	2.7	-	5.5	V
WDIN Input Pulse Width	t_{WDIN}	10	-	125	ms
WDIN Minimum ON Pulse / OFF Pulse	t_{WDP}	-	-	100	µs

Electrical Characteristics (Unless otherwise specified V_{DD}=2.7 V to 5.5 V, -40 °C ≤ Ta ≤ +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
All						
Circuit Current	I_{VDD}	440	785	1320	µA	V_{DD}=4.1 V, R_{RTW}=27 kΩ, XRSTOUT,PG1,PG2,PG3,PG4=H
VDD Power On Reset Threshold Voltage (Falling)	V_{VDDUV1}	2.25	2.50	2.65	V	VDD monitor
VDD Power On Reset Threshold Voltage (Rising)	V_{VDDUV2}	2.30	2.55	2.70	V	VDD monitor
VDD Power On Reset Hysteresis	V_{VDDHYS}	-	50	-	mV	
Power Good						
DIN1 Power Good Low Detect Voltage	V_{UVD1}	0.698	0.720	0.742	V	DIN1 Pin Voltage=Sweep down
DIN1 Power Good High Detect Voltage	V_{OVD1}	0.854	0.880	0.906	V	DIN1 Pin Voltage=Sweep up
DIN1 Input Filter Time	t_{DIN1}	50	75	100	µs	
PG1 Low Voltage	V_{PG1L}	-	-	0.3	V	I_{PG1}=1 mA
PG1 Leak Current	I_{LPG1}	-	-	2	µA	V_{PG1}=5.5 V
PG1 Assertion Delay Time	t_{PG1}	7	10	13	ms	
DIN2 Power Good Low Detect Voltage	V_{UVD2}	0.698	0.720	0.742	V	DIN2 Pin Voltage=Sweep down
DIN2 Power Good High Detect Voltage	V_{OVD2}	0.854	0.880	0.906	V	DIN2 Pin Voltage=Sweep up
DIN2 Input Filter Time	t_{DIN2}	50	75	100	µs	
PG2 Low Voltage	V_{PG2L}	-	-	0.3	V	I_{PG2}=1 mA
PG2 Leak Current	I_{LPG2}	-	-	2	µA	V_{PG2}=5.5 V
PG2 Assertion Delay Time	t_{PG2}	7	10	13	ms	
DIN3 Power Good Low Detect Voltage	V_{UVD3}	0.698	0.720	0.742	V	DIN3 Pin Voltage=Sweep down
DIN3 Power Good High Detect Voltage	V_{OVD3}	0.854	0.880	0.906	V	DIN3 Pin Voltage=Sweep up
DIN3 Input Filter Time	t_{DIN3}	50	75	100	µs	
PG3 Low Voltage	V_{PG3L}	-	-	0.3	V	I_{PG3}=1 m A
PG3 Leak Current	I_{LPG3}	-	-	2	µA	V_{PG3}=5.5 V
PG3 Assertion Delay Time	t_{PG3}	7	10	13	ms	
DIN4 Power Good Low Detect Voltage	V_{UVD4}	0.698	0.720	0.742	V	DIN4 Pin Voltage=Sweep down
DIN4 Power Good High Detect Voltage	V_{OVD4}	0.854	0.880	0.906	V	DIN4 Pin Voltage=Sweep up
DIN4 Input Filter Time	t_{DIN4}	50	75	100	µs	
PG4 Low Voltage	V_{PG4L}	-	-	0.3	V	I_{PG4}=1 mA
PG4 Leak Current	I_{LPG4}	-	-	2	µA	V_{PG4}=5.5 V
PG4 Assertion Delay Time	t_{PG4}	7	10	13	ms	

Electrical Characteristics (Unless otherwise specified V_{DD}=2.7 V to 5.5 V, -40 °C ≤ Ta ≤ +125 °C) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD Power On Reset						
RSTIN Power Good Low Detect Voltage	V_{UVDRST}	0.698	0.720	0.742	V	RSTIN Pin Voltage=Sweep down
RSTIN Power Good High Detect Voltage	V_{OVDRST}	0.854	0.880	0.906	V	RSTIN Pin Voltage=Sweep up
RSTIN Input Filter Time	t_{RSTIN}	50	75	100	µs	
XRSTOUT Low Voltage	V_{XRSTL}	-	-	0.3	V	I_{VDDRST}=1 mA
XRSTOUT Leak Current	I_{XRST}	-	-	10	µA	V_{VDDRST}=5.5 V
XRSTOUT Assertion Delay Time	t_{XRSTL}	7	10	13	ms	
Watch Dog Timer						
FAST Timeout Detect1	t_{WF1}	9.0	11.2	13.5	ms	R_{RTW}=10 kΩ
SLOW Timeout Detect1	t_{WS1}	17.9	22.4	26.9	ms	R_{RTW}=10 kΩ
FAST/SLOW Normal Time1	t_{OK1}	13.6	15.7	17.8	ms	R_{RTW}=10 kΩ
FAST Timeout Detect2	t_{WF2}	24.4	30.5	36.6	ms	R_{RTW}=27 kΩ
SLOW Timeout Detect2	t_{WS2}	48.8	61.0	73.2	ms	R_{RTW}=27 kΩ
FAST/SLOW Normal Time2	t_{OK2}	36.7	42.7	48.7	ms	R_{RTW}=27 kΩ
FAST Timeout Detect3	t_{WF3}	42.5	53.2	63.8	ms	R_{RTW}=47 kΩ
SLOW Timeout Detect3	t_{WS3}	85.0	106.3	127.6	ms	R_{RTW}=47 kΩ
FAST/SLOW Normal Time3	t_{OK3}	63.9	74.4	84.9	ms	R_{RTW}=47 kΩ
WDIN Detect Minimum Pulse Width	t_{WDIN}	20	-	-	µs	
WDIN Initial Mask Time	t_{WDIM}	325	500	675	ms	
WDIN Pull-down Resistor Value	R_{WDIN}	50	100	150	kΩ	V_{DD}<5 V
WDIN Low Level Input Voltage	V_{WDINL}	-	-	0.2 x V_{DD}	V	
WDIN High Level Input Voltage	V_{WDINH}	0.8 x V_{DD}	-	-	V	
WDEN Pull-down Resistor Value	R_{WDEN}	50	100	150	kΩ	V_{DD}<5 V
WDEN Low Level Input Voltage	V_{WDENL}	-	-	0.2 x V_{DD}	V	
WDEN High Level Input Voltage	V_{WDENH}	0.8 x V_{DD}	-	-	V	
WDOUT Output High Voltage	V_{OHWDO}	V_{DD} -0.3	-	-	V	I_{WDOUT}=-3 mA
WDOUT Output Low Voltage	V_{OLWDO}	-	-	0.3	V	I_{WDOUT}=+3 mA

Typical Performance Curves

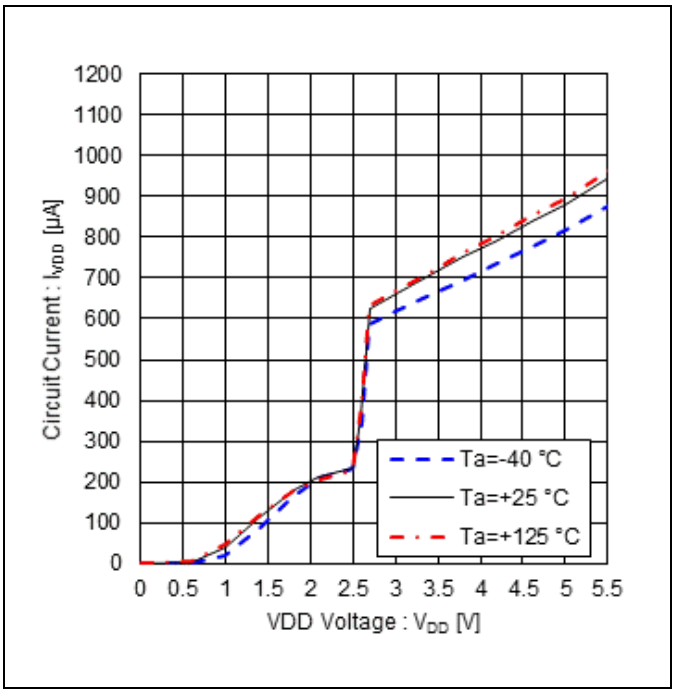


Figure 6. Circuit Current vs VDD Voltage

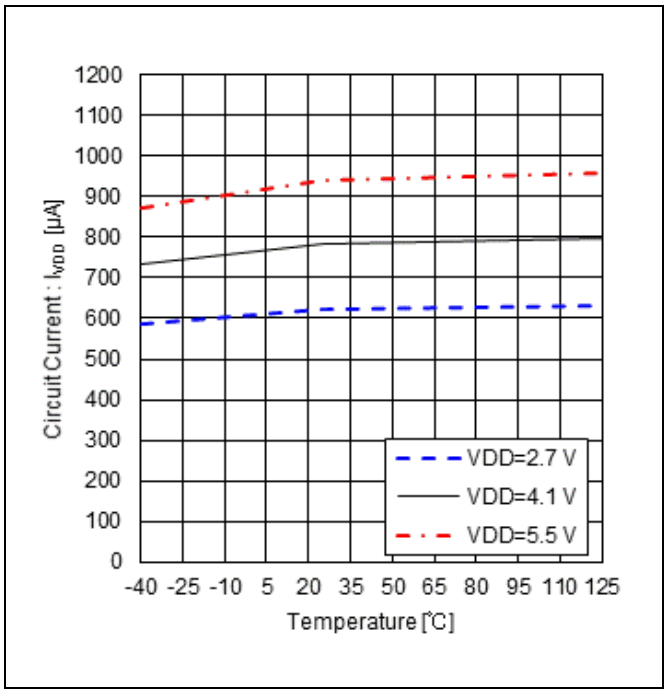


Figure 7. Circuit Current vs Temperature

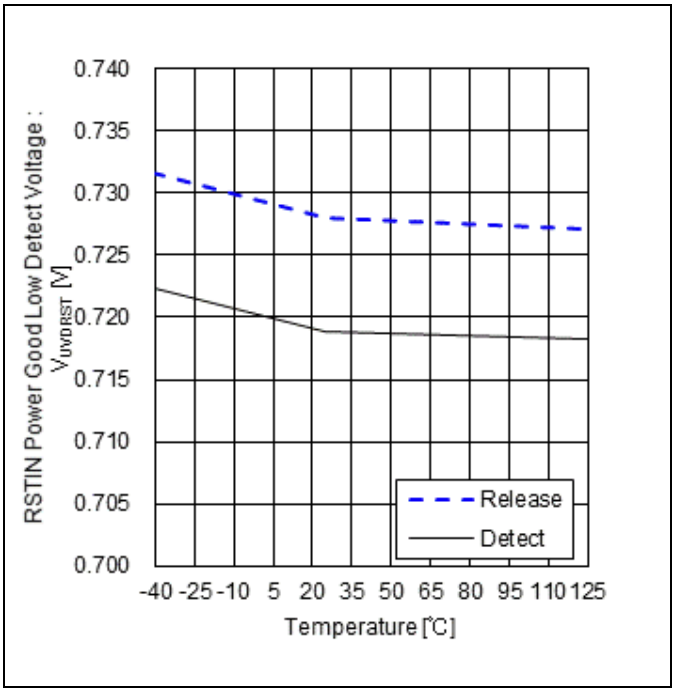


Figure 8. RSTIN Power Good Low Detect Voltage vs Temperature
(“RSTIN UVD”, V_{DD}=3.3 V)

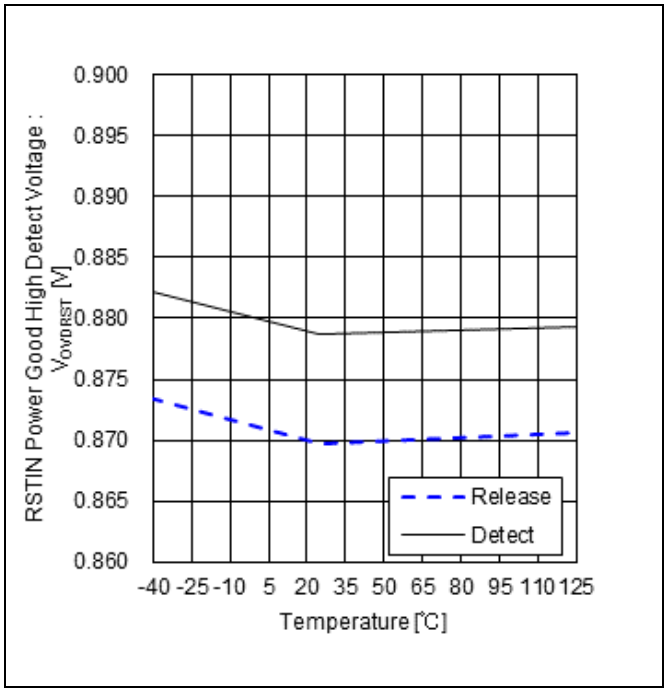


Figure 9. RSTIN Power Good High Detect Voltage vs Temperature
(“RSTIN OVD”, V_{DD}=3.3 V)

Typical Performance Curves - continued

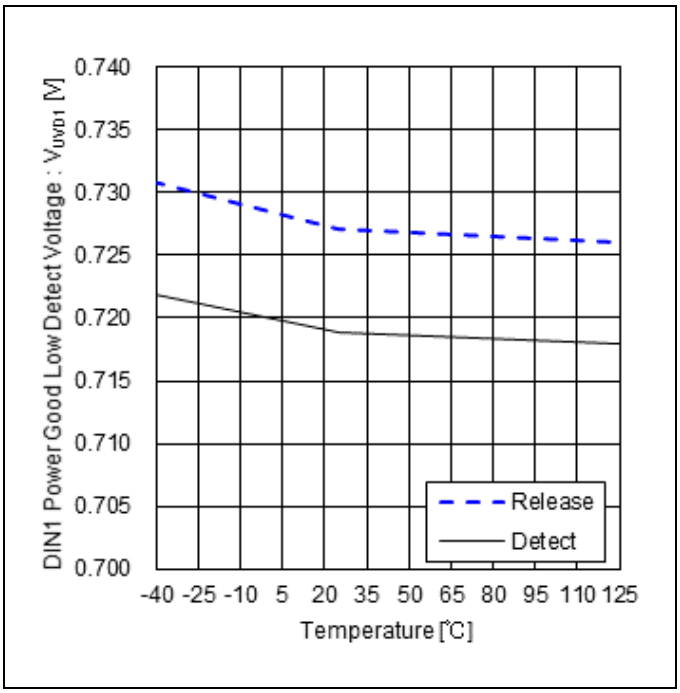


Figure 10. DIN1 Power Good Low Detect Voltage vs Temperature ("DIN1 UVD", V_{DD}=3.3 V)

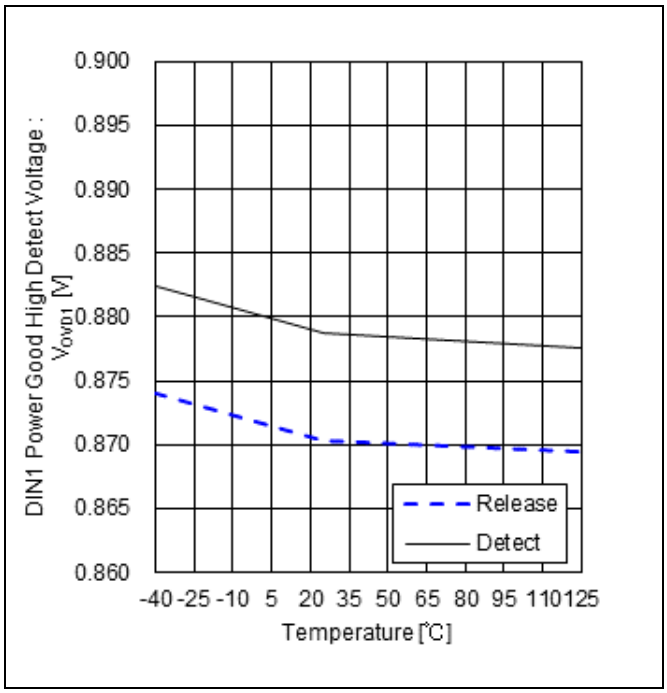


Figure 11. DIN1 Power Good High Detect Voltage vs Temperature ("DIN1 OVD", V_{DD}=3.3 V)

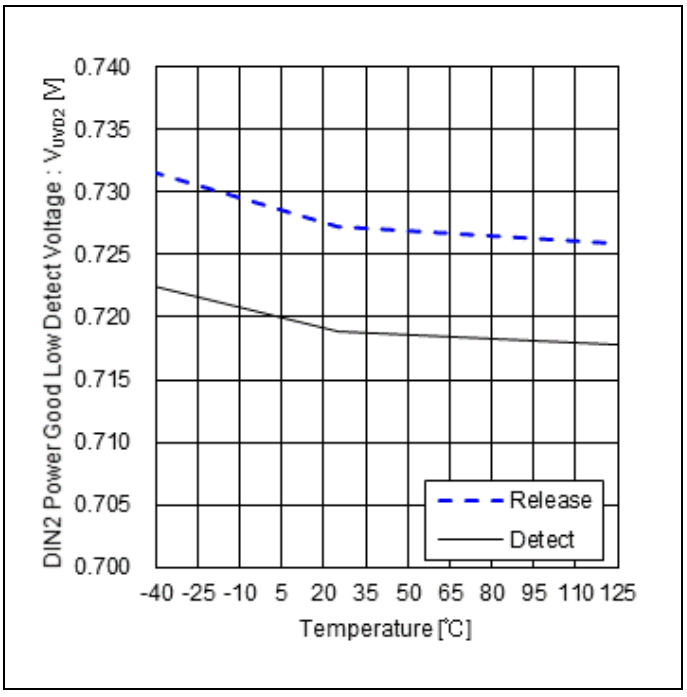


Figure 12. DIN2 Power Good Low Detect Voltage vs Temperature ("DIN2 UVD", V_{DD}=3.3 V)

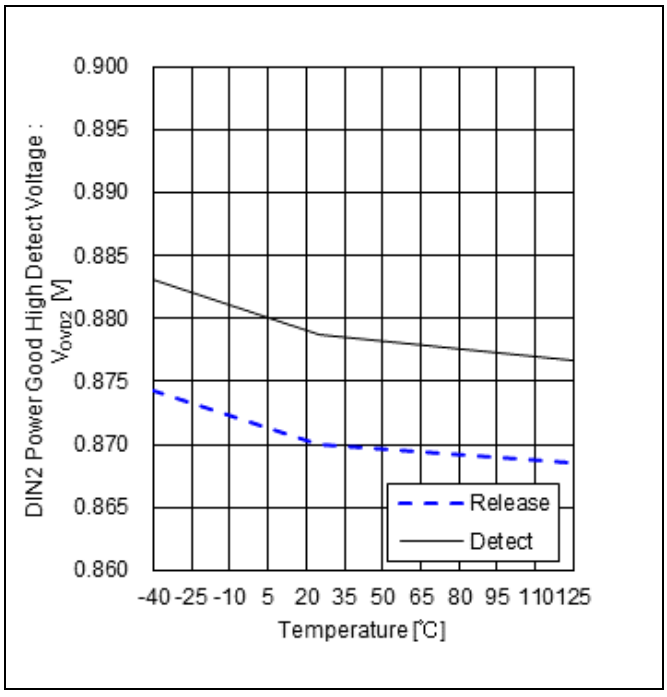


Figure 13. DIN2 Power Good High Detect Voltage vs Temperature ("DIN2 OVD", V_{DD}=3.3 V)

Typical Performance Curves - continued

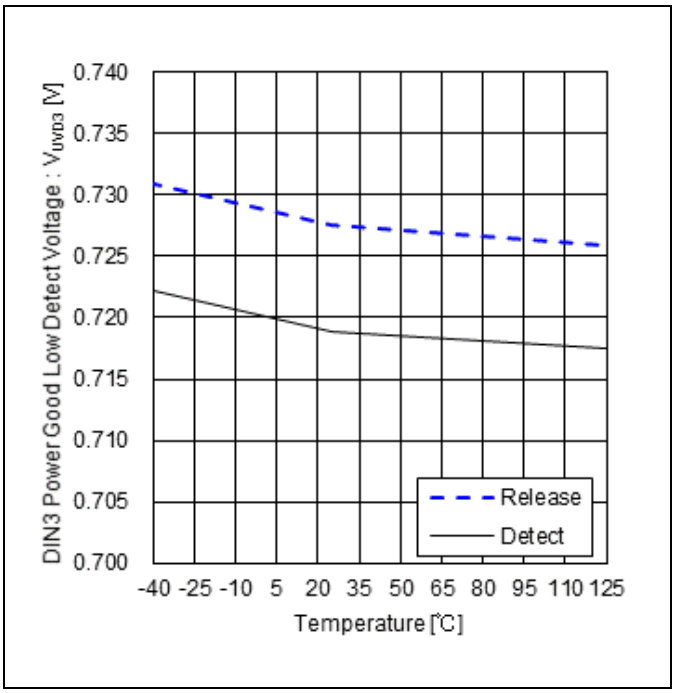


Figure 14. DIN3 Power Good Low Detect Voltage vs Temperature ("DIN3 UVD", V_{DD}=3.3 V)

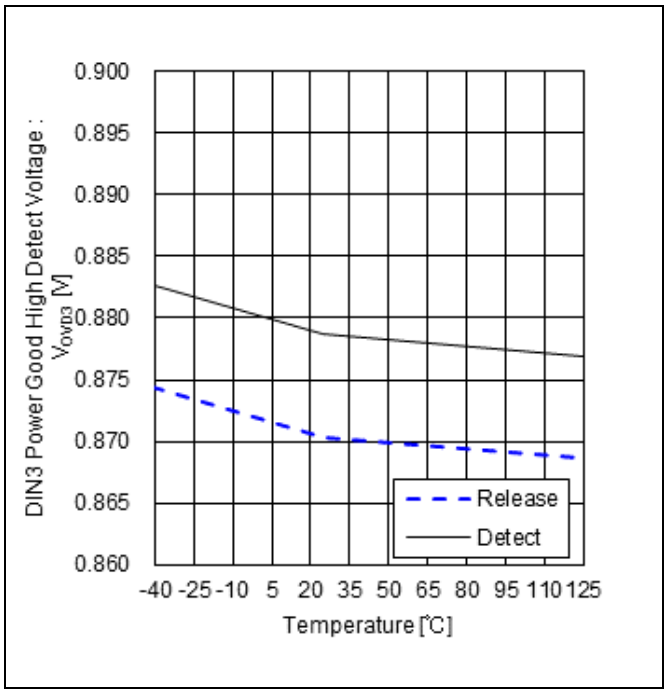


Figure 15. DIN3 Power Good High Detect Voltage vs Temperature ("DIN3 OVD", V_{DD}=3.3 V)

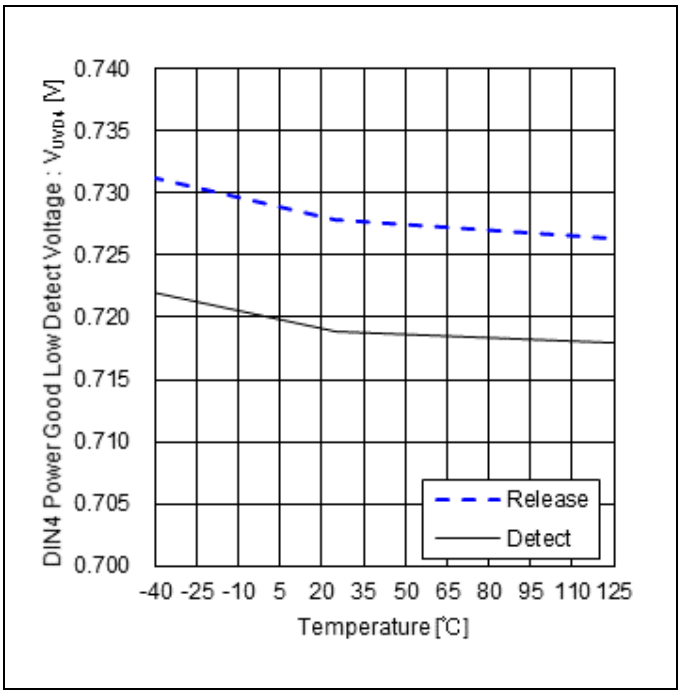


Figure 16. DIN4 Power Good Low Detect Voltage vs Temperature ("DIN4 UVD", V_{DD}=3.3 V)

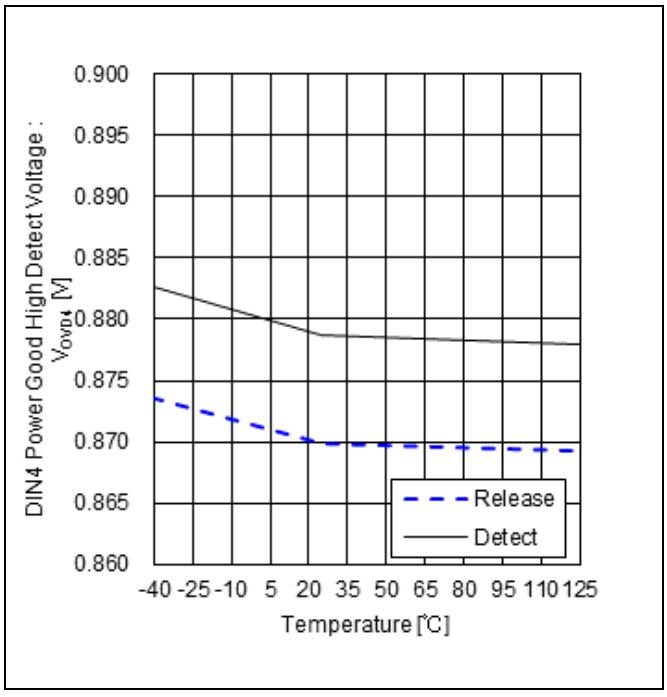


Figure 17. DIN4 Power Good High Detect Voltage vs Temperature ("DIN4 OVD", V_{DD}=3.3 V)

Typical Performance Curves - continued

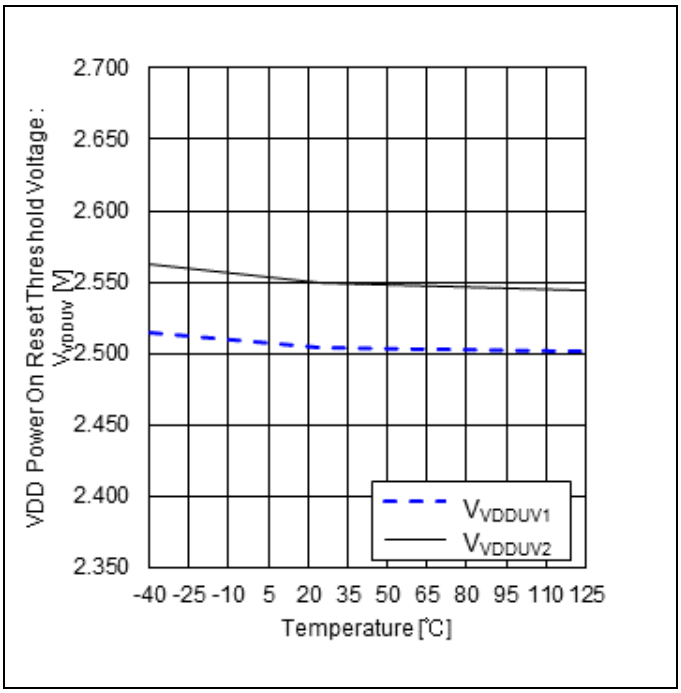


Figure 18. VDD Power On Reset Threshold Voltage vs Temperature

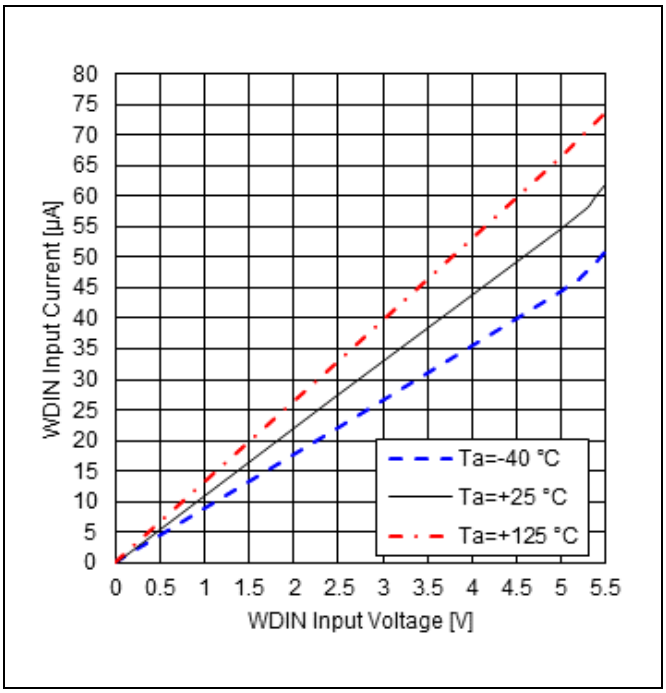


Figure 19. WDIN Input Current vs WDIN Input Voltage ("WDIN Pull-down Resistor Value", V_{DD}=3.3 V)

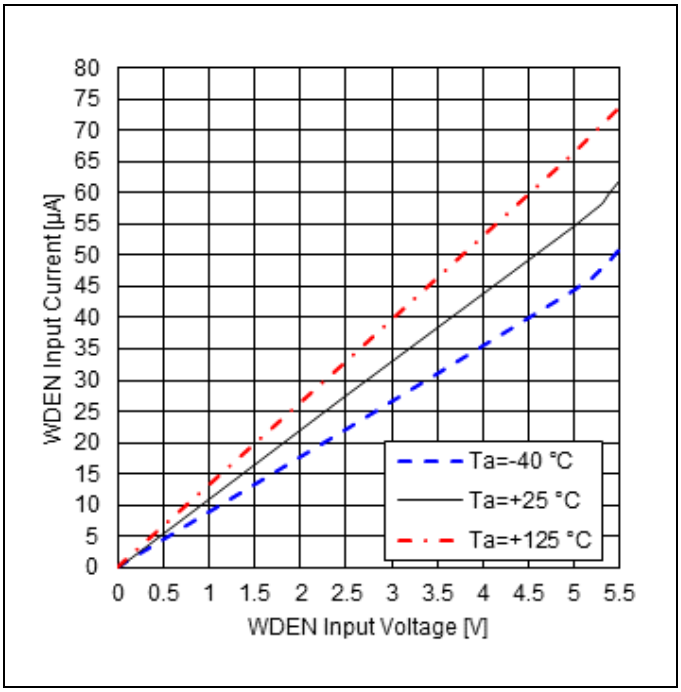


Figure 20. WDEN Input Current vs WDEN Input Voltage ("WDEN Pull-down Resistor Value", V_{DD}=3.3 V)

Timing Chart

Figure 21 shows ON/OFF normal sequence.
When UVLO (2.55 V) monitoring the VDD pin is released, internal OSC for DIGITAL BLOCK starts to work. Then after RSTIN voltage reaches UVD release (adjustable), BIST starts to do self-test. If the BIST is normal, XRSTOUT goes to High at 10 ms after RSTIN UVD released. If the BIST is abnormal, XRSTOUT, PG1 to PG4 and WDOUT stays at Low.
XRSTOUT goes to Low when either of 2 monitoring functions (RSTIN UVD or Watchdog Timer) is detected.
WDT block has initial mask time (Typ 500 ms). Even though High voltage is given to WDEN within this time from RSTIN UVD released, WDT is not enabled. For example, as Figure 22 shows, in WDEN tied to VDD case WDT is enabled 500 ms after RSTIN UVD released.
WDEN input signal works as an enable of Watchdog Timer. Even though clocks are input to the WDIN pin, they are ignored as long as WDEN=Low. WDOUT is just a buffered version output of WDEN input and processor can use this output to confirm if WDEN is correctly controlled by itself.

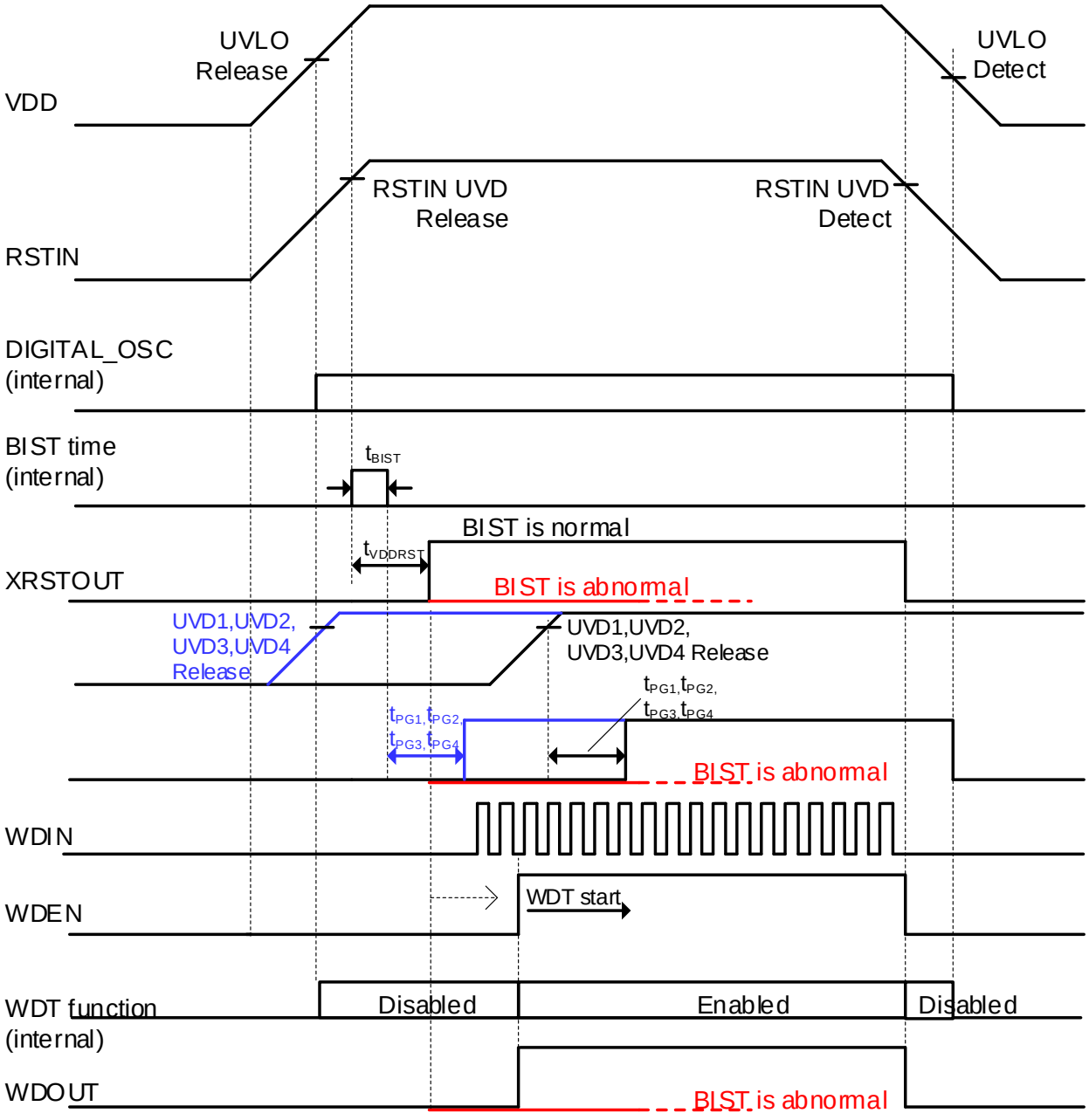


Figure 21. Power ON/OFF Normal Sequence (WDEN is controlled by external signal)

Timing Chart - continued

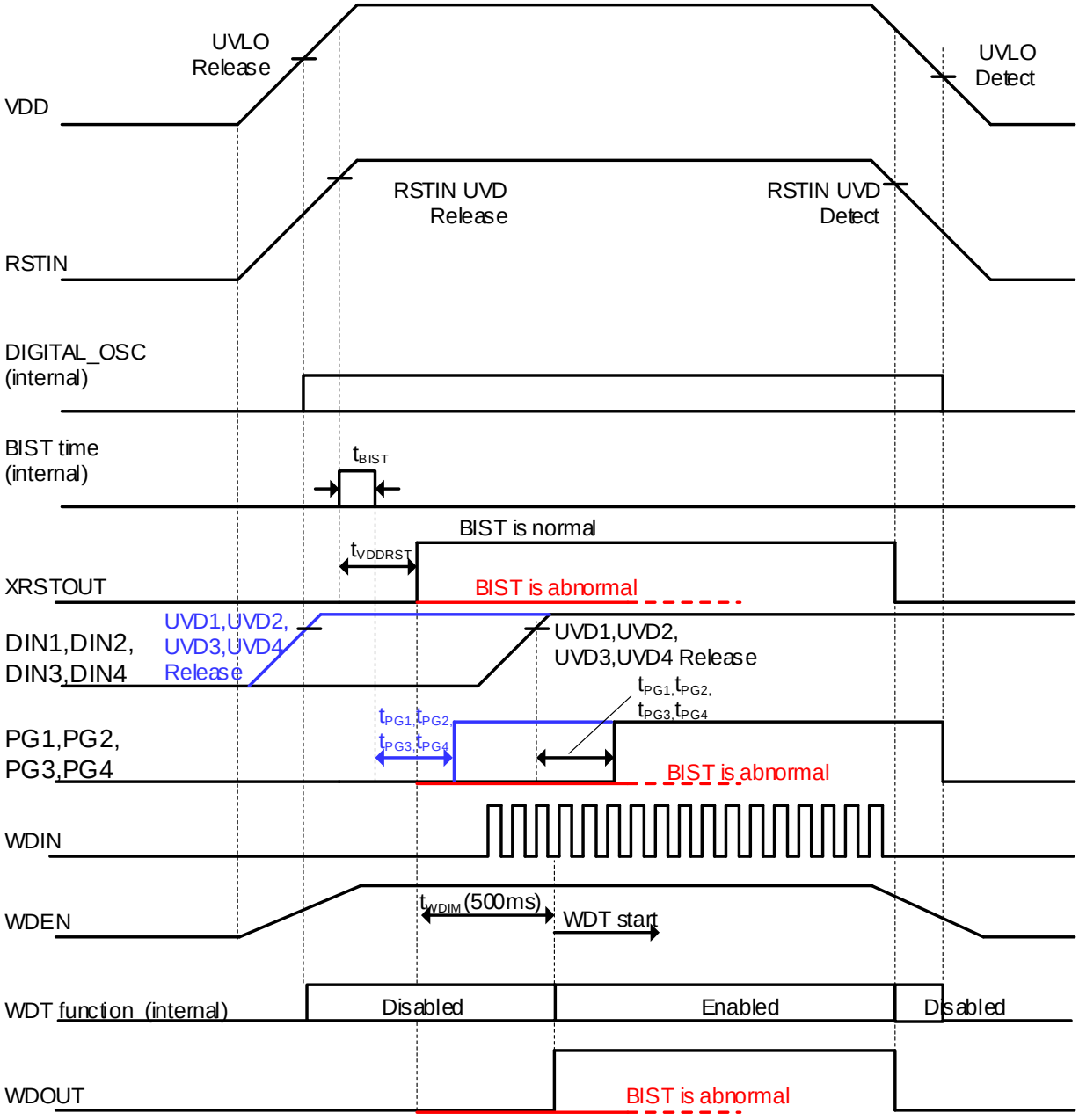


Figure 22. Power ON/OFF Sequence (WDEN is externally pulled-up to VDD)

Timing Chart - continued

Figure 23 shows monitoring sequence with VDD POR, DIN1, DIN2, DIN3 and DIN4 voltage detection and WDT monitoring. XRSTOUT is qualified by either of RSTIN (VDD POR) and WDIN (WDT) and outputs Low level voltage when these are detected.
When WDEN becomes Low, WDOUT goes to Low and WDT stops to work immediately.
PG1, PG2, PG3 and PG4 are de-asserted immediately de-bounce time by internal DIGITAL de-bounce filter when the corresponding DIN1, DIN2, DIN3 and DIN4 input voltage goes out of PG window (±10 %). PG1, PG2, PG3 and PG4 are asserted at 10 ms after DIN1, DIN2, DIN3 and DIN4 input voltage becomes inside PG window.

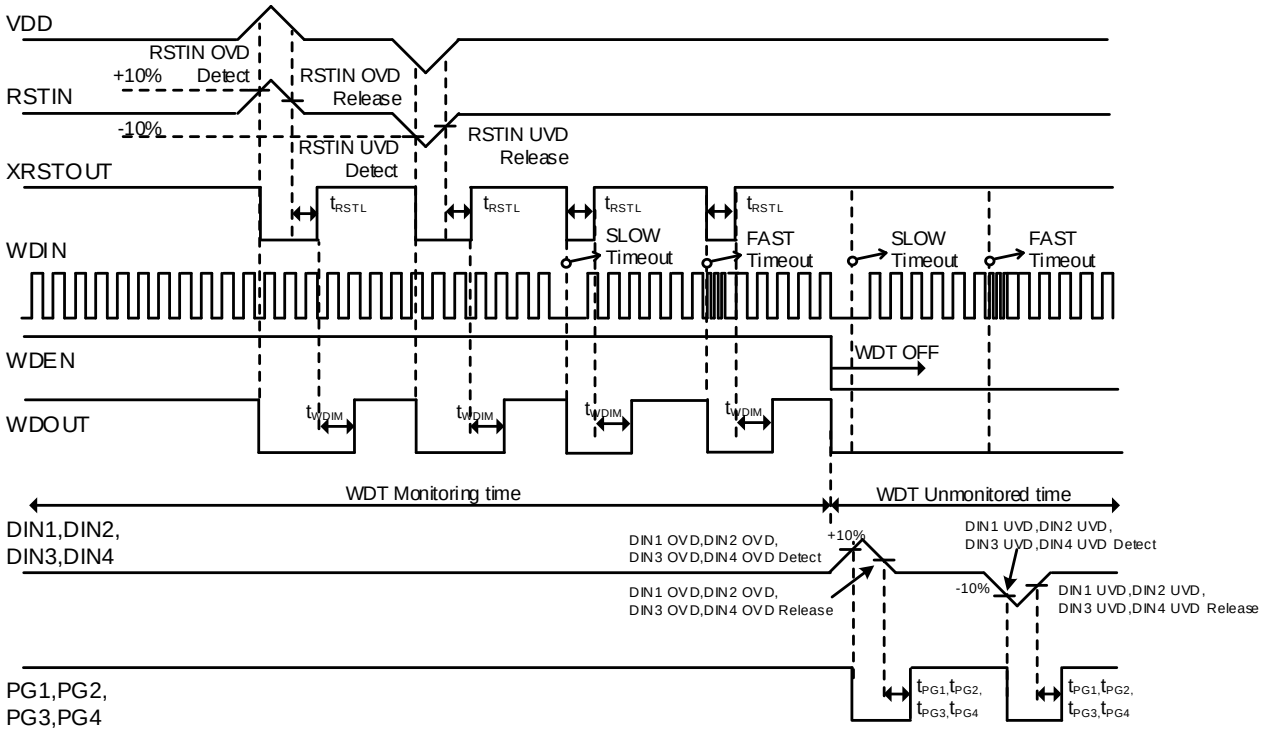


Figure 23. Monitoring Sequence 1

Timing Chart - continued

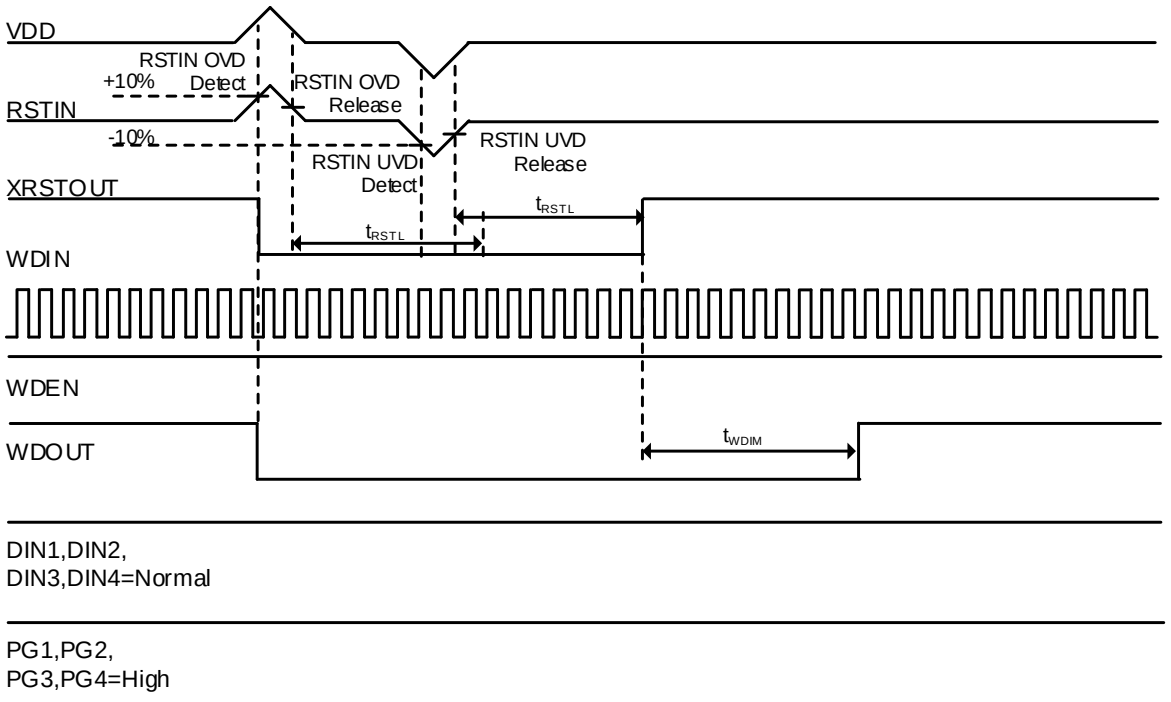


Figure 24. Monitoring Sequence 2 (2nd reset factor appears and disappears within t_{RSTL})

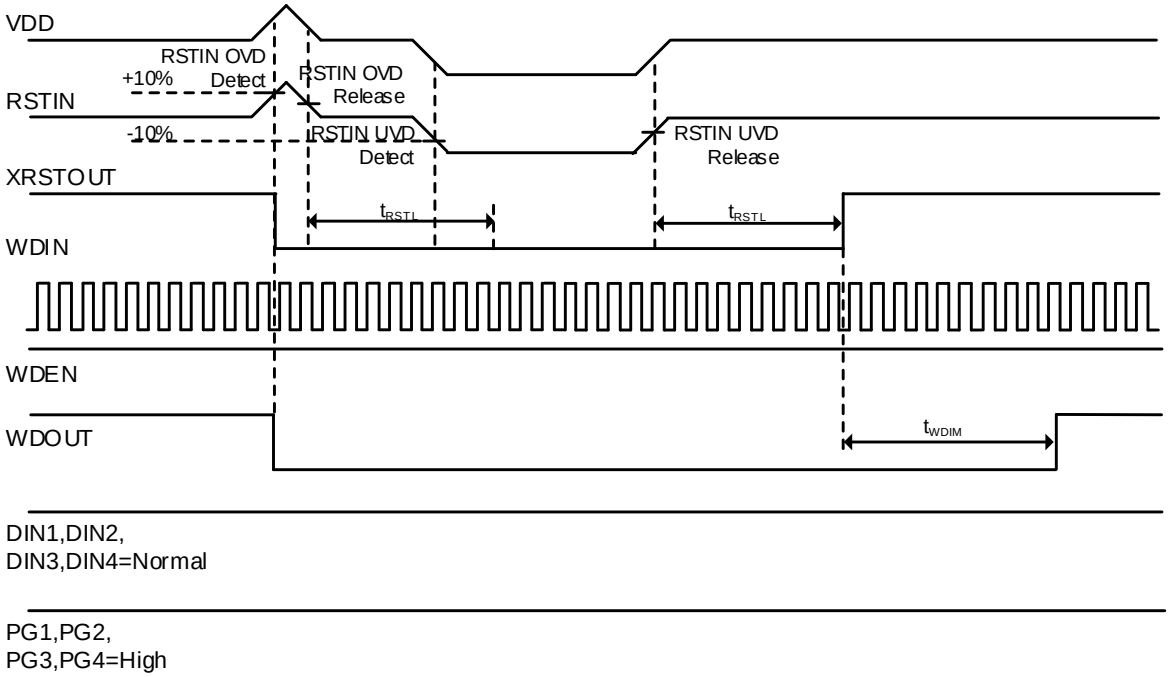


Figure 25. Monitoring Sequence 3 (2nd reset factor appears within t_{RSTL} and disappear after t_{RSTL})

Application Example

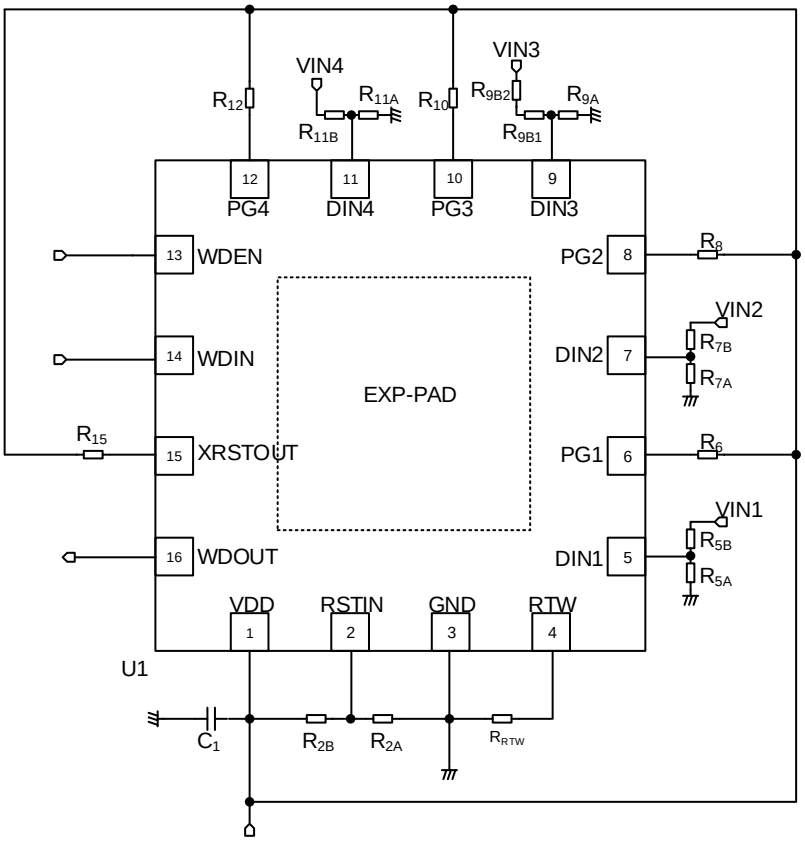


Figure 26. Typical Application Schematic

Example of Constant Setting

V_{DD}=3.3 V, R_{RTW}=27 kΩ, VIN1=3.3 V, VIN2=1.8 V, VIN3=1.5 V, VIN4=1.2 V

Item	Value	Unit	Parts Number	Vendor
U1	-	-	BD39040MUF-C	ROHM
C_1	0.22	μF	GCM188R71C224KA01	MURATA
R_{2A}	24	kΩ	MCR01MZPD2402	ROHM
R_{2B}	75	kΩ	MCR01MZPD7502	ROHM
R_{RTW}	27	kΩ	MCR01MZPD2702	ROHM
R_{5A}	24	kΩ	MCR01MZPD2402	ROHM
R_{5B}	75	kΩ	MCR01MZPD7502	ROHM
R_6	10	kΩ	MCR01MZPD1002	ROHM
R_{7A}	24	kΩ	MCR01MZPD2402	ROHM
R_{7B}	30	kΩ	MCR01MZPD3002	ROHM
R_8	10	kΩ	MCR01MZPD1002	ROHM
R_{9A}	24	kΩ	MCR01MZPD2402	ROHM
R_{9B1}	10	kΩ	MCR01MZPD1002	ROHM
R_{9B2}	11	kΩ	MCR01MZPD1102	ROHM
R_{10}	10	kΩ	MCR01MZPD1002	ROHM
R_{11A}	20	kΩ	MCR01MZPD2002	ROHM
R_{11B}	10	kΩ	MCR01MZPD1002	ROHM
R_{12}	10	kΩ	MCR01MZPD1002	ROHM
R_{15}	10	kΩ	MCR01MZPD1002	ROHM

Application Example - continued

Procedure for Selecting Application Components

(1) Selecting input capacitor (C_1)
Place a ceramic capacitor connect to GND nearest the IC for the VDD pin.
Please consider temperature change, DC bias characteristics and dispersion enough, and it is necessary to choose the product superior (over 0.1 µF at least) in thermal characteristics such as B characteristics or X7R characteristics.
The capacitor 1.5 times to 2 times larger than a limit is recommended about the pressure-resistant.

(2) Selecting a resistor of input pin (R_{2A}, R_{2B}, R_{5A}, R_{5B}, R_{7A}, R_{7B}, R_{9A}, R_{9B1}, R_{9B2}, R_{11A}, R_{11B})
Set a resistor divider voltage 0.8 V to input voltage V_{DD}, VIN1, VIN2, VIN3, VIN4.

$$\mathrm{RSTIN} = 0.8\,V = V_{DD} \times \frac{R_{2A}}{R_{2A} + R_{2B}}$$

$$\mathrm{DIN1} = 0.8\,V = \mathrm{VIN1} \times \frac{R_{5A}}{R_{5A} + R_{5B}}$$

$$\mathrm{DIN2} = 0.8\,V = \mathrm{VIN2} \times \frac{R_{7A}}{R_{7A} + R_{7B}}$$

$$\mathrm{DIN3} = 0.8\,V = \mathrm{VIN3} \times \frac{R_{9A}}{R_{9A} + R_{9B1} + R_{9B2}}$$

$$\mathrm{DIN4} = 0.8\,V = \mathrm{VIN4} \times \frac{R_{11A}}{R_{11A} + R_{11B}}$$

(3) Selecting a resistor of output pin (R_6, R_8, R_{10}, R_{12}, R_{15})
Set more than 10 kΩ pull-up resistor connects to the VDD pin.
Please consider thermal characteristics and dispersion enough, and it is necessary to choose a resistor over 7.5 kΩ.
The PG1 to PG4 pins can be connected and used to OR output. In this case also, choose total impedance over 7.5 kΩ.

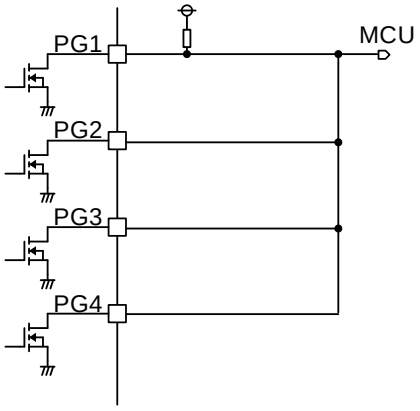


Figure 27. PG1, PG2, PG3, PG4 OR Output

(4) Selecting WDT (R_{RTW})
Place a resistor nearest GND for the RTW pin.
Change RTW resistor value enables WDT setting time change. Settable range is 10 kΩ to 47 kΩ.
Please consider thermal characteristics and dispersion enough, and it is necessary to choose component under ±1.0 %.
Refer to Figure 5 for the setting time.

(5) Expose thermal pad
The exposed thermal pad is highly recommended for GND connection.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes - continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

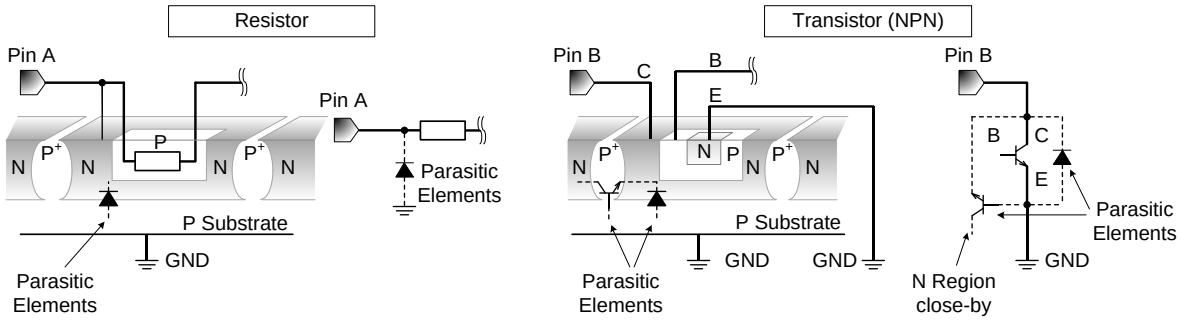
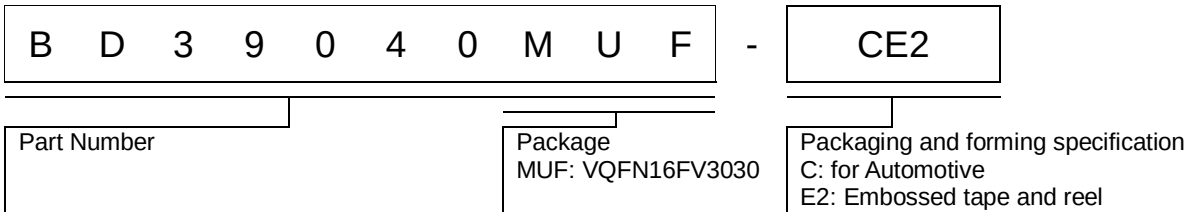


Figure 28. Example of Monolithic IC Structure

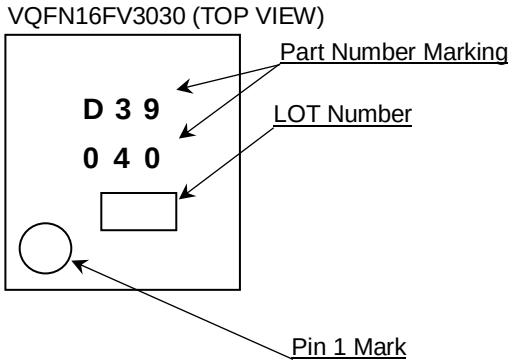
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

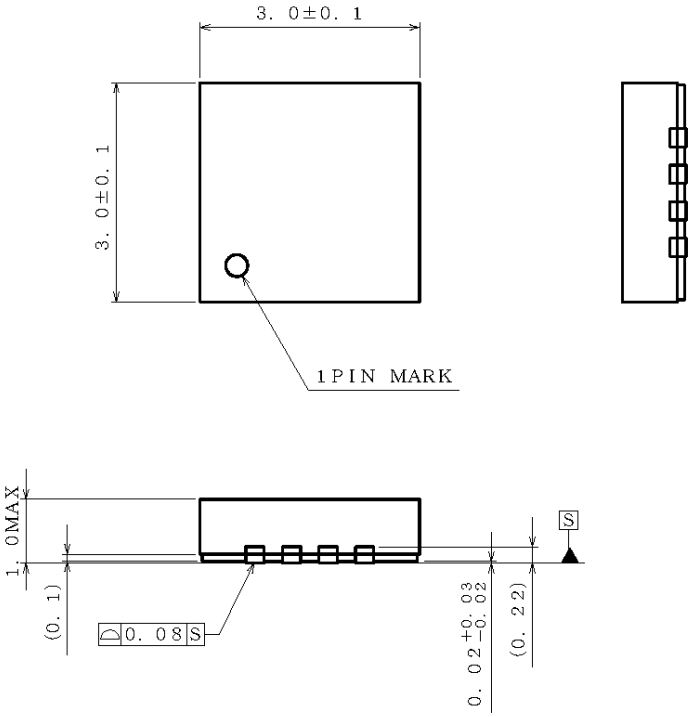


Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN16FV3030

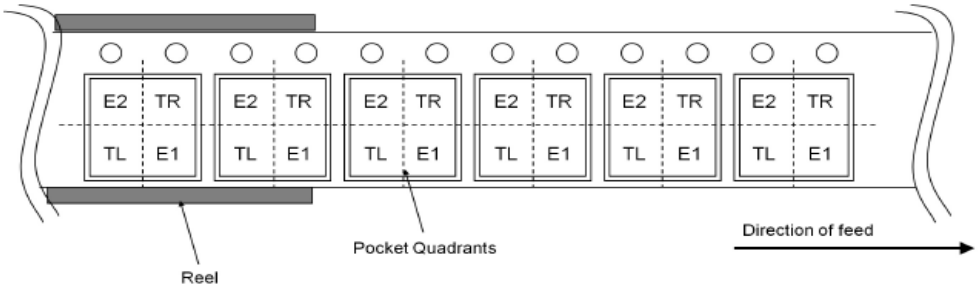


(UNIT : mm)
PKG : VQFN16FV3030
Drawing No. EX396−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
15.Feb.2019	Rev.001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

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