THE DATASHEET OF

CY96F346RSBPMC-GS-UJE2

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CY96345/346
CY96F346/F347/F348

F²MC-16FX, CY96340 Series, 16-bit Proprietary Microcontroller Datasheet

CY96340 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

- 0.18µm CMOS

CPU

- F²MC-16FX CPU
- Up to 56 MHz internal, 17.8 ns instruction cycle time
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
- 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
- Up to 56 MHz external clock for devices with fast clock input feature
- 32-100 kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
- Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
- Clock modulator

On-chip voltage regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

Low voltage reset

- Reset is generated when supply voltage is below minimum

Code Security

- Protects ROM content from unintended read-out

Memory Patch Function

- Replaces ROM content
- Can also be used to implement embedded debug support

DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer,
  17-bit Sub clock timer)
- Watchdog Timer

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I²C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

A/D Converter Reference Voltage switch

- 2 independent positive A/D converter reference voltages available

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

External bus interface

- 8-bit or 16-bit bidirectional data
- Up to 24-bit addresses
- 6 chip select signals
- Multiplexed address/data lines
- Wait state request
- External bus master possible
- Timing programmable

Alarm comparator

- Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds
- Threshold voltages defined externally or generated internally
- Status is readable, interrupts can be masked separately

I/O Ports

- Virtually all external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices)
- Bit-wise programmable pull-up resistor
- Bit-wise programmable output driving strength for EMI optimization

Packages

- 100-pin plastic QFP and LQFP

Flash Memory

- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Number of erase cycles: 10,000 times
- Data retention time: 20 years
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

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Package Dimension CY96(F)34x QFP 100P 100
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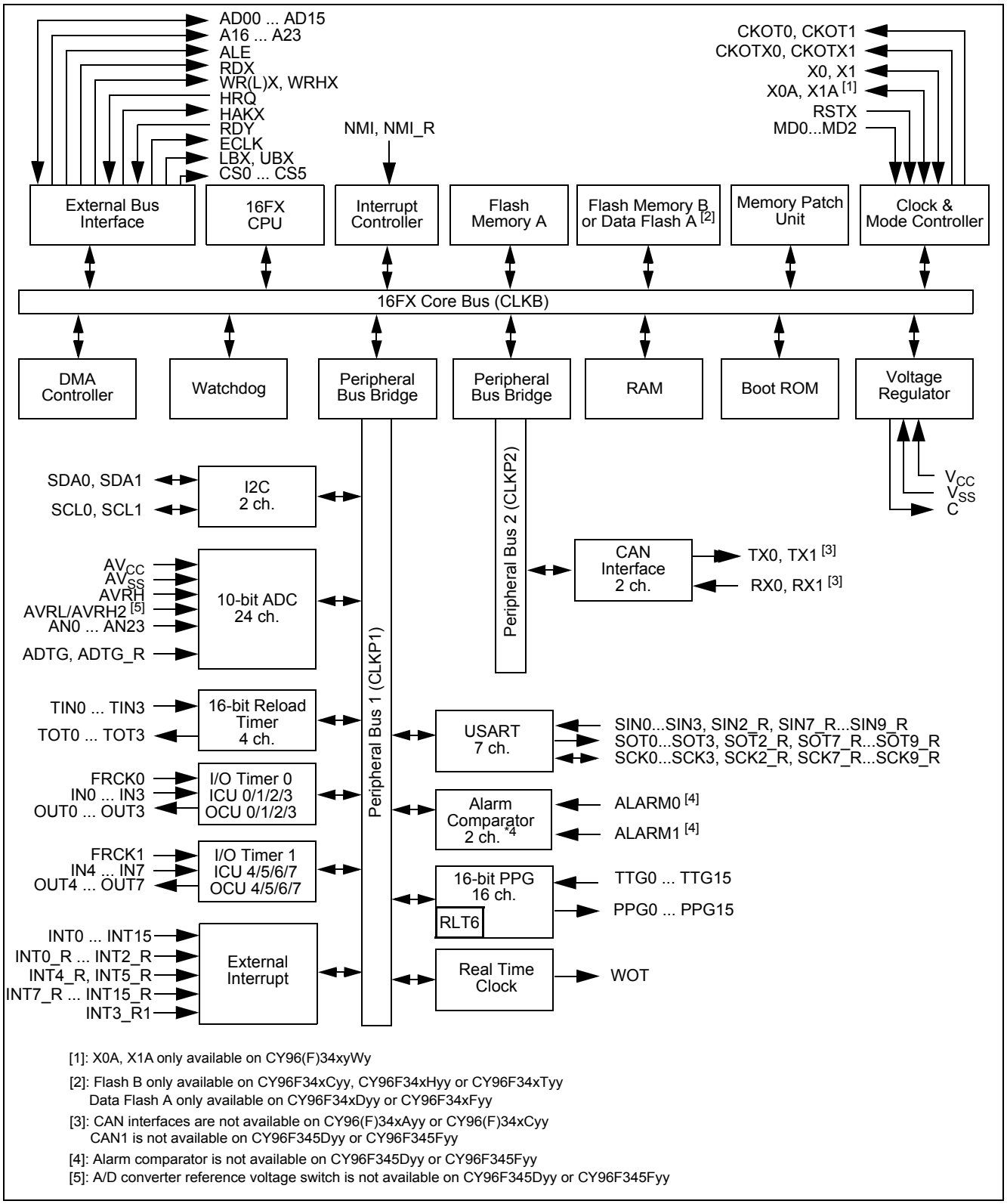
1. Product Lineup

Features		CY96V300B	CY96(F)34x
Product type		Evaluation sample	Flash product: CY96F34x Mask ROM product: CY9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	CY96345Y, CY96345R
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		CY96F345F, CY96F345D
288KB	16KB		CY96F346Y, CY96346Y, CY96F346R, CY96346R, CY96F346A
416KB	16KB		CY96F347Y, CY96F347R, CY96F347A
544KB	24KB		CY96F348Y, CY96F348R, CY96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		CY96F348T, CY96F348H, CY96F348C
Package		BGA416	LQI100 PQH100
DMA		16 channels	6 channels
USART		10 channels	7 channels

Features	CY96V300B	CY96(F)34x
I^2C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except CY96F345Dyy or CY96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	CY96(F)34xAyy or CY96(F)34xCyy: no CY96F345Dyy or CY96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	CY96F345Dyy or CY96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

2. Block Diagram

Figure 1. Block diagram of CY96(F)34x



[1]: X0A, X1A only available on CY96(F)34xyWy

[2]: Flash B only available on CY96F34xCyy, CY96F34xHyy or CY96F34xTyy
Data Flash A only available on CY96F34xDyy or CY96F34xFyy

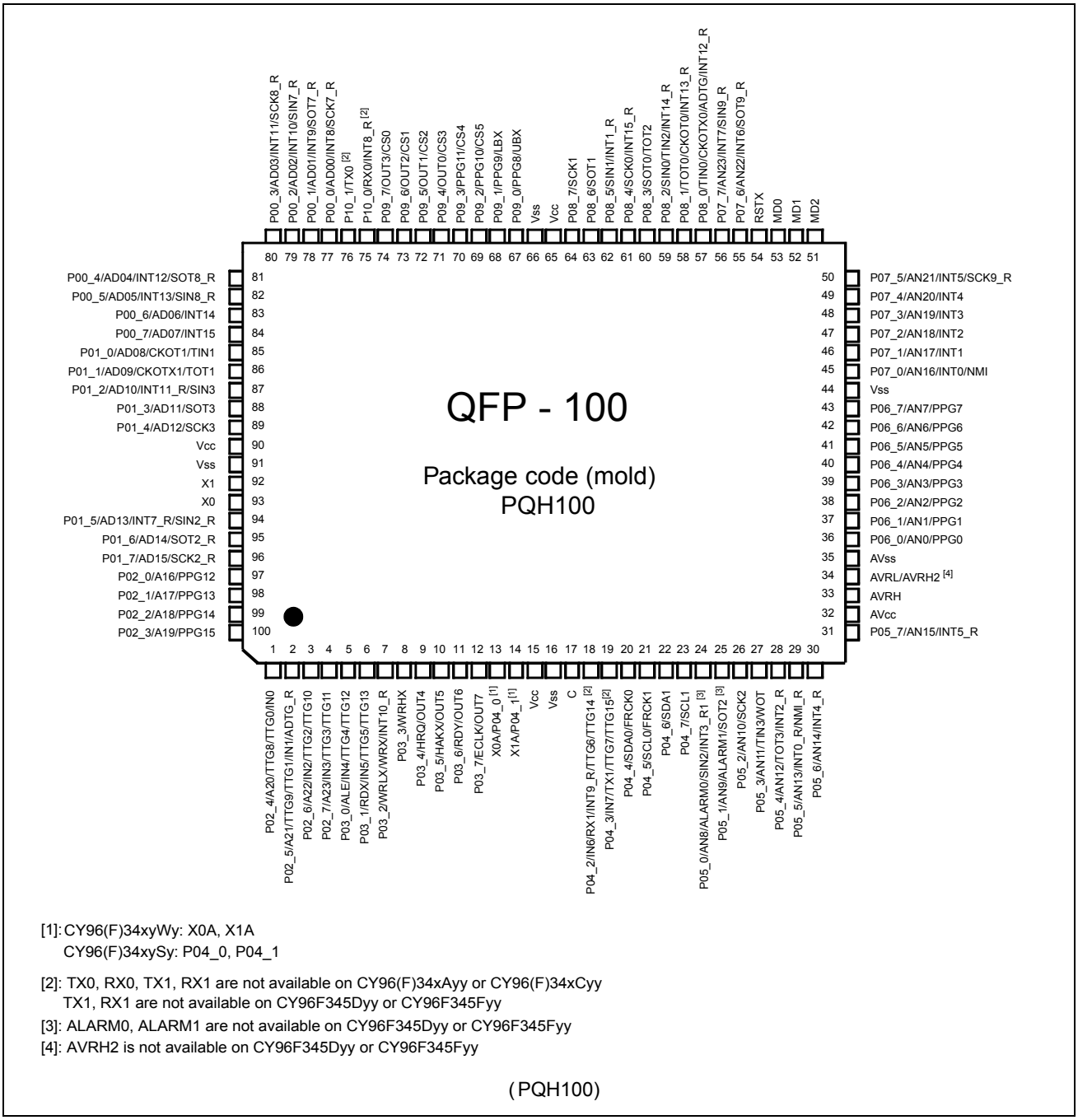
[3]: CAN interfaces are not available on CY96(F)34xAyy or CY96(F)34xCyy
CAN1 is not available on CY96F345Dyy or CY96F345Fyy

[4]: Alarm comparator is not available on CY96F345Dyy or CY96F345Fyy

[5]: A/D converter reference voltage switch is not available on CY96F345Dyy or CY96F345Fyy

3. Pin Assignments

Figure 2. Pin assignment of CY96(F)34x (PQH100)



[1]: CY96(F)34xyWy: X0A, X1A
CY96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on CY96(F)34xAyy or CY96(F)34xCyy
TX1, RX1 are not available on CY96F345Dyy or CY96F345Fyy

[3]: ALARM0, ALARM1 are not available on CY96F345Dyy or CY96F345Fyy

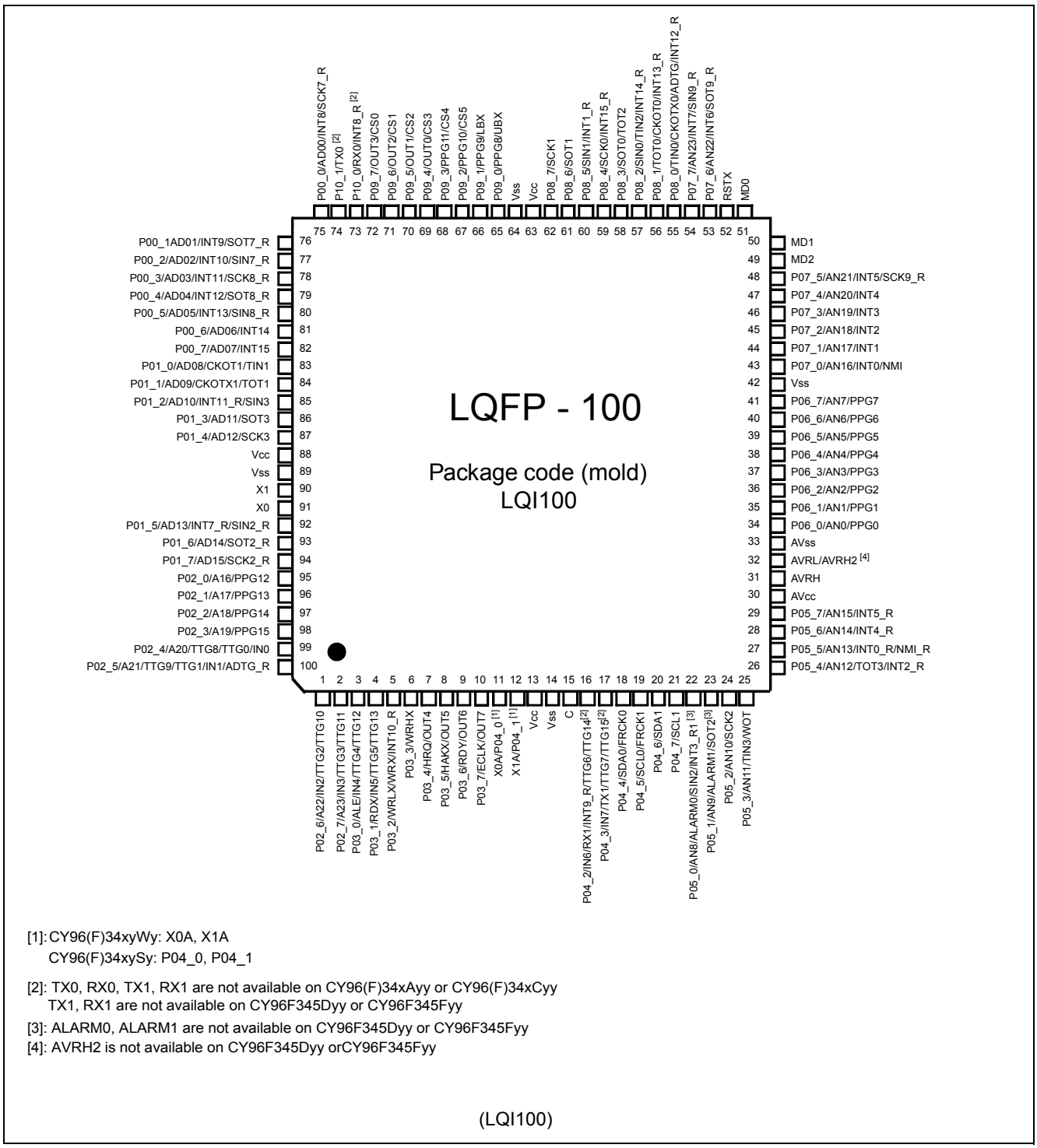
[4]: AVRH2 is not available on CY96F345Dyy or CY96F345Fyy

(PQH100)

Remark:

CY96(F)34x products are pin-compatible to F^{2}MC-16LX family CY90340 series.

Figure 3. Pin assignment of CY96(F)34x (LQI100)



[1]: CY96(F)34xyWy: X0A, X1A
CY96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on CY96(F)34xAyy or CY96(F)34xCyy
TX1, RX1 are not available on CY96F345Dyy or CY96F345Fyy

[3]: ALARM0, ALARM1 are not available on CY96F345Dyy or CY96F345Fyy

[4]: AVRH2 is not available on CY96F345Dyy orCY96F345Fyy

(LQI100)

Remark:

CY96(F)34x products are pin-compatible to F^{2}MC-16LX family CY90340 series.

4. Pin Function Description

Table 1: Pin Function description

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output

Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I^2C interface n clock I/O input/output
SDAn	I2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

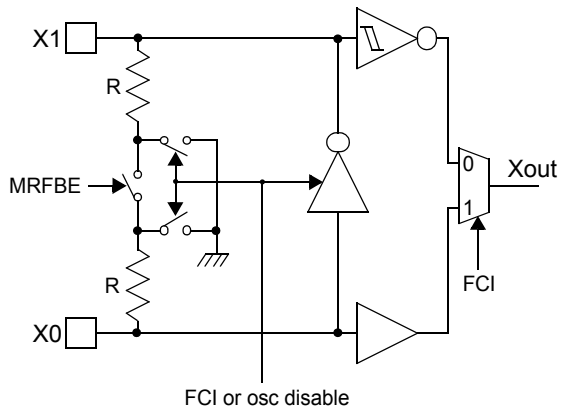
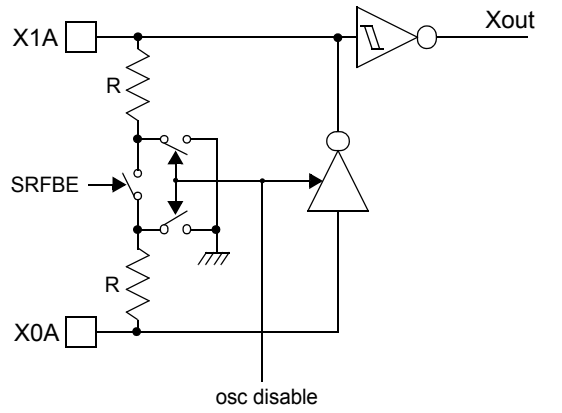
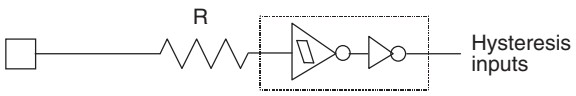
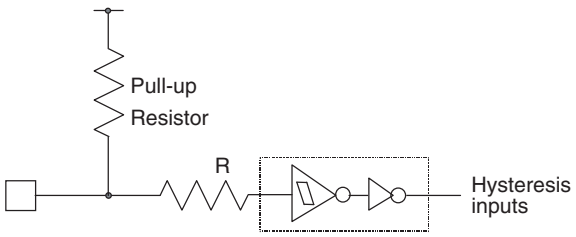
5. Pin Circuit Type

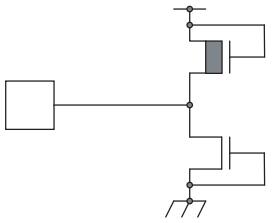
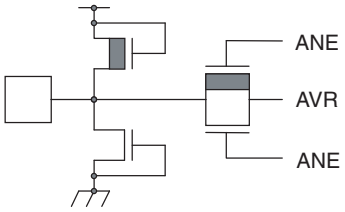
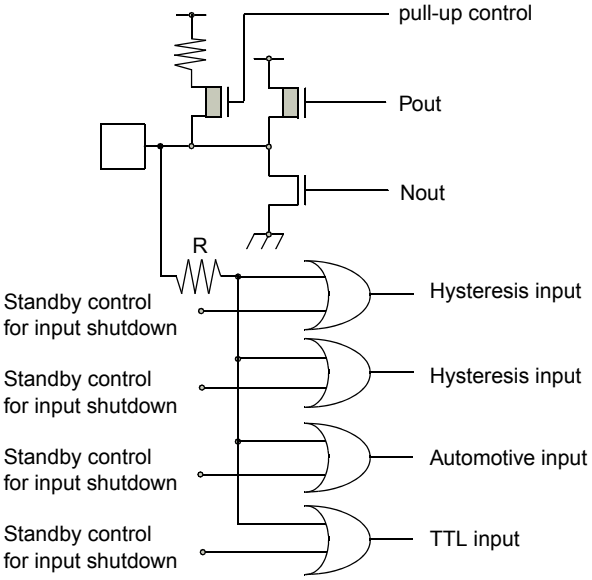
Table 2: Pin circuit types

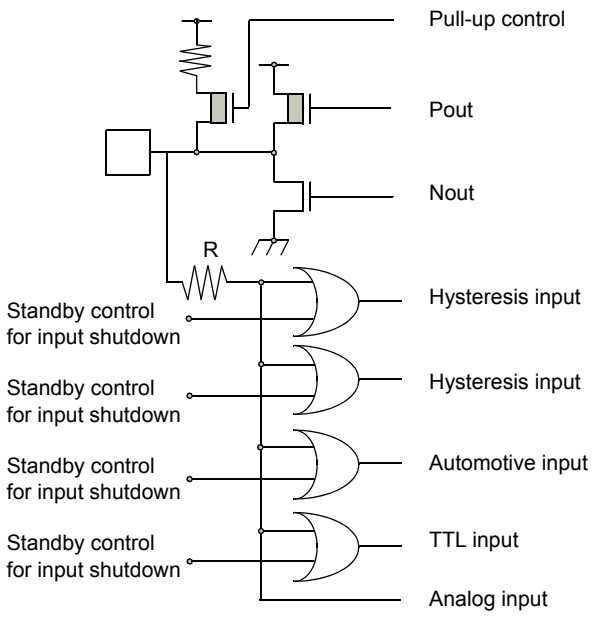
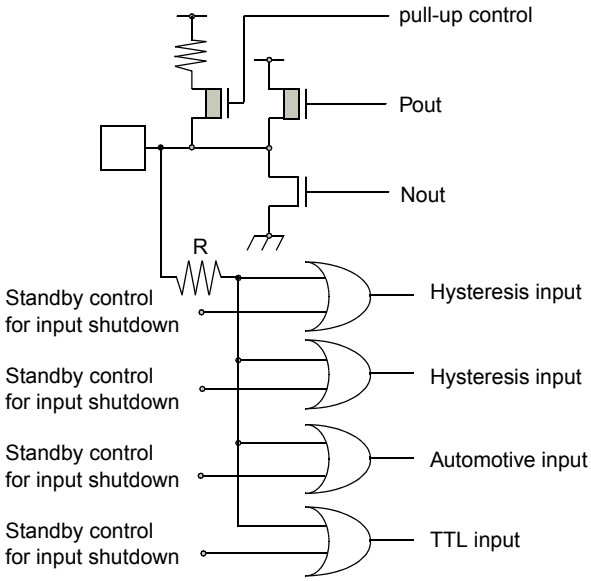
LQI100		PQH100	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to " I/O Circuit Type" for details on the I/O circuit types
[2]: Devices with suffix "W"
[3]: Devices without suffix "W"

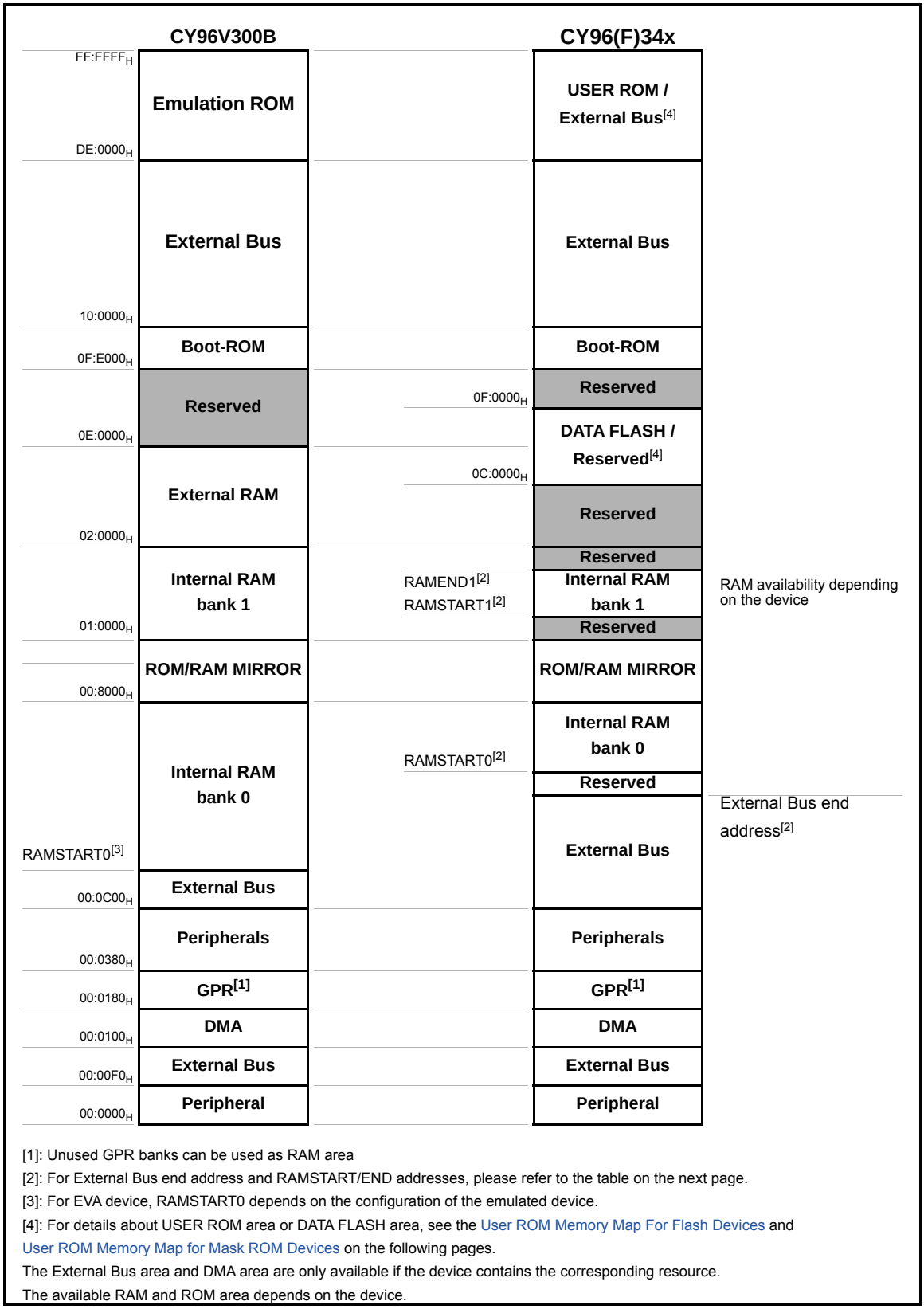
6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device:CMOS Hysteresis input pin ■ Flash device:CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

7. Memory Map



[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the User ROM Memory Map For Flash Devices and User ROM Memory Map for Mask ROM Devices on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAM Start/End and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
CY96(F)345	8KByte	-	$00:21FF_H$	$00:6240_H$	-	-
CY96(F)346,CY96F347	16KByte	-	$00:21FF_H$	$00:4240_H$	-	-
CY96F348	24KByte	-	$00:21FF_H$	$00:2240_H$	-	-

8. User ROM Memory Map For Flash Devices

CY96F345D
CY96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$

Alternative mode CPU address	Flash memory mode address	CY96F346Y CY96F346R CY96F346A Flash size 288kByte	CY96F347Y CY96F347R CY96F347A Flash size 416kByte	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	S37 - 64K	S37 - 64K	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$	S36 - 64K	S36 - 64K	
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		S35 - 64K	
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		S34 - 64K	
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$			
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$			
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$			
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$			
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$	External bus		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		External bus	
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$			
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$			
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$			
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$			
$E0:FFFF_H$ $E0:0000_H$				
$DF:FFFF_H$ $DF:8000_H$		Reserved	Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	Reserved	

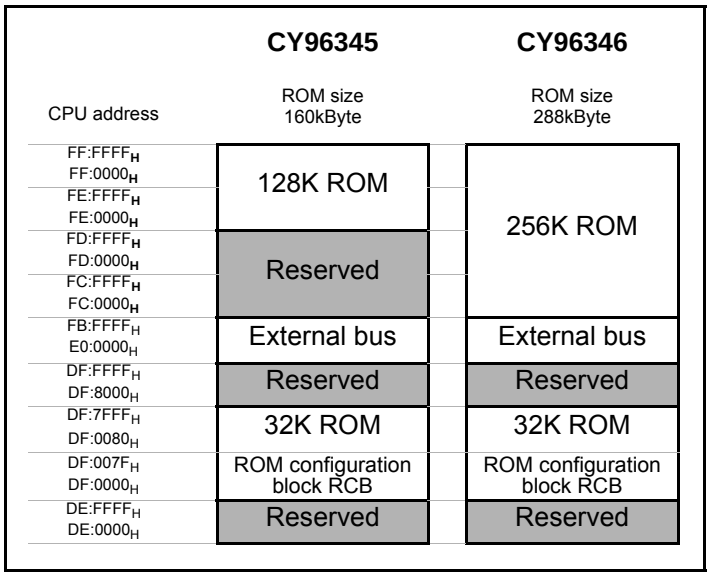
[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

Alternative mode CPU address	Flash memory mode address	CY96F348Y CY96F348R CY96F348A Flash size 544kByte	CY96F348T CY96F348H CY96F348C Flash size 576kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	S37 - 64K	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	S36 - 64K	S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$	S35 - 64K	S35 - 64K	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$	S34 - 64K	S34 - 64K	
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$	S33 - 64K	S33 - 64K	
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$	S32 - 64K	S32 - 64K	
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$	External bus	External bus	
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$			
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$			
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$			
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$			
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$			
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$			
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$			
E0:FFFF$_H$ E0:0000$_H$				
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K [1]	SA0 - 8K [1]	
DE:FFFF$_H$ DE:8000$_H$		Reserved	Reserved	
DE:7FFF$_H$ DE:6000$_H$	1E:7FFF$_H$ 1E:6000$_H$		SB3 - 8K	Flash B
DE:5FFF$_H$ DE:4000$_H$	1E:5FFF$_H$ 1E:4000$_H$		SB2 - 8K	
DE:3FFF$_H$ DE:2000$_H$	1E:3FFF$_H$ 1E:2000$_H$		SB1 - 8K	
DE:1FFF$_H$ DE:0000$_H$	1E:1FFF$_H$ 1E:0000$_H$		SB0 - 8K [2]	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

9. User ROM Memory Map for Mask ROM Devices



10. Serial Programming Communication Interface

Table 3: USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

CY96F34x			
Pin number	Pin number	USART Number	Normal function
LQFP-100	QFP-100		
57	59	USART0	SIN0
58	60		SOT0
59	61		SCK0
60	62	USART1	SIN1
61	63		SOT1
62	64		SCK1
22	24	USART2	SIN2
23	25		SOT2
24	26		SCK2
85	87	USART3	SIN3
86	88		SOT3
87	89		SCK3

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 76/78.If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

11. I/O Map

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000_H	I/O Port P00 - Port Data Register	PDR00		R/W
000001_H	I/O Port P01 - Port Data Register	PDR01		R/W
000002_H	I/O Port P02 - Port Data Register	PDR02		R/W
000003_H	I/O Port P03 - Port Data Register	PDR03		R/W
000004_H	I/O Port P04 - Port Data Register	PDR04		R/W
000005_H	I/O Port P05 - Port Data Register	PDR05		R/W
000006_H	I/O Port P06 - Port Data Register	PDR06		R/W
000007_H	I/O Port P07 - Port Data Register	PDR07		R/W
000008_H	I/O Port P08 - Port Data Register	PDR08		R/W
000009_H	I/O Port P09 - Port Data Register	PDR09		R/W
$00000A_H$	I/O Port P10 - Port Data Register	PDR10		R/W
$00000B_H$-000017_H	Reserved			-
000018_H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019_H	ADC0 - Control Status register High	ADCSH		R/W
$00001A_H$	ADC0 - Data Register Low	ADCRL	ADCR	R
$00001B_H$	ADC0 - Data Register High	ADCRH		R
$00001C_H$	ADC0 - Setting Register		ADSR	R/W
$00001D_H$	ADC0 - Setting Register			R/W
$00001E_H$	ADC0 - Extended Configuration Register	ADECR		R/W
$00001F_H$	Reserved			-
000020_H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021_H	FRT0 - Data register of free-running timer			R/W
000022_H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023_H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024_H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025_H	FRT1 - Data register of free-running timer			R/W
000026_H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027_H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028_H	OCU0 - Output Compare Control Status	OCS0		R/W
000029_H	OCU1 - Output Compare Control Status	OCS1		R/W
$00002A_H$	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00002B_H$	OCU0 - Compare Register			R/W
$00002C_H$	OCU1 - Compare Register		OCCP1	R/W
$00002D_H$	OCU1 - Compare Register			R/W
$00002E_H$	OCU2 - Output Compare Control Status	OCS2		R/W
$00002F_H$	OCU3 - Output Compare Control Status	OCS3		R/W
000030_H	OCU2 - Compare Register		OCCP2	R/W
000031_H	OCU2 - Compare Register			R/W
000032_H	OCU3 - Compare Register		OCCP3	R/W
000033_H	OCU3 - Compare Register			R/W
000034_H	OCU4 - Output Compare Control Status	OCS4		R/W
000035_H	OCU5 - Output Compare Control Status	OCS5		R/W
000036_H	OCU4 - Compare Register		OCCP4	R/W
000037_H	OCU4 - Compare Register			R/W
000038_H	OCU5 - Compare Register		OCCP5	R/W
000039_H	OCU5 - Compare Register			R/W
$00003A_H$	OCU6 - Output Compare Control Status	OCS6		R/W
$00003B_H$	OCU7 - Output Compare Control Status	OCS7		R/W
$00003C_H$	OCU6 - Compare Register		OCCP6	R/W
$00003D_H$	OCU6 - Compare Register			R/W
$00003E_H$	OCU7 - Compare Register		OCCP7	R/W
$00003F_H$	OCU7 - Compare Register			R/W
000040_H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041_H	ICU0/ICU1 - Edge register	ICE01		R/W
000042_H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043_H	ICU0 - Capture Register High	IPCPH0		R
000044_H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045_H	ICU1 - Capture Register High	IPCPH1		R
000046_H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047_H	ICU2/ICU3 - Edge register	ICE23		R/W
000048_H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049_H	ICU2 - Capture Register High	IPCPH2		R
$00004A_H$	ICU3 - Capture Register Low	IPCPL3	IPCP3	R
$00004B_H$	ICU3 - Capture Register High	IPCPH3		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00004C_H$	ICU4/ICU5 - Control Status Register	ICS45		R/W
$00004D_H$	ICU4/ICU5 - Edge register	ICE45		R/W
$00004E_H$	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
$00004F_H$	ICU4 - Capture Register High	IPCPH4		R
000050_H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051_H	ICU5 - Capture Register High	IPCPH5		R
000052_H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053_H	ICU6/ICU7 - Edge register	ICE67		R/W
000054_H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055_H	ICU6 - Capture Register High	IPCPH6		R
000056_H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057_H	ICU7 - Capture Register High	IPCPH7		R
000058_H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059_H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
$00005A_H$	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
$00005B_H$	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
$00005C_H$	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
$00005D_H$	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
$00005E_H$	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
$00005F_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060_H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061_H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062_H	RLT0 - Reload Register - for writing		TMRLR0	W
000062_H	RLT0 - Reload Register - for reading		TMR0	R
000063_H	RLT0 - Reload Register - for writing			W
000063_H	RLT0 - Reload Register - for reading			R
000064_H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065_H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066_H	RLT1 - Reload Register - for writing		TMRLR1	W
000066_H	RLT1 - Reload Register - for reading		TMR1	R
000067_H	RLT1 - Reload Register - for writing			W
000067_H	RLT1 - Reload Register - for reading			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000068_H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069_H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
$00006A_H$	RLT2 - Reload Register - for writing		TMRLR2	W
$00006A_H$	RLT2 - Reload Register - for reading		TMR2	R
$00006B_H$	RLT2 - Reload Register - for writing			W
$00006B_H$	RLT2 - Reload Register - for reading			R
$00006C_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
$00006D_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
$00006E_H$	RLT3 - Reload Register - for writing		TMRLR3	W
$00006E_H$	RLT3 - Reload Register - for reading		TMR3	R
$00006F_H$	RLT3 - Reload Register - for writing			W
$00006F_H$	RLT3 - Reload Register - for reading			R
000070_H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071_H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074_H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075_H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076_H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077_H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078_H	PPG0 - Timer register		PTMR0	R
000079_H	PPG0 - Timer register			R
$00007A_H$	PPG0 - Period setting register		PCSR0	W
$00007B_H$	PPG0 - Period setting register			W
$00007C_H$	PPG0 - Duty cycle register		PDUT0	W
$00007D_H$	PPG0 - Duty cycle register			W
$00007E_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
$00007F_H$	PPG0 - Control status register High	PCNH0		R/W
000080_H	PPG1 - Timer register		PTMR1	R
000081_H	PPG1 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W
$0000A1_H$	PPG4 - Duty cycle register			W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$	PPG5 - Timer register		PTMR5	R
$0000A5_H$	PPG5 - Timer register			R
$0000A6_H$	PPG5 - Period setting register		PCSR5	W
$0000A7_H$	PPG5 - Period setting register			W
$0000A8_H$	PPG5 - Duty cycle register		PDUT5	W
$0000A9_H$	PPG5 - Duty cycle register			W
$0000AA_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W
$0000AB_H$	PPG5 - Control status register High	PCNH5		R/W
$0000AC_H$	I2C0 - Bus Status Register	IBSR0		R
$0000AD_H$	I2C0 - Bus Control Register	IBCR0		R/W
$0000AE_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
$0000AF_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
$0000B0_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
$0000B1_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
$0000B2_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
$0000B3_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
$0000B4_H$	I2C0 - Data Register	IDAR0		R/W
$0000B5_H$	I2C0 - Clock Control Register	ICCR0		R/W
$0000B6_H$	I2C1 - Bus Status Register	IBSR1		R
$0000B7_H$	I2C1 - Bus Control Register	IBCR1		R/W
$0000B8_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
$0000B9_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
$0000BA_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
$0000BB_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
$0000BC_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
$0000BD_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
$0000BE_H$	I2C1 - Data Register	IDAR1		R/W
$0000BF_H$	I2C1 - Clock Control Register	ICCR1		R/W
$0000C0_H$	USART0 - Serial Mode Register	SMR0		R/W
$0000C1_H$	USART0 - Serial Control Register	SCR0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000C2_H$	USART0 - TX Register	TDR0		W
$0000C2_H$	USART0 - RX Register	RDR0		R
$0000C3_H$	USART0 - Serial Status	SSR0		R/W
$0000C4_H$	USART0 - Control/Com. Register	ECCR0		R/W
$0000C5_H$	USART0 - Ext. Status Register	ESCR0		R/W
$0000C6_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
$0000C7_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W
$0000C8_H$	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
$0000C9_H$	Reserved			-
$0000CA_H$	USART1 - Serial Mode Register	SMR1		R/W
$0000CB_H$	USART1 - Serial Control Register	SCR1		R/W
$0000CC_H$	USART1 - TX Register	TDR1		W
$0000CC_H$	USART1 - RX Register	RDR1		R
$0000CD_H$	USART1 - Serial Status	SSR1		R/W
$0000CE_H$	USART1 - Control/Com. Register	ECCR1		R/W
$0000CF_H$	USART1 - Ext. Status Register	ESCR1		R/W
$0000D0_H$	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
$0000D1_H$	USART1 - Baud Rate Generator Register High	BGRH1		R/W
$0000D2_H$	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
$0000D3_H$	Reserved			-
$0000D4_H$	USART2 - Serial Mode Register	SMR2		R/W
$0000D5_H$	USART2 - Serial Control Register	SCR2		R/W
$0000D6_H$	USART2 - TX Register	TDR2		W
$0000D6_H$	USART2 - RX Register	RDR2		R
$0000D7_H$	USART2 - Serial Status	SSR2		R/W
$0000D8_H$	USART2 - Control/Com. Register	ECCR2		R/W
$0000D9_H$	USART2 - Ext. Status Register	ESCR2		R/W
$0000DA_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
$0000DB_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
$0000DC_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
$0000DD_H$	Reserved			-
$0000DE_H$	USART3 - Serial Mode Register	SMR3		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000DF_H$	USART3 - Serial Control Register	SCR3		R/W
$0000E0_H$	USART3 - TX Register	TDR3		W
$0000E0_H$	USART3 - RX Register	RDR3		R
$0000E1_H$	USART3 - Serial Status	SSR3		R/W
$0000E2_H$	USART3 - Control/Com. Register	ECCR3		R/W
$0000E3_H$	USART3 - Ext. Status Register	ESCR3		R/W
$0000E4_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
$0000E5_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
$0000E6_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
$0000E7_H$-$0000EF_H$	Reserved			-
$0000F0_H$-$0000FF_H$	External Bus area	EXTBUS0		R/W
000100_H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101_H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102_H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103_H	DMA0 - DMA control register	DMACS0		R/W
000104_H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105_H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106_H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107_H	DMA0 - Data counter high byte	DCTH0		R/W
000108_H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109_H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
$00010A_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
$00010B_H$	DMA1 - DMA control register	DMACS1		R/W
$00010C_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
$00010D_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
$00010E_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
$00010F_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110_H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111_H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112_H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113_H	DMA2 - DMA control register	DMACS2		R/W
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121_H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122_H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123_H	DMA4 - DMA control register	DMACS4		R/W
000124_H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125_H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126_H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127_H	DMA4 - Data counter high byte	DCTH4		R/W
000128_H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129_H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
$00012A_H$	DMA5 - Buffer address pointer high byte	BAPH5		R/W
$00012B_H$	DMA5 - DMA control register	DMACS5		R/W
$00012C_H$	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
$00012D_H$	DMA5 - I/O register address pointer high byte	IOAH5		R/W
$00012E_H$	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
$00012F_H$	DMA5 - Data counter high byte	DCTH5		R/W
000130_H-$00017F_H$	Reserved			-
000180_H-$00037F_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380_H	DMA0 - Interrupt select	DISEL0		R/W
000381_H	DMA1 - Interrupt select	DISEL1		R/W
000382_H	DMA2 - Interrupt select	DISEL2		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000383_H	DMA3 - Interrupt select	DISEL3		R/W
000384_H	DMA4 - Interrupt select	DISEL4		R/W
000385_H	DMA5 - Interrupt select	DISEL5		R/W
000386_H-$00038F_H$	Reserved			-
000390_H	DMA - Status register low byte	DSRL	DSR	R/W
000391_H	DMA - Status register high byte	DSRH		R/W
000392_H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393_H	DMA - Stop status register high byte	DSSRH		R/W
000394_H	DMA - Enable register low byte	DERL	DER	R/W
000395_H	DMA - Enable register high byte	DERH		R/W
000396_H-$00039F_H$	Reserved			-
$0003A0_H$	Interrupt level register	ILR	ICR	R/W
$0003A1_H$	Interrupt index register	IDX		R/W
$0003A2_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
$0003A3_H$	Interrupt vector table base register High	TBRH		R/W
$0003A4_H$	Delayed Interrupt register	DIRR		R/W
$0003A5_H$	Non Maskable Interrupt register	NMI		R/W
$0003A6_H$-$0003AB_H$	Reserved			-
$0003AC_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
$0003AD_H$	EDSU communication interrupt selection High	EDSU2H		R/W
$0003AE_H$	ROM mirror control register	ROMM		R/W
$0003AF_H$	EDSU configuration register	EDSU		R/W
$0003B0_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
$0003B1_H$	Memory patch control/status register ch 0/1			R/W
$0003B2_H$	Memory patch control/status register ch 2/3		PFCS1	R/W
$0003B3_H$	Memory patch control/status register ch 2/3			R/W
$0003B4_H$	Memory patch control/status register ch 4/5		PFCS2	R/W
$0003B5_H$	Memory patch control/status register ch 4/5			R/W
$0003B6_H$	Memory patch control/status register ch 6/7		PFCS3	R/W
$0003B7_H$	Memory patch control/status register ch 6/7			R/W
$0003B8_H$	Memory Patch function - Patch address 0 low	PFAL0		R/W
$0003B9_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003BA_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
$0003BB_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
$0003BC_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
$0003BD_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
$0003BE_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
$0003BF_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
$0003C0_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
$0003C1_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
$0003C2_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
$0003C3_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
$0003C4_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
$0003C5_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
$0003C6_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
$0003C7_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
$0003C8_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
$0003C9_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
$0003CA_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
$0003CB_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
$0003CC_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
$0003CD_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
$0003CE_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
$0003CF_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
$0003D9_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003DA_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
$0003DB_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
$0003DC_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
$0003DD_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
$0003DE_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
$0003DF_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
$0003E0_H$	Data Flash Control and Status register A	DFCSA		R/W
$0003E1_H$	Data Flash Write command sequencer Control register A	DFWCA		R/W
$0003E2_H$	Data Flash Write command sequencer Status register A	DFWSA		R/W
$0003E3_H$-$0003F0_H$	Reserved			-
$0003F1_H$	Memory Control Status Register A	MCSRA		R/W
$0003F2_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
$0003F3_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
$0003F4_H$	Reserved			-
$0003F5_H$	Memory Control Status Register B	MCSRB		R/W
$0003F6_H$	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
$0003F7_H$	Memory Timing Configuration Register B High	MTCRBH		R/W
$0003F8_H$	Flash Memory Write Control register 0	FMWC0		R/W
$0003F9_H$	Flash Memory Write Control register 1	FMWC1		R/W
$0003FA_H$	Flash Memory Write Control register 2	FMWC2		R/W
$0003FB_H$	Flash Memory Write Control register 3	FMWC3		R/W
$0003FC_H$	Flash Memory Write Control register 4	FMWC4		R/W
$0003FD_H$	Flash Memory Write Control register 5	FMWC5		R/W
$0003FE_H$-$0003FF_H$	Reserved			-
000400_H	Standby Mode control register	SMCR		R/W
000401_H	Clock select register	CKSR		R/W
000402_H	Clock Stabilization select register	CKSSR		R/W
000403_H	Clock monitor register	CKMR		R
000404_H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405_H	Clock Frequency control register High	CKFCRH		R/W
000406_H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407_H	PLL Control register High	PLLCRH		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000408_H	RC clock timer control register	RCTCR		R/W
000409_H	Main clock timer control register	MCTCR		R/W
$00040A_H$	Sub clock timer control register	SCTCR		R/W
$00040B_H$	Reset cause and clock status register with clear function	RCCSRC		R
$00040C_H$	Reset configuration register	RCR		R/W
$00040D_H$	Reset cause and clock status register	RCCSR		R
$00040E_H$	Watch dog timer configuration register	WDTC		R/W
$00040F_H$	Watch dog timer clear pattern register	WDTCP		W
000410_H-000414_H	Reserved			-
000415_H	Clock output activation register	COAR		R/W
000416_H	Clock output configuration register 0	COCR0		R/W
000417_H	Clock output configuration register 1	COCR1		R/W
000418_H	Clock Modulator control register	CMCR		R/W
000419_H	Reserved			-
$00041A_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
$00041B_H$	Clock Modulator Parameter register High	CMPRH		R/W
$00041C_H$-$00042B_H$	Reserved			-
$00042C_H$	Voltage Regulator Control register	VRCR		R/W
$00042D_H$	Clock Input and LVD Control Register	CILCR		R/W
$00042E_H$-$00042F_H$	Reserved			-
000430_H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431_H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432_H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433_H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434_H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439_H	I/O Port P09 - Data Direction Register	DDR09		R/W
$00043A_H$	I/O Port P10 - Data Direction Register	DDR10		R/W
$00043B_H$-000443_H	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461_H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462_H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473_H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000474_H	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475_H	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476_H	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477_H-$00047F_H$	Reserved			-
000480_H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481_H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482_H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483_H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484_H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485_H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486_H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487_H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488_H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489_H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
$00048A_H$	I/O Port P10 - Port Output Drive Register	PODR10		R/W
$00048B_H$-$00049B_H$	Reserved			-
$00049C_H$	I/O Port P08 - Port High Drive Register	PHDR08		R/W
$00049D_H$	I/O Port P09 - Port High Drive Register	PHDR09		R/W
$00049E_H$	I/O Port P10 - Port High Drive Register	PHDR10		R/W
$00049F_H$-$0004A7_H$	Reserved			-
$0004A8_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
$0004A9_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
$0004AA_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
$0004AB_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
$0004AC_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
$0004AD_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
$0004AE_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
$0004AF_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
$0004B0_H$	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
$0004B1_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
$0004B2_H$	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
$0004B3_H$-$0004BB_H$	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004BC_H$	I/O Port P00 - External Pin State Register	EPSR00		R
$0004BD_H$	I/O Port P01 - External Pin State Register	EPSR01		R
$0004BE_H$	I/O Port P02 - External Pin State Register	EPSR02		R
$0004BF_H$	I/O Port P03 - External Pin State Register	EPSR03		R
$0004C0_H$	I/O Port P04 - External Pin State Register	EPSR04		R
$0004C1_H$	I/O Port P05 - External Pin State Register	EPSR05		R
$0004C2_H$	I/O Port P06 - External Pin State Register	EPSR06		R
$0004C3_H$	I/O Port P07 - External Pin State Register	EPSR07		R
$0004C4_H$	I/O Port P08 - External Pin State Register	EPSR08		R
$0004C5_H$	I/O Port P09 - External Pin State Register	EPSR09		R
$0004C6_H$	I/O Port P10 - External Pin State Register	EPSR10		R
$0004C7_H$-$0004CF_H$	Reserved			-
$0004D0_H$	ADC analog input enable register 0	ADER0		R/W
$0004D1_H$	ADC analog input enable register 1	ADER1		R/W
$0004D2_H$	ADC analog input enable register 2	ADER2		R/W
$0004D3_H$	ADC analog input enable register 3	ADER3		R/W
$0004D4_H$	ADC analog input enable register 4	ADER4		R/W
$0004D5_H$	Reserved			-
$0004D6_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
$0004D7_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
$0004D8_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
$0004D9_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
$0004DA_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
$0004DB_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
$0004DC_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
$0004DD_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W
$0004E3_H$	RTC - Second Register	WTSR		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$00053D_H$	Reserved			-
$00053E_H$	USART7 - Serial Mode Register	SMR7		R/W
$00053F_H$	USART7 - Serial Control Register	SCR7		R/W
000540_H	USART7 - Serial TX Register	TDR7		W
000540_H	USART7 - Serial RX Register	RDR7		R
000541_H	USART7 - Serial Status Register	SSR7		R/W
000542_H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543_H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544_H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545_H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546_H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547_H	Reserved			-
000548_H	USART8 - Serial Mode Register	SMR8		R/W
000549_H	USART8 - Serial Control Register	SCR8		R/W
$00054A_H$	USART8 - Serial TX Register	TDR8		W
$00054A_H$	USART8 - Serial RX Register	RDR8		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00054B_H$	USART8 - Serial Status Register	SSR8		R/W
$00054C_H$	USART8 - Ext. Control/Com. Register	ECCR8		R/W
$00054D_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
$00054E_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
$00054F_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550_H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551_H	Reserved			-
000552_H	USART9 - Serial Mode Register	SMR9		R/W
000553_H	USART9 - Serial Control Register	SCR9		R/W
000554_H	USART9 - Serial TX Register	TDR9		W
000554_H	USART9 - Serial RX Register	RDR9		R
000555_H	USART9 - Serial Status Register	SSR9		R/W
000556_H	USART9 - Ext. Control/Com. Register	ECCR9		R/W
000557_H	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558_H	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559_H	USART9 - Baud Rate Generator Register High	BGRH9		R/W
$00055A_H$	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
$00055B_H$-$00055F_H$	Reserved			-
000560_H	ALARM0 - Control Status Register	ACSR0		R/W
000561_H	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562_H	ALARM1 - Control Status Register	ACSR1		R/W
000563_H	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564_H	PPG6 - Timer register		PTMR6	R
000565_H	PPG6 - Timer register			R
000566_H	PPG6 - Period setting register		PCSR6	W
000567_H	PPG6 - Period setting register			W
000568_H	PPG6 - Duty cycle register		PDUT6	W
000569_H	PPG6 - Duty cycle register			W
$00056A_H$	PPG6 - Control status register Low	PCNL6	PCN6	R/W
$00056B_H$	PPG6 - Control status register High	PCNH6		R/W
$00056C_H$	PPG7 - Timer register		PTMR7	R
$00056D_H$	PPG7 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00056E_H$	PPG7 - Period setting register		PCSR7	W
$00056F_H$	PPG7 - Period setting register			W
000570_H	PPG7 - Duty cycle register		PDUT7	W
000571_H	PPG7 - Duty cycle register			W
000572_H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573_H	PPG7 - Control status register High	PCNH7		R/W
000574_H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575_H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576_H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577_H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578_H	PPG8 - Timer register		PTMR8	R
000579_H	PPG8 - Timer register			R
$00057A_H$	PPG8 - Period setting register		PCSR8	W
$00057B_H$	PPG8 - Period setting register			W
$00057C_H$	PPG8 - Duty cycle register		PDUT8	W
$00057D_H$	PPG8 - Duty cycle register			W
$00057E_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
$00057F_H$	PPG8 - Control status register High	PCNH8		R/W
000580_H	PPG9 - Timer register		PTMR9	R
000581_H	PPG9 - Timer register			R
000582_H	PPG9 - Period setting register		PCSR9	W
000583_H	PPG9 - Period setting register			W
000584_H	PPG9 - Duty cycle register		PDUT9	W
000585_H	PPG9 - Duty cycle register			W
000586_H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587_H	PPG9 - Control status register High	PCNH9		R/W
000588_H	PPG10 - Timer register		PTMR10	R
000589_H	PPG10 - Timer register			R
$00058A_H$	PPG10 - Period setting register		PCSR10	W
$00058B_H$	PPG10 - Period setting register			W
$00058C_H$	PPG10 - Duty cycle register		PDUT10	W
$00058D_H$	PPG10 - Duty cycle register			W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00058E_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
$00058F_H$	PPG10 - Control status register High	PCNH10		R/W
000590_H	PPG11 - Timer register		PTMR11	R
000591_H	PPG11 - Timer register			R
000592_H	PPG11 - Period setting register		PCSR11	W
000593_H	PPG11 - Period setting register			W
000594_H	PPG11 - Duty cycle register		PDUT11	W
000595_H	PPG11 - Duty cycle register			W
000596_H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597_H	PPG11 - Control status register High	PCNH11		R/W
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$	PPG13 - Timer register		PTMR13	R
$0005A5_H$	PPG13 - Timer register			R
$0005A6_H$	PPG13 - Period setting register		PCSR13	W
$0005A7_H$	PPG13 - Period setting register			W
$0005A8_H$	PPG13 - Duty cycle register		PDUT13	W
$0005A9_H$	PPG13 - Duty cycle register			W
$0005AA_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
$0005AB_H$	PPG13 - Control status register High	PCNH13		R/W
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
$0006E9_H$	External Bus - Area configuration register 4 High	EACH4		R/W
$0006EA_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
$0006EB_H$	External Bus - Area configuration register 5 High	EACH5		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006EC_H$	External Bus - Area select register 2	EAS2		R/W
$0006ED_H$	External Bus - Area select register 3	EAS3		R/W
$0006EE_H$	External Bus - Area select register 4	EAS4		R/W
$0006EF_H$	External Bus - Area select register 5	EAS5		R/W
$0006F0_H$	External Bus - Mode register	EBM		R/W
$0006F1_H$	External Bus - Clock and Function register	EBCF		R/W
$0006F2_H$	External Bus - Address output enable register 0	EBAE0		R/W
$0006F3_H$	External Bus - Address output enable register 1	EBAE1		R/W
$0006F4_H$	External Bus - Address output enable register 2	EBAE2		R/W
$0006F5_H$	External Bus - Control signal register	EBCS		R/W
$0006F6_H$-$0006FF_H$	Reserved			-
000700_H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701_H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702_H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703_H	CAN0 - Status register High (reserved)	STATRH0		R
000704_H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705_H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706_H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707_H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708_H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709_H	CAN0 - Interrupt Register High	INTRH0		R
$00070A_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
$00070B_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
$00070C_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
$00070D_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
$00070E_H$-$00070F_H$	Reserved			-
000710_H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711_H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712_H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713_H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714_H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
$00074E_H$	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00074F_H$	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750_H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751_H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752_H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753_H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754_H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755_H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756_H-$00077F_H$	Reserved			-
000780_H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781_H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782_H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783_H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784_H-$00078F_H$	Reserved			-
000790_H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791_H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792_H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793_H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794_H-$00079F_H$	Reserved			-
$0007A0_H$	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
$0007A1_H$	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
$0007A2_H$	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
$0007A3_H$	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
$0007A4_H$-$0007AF_H$	Reserved			-
$0007B0_H$	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
$0007B1_H$	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
$0007B2_H$	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
$0007B3_H$	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
$0007B4_H$-$0007CD_H$	Reserved			-
$0007CE_H$	CAN0 - Output enable register	COER0		R/W
$0007CF_H$-$0007FF_H$	Reserved			-
000800_H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$-$00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814_H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815_H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816_H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817_H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818_H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819_H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
$00081A_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
$00081B_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
$00081C_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
$00081D_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
$00081E_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
$00081F_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820_H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821_H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822_H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000823_H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824_H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825_H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826_H-$00083F_H$	Reserved			-
000840_H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841_H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842_H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843_H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844_H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845_H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846_H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847_H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848_H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849_H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
$00084A_H$	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
$00084B_H$	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
$00084C_H$	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
$00084D_H$	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
$00084E_H$	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
$00084F_H$	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850_H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851_H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852_H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853_H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854_H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855_H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856_H-$00087F_H$	Reserved			-
000880_H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881_H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882_H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883_H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884_H-$00088F_H$	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000890_H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891_H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892_H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893_H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894_H-$00089F_H$	Reserved			-
$0008A0_H$	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
$0008A1_H$	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
$0008A2_H$	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
$0008A3_H$	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
$0008A4_H$-$0008AF_H$	Reserved			-
$0008B0_H$	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
$0008B1_H$	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
$0008B2_H$	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
$0008B3_H$	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
$0008B4_H$-$0008CD_H$	Reserved			-
$0008CE_H$	CAN1 - Output enable register	COER1		R/W
$0008CF_H$-$0009FF_H$	Reserved			-
$000A00_H$	DMA - IO address block register 0	IOABK0		R/W
$000A01_H$	DMA - IO address block register 1	IOABK1		R/W
$000A02_H$	DMA - IO address block register 2	IOABK2		R/W
$000A03_H$	DMA - IO address block register 3	IOABK3		R/W
$000A04_H$	DMA - IO address block register 4	IOABK4		R/W
$000A05_H$	DMA - IO address block register 5	IOABK5		R/W
$000A06_H$-$000BFF_H$	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

12. Interrupt Vector Table

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	RESERVED	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	CAN0	No	33	CAN Controller 0 (except CY96(F)34xAyy or CY96(F)34xCyy)
34	374_H	CAN1	No	34	CAN Controller 1 (except CY96(F)34xAyy, CY96(F)34xCyy, CY96F345Dyy or CY96F345Fyy)
35	370_H	PPG0	Yes	35	Programmable Pulse Generator 0
36	$36C_H$	PPG1	Yes	36	Programmable Pulse Generator 1
37	368_H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364_H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360_H	PPG4	Yes	39	Programmable Pulse Generator 4
40	$35C_H$	PPG5	Yes	40	Programmable Pulse Generator 5
41	358_H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354_H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350_H	PPG8	Yes	43	Programmable Pulse Generator 8
44	$34C_H$	PPG9	Yes	44	Programmable Pulse Generator 9
45	348_H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344_H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340_H	PPG12	Yes	47	Programmable Pulse Generator 12
48	$33C_H$	PPG13	Yes	48	Programmable Pulse Generator 13
49	338_H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334_H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330_H	RLT0	Yes	51	Reload Timer 0
52	$32C_H$	RLT1	Yes	52	Reload Timer 1
53	328_H	RLT2	Yes	53	Reload Timer 2
54	324_H	RLT3	Yes	54	Reload Timer 3
55	320_H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	$31C_H$	ICU0	Yes	56	Input Capture Unit 0
57	318_H	ICU1	Yes	57	Input Capture Unit 1
58	314_H	ICU2	Yes	58	Input Capture Unit 2
59	310_H	ICU3	Yes	59	Input Capture Unit 3

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except CY96F345Dyy or CY96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except CY96F345Dyy or CY96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only CY96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	LINR9	Yes	93	LIN USART 9 RX
94	284_H	LINT9	Yes	94	LIN USART 9 TX
95	280_H	RTC0	No	95	Real Timer Clock
96	$27C_H$	CAL0	No	96	Clock Calibration Unit
97	278_H	DFLASH_A	Yes	97	Data Flash A (only CY96F345Dyy, CY96F345Fyy)

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

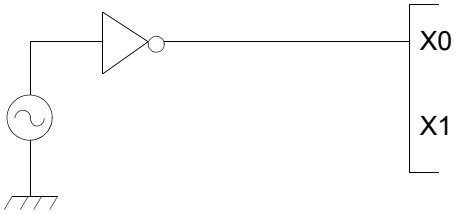
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

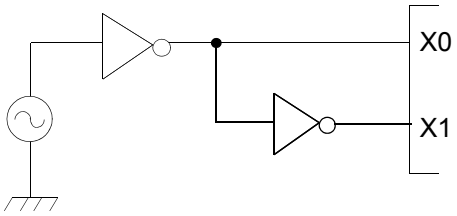
13.3.1 Single phase external clock

■ When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

■ When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.Therefore, design a printed circuit board so as to avoid noise.Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [1]
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V [2]
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V [2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purposeI/O pins [3]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purposeI/O pins [3]
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) [4]	P_D	-	430[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=90°C
		-	540[5]	mW	T_A=125°C, no Flash program/erase [6]
Permitted Power dissipation (CY96F346/F347/F348 in LQFP package) [4]	P_D	-	375[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=85°C
		-	470[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	560[5]	mW	T_A=120°C, no Flash program/erase [6]
Permitted Power dissipation (CY96F345 in LQFP package) [4]	P_D	-	335[5]	mW	T_A=105°C
		-	670[5]	mW	T_A=85°C
		-	840[5]	mW	T_A=75°C
		-	420[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	590[5]	mW	T_A=115°C, no Flash program/erase [6]

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	350	mW	T_A=105°C
		-	360	mW	T_A=125°C [6]
Operating ambient temperature	T_A	0	+70	°C	CY96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	°C	

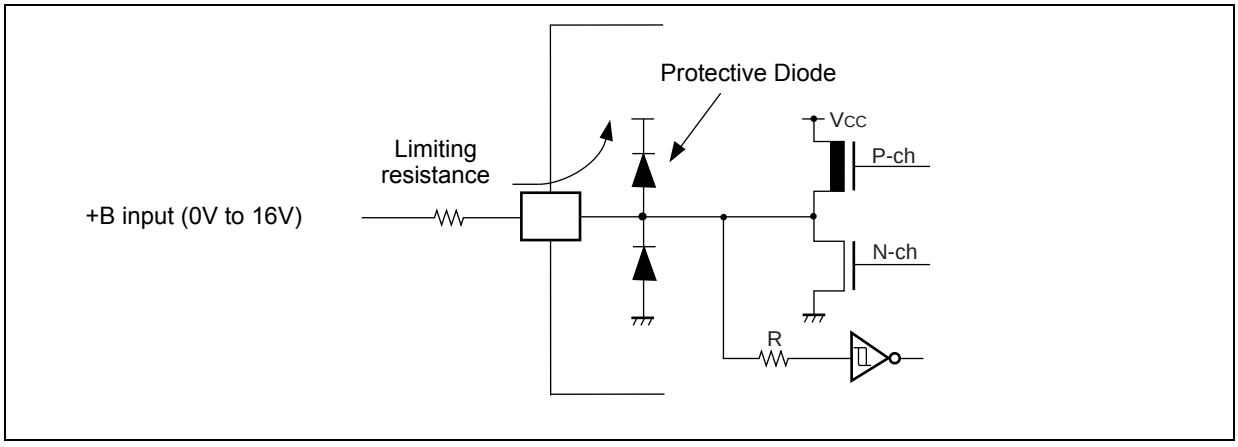
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.I_A is the analog current consumption into AV_{CC}.

[5]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hys-teresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in CY96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscil-lation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hys-teresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in CY96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -2mA / $3.0V \leq V_{CC} < 4.5V$ I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -5mA / $3.0V \leq V_{CC} < 4.5V$ I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH3}	3mA outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -3mA / $3.0V \leq V_{CC} < 4.5V$ I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA	-	-	0.4	V	Driving strength set to 2mA
			3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA					
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA	-	-	0.4	V	Driving strength set to 5mA
			3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA					
	V_{OL3}	3mA outputs	3.0V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	µA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	V_{CC} = 3.3V ± 10%	40	100	160	kΩ	
			V_{CC} = 5.0V ± 10%	25	50	100	kΩ	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes[1]	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	35	44	mA	Flash devices at 0 Flash wait states
			+125°C	36	47		
			+25°C	17	23	mA	CY96345/346 at 0 ROM wait states
			+125°C	18	25		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz,CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	44	57	mA	CY96F346/F347/F348 at 2 Flash wait states
			+125°C	45	60		
			+25°C	25	35	mA	CY96345/346 at 2 ROM wait states
			+125°C	26	37		
		PLL Run mode with CLKS1/2 = 72MHz, CLKB = CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	50	mA	CY96F346/F347/F348Y/R/Ayy at 1 Flash wait state
			+125°C	39	53		
		PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	51	mA	CY96F345 at 1 Flash wait state
			+125°C	40	54		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	49	62	mA	CY96F348T/H/CyB/C at 1 Flash wait state
			+125°C	50	65		
			+25°C	26	36	mA	CY96345/346 at 1 ROM wait state
			+125°C	27	38		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.5	5.5	mA	Flash devices at 1 Flash wait state
			+125°C	5.1	8.5		
			+25°C	2.5	3.5	mA	CY96345/346 at 1 ROM wait state
			+125°C	3.1	5.5		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes[1]	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	CY96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	CY96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	CY96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
			+25°C	0.4	0.6	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.6	2		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	CY96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	CY96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	CY96345/346
			+125°C	14.3	17		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	CY96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	11	13.5	mA	CY96F345
			+125°C	11.7	16		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	CY96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	CY96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	CY96345/346
			+125°C	2	3.8		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.9	1.4	mA	Flash devices
			+125°C	1.5	4.1		
			+25°C	0.9	1.4	mA	CY96345/346
			+125°C	1.5	3.1		
	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.5	mA	CY96F346/F347/F348
			+125°C	0.8	3.4		
			+25°C	0.09	0.2	mA	CY96F345
			+125°C	0.59	3.1		
			+25°C	0.3	0.5	mA	CY96345/346
			+125°C	0.8	2.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.06	0.15	mA	Flash devices
			+125°C	0.56	3		
			+25°C	0.06	0.15	mA	CY96345/346
			+125°C	0.56	1.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	Flash devices
			+125°C	0.54	2.9		
			+25°C	0.04	0.12	mA	CY96345/346
			+125°C	0.54	1.85		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	1.6	2	mA	Flash devices
			+125°C	2.1	5		
			+25°C	1.6	2	mA	CY96345/346
			+125°C	2.1	4		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	CY96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	CY96345/346
			+125°C	0.85	2.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15		CY96345/346
			+125°C	0.6	1.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	CY96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	CY96345/346
			+125°C	0.85	2.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15	mA	CY96345/346
			+125°C	0.6	1.9		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	CY96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	CY96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	CY96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	CY96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	CY96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	CY96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	CY96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	CY96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

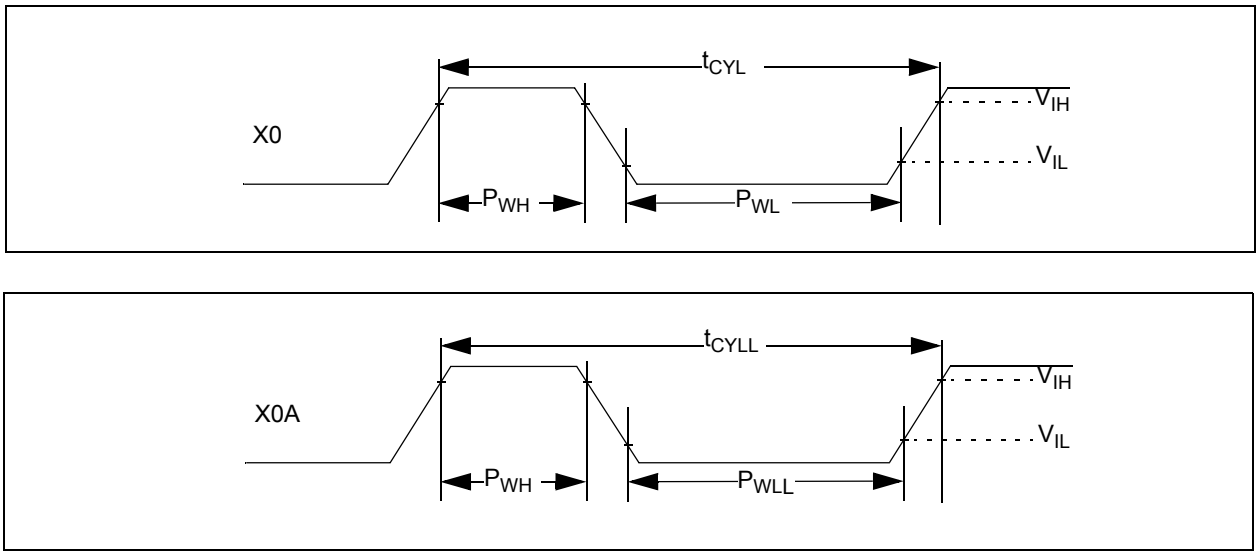
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}
[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.							

14.4 AC Characteristics

14.4.1 Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in CY96F34xY/R/AxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in CY96F34xY/R/AxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	



14.4.2 Internal Clock timing

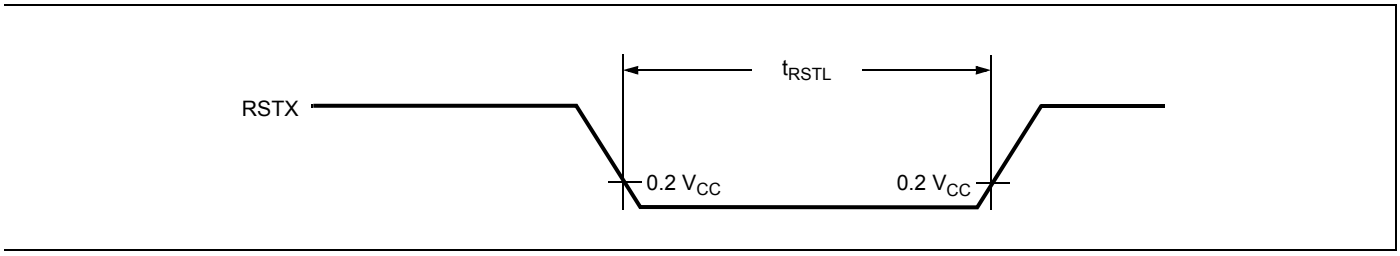
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	CY96F348T/H/CxB/C
		0	72	0	80	MHz	CY96F345
		0	68	0	74	MHz	CY96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	CY96F345
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	CY96F34xY/R/Axx

14.4.3 External Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

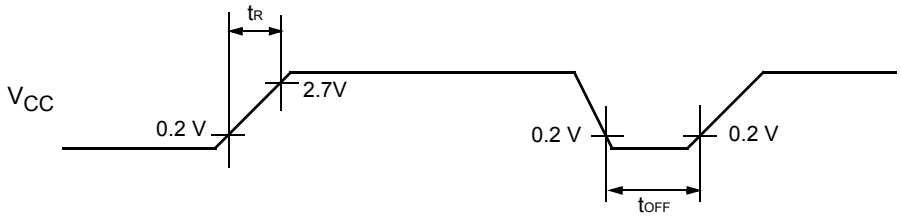
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



14.4.4 Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



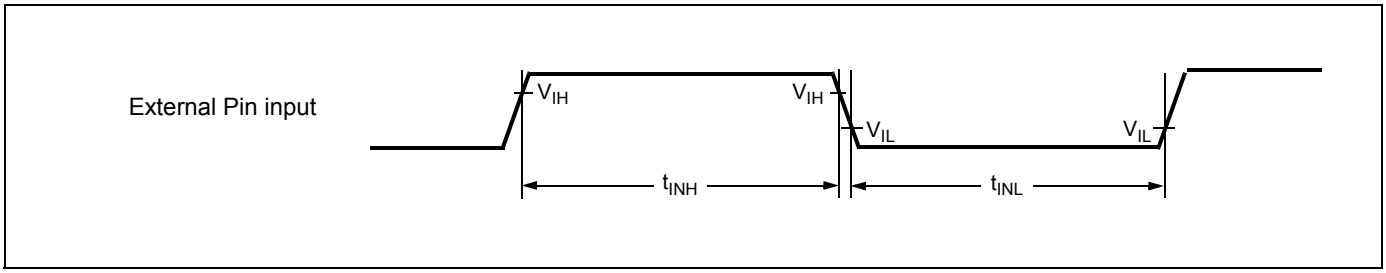
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

14.4.5 External Input timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	-	200	-	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 ($t_{CLKP1}=1/f_{CLKP1}$)	-	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



14.4.6 External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

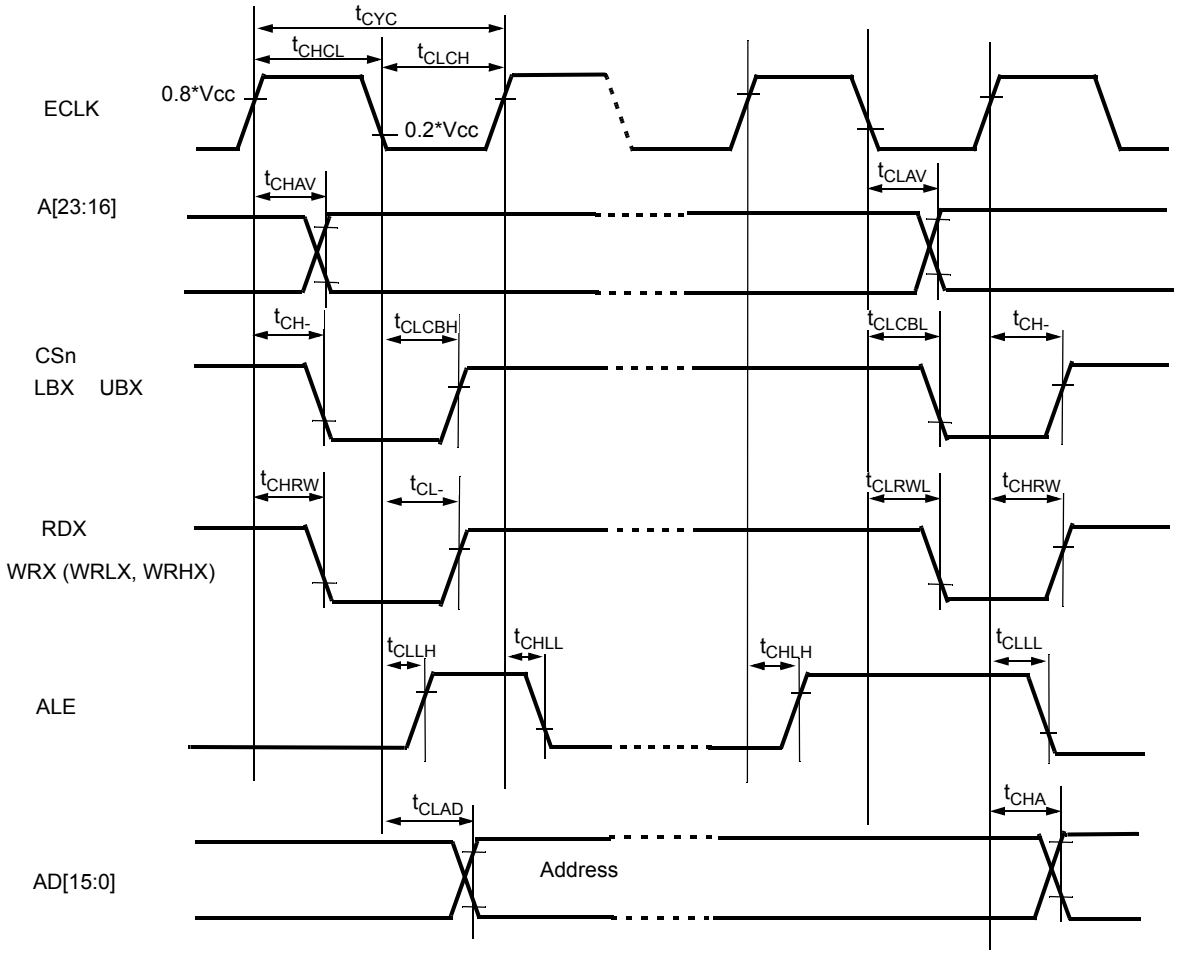
14.4.7 Basic Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	25	-	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	-	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	-	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Refer to the Hardware Manual for detailed Timing Charts

14.4.8 Bus Timing (Read)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

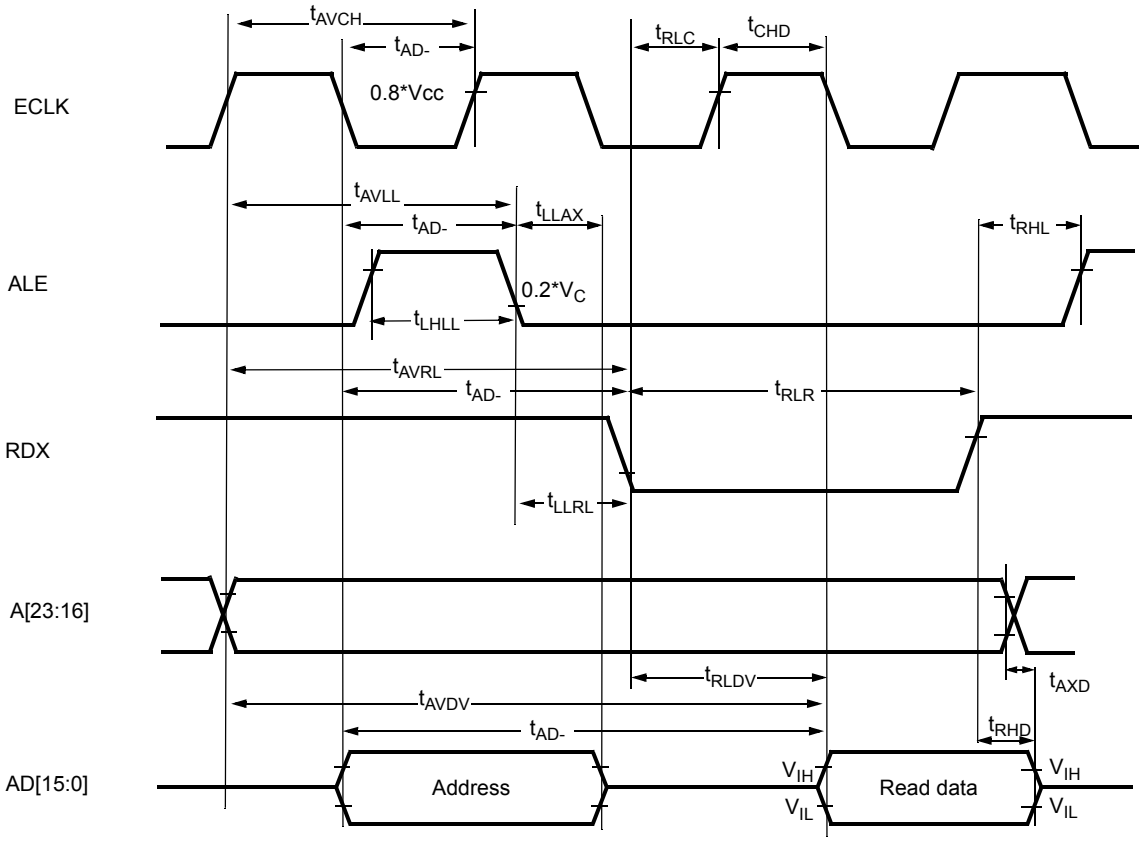
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	– 10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	-	ns	
			EACL:STS=1	$t_{CYC} - 8$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC}$ – 60	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC}$ – 60		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2$ – 60	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2$ – 60		
RDX pulse width	t_{RLRH}	RDX	-	$3t_{CYC}/2$ – 8	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3t_{CYC}/2$ – 55	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	-	0	-	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2$ – 15	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2$ – 15	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	t_{CYC} – 20	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2$ – 20	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2$ – 15	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2$ – 15	-	ns	
			EACL:STS=1	– 15	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	t_{CYC} – 55	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.4.9 Bus Timing (Write)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

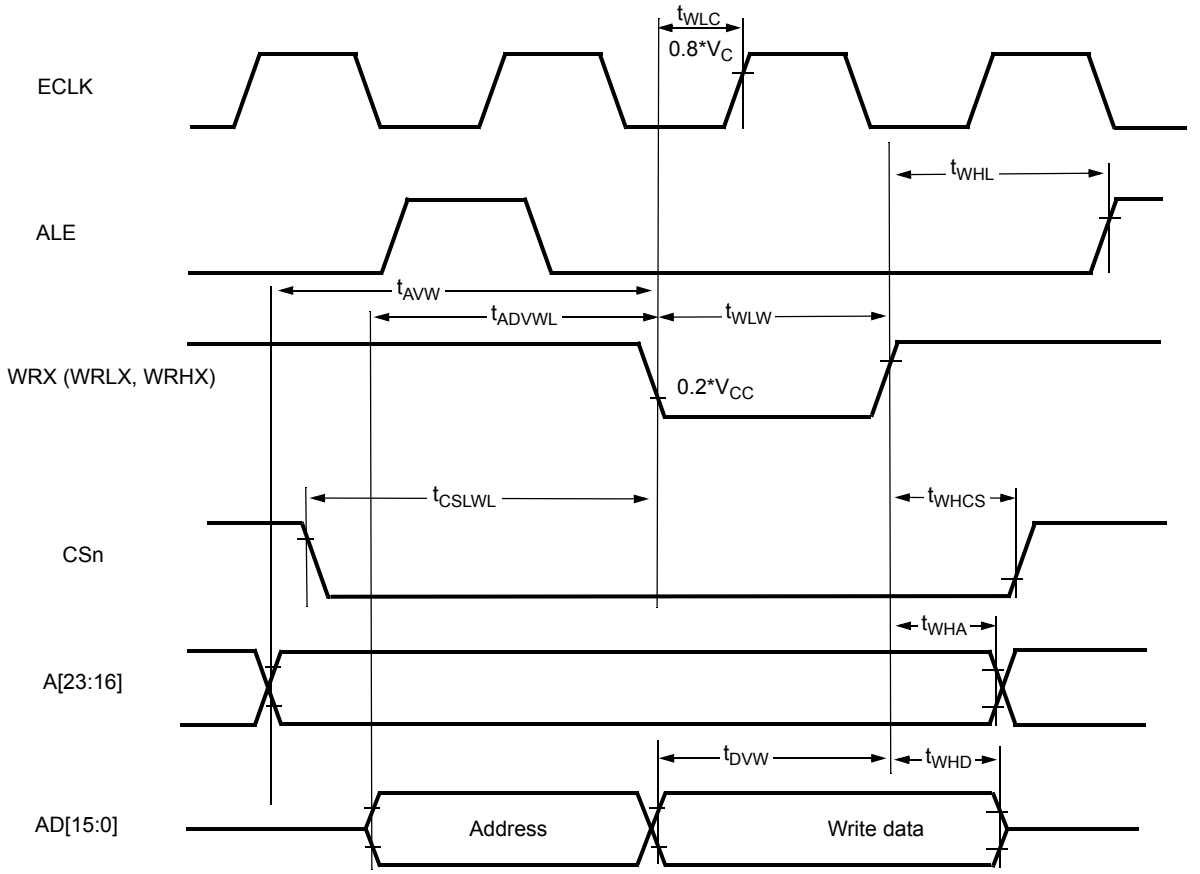
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 5$	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 20$	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 15$	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 15$	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 15$		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 15$	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	t_{CYC} – 8	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC} – 25	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2$ – 20	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2$ – 20	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ – 15	-	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} – 15	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2$ – 15	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2$ – 20	ns	
			EACL:ACE=1	-	$5t_{CYC}/2$ – 20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2$ – 20	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.4.10 Ready Input Timing

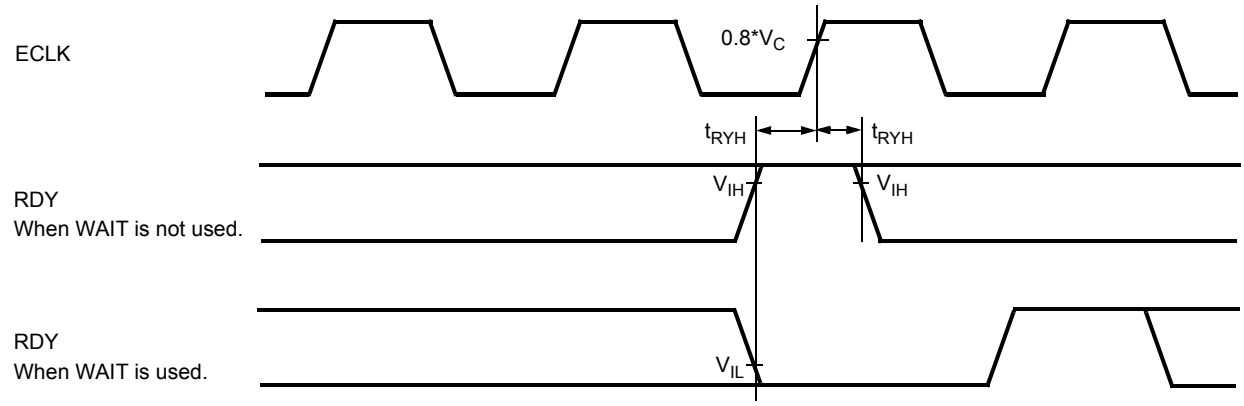
(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	35	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	45	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.



Refer to the Hardware Manual for detailed Timing Charts

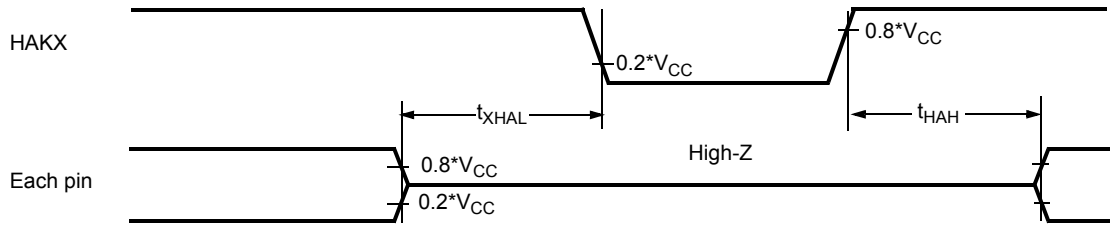
14.4.11 Hold Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 [1]	-	$N*t_{CLKP1}$ - 30 [1]	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2$ + 10	-	$t_{CLKP1}/2$ + 10	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

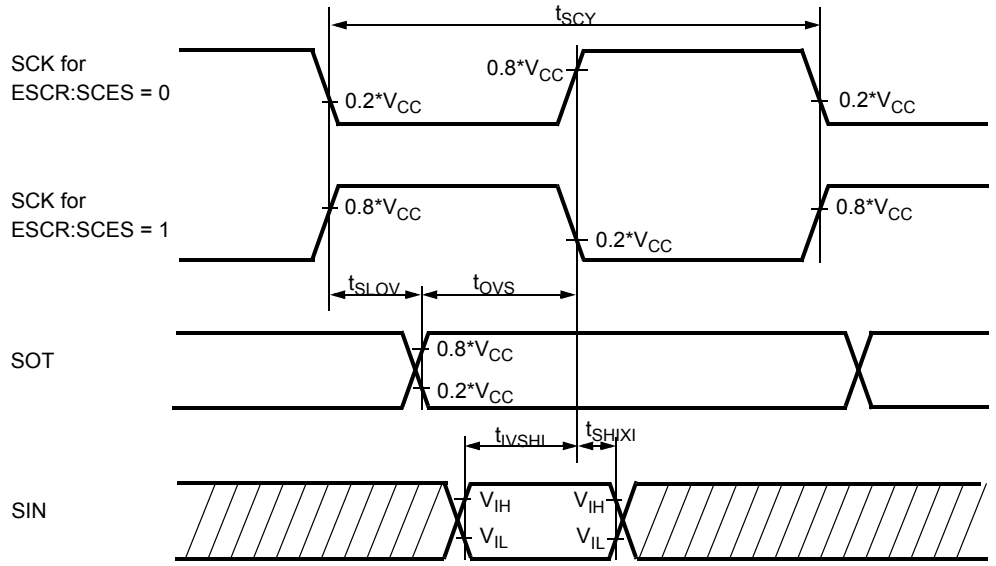
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “CY96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

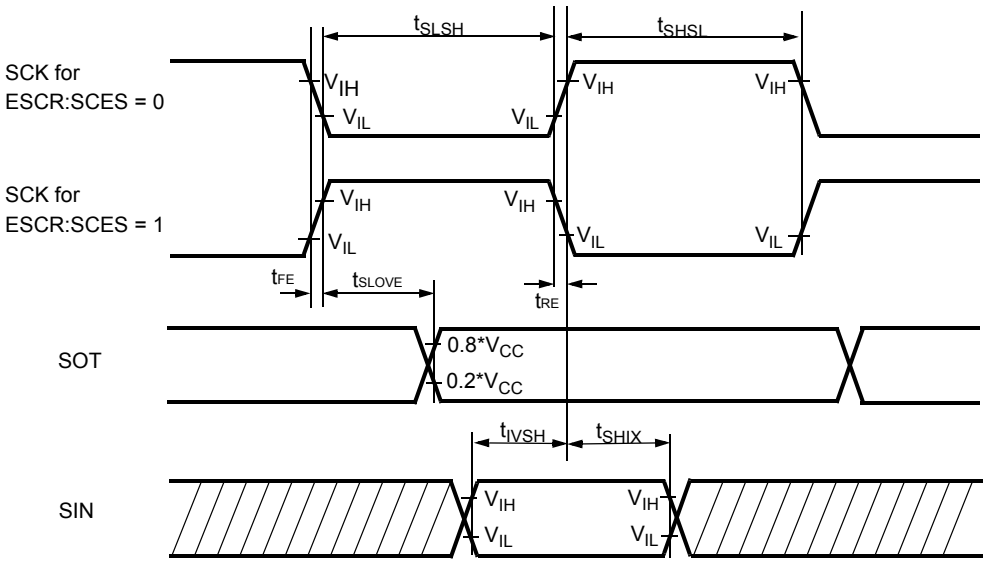
- if t_{SCYCI} = $2*k*t_{CLKP1}$, then N = k, where k is an integer > 2
- if t_{SCYCI} = $(2*k+1)*t_{CLKP1}$, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
$4*t_{CLKP1}$	2
$5*t_{CLKP1}$,	3
$7*t_{CLKP1}$,	4
...	...



Internal Shift Clock Mode



External Shift Clock Mode

14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

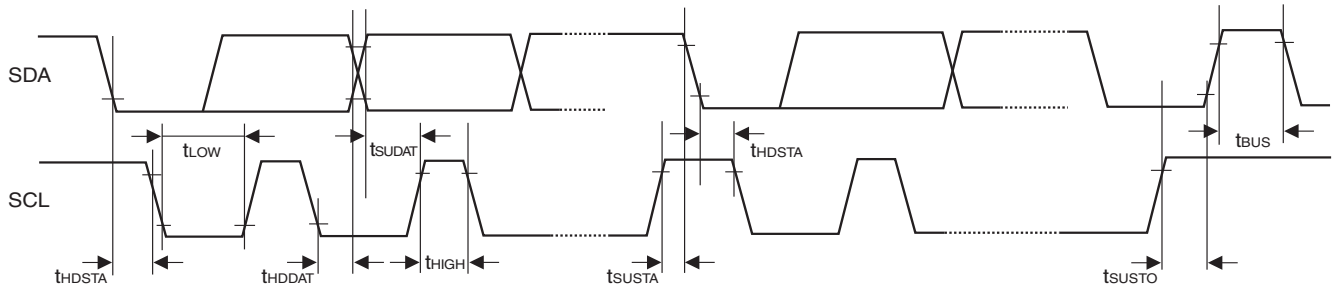
Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL¬	t_{HDSTA}		4.0	-	0.6	-	µs
"L" width of the SCL clock	t_{LOW}		4.7	-	1.3	-	µs
"H" width of the SCL clock	t_{HIGH}		4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↓→SDA↑	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold timeSCL↑→SDA↑↓	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs
Data set-up timeSDA↑↓→SCL↑	t_{SUDAT}		250	-	100	-	ns
Set-up time for STOP conditionSCL↑→SDA↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	-	1.3	-	µs

[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT}≥ 250 ns must then be met.

[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



14.5 Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

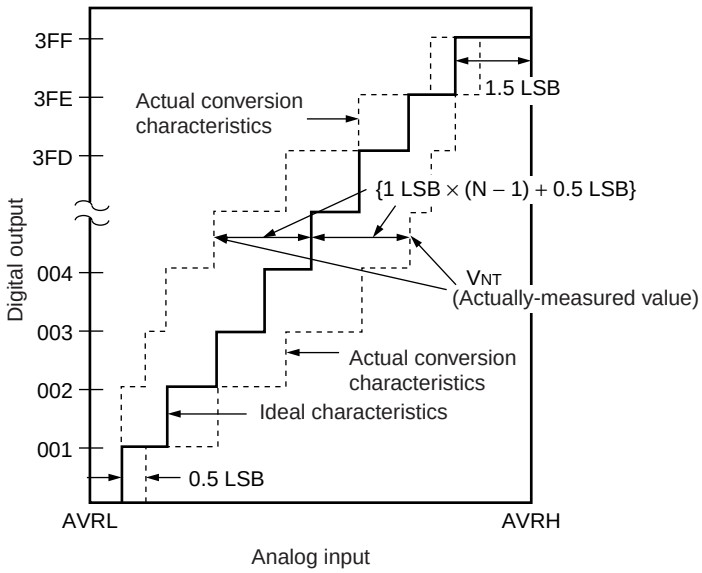
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input curren	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	T_A = 125 °C,AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH 2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

14.5.1 Definition of A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.
- Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Zero reading voltage: Input voltage which results in the minimum conversion value.
- Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\ [\text{V}]$$

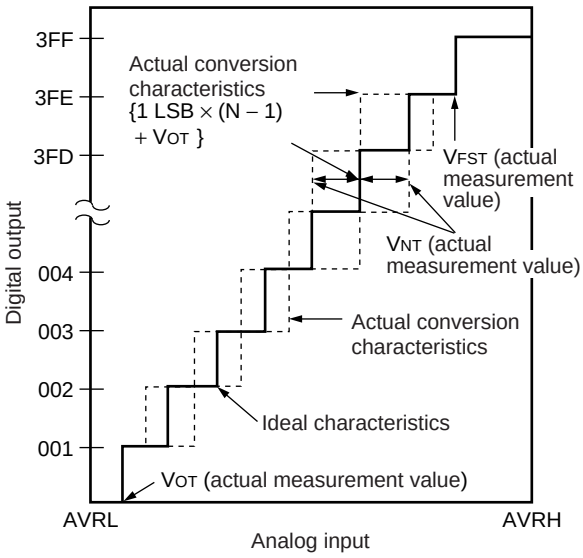
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

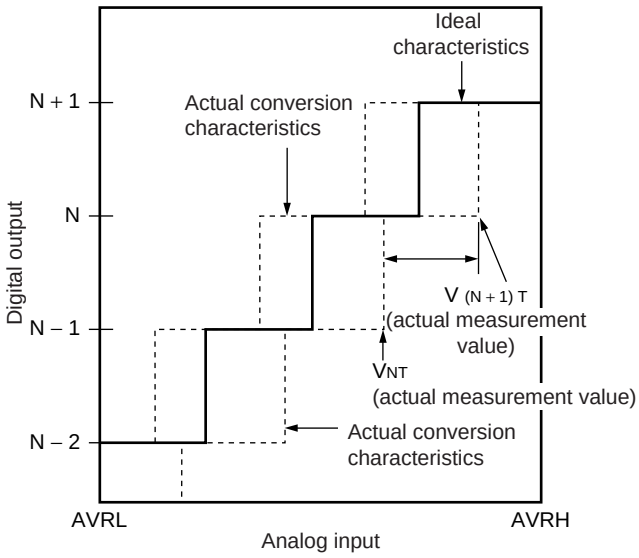
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N: A/D converter digital output value

V_{OT}: Voltage at which digital output transits from "000_H" to "001_H."

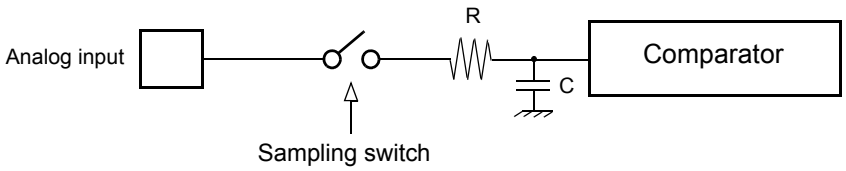
V_{FST}: Voltage at which digital output transits from "$3FE_H$" to "$\#FF_H$."

14.5.2 Notes on A/D Converter Section

■ About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model:



Reference value:
C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where τ = RC. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = 7 ∞ (R_{ext} + 2.6kΩ) × C for 4.5 ≤ AV_{cc} ≤ 5.5

T_{samp} [min] = 7 ∞ (R_{ext} + 12.1kΩ) × C for 3.0 ≤ AV_{cc} ≤ 4.5

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

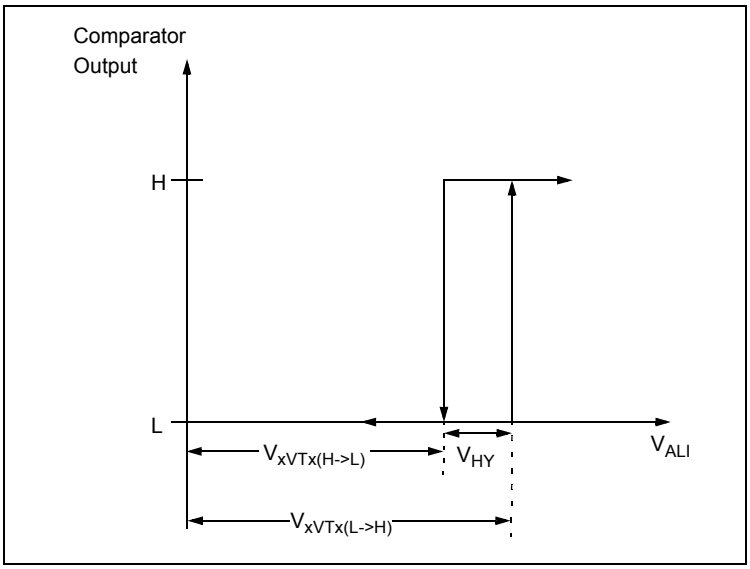
■ About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

14.6 Alarm Comparator

(T_A = -40 °C to +125 °C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 °C
			-3	-	+3	µA	T_A = 125 °C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	


Comparator
Output
H
L
$V_{xVTx(H->L)}$
V_{HY}
V_{ALI}
$V_{xVTx(L->H)}$

14.7 Low Voltage Detector Characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: CY96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

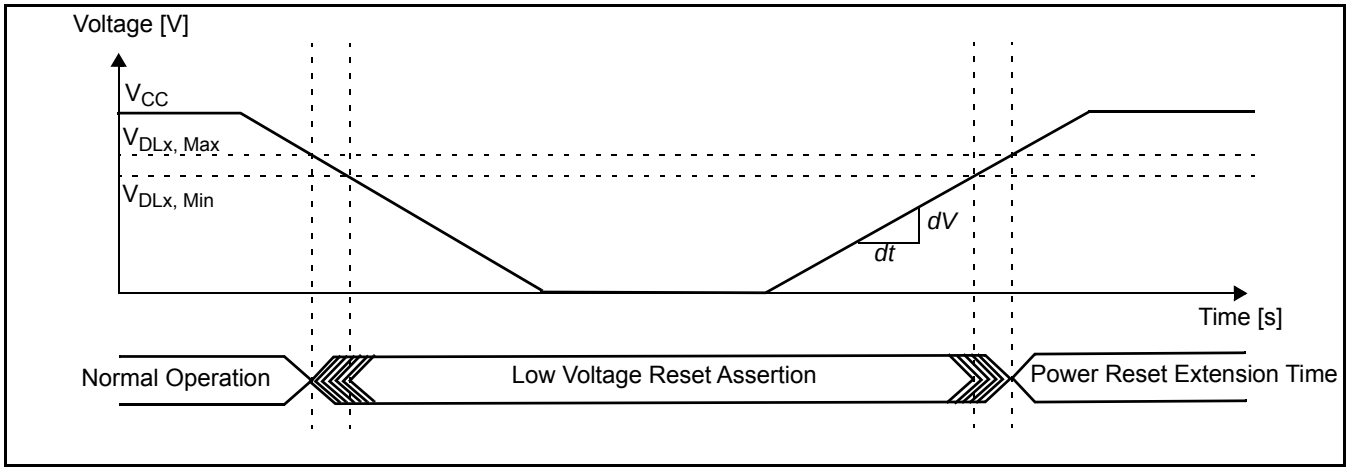
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

14.7.1 Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



14.8 Flash Memory Program/erase Characteristics

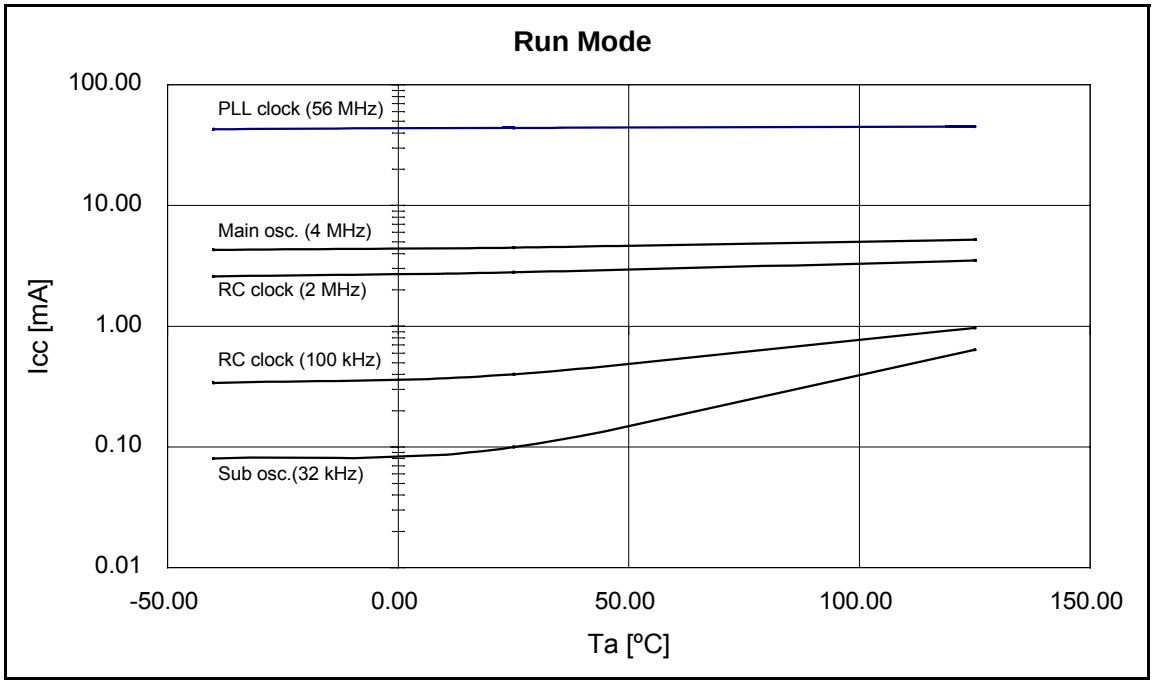
(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

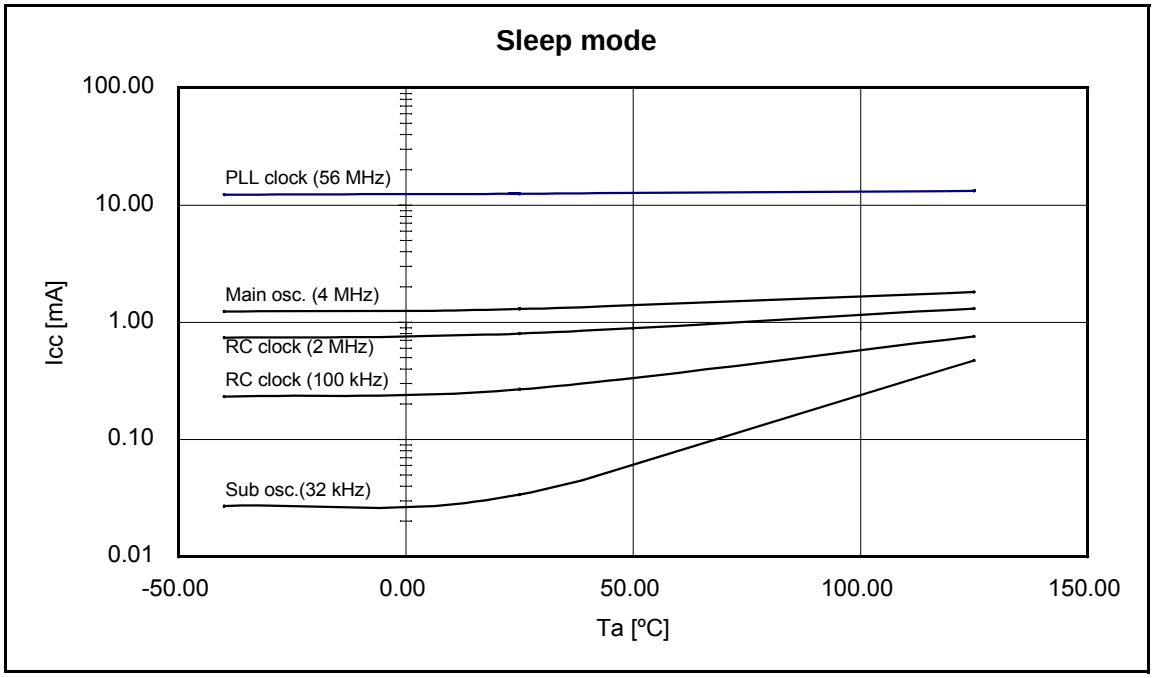
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time Program/Data Flash (Main Flash)	-	0.9	3.6	s	Without erasure pre-programming time
Sector erase time Data Flash	-	0.5	2	s	Without erasure pre-programming time
	-	0.8	3.6	s	Including erasure pre-programming time
Chip erase time Program/Data Flash (Main Flash)	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Chip erase timeData Flash	-	2.5	10	s	Without erasure pre-programming time
	-	3.7	16.4	s	Including erasure pre-programming time
Word (16-bit width) programming time Program/Data Flash (Main Flash)	-	23	370	us	Without overhead time for submitting write command
Byte (8-bit width) programming time Data Flash	-	15	100	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	100 000 Program/Erase cycles are under evaluation by Cypress
Flash data retention time	20	-	-	year	[1]

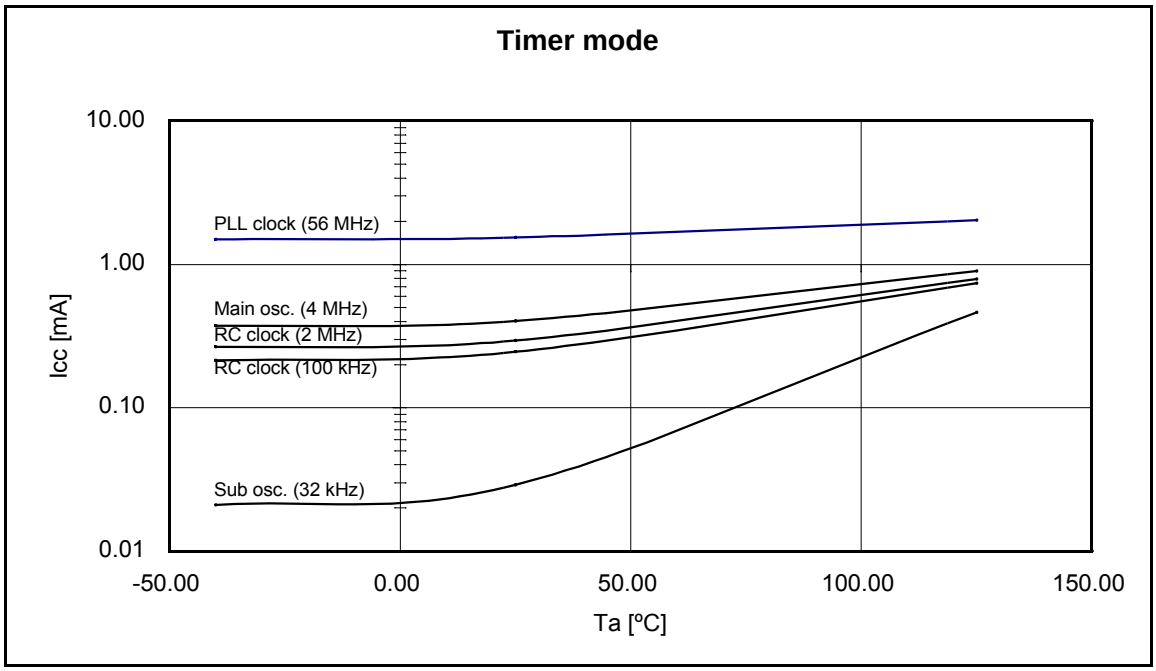
[1]: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85^{o}C)

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.






Timer mode
10.00
1.00
0.10
0.01
Icc [mA]
PLL clock (56 MHz)
Main osc. (4 MHz)
RC clock (2 MHz)
RC clock (100 kHz)
Sub osc. (32 kHz)
-50.00
0.00
50.00
100.00
150.00
Ta [ºC]

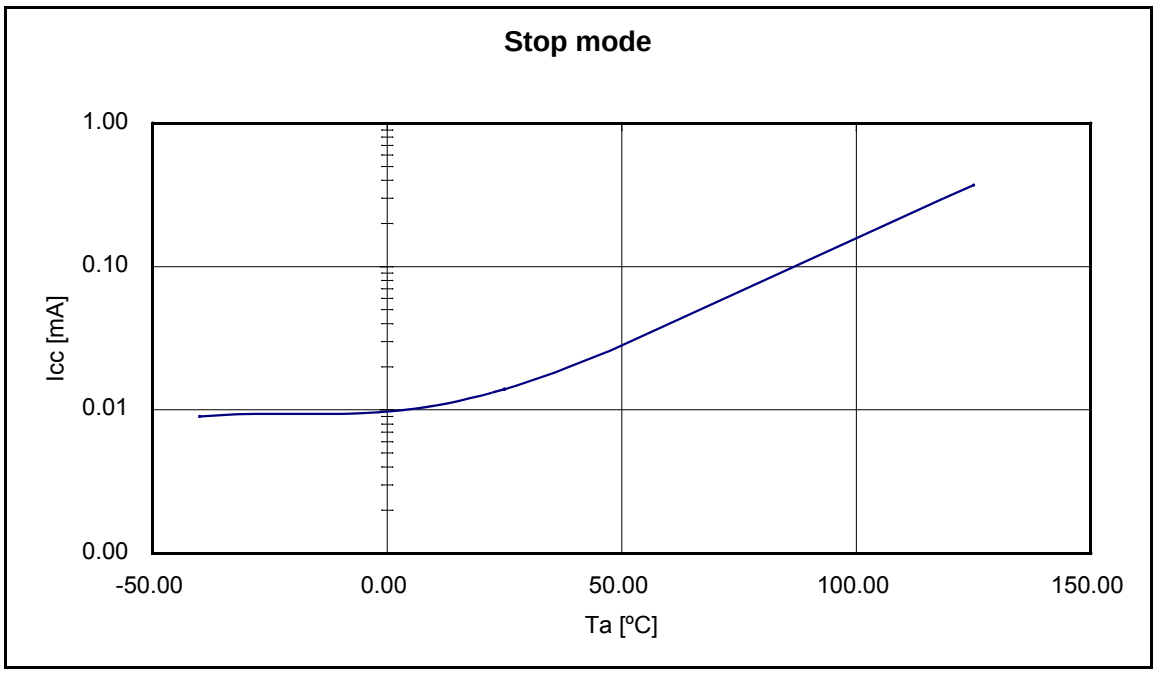

Stop mode
1.00
0.10
0.01
0.00
Icc [mA]
-50.00
0.00
50.00
100.00
150.00
Ta [ºC]

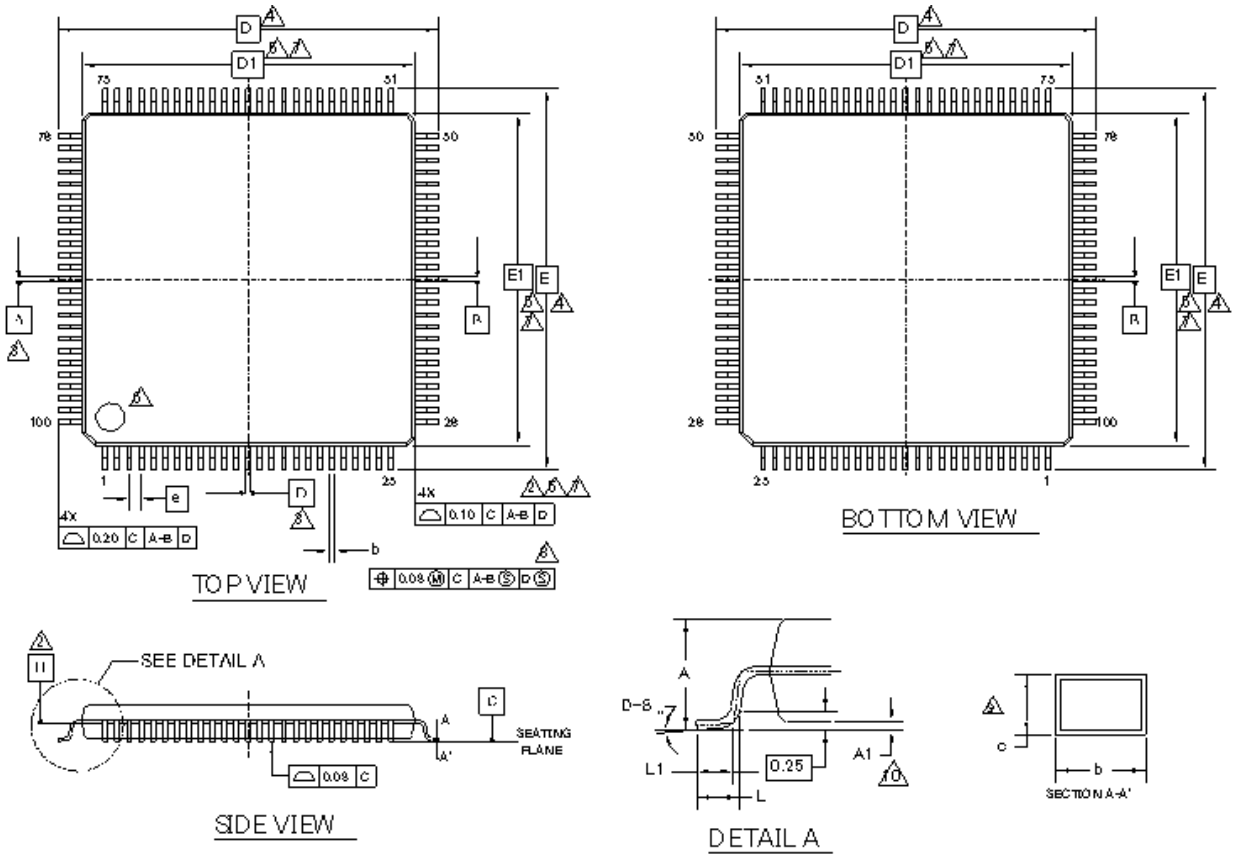
Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

16. Package Dimension CY96(F)34x LQFP 100P



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

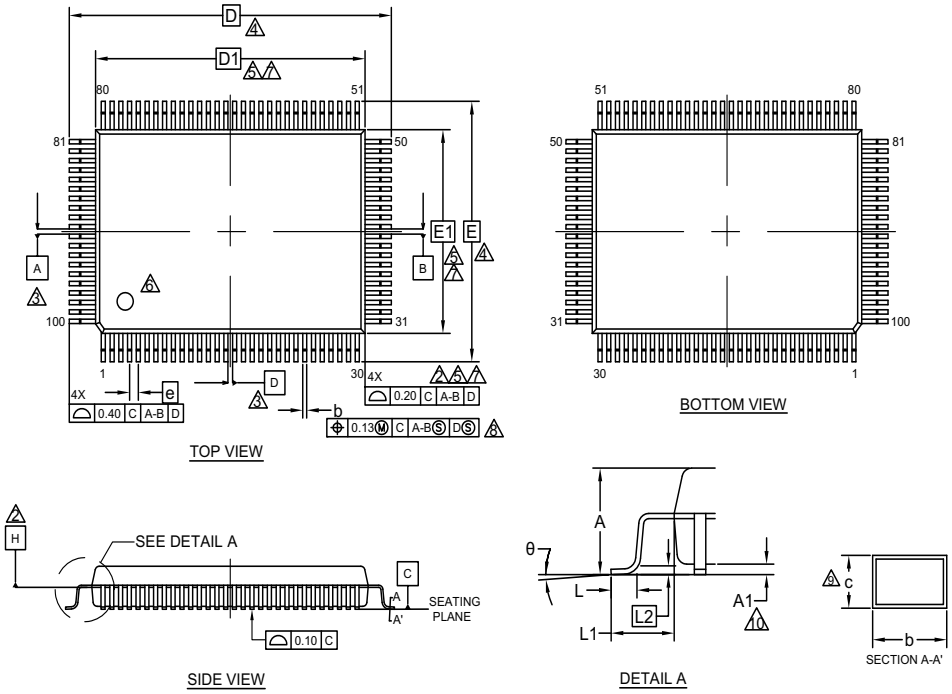
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *A

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQT100 REV*A

17. Package Dimension CY96(F)34x QFP 100P



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15156 **

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
CY96345RSAPMC-GSE1	ROM (160KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96346RSAPMC-GSE2	ROM (288KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F345DSBPMC-GS-UJE1	Flash A (160KB) Data Flash A (64KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F346RSAPMCR-GS-UJE2	Flash A (288KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F346RWAPMCR-GS-UJE2		Yes		
CY96F346RSAPQCR-GS-UJE2		No	No	100 pin Plastic QFP (PQH100)
CY96F346RWAPQCR-GS-UJE2		Yes		
CY96F346RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F346RWBPMC-GS-UJE2		Yes		
CY96F346RSBPQC-GS-UJE2		No	No	100 pin Plastic QFP (PQH100)
CY96F346RWBPQC-GS-UJE2		Yes		
CY96F346RSCPMC-GS-UJE1		No	No	100 pin Plastic LQFP (LQI100)
CY96F347RSAPQCR-GS-UJE2	Flash A (416KB)	No	No	100 pin Plastic QFP (PQH100)
CY96F347RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSAPMCR-GS-UJE2	Flash A (544KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSAPQCR-GS-UJE2				100 pin Plastic QFP (PQH100)
CY96F348RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSBPQC-GS-UJE2				100 pin Plastic QFP (PQH100)
CY96F348RSBPQCR-GS-UJE2				
CY96F348RWCPMC-G-UJE2		Yes	No	100 pin Plastic LQFP (LQI100)
CY96F348HSBPMCR-GSE2	Flash A (544KB) Flash B (32KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSBPQCR-GSE2		No	No	100 pin Plastic QFP (PQH100)
CY96F348HSCPMC-GSE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSCPMC-GSE1		No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSCPQC-GSE2		No	No	100 pin Plastic QFP (PQH100)

18.2 MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
CY96F346ASBPMCR-GS-UJE2	Flash A (288KB)	No	100 pin Plastic LQFP (LQI100)
CY96F346ASBPQC-G-UJE2			100 pin Plastic QFP (PQH100)
CY96F347ASBPMC-GS-UJE2	Flash A (416KB)		100 pin Plastic LQFP (LQI100)
CY96F348ASBPMC-GS-UJE2	Flash A (544KB)		

This datasheet is also valid for the following outdated devices:

CY96F346YSA, CY96F346YWA,
CY96F347YSA, CY96F347YWA, CY96F347RWA,
CY96F348YSA, CY96F348YWA, CY96F348RWA,
CY96F348TSB, CY96F348TWB, CY96F348HWB,
CY96F346ASA, CY96F346AWA,
CY96F347ASA, CY96F347AWA,
CY96F348ASA, CY96F348AWA,
CY96F348CSB, CY96F348CWB

19. Major Changes

Page	Section	Change Results
Rev *A		
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)
Rev *B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
1	-	Deleted the following comment. MB96F345: These devices are under development and specification is preliminary. These products under development may change its specification without notice.
7	1. Product Lineup	Deleted the following comment. [1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.
63	14. Electrical Characteristics 14.3 DC characteristics	Updated below I_{CCPLL} value for MB96F345 at 1 Flash wait state. "PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)" "T_A = +25 °C" (before) Typ: TBD Max: TBD (after) Typ: 38 Max: 51 "T_A = +125 °C" (before) Typ: TBD Max: TBD (after) Typ: 40 Max: 54

Page	Section	Change Results
65	14. Electrical Characteristics 14.3 DC characteristics	Updated below I_{CCSPLL} value for MB96F345. "PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)" "T_A = +25 °C" (before) Typ: TBD Max: TBD (after) Typ: 11 Max: 13.5 "T_A = +125 °C" (before) Typ: TBD Max: TBD (after) Typ: 11.7 Max: 16
10 101 103, 104	3. Pin Assignment 16. Package Dimension CY96(F)34x LQFP 100P 18. Ordering Information	Package description modified to JEDEC description. (before) FPT-100P-M20 (after) LQI100
9 102 103, 104	3. Pin Assignment 17. Package Dimension CY96(F)34x QFP 100P 18. Ordering Information	Package description modified to JEDEC description. (before) FPT-100P-M22 (after) PQH100

Page	Section	Change Results
103, 104	18. Ordering Information	Deleted the following comment. [1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice. Deleted the following part number. - MB96345YSA PQC-GSE2 - MB96345RSA PQC-GSE2 - MB96345YWA PQC-GSE2 - MB96345RWA PQC-GSE2 - MB96345YSA PMC-GSE2 - MB96345RSA PMC-GSE2 - MB96345YWA PMC-GSE2 - MB96345RWA PMC-GSE2 - MB96346YSA PQC-GSE2 - MB96346RSA PQC-GSE2 - MB96346YWA PQC-GSE2 - MB96346RWA PQC-GSE2 - MB96346YSA PMC-GSE2 - MB96346YWA PMC-GSE2 - MB96346RWA PMC-GSE2 - MB96F345FSA PQC-GSE2 - MB96F345DSA PQC-GSE2 - MB96F345FWA PQC-GSE2 - MB96F345DWA PQC-GSE2 - MB96F345FSA PMC-GSE2 - MB96F345DSA PMC-GSE2 - MB96F345FWA PMC-GSE2 - MB96F345DWA PMC-GSE2 - MB96F346YSB PQC-GSE2 - MB96F346YWB PQC-GSE2 - MB96F346YSB PMC-GSE2 - MB96F346YWB PMC-GSE2 - MB96F347YSB PQC-GSE2 - MB96F347RSB PQC-GSE2 - MB96F347YWB PQC-GSE2 - MB96F347RWB PQC-GSE2 - MB96F347YSB PMC-GSE2 - MB96F347YWB PMC-GSE2 - MB96F347RWB PMC-GSE2 - MB96F348YSB PQC-GSE2 - MB96F348YWB PQC-GSE2 - MB96F348RWB PQC-GSE2 - MB96F348YSB PMC-GSE2 - MB96F348YWB PMC-GSE2 - MB96F348RWB PMC-GSE2 - MB96F348TSC PQC-GSE2 - MB96F348TWC PQC-GSE2 - MB96F348HWC PQC-GSE2 - MB96F348TSC PMC-GSE2 - MB96F348TWC PMC-GSE2 - MB96F348HWC PMC-GSE2 - MB96V300BRB-ES(for evaluation)

Page	Section	Change Results
103, 104	18. Ordering Information	Deleted the following part number. (Continue) - MB96F346ASB PQC-GSE2 - MB96F346AWB PQC-GSE2 - MB96F346ASB PMC-GSE2 - MB96F346AWB PMC-GSE2 - MB96F347ASB PQC-GSE2 - MB96F347AWB PQC-GSE2 - MB96F347AWB PMC-GSE2 - MB96F348ASB PQC-GSE2 - MB96F348AWB PQC-GSE2 - MB96F348AWB PMC-GSE2 - MB96F348CSC PQC-GSE2 - MB96F348CWC PQC-GSE2 - MB96F348CSC PMC-GSE2 - MB96F348CWC PMC-GSE2 Revised the following parts number. (before) - MB96346RSA PMC-GSE2 - MB96F346RSB PQC-GSE2 - MB96F346RWB PQC-GSE2 - MB96F346RSB PMC-GSE2 - MB96F346RWB PMC-GSE2 - MB96F347RSB PMC-GSE2 - MB96F348RSB PQC-GSE2 - MB96F348RSB PMC-GSE2 - MB96F348HSC PQC-GSE2 - MB96F348HSC PMC-GSE2 - MB96F347ASB PMC-GSE2 - MB96F348ASB PMC-GSE2 (after) - CY96346RSAPMC-GSE2 - CY96F346RSBPQC-GS-UJE2 - CY96F346RWBPQC-GS-UJE2 - CY96F346RSBPMC-GS-UJE2 - CY96F346RWBPMC-GS-UJE2 - CY96F347RSBPMC-GS-UJE2 - CY96F348RSBPQC-GS-UJE2 - CY96F348RSBPMC-GS-UJE2 - CY96F348HSCPQC-GS-UJE2 - CY96F348HSCPMC-GS-UJE2 - CY96F347ASBPMC-GS-UJE2 - CY96F348ASBPMC-GS-UJE2 Added the following parts number. - CY96345RSAPMC-GSE1 - CY96F345DSBPMC-GS-UJE1 - CY96F346RSAPMCR-GS-UJE2 - CY96F346RWAPMCR-GS-UJE2 - CY96F346RSAPQCR-GS-UJE2 - CY96F346RWAPQCR-GS-UJE2 - CY96F346RSCPMC-GS-UJE1 - CY96F347RSAPQCR-GS-UJE2 - CY96F348RSAPMCR-GS-UJE2 - CY96F348RSAPQCR-GS-UJE2 - CY96F348RSBPQCR-GS-UJE2 - CY96F348RWCPMC-G-UJE2 - CY96F348HSBPMCR-GSE2 - CY96F348HSBPQCR-GSE2 - CY96F348HSCPMC-GSE1 - CY96F346ASBPMCR-GS-UJE2 - CY96F346ASBPQC-G-UJE2

Page	Section	Change Results
103, 104	18. Ordering Information	Changed and deleted the parts number in Note. (before) MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA, MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA, MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA, MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB, MB96F346ASA, MB96F346AWA, MB96F347ASA, MB96F347AWA, MB96F348ASA, MB96F348AWA, MB96F348CSB, MB96F348CWB (after) CY96F346YSA, CY96F346YWA, CY96F347YSA, CY96F347YWA, CY96F347RWA, CY96F348YSA, CY96F348YWA, CY96F348RWA, CY96F348TSB, CY96F348TWB, CY96F348HWB, CY96F346ASA, CY96F346AWA, CY96F347ASA, CY96F347AWA, CY96F348ASA, CY96F348AWA, CY96F348CSB, CY96F348CWB
105	19. Major Changes	Changed section title and section number. (before) 20. Main Changes in this Edition (after) 19. Major Changes
110	20. Revision History	Changed section number. (before) 19. Revision History (after) 20. Revision History

20. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices” ■ Parallel Flash programming pinning removed ■ IO map table regenerated: ❒ Port register: Naming style corrected ❒ Memory control registers renamed (Main/Sat -> A/B) ❒ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

Revision	Date	Modification
9	2009-01-09	■ Format adjusted to official Cypress datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ Note about devices under development modified ■ I/O map: Note added about reserved addresses ■ ICCSPLL for CLKS1=96MHz mode: increased by 1mA ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Lineup: Term “Data Flash” replaced by “independent 32KB Flash” ■ Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F345 added ■ Preliminary DC spec of MB96345/346 added ■ Permitted power dissipation of Flash devices in QFP package improved ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ “Preliminary” watermark removed
10	To be released	■ I/O map: IOABK0-5 added at address 000A00H-000A05H ■ Ordering Information: Suffix “A” added to all MB96F345 device versions ■ AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg

NOTE: Please see “Document History” for later revised information.

Document History

Spansion Publication Number: **DS07-13802-3E**

Document Title: CY96345/346, CY96F346/F347/F348, F^{2}MC-16FX, CY96340 Series, 16-bit Proprietary Microcontroller Datasheet Document Number: 002-04579				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/01/2016	Updated to Cypress template
*B	6184340	GSHI	05/31/2018	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 3.Pin Assignments 16.Package Dimension 17.Package Dimension 18.Ordering Information Added 19. Major Changes For details, please see 19.Major Changes

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