THE DATASHEET OF

PI4IOE5V6416ZDEX

Low-Voltage Translating 16-bit I2C-bus I/O Expander

Features

- Operation power supply voltage from 1.65V to 5.5V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8/2.5/3.3/5V SCL/SDA and 1.8/2.5/3.3/5V Port
- Low standby current consumption:
  - 1.5 μA typical at 5 V V_{DD}
  - 1 μA typical at 3.3 V V_{DD}
- 400kHz I^2C-bus interface
- Compliant with the I^2C-bus Fast and Standard modes
- Programmable Push-pull/Open-drain output stages
- Programmable output drive strength and pull-up/down resistor
- Power-on reset
- Active LOW open-drain interrupt output
- Active LOW reset input
- Latch-up tested (exceeds 100mA)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Packaging (Pb-free & Green):
  - 24-Pin TQFN (ZD24)
  - 24-Pin TSSOP (L24)

Description

The PI4IOE5V6416 is a 16-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I^2C-bus interface.

It provides a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc.

It can operate from 1.65 V to 5.5 V on the GPIO-port side and 1.65 V to 5.5 V on the SDA/SCL side. This allows the PI4IOE5V6416 to interface with next generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power.

The bidirectional voltage-level translation in the PI4IOE5V6416 is provided through $V_{DD(I2C\_bus)}$. $V_{DD(I2C\_bus)}$ should be connected to the V_{DD} of the external SCL/SDA lines. The voltage level on the GPIO-port of the PI4IOE5V6416 is determined by $V_{DD(P)}$.

At power on, the I/Os are configured as inputs; however, the system master can enable the I/Os as either inputs or outputs by writing to the I/O direction bits. The data for each input or output is kept in the corresponding Input or Output register. All registers can be read by the system master.

PI4IOE5V6416 has open-drain interrupt ($\overline{INT}$) output pin that goes LOW when the input state of a GPIO-port changes from the input-state default register value. The device also has an interrupt masking feature by which the user can mask the interrupt from an individual GPIO-port.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

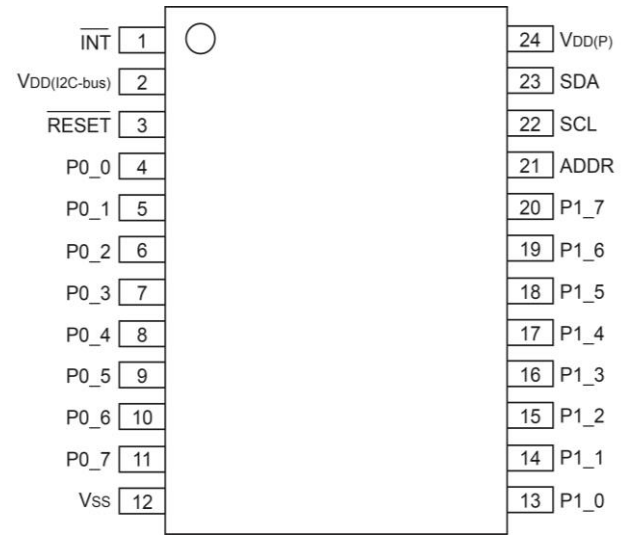


Fig.1 24-pin TSSOP

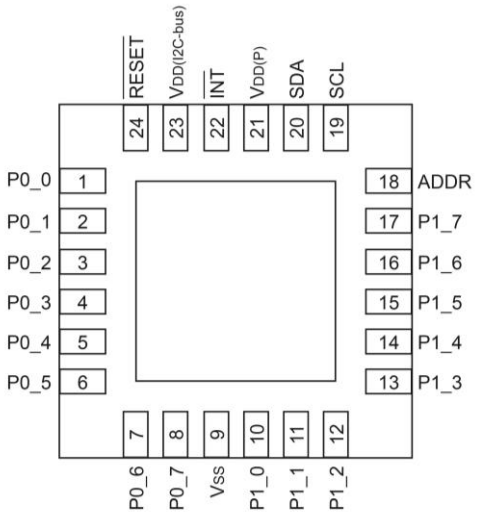


Fig.2 24-pin TQFN

Pin Description

Pin Name	24-pin TSSOP	24-pin TQFN	24-pin VFBGA	Description
$\overline{INT}$	1	22	A3	Interrupt output. Connect to $V_{DD(I2C-bus)}$ or $V_{DD(P)}$ through a pull-up resistor.
$V_{DD(I2C\_bus)}$	2	23	B3	Supply voltage of I2C-bus. Connect directly to the VDD of the external I2C master. Provides voltage-level translation.
$\overline{RESET}$	3	24	A2	Active LOW reset input. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor if no active connection is used.
P0_0	4	1	A1	Port 0 input/output 0.
P0_1	5	2	C3	Port 0 input/output 1.
P0_2	6	3	B1	Port 0 input/output 2.
P0_3	7	4	C1	Port 0 input/output 3.
P0_4	8	5	C2	Port 0 input/output 4.
P0_5	9	6	D1	Port 0 input/output 5.
P0_6	10	7	E1	Port 0 input/output 6.
P0_7	11	8	D2	Port 0 input/output 7.
V_{SS}	12	9	E2	Ground
P1_0	13	10	E3	Port 1 input/output 0.
P1_1	14	11	E4	Port 1 input/output 1.
P1_2	15	12	D3	Port 1 input/output 2.
P1_3	16	13	E5	Port 1 input/output 3.
P1_4	17	14	D4	Port 1 input/output 4.
P1_5	18	15	D5	Port 1 input/output 5.
P1_6	19	16	C5	Port 1 input/output 6.
P1_7	20	17	C4	Port 1 input/output 7.
ADDR	21	18	B5	Address input. Connect directly to $V_{DD(P)}$ or ground.
SCL	22	19	A5	Serial clock bus. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor.
SDA	23	20	A4	Serial data bus. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor.
$V_{DD(P)}$	24	21	B4	Supply voltage of PI4IOE5V6416 for Port P.

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin (Input / Output)	-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current through $V_{DD(P)}$	160mA
Ground supply current	200mA
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum junction temperature ,T j(max)	125℃
ESD (HBM)	2kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD(I2C-bus)}$	I^2C-bus supply voltage		1.65	-	5.5	V
$V_{DD(P)}$	GPIO port supply voltage		1.65	-	5.5	V
V_{IN}	Input voltage on ADDR, P1_7 to P0_0		0	-	$V_{DD(P)}$	V
	Input voltage on SCL, SDA, $\overline{\text{RESET}}$		0	-	$V_{DD(I2C\_BUS)}$	V
I_{OH}	High-Level Output Current		-	-	10	mA
I_{OL}	Low-Level Output Current		-	-	25	mA

Static Characteristics

$V_{DD(I2C\_bus)}$ = 1.65 V to 5.5 V; Temp = -40℃ to +85℃; unless otherwise specified. Typical values are at Temp = 25℃.

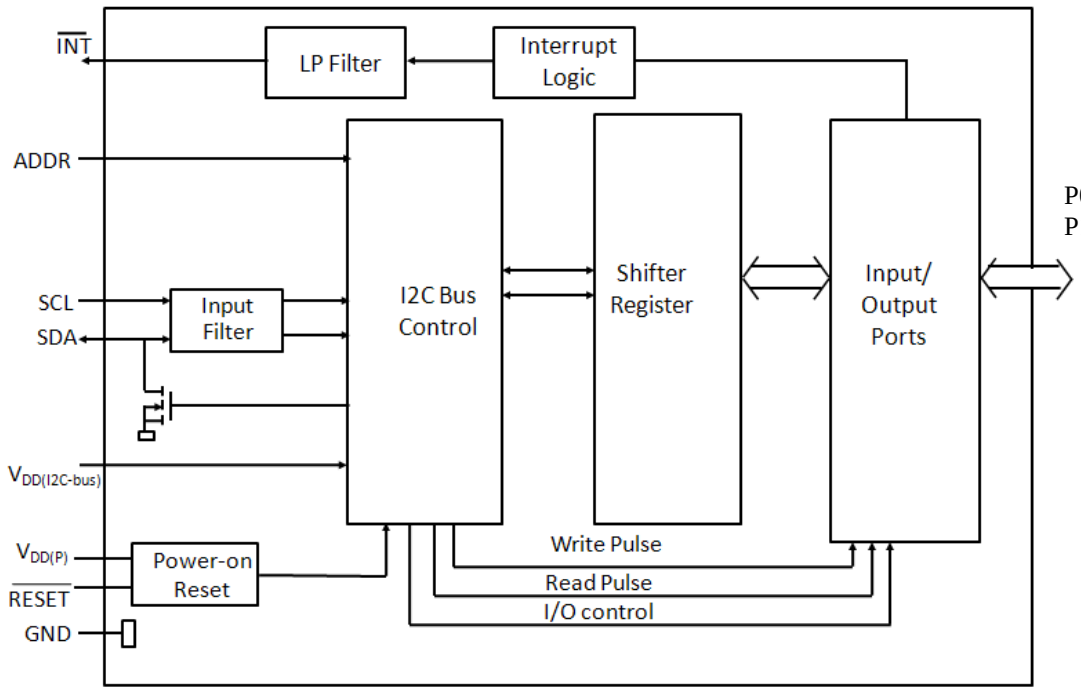
Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Power supply							
I_{DD}	Supply current	Standby mode I/O = inputs; f_{SCL} = 0 kHz	$V_{DD(P)}$=3.6-5.5V	-	1.5	7	μA
			$V_{DD(P)}$=2.3-3.6V		1	3.2	
			$V_{DD(P)}$=1.65-2.3V		0.5	1.7	
		Standby mode I/O = inputs; f_{SCL} = 400 kHz	$V_{DD(P)}$=3.6-5.5V	-	10	25	
			$V_{DD(P)}$=2.3-3.6V		6.5	15	
			$V_{DD(P)}$=1.65-2.3V		4	9	
		Active mode I/O = inputs; f_{SCL} = 400 kHz, continuous register read	$V_{DD(P)}$=3.6-5.5V	-	60	125	
			$V_{DD(P)}$=2.3-3.6V		40	75	
			$V_{DD(P)}$=1.65-2.3V		20	45	
V_{POR}	Power-on reset voltage	Rising		-	1.1-	1.4	V
		Falling		0.5	-	-	
$T_{d(rst)}$	Reset time	Time of $V_{DD(P)}$ drop to $V_{POR(min)}$ − 50 mV for successful Power-on reset		1	-	-	μs
Input SCL, input/output SDA							
V_{IL}	Low level input voltage			-0.5	-	0.3 $V_{DD(I2C-bus)}$	V
V_{IH}	High level input voltage			0.7 $V_{DD(I2C-bus)}$	-	5.5	V
I_{OL}	SDA Low level output current	V_{OL}= 0.4 V		3	-	-	mA
I_L	Leakage current	V_{IN} = $V_{DD(I2C\_bus)}$ or V_{SS}		-1	-	1	μA
C_i	Input capacitance	V_{IN} = V_{SS}		-	7	8	pF
Interrupt $\overline{INT}$							
I_{OL}	Low level output current	V_{OL}=0.4V		3	-	-	mA
C_o	Output capacitance			-	7	8	pF
Select inputs ADDR and $\overline{RESET}$							
V_{IL}	RESET Low level input voltage			-0.5	-	0.3 $V_{DD(I2C-bus)}$	V
	ADDR Low level input voltage			-0.5	-	0.3 $V_{DD(P)}$	
V_{IH}	RESET High level input voltage			0.7 $V_{DD(I2C-bus)}$	-	5.5	V
	ADDR High level input voltage			0.7 $V_{DD(P)}$	-	5.5	
I_L	Input leakage current			-1	-	1	μA
Ci	Input capacitance			-	6	7	pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low-level input voltage	P0 – P7	-0.5	-	$+0.3*V_{DD(P)}$	V
V_{IH}	High-level input voltage	P0 – P7	$0.7*V_{DD(P)}$	-	5.5	V
V_{OH}	High-level output voltage	I_{OH} = -2.5mA; CCX.X=00b I_{OH} = -5mA; CCX.X=01b I_{OH} = -7.5mA; CCX.X=10b I_{OH} = -10mA; CCX.X=11b				
		$V_{DD(P)}$ = 1.65 V	1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.7	-	-	
		$V_{DD(P)}$ = 3 V	2.5	-	-	
		$V_{DD(P)}$ = 4.5 V	4.0	-	-	
V_{OL}	Low-level output voltage	I_{OL} = 2.5mA; CCX.X=00b I_{OL} = 5mA; CCX.X=01b I_{OL} = 7.5mA; CCX.X=10b I_{OL} = 10mA; CCX.X=11b				
		$V_{DD(P)}$ = 1.65 V	-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.3	
		$V_{DD(P)}$ = 3 V	-	-	0.25	
		$V_{DD(P)}$ = 4.5 V	-	-	0.2	
I_{IH}	High-level input current	P port; $V_I = V_{DD(P)}$	-	-	1	µA
I_{IL}	Low-level input current	P port; $V_I = V_{SS}$	-	-	1	µA
$R_{pu(int)}$	Internal pull-up resistance	Input/Output	50	100	150	kΩ
$R_{pd(int)}$	Internal pull-down resistance	Input/Output	50	100	150	kΩ

Dynamic Characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	ns
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	ns
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
t_f	Fall time of both SDA and SCL signals	-	300	20 x (VDD/5.5V)	300	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns
Interrupt timing						
$t_{V(INT)}$	Valid time on pin $\overline{INT}$	-	1	-	1	µs
$t_{RST(INT)}$	Reset time on pin $\overline{INT}$	-	1	-	1	µs
Reset timing						
$t_{w(rst)}$	Reset pulse width	30	-	30	-	ns
t_{rst_rec}	Reset recovery time	200	-	200	-	ns
t_{rst}	Reset time	600	-	600	-	ns
P Port timing						
$t_{V(Q)}$	Data output valid time (from SCL to P Port)	-	400	-	400	ns
$t_{SU(D)}$	Data input setup time (from P Port to SCL)	0	-	0	-	ns
$t_{h(D)}$	Data input hold time (from P Port to SCL)	300	-	300	-	ns

Block Diagram



Note: All I/Os are set to inputs at reset.

Fig7: Block diagram

Functional Description

I²C Read /Write Procedures

Figure 6 and Figure 7 illustrate compatible I²C write and read sequences.

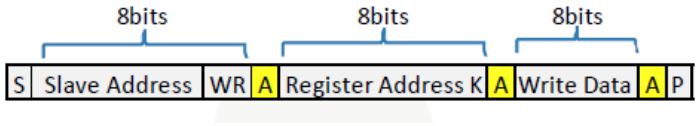
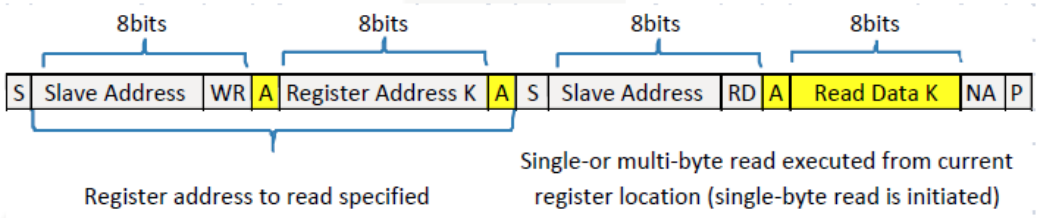
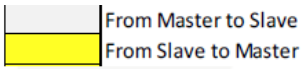


Fig 6. I²C Write Sequence



Note : if register is not specified , the master reads from the current register

Fig 7. I²C Read Sequence

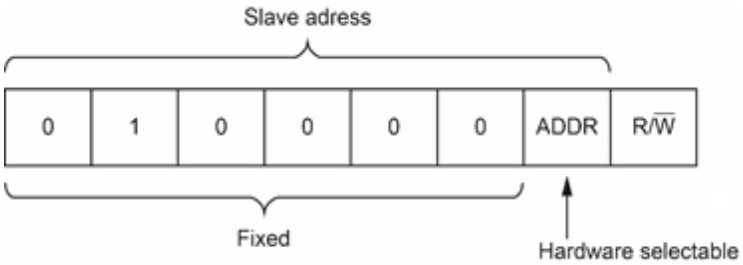


S Start P Stop NA Not Acknowledge A Acknowledge WR Write RD Read

a. Slave Address

The address of the PI4IOE5V6416 is shown in Figure 10.

Fig. 10: PI4IOE5V6416 address



ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

b. Register Address

Following the successful acknowledgement of the address byte, the bus master sends a register address, which is stored in the Pointer register in the PI4IOE5V6416. The data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, Configuration, or the extended features of the device). This register is write only.

Table 3: Interface definition

Register Address Bits								Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0			
0	0	0	0	0	0	0	0	Input port 0	read byte	xxxx xxxx
0	0	0	0	0	0	0	1	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	Configuration port 1	read/write byte	1111 1111
0	1	0	0	0	0	0	0	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	1	0	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	0	1	1	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	1	0	0	Input latch register 0	read/write byte	0000 0000
0	1	0	0	0	1	0	1	Input latch register 1	read/write byte	0000 0000
0	1	0	0	0	1	1	0	Pull-up/pull-down enable register 0	read/write byte	0000 0000
0	1	0	0	0	1	1	1	Pull-up/pull-down enable register 1	read/write byte	0000 0000
0	1	0	0	1	0	0	0	Pull-up/pull-down selection register 0	read/write byte	1111 1111
0	1	0	0	1	0	0	1	Pull-up/pull-down selection register 1	read/write byte	1111 1111
0	1	0	0	1	0	1	0	Interrupt mask register 0	read/write byte	1111 1111
0	1	0	0	1	0	1	1	Interrupt mask register 1	read/write byte	1111 1111
0	1	0	0	1	1	0	0	Interrupt status register 0	read byte	0000 0000
0	1	0	0	1	1	0	1	Interrupt status register 1	read byte	0000 0000
0	1	0	0	1	1	1	1	Output port configuration register	read/write byte	0000 0000

c. Register Description

i. Input Port Register Pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level.

Table 4: Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Name	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 5: Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Name	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

ii. Output Port Register Pair (02h, 03h)

The Output port registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Table 6: Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Name	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 7: Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Name	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

iii. Polarity Inversion Register Pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained

Table 8: Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Name	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 9: Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Name	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

iv. Configuration Register Pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Table 10: Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Name	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 11: Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Name	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

v. Output Drive Strength Register Pairs (40h, 41h, 42h, 43h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41 CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41 CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25, 01b = 0.5, 10b = 0.75 or 11b = 1 of the drive capability of the I/O. See Section 9.2 “Output drive strength control” for more details.

Table 12: Current control port 0 register (address 40h)

Bit	7	6	5	4	3	2	1	0
Name	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 13: Current control port 0 register (address 41h)

Bit	7	6	5	4	3	2	1	0
Name	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 14: Current control port 1 register (address 42h)

Bit	7	6	5	4	3	2	1	0
Name	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 15: Current control port 1 register (address 43h)

Bit	7	6	5	4	3	2	1	0
Name	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

vi. Input Latch Register Pair (44h, 45h)

The input latch registers (registers 44 and 45) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level.

Table 16: Input latch port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Name	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 17: Input latch port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Name	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

vii. Pull-up/Pull-down Enable Register Pair (46h, 47h)

These registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs. Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor.

Table 18: Pull-up/pull-down enable port 0 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Name	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 19: Pull-up/pull-down enable port 1 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Name	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

viii. Pull-up/pull-down Selection Register Pair (48h, 49h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 k pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 k pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 k with minimum of 50 k and maximum of 150 k.

Table 20: Pull-up/pull-down selection port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Name	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 21: Pull-up/pull-down selection port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Name	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

ix. Interrupt Mask Register Pair (4Ah, 4Bh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted. When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted.

Table 22: Interrupt mask port 0 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Name	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 23: Interrupt mask port 1 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Name	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

x. Interrupt Status Register Pair (4Ch, 4Dh)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0.

Table 24: Interrupt status port 0 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Name	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 25: Interrupt status port 1 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Name	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

xi. Output Port Configuration Register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull. A logic 1 configures the I/O as open-drain and the recommended command sequence is to program this register (4Fh) before the configuration register (06h and 07h) sets the port pins as outputs. ODEN0 configures Port 0_x and ODEN1 configures Port 1_x.

Table 25: Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Name	Reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

d. I/O Port

When an I/O is configured as an input, the pull-up FET and pull-down FET are off, which creates a high-impedance input. If the I/O is configured as an output, there are low impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS} depending on the state of the Output Port Register. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. Pull-up/down FETs series with resistors are enabled accordingly to the Pull-up or Pull-down Select Register and the Pull-up or Pull-down Enable Register. When the GPIO-port is set as an output, the input buffers are disabled such that the bus is allowed to float.

e. Power-on Reset

When power is applied to $V_{DD(P)}$, an internal power-on reset holds the PI4IOE5V6416 in a reset condition until $V_{DD(P)}$ has reached V_{POR} . At that point, the reset condition is released and the PI4IOE5V6416 registers will initialize to their default states.

f. Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PI4IOE5V6416 registers are changed to their default state once $\overline{\text{RESET}}$ is low (0). Only when $\overline{\text{RESET}}$ is high (1), GPIO registers can be accessed by the I^2C pin. This input requires a pull-up resistor to $V_{DD(I2C\_bus)}$, if no active connection is used.

g. Interrupt Output ($\overline{INT}$)

The $\overline{INT}$ pin is a LOW-asserted open-drain output and requires an external pull-up resistor. The PI4IOE5V6416 signals an interrupt to the processor when an event occurs, removing the need for the processor to continuously poll the PI4IOE5V6416 registers.

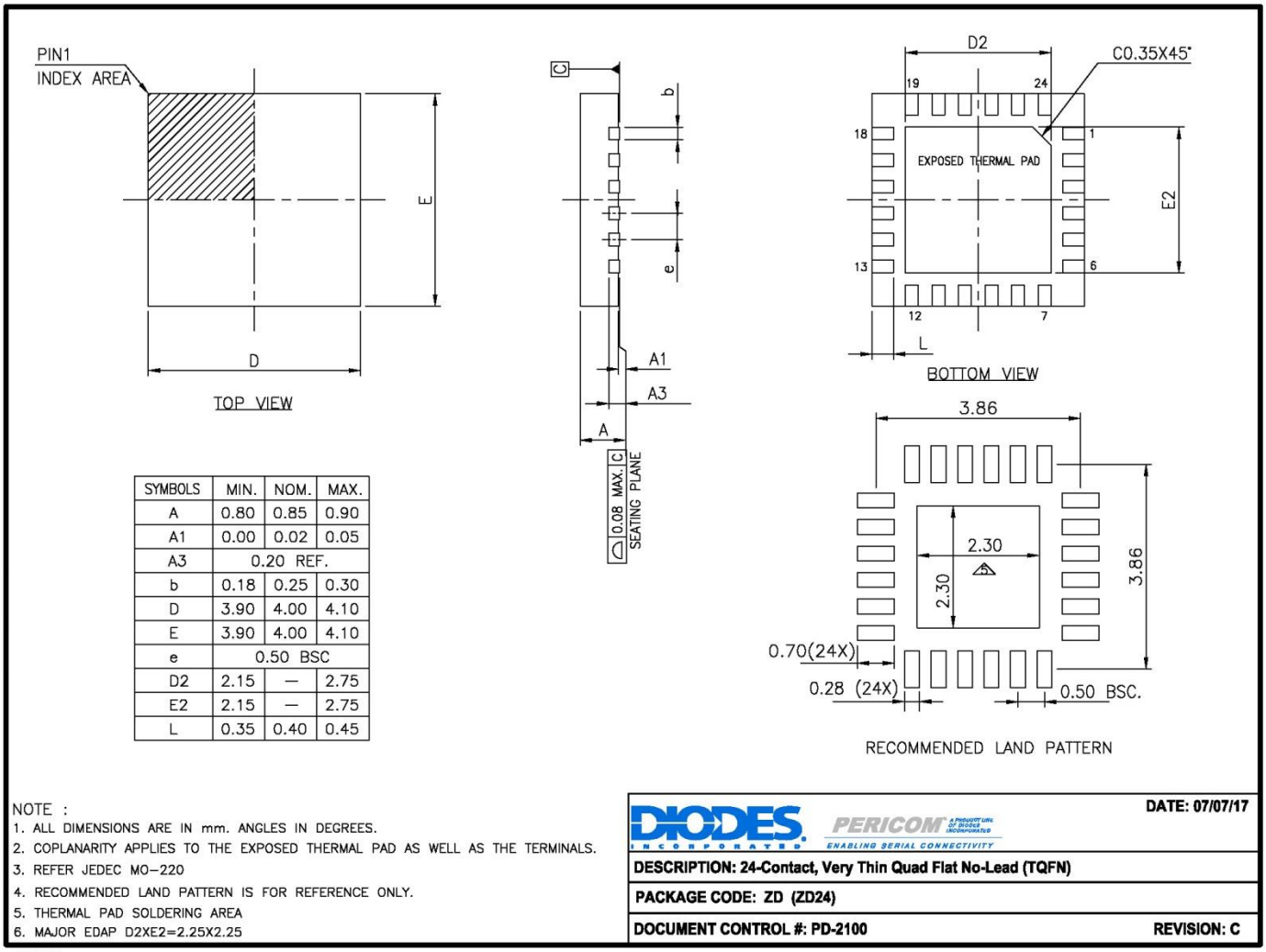
An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical

24-TQFN (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.50 BSC	
D2	2.15	—	2.75
E2	2.15	—	2.75
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA
6. MAJOR EDAP D2XE2=2.25X2.25

DATE: 07/07/17

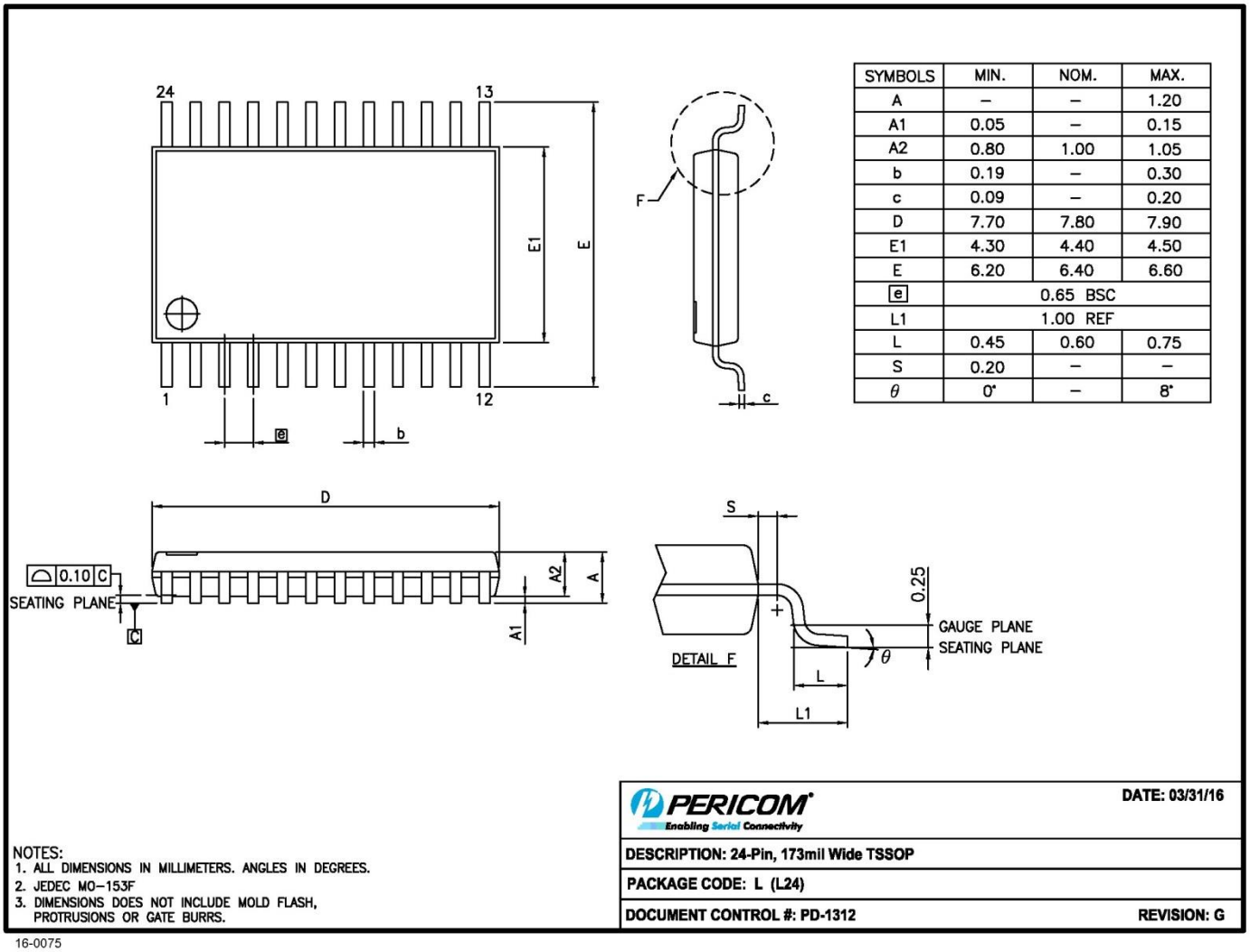
DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD24)

DOCUMENT CONTROL #: PD-2100 REVISION: C

17-0533

24-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity — DATE: 03/31/16

DESCRIPTION: 24-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L24)

DOCUMENT CONTROL #: PD-1312 — REVISION: G

16-0075

For latest package info.
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Ordering Information

Part No.	Package Code	Package
PI4IOE5V6416ZDEX	ZD	24-Contact, Very Thin Quad Flat No-Lead (TQFN)
PI4IOE5V6416LEX	L	24-Pin, 173mil Wide (TSSOP)

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