



**THE DATASHEET OF
74FCT38075SCMGI**



Description

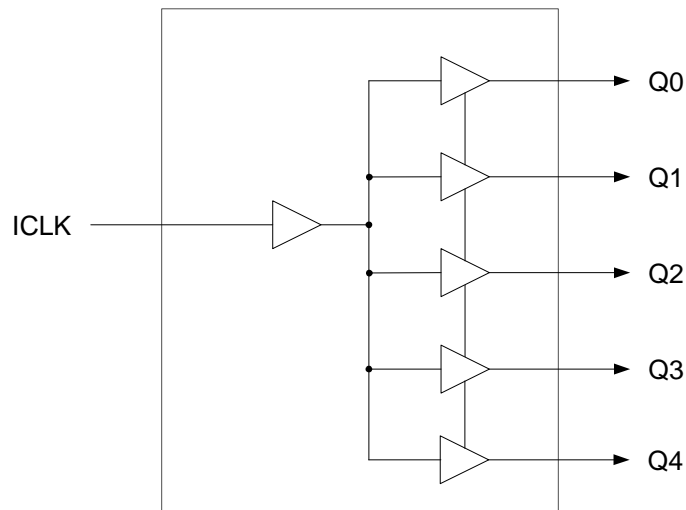
The 74FCT38075S is a low skew, single input to five output, clock buffer. The 74FCT38075S has best in class additive phase Jitter of sub 50 fsec.

IDT makes many non-PLL and PLL based low output skew devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

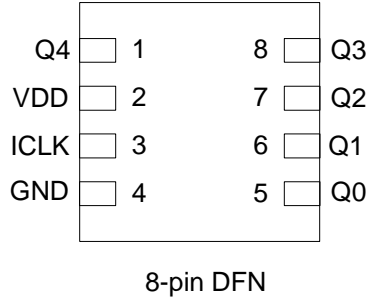
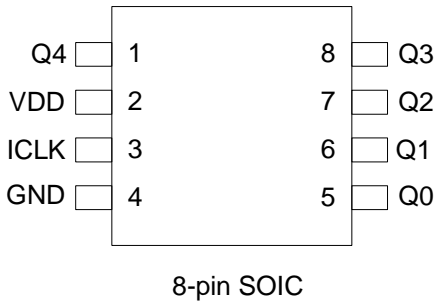
Features

- Extremely low RMS Additive Phase Jitter: 50fs
- Low output skew: 50ps
- Packaged in 8-pin SOIC and 8-pin DFN
- Pb (lead) free package
- Low power CMOS technology
- Operating voltages of 1.8V to 3.3V
- Extended temperature range (-40°C to +105°C)

Block Diagram



Pin Assignments



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	Q4	Output	Clock Output 4.
2	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
3	ICLK	Input	Clock input.
4	GND	Power	Connect to ground.
5	Q0	Output	Clock output 0.
6	Q1	Output	Clock output 1.
7	Q2	Output	Clock Output 2.
8	Q3	Output	Clock Output 3.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 2 and GND on pin 4, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 74FCT38075S is capable of, careful attention must be paid to board layout. Essentially, all five outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 74FCT38075S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Outputs	-0.5 V to VDD+0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40° to +105°C
Storage Temperature	-65° to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7 x VDD		1.89	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V _{OH}	I _{OH} = -10 mA	1.3			V
Output Low Voltage	V _{OL}	I _{OL} = 10mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		13		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7 x VDD		2.625	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V _{OH}	I _{OH} = -16 mA	1.8			V
Output Low Voltage	V _{OL}	I _{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		18		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7 x VDD		3.465	V
Input Low Voltage, ICLK	V _{IL}	Note 1			0.3 x VDD	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.2			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		22		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	ICLK		5		pF

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t _{OR}	0.36 to 1.44 V, C _L =5 pF		0.6	1.0	ns
Output Fall Time	t _{OF}	1.44 to 0.36 V, C _L =5 pF		0.6	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		135MHz, Note 1	1.5	3	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t _{OR}	0.5 to 2.0 V, C _L =5 pF		0.6	1.0	ns
Output Fall Time	t _{OF}	2.0 to 0.5 V, C _L =5 pF		0.6	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		135MHz, Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

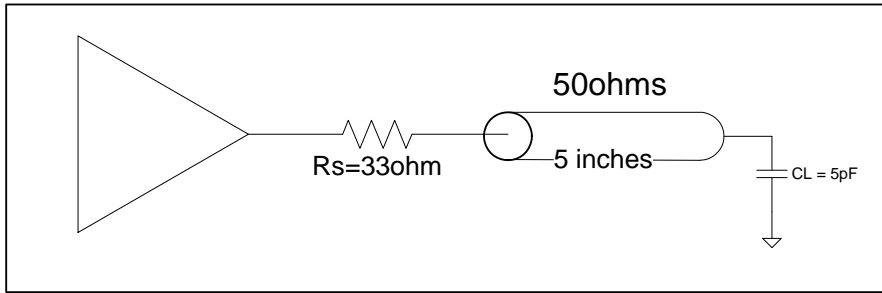
VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t _{OR}	0.66 to 2.64 V, C _L =5 pF		0.6	1.0	ns
Output Fall Time	t _{OF}	2.64 to 0.66 V, C _L =5 pF		0.6	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Propagation Delay		135MHz, Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

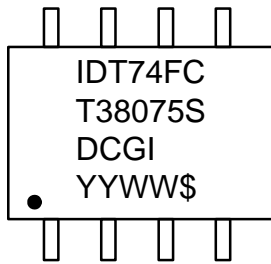
Test Load and Circuit



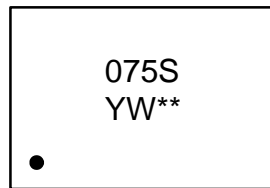
Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	1 m/s air flow		140		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	3 m/s air flow		120		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	θ_{JC}			40		$^{\circ}\text{C}/\text{W}$

Marking Diagrams



8-pin SOIC

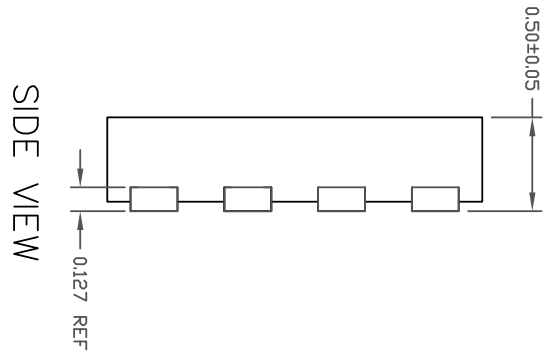
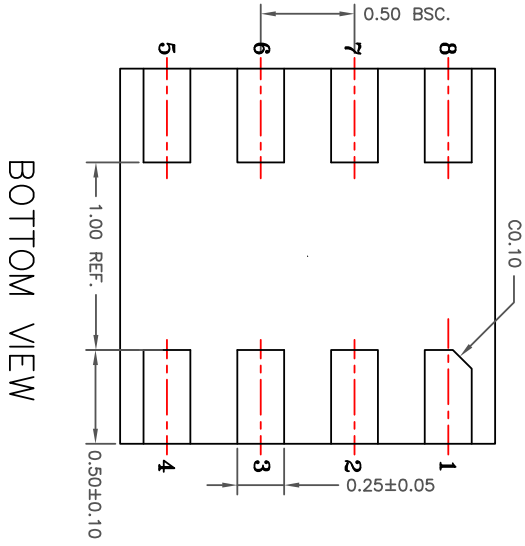
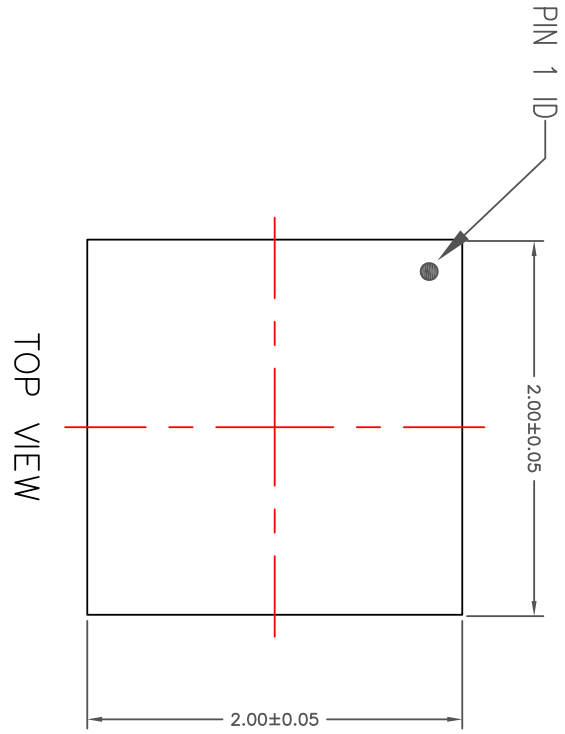


8-pin DFN

Notes:

1. “**” is the lot number.
2. “YYWW” or “YW” are the last digits of the year and week that the part was assembled.
3. “G” denotes RoHS compliant package.
4. “\$” denotes mark code.
5. “I” denotes extended temperature range device.

Package Outline and Package Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)

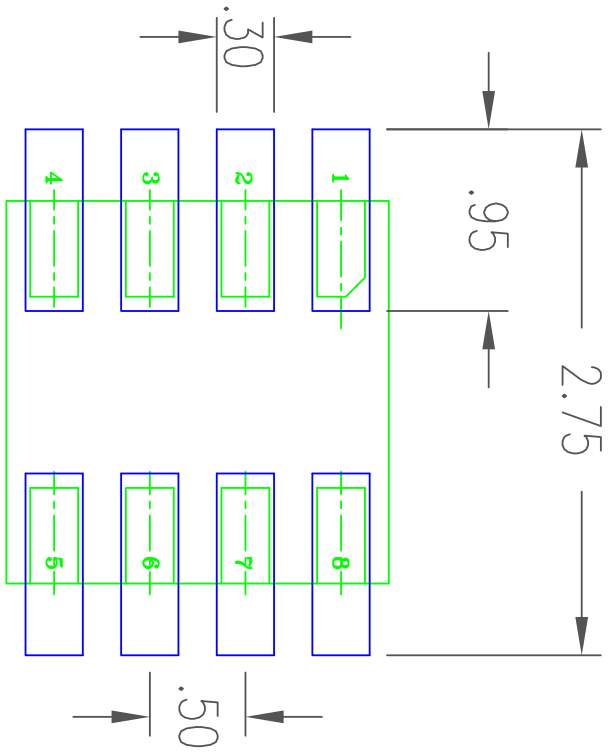


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	JHUA

- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
 2. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED		 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674
DECIMAL	ANGULAR	
XXX	±	www.idt.com
XXXX		
XXXXX		
APPROVALS	DATE	TITLE
DRAWN: <i>dad</i>	09/10/14	CM08 PACKAGE OUTLINE
CHECKED: <i>zda</i>	09/10/14	2.0 X 2.0 mm BODY
		0.5mm PITCH VFOFN
SIZE	DRAWING No.	REV
C	PSC-4490	00
DO NOT SCALE DRAWING		SHEET 1 OF 2

Package Outline and Package Dimensions, cont. (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



RECOMMENDED LAND PATTERN DIMENSION

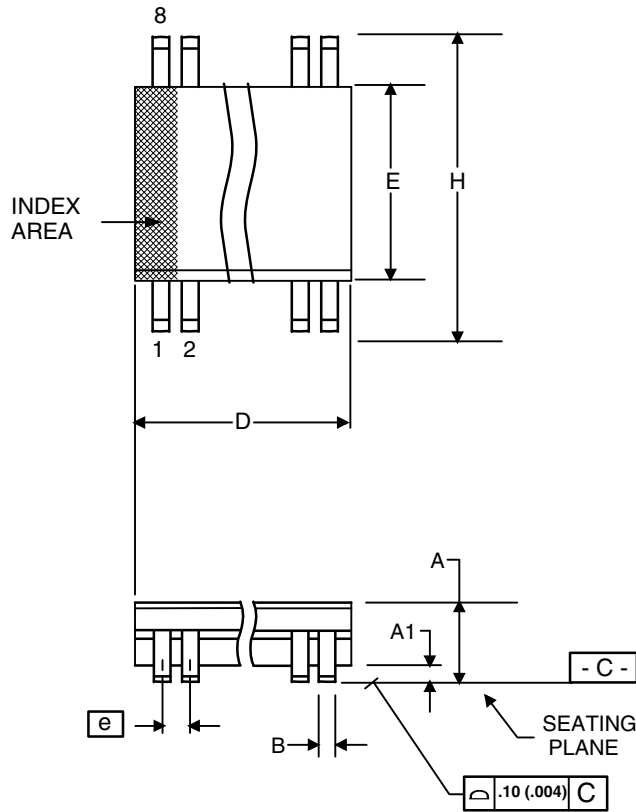
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

REVISIONS		
REV	DESCRIPTION	DATE
00	INITIAL RELEASE	09/18/14

TOLERANCES UNLESS SPECIFIED		8024 SILVER CREEK SAN JOSE, CA 95131 PHONE: (408) 284-1100 FAX: (408) 492-8671	
DECIMAL	ANGULAR	DATE	TITLE
XXX±	±	09/19/14	CMG8 PACKAGE OUTLINE
XXXX			2.0 X 2.0 mm BODY
XXXXE			0.5 mm PITCH VFOFN
APPROVALS	DATE	SIZE	DRAWING No.
DRAWN	09/19/14	C	PSC-4490
CHECKED			
DO NOT SCALE DRAWING			

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)



Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
a	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
74FCT38075SDCGI	see page 6	Tubes	8-pin SOIC	-40° to +105°C
74FCT38075SDCGI8		Tape and Reel	8-pin SOIC	-40° to +105°C
74FCT38075SCMGI		Cut Tape	8-pin DFN	-40° to +105°C
74FCT38075SCMGI8		Tape and Reel	8-pin DFN	-40° to +105°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/18/15	B. Chandhoke	Initial release.

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