THE DATASHEET OF

ADIN2111CCPZ

www.win-source.net 0086-755-83957316

Data Sheet

ADIN2111

Low Complexity, 2-Port Ethernet Switch with Integrated 10BASE-T1L PHYs

FEATURES

- 10BASE-T1L IEEE Standard 802.3cg-2019 compliant
- Cable reach up to 1700 m
- Integrated switch with SPI
  - Supports OPEN Alliance 10BASE-T1x MACPHY SPI
  - Frame forwarding rules between ports and host
  - 16 MAC address filters
  - High and low priority queues with 28 kB buffer
  - Cut through or store and forward operation
  - IEEE 1588 timestamp support
  - Statistic counters
- Low power consumption: 77 mW (dual supply, 1.0 V p-p)
- Supports 1.0 V p-p and 2.4 V p-p transmit levels
- 2-pin MDI (receive, transmit)
- Internal termination resistors
- Autonegotiation capability
- Diagnostics
  - Cable fault detection with TDR
  - Link quality indicator with MSE
  - Link diagnostics and IEEE test modes
- 25 MHz crystal or external clock input
- Single or dual supply with 1.8 V or 3.3 V operation
- Electromagnetic compatibility (EMC) test standards
  - IEC 61000-4-4 electrical fast transient (±4 kV)
  - IEC 61000-4-2 ESD (±4 kV contact discharge)
  - IEC 61000-4-2 ESD (±8 kV air discharge)
  - IEC 61000-4-6 conducted immunity (10 V/m)
  - IEC 61000-4-5 surge (±4 kV)
  - IEC 61000-4-3 radiated immunity (Class A)
  - EN55032 radiated emissions (Class B)
- Small package: 48-lead, 7 mm × 7 mm LFCSP
- Temperature range
  - Industrial: −40°C to +85°C
  - Extended: −40°C to +105°C

APPLICATIONS

- Building automation and fire safety
- Factory automation
- Condition monitoring and machine connectivity

FUNCTIONAL BLOCK DIAGRAM

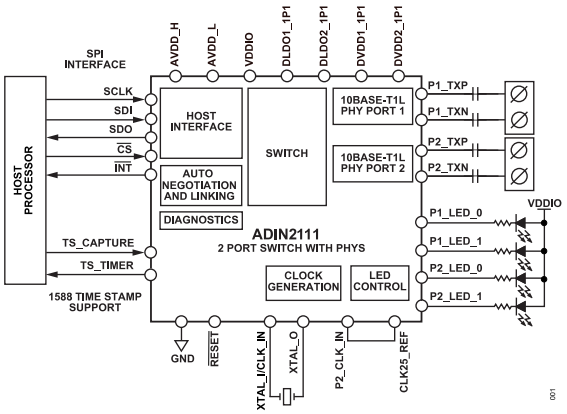

Figure 1.

GENERAL DESCRIPTION

The ADIN2111 is a low power, 2-port 10BASE-T1L transceiver designed for industrial Ethernet applications, and is compliant with the IEEE® 802.3cg-2019™ Ethernet standard for long reach, 10 Mbps single pair Ethernet (SPE). Featuring an integrated media access control (MAC) and a switch, the ADIN2111 enables direct connectivity with a variety of controllers via a serial peripheral interface (SPI). The switch (cut through or store and forward) supports various routing configurations between the two Ethernet ports and the SPI host port providing a flexible solution for line, daisy-chain, or ring network topologies.

The ADIN2111 can be used in unmanaged configurations where the device automatically forwards the traffic between the two Ethernet ports.

The device integrates the switch, two Ethernet physical layer (PHY) cores with a MAC interface and all the associated analog circuitry, and input and output clock buffering. The device also includes internal buffer queues, the SPI and subsystem registers, as well as the control logic to manage the reset and clock control and hardware pin configuration.

The ADIN2111 has an integrated voltage supply monitoring circuit and power-on reset (POR) circuitry to improve system level robustness. The 4-wire SPI for communication with the host can be configured to OPEN Alliance SPI or generic SPI. Both modes support optional data protection or cyclic redundancy check (CRC).

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. A

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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2/2023—Rev. 0 to Rev. A

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Added Analog Inputs and Outputs, MDI Gain Offset Parameter, Table 2 ... 5
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12/2021—Revision 0: Initial Version

SPECIFICATIONS

AVDD_H = AVDD_L = VDDIO = 3.3 V, DVDD_1P1 from internal low dropout (LDO) regulator (DVDD_1P1 = DLDO_1P1), and all specifications at −40°C to +105°C, unless otherwise noted.

Table 1. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS/OUTPUTS					Applies to the SPI pins, $\overline{INT}$, $\overline{RESET}$, and Px_LED_0 and Px_LED_1 pins
VDDIO = 3.3 V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (minimum) = 2 mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (minimum) = 2 mA
VDDIO = 2.5 V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (minimum) = 2 mA
V_{OH}	2.0			V	I_{OH} (minimum) = 2 mA
VDDIO = 1.8 V					
V_{IL}			0.3 × VDDIO	V	
V_{IH}	0.7 × VDDIO			V	
V_{OL}			0.2 × VDDIO	V	I_{OL} (minimum) = 2 mA
V_{OH}	0.8 × VDDIO			V	I_{OH} (minimum) = 2 mA
$\overline{RESET}$ Deglitch Time	0.3	0.5	1	µs	
LED OUTPUT					
Output Drive Current			8	mA	VDDIO = 3.3 V
			6	mA	VDDIO = 2.5 V
			4	mA	VDDIO = 1.8 V
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I/CLK_IN pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−30		+30	ppm	
Crystal Drive Level		<200		µW	
Crystal Equivalent Series Resistance (ESR)			60	Ω	
XTAL_I, XTAL_O Input Capacitance ($C_{IN,EQ}$)		1.5		pF	Equivalent parallel differential input capacitance looking into XTAL_I/CLK_IN pin and XTAL_O pin
Crystal Load Capacitance (C_L)[1]		10	18	pF	Including PCB trace capacitance and XTAL_I, XTAL_O $C_{IN,EQ}$
Start-Up Time			2	ms	Crystal oscillator only
Clock Input (CLK_IN)					
Clock Input Frequency		25		MHz	Requirements for external clock applied to XTAL_I pin
Clock Input Voltage Range	0.8		2.5	V p-p	
Clock Input Duty Cycle	45		55	%	Input clock duty cycle 50%
XTAL_I Input Impedance ($Z_{IN,EQ}$)					
Driving Point Resistance (R_P)[2]		6		kΩ	R_P||C_P
Driving Point Capacitance (C_P)[2]		3		pF	
Jitter Tolerance (RMS)			40	ps	
CLK25_REF Clock Output					
CLK25_REF Frequency		25		MHz	
V_{OH}		1.05		V	Load = 10 pF
V_{OL}		0		V	Load = 10 pF
CLK25_REF Duty Cycle	45		55	%	Load = 10 pF

SPECIFICATIONS

Table 1. General Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK25_REF Frequency Tolerance	−50		+50	ppm	
Long-Term Jitter (RMS)			40	ps	

[1] Load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

[2] R_P and C_P are the values of the equivalent parallel RC circuit to ac ground ($R_P||C_P$), modeling the driving point impedance of the XTAL_I/CLK_IN pin.

Table 2. 10BASE-T1L Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltage Range					
AVDD_H	3.13	3.3	3.46	V	2.4 V p-p or 1.0 V p-p transmit level
AVDD_L	1.71	1.8 or 3.3	3.46	V	
DVDD1_1P1, DVDD2_1P1	1.0	1.1	1.2	V	
VDDIO	1.71	1.8, 2.5, or 3.3	3.46	V	
1.0 V p-p Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = DLDO_1P1
AVDD_H/AVDD_L/VDDIO Supply Current (I_{AVDD_H}/ I_{AVDD_L}/I_{VDDIO})		50		mA	Measured current ($I_{measured}$) = I_{AVDD_H} + I_{AVDD_L} + I_{VDDIO}
Power Consumption		90		mW	100% data throughput, full activity
		22		mW	Software power-down mode
1.0 V p-p Transmit Level (Dual Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = external 1.1 V
AVDD_H/AVDD_L/VDDIO Supply Current		30		mA	$I_{measured}$ = I_{AVDD_H} + I_{AVDD_L} + I_{VDDIO}
DVDD Supply Current (I_{DVDD})		20		mA	Supply for DVDD1_1P1 and DVDD2_1P1 pins, $I_{measured}$ = I_{DVDD}
Power Consumption		77		mW	100% data throughput, full activity
2.4 V p-p Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 3.3 V, DVDD_1P1 = DLDO_1P1
AVDD_H/AVDD_L/VDDIO Supply Current		65		mA	$I_{measured}$ = I_{AVDD_H} + I_{AVDD_L} + I_{VDDIO}
Power Consumption		215		mW	100% data throughput, full activity
		44		mW	Software power-down mode
2.4 V p-p Transmit Level (Dual Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = DLDO_1P1
AVDD_H Supply Current		32.5		mA	$I_{measured}$ = I_{AVDD_H}
AVDD_L/VDDIO Supply Current		30		mA	$I_{measured}$= I_{AVDD_L} + I_{VDDIO}
Power Consumption		162		mW	100% data throughput, full activity
		22		mW	Software power-down mode
2.4 V p-p Transmit Level (Triple Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = external 1.1 V
AVDD_H Supply Current		33		mA	$I_{measured}$ = I_{AVDD_H}
AVDD_L/VDDIO Supply Current		10		mA	$I_{measured}$ = I_{AVDD_L} + I_{VDDIO}
DVDD Supply Current		20		mA	External supply for DVDD1_1P1 and DVDD2_1P1 pins, $I_{measured}$ = I_{DVDD}
Power Consumption		149		mW	100% data throughput, full activity
ANALOG INPUTS AND OUTPUTS					
MDI Gain Offset	−7.5		+3.5	%	
TIMING/LATENCY					
Port to Port Latency					
PHY Rx		6.4		µs	PHY 1 or PHY 2 Rx latency
Switch		12.6		µs	
PHY Tx		3.2		µs	PHY 1 or PHY 2 Tx latency
Total Latency		22.2		µs	
System/PHY 1 Reset to Standby Delay			50	ms	Delay after $\overline{\text{RESET}}$ pin released; internal MAC registers and Port 1 PHY registers accessible

SPECIFICATIONS

Table 2. 10BASE-T1L Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHY 2 Reset to Standby Delay			90	ms	Delay after $\overline{\text{RESET}}$ pin released and Port 2 PHY registers accessible

TIMING CHARACTERISTICS

POWER-UP TIMING

Table 3. Power-Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t_1	Minimum time interval to internal power good[1]	20		43	ms
t_2	Hardware configuration latch time	6	8	14	µs
t_3	Management interface (SPI) active			50	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

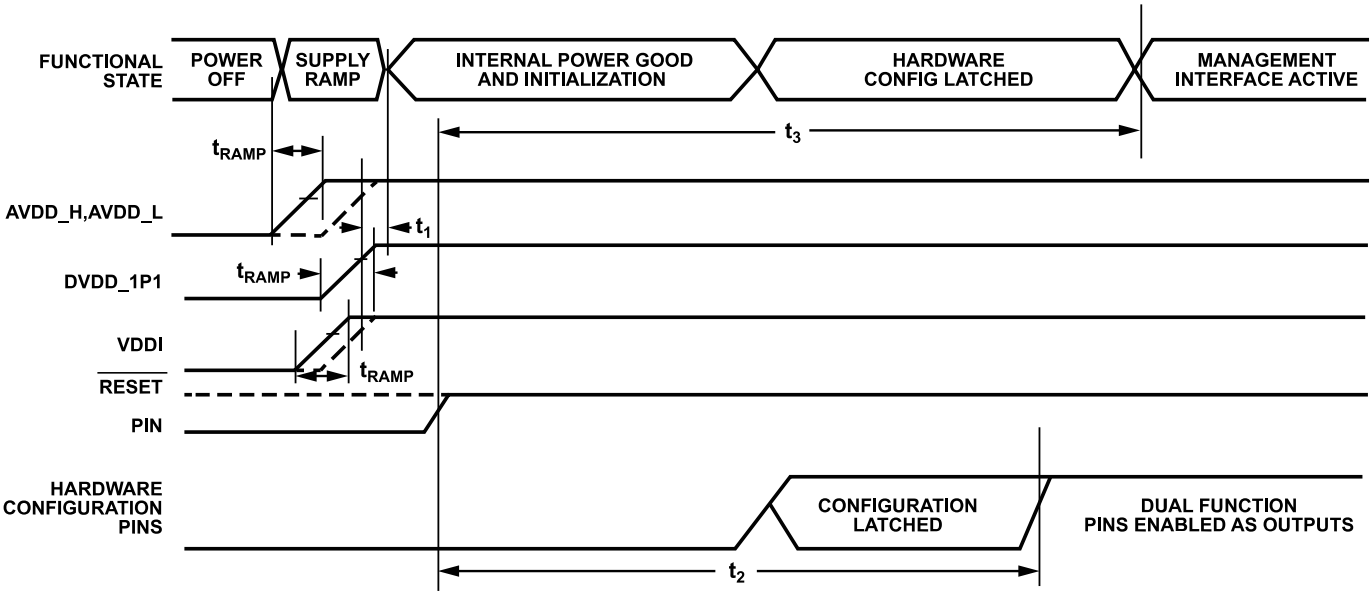


Figure 2. Power-Up Timing

SPI

Table 4.

Parameter[1, 2]	Description	Min	Typ	Max	Unit
t_1	SCLK cycle time	40			ns
t_2	SCLK high time	17			ns
t_3	SCLK low time	17			ns
t_4	$\overline{CS}$ falling edge to SCLK rising edge setup time	17			ns
t_5	Last SCLK rising edge to $\overline{CS}$ rising edge	17			ns
t_6	$\overline{CS}$ high time	40			ns
t_7	Data setup time	5			ns
t_8	Data hold time	5			ns
t_9[3]	SCLK falling edge to SDO valid			12	ns
t_{10}[3]	$\overline{CS}$ rising edge to SDO tristate			15	ns
t_{11}[3]	$\overline{CS}$ falling edge to SDO valid (for readback MSB only)			12	ns

[1] Guaranteed by design and characterization. Not production tested.

[2] All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of VDDIO) and timed from a voltage level of 1.2 V.

TIMING CHARACTERISTICS

[3] Capacitive load on the SDO pin is 10 pF.

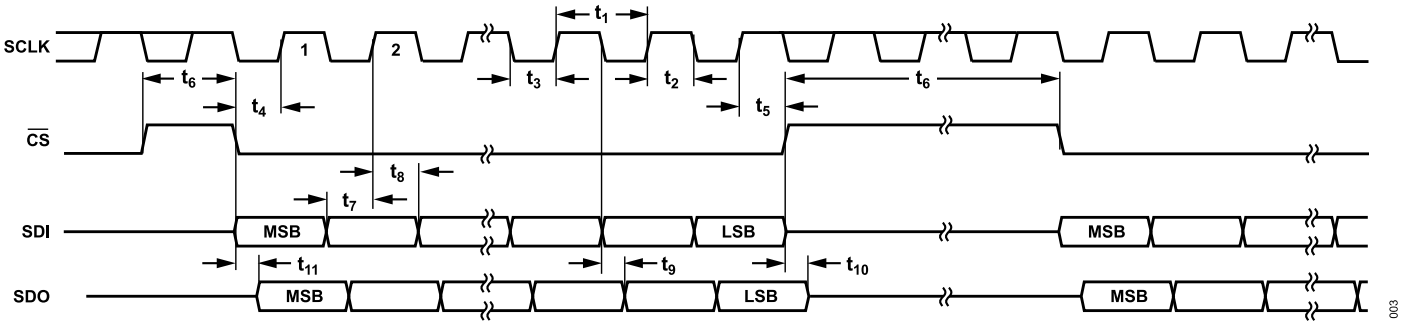


Figure 3. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDDIO to GND	−0.3 V to +4 V
DVDD1_1P1, DVDD2_1P1, DLDO1_1P1, DLDO2_1P1, to GND	−0.3 V to +1.35 V
AVDD_H, AVDD_L to GND	−0.3 V to +4 V
SPI[1], $\overline{\text{INT}}$ to GND	−0.3 V to VDDIO + 0.3 V
P1_TXN, P1_TXP, P2_TXN, P2_TXP to GND	−0.3 V to AVDD + 0.3 V
P1_LED_0, P2_LED_0, P1_LED_1, P2_LED_1, $\overline{\text{RESET}}$ to GND	−0.3 V to VDDIO + 0.3 V
XTAL_I/CLK_IN to GND	−0.3 V to 2.75 V
XTAL_O, CLK25_REF to GND	−0.3 V to 1.35 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +85°C
Extended	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] See the Pin Configuration and Function Descriptions section for a full list of SPI pins.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
CP-48-13[2]	45	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

[2] Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADIN2111

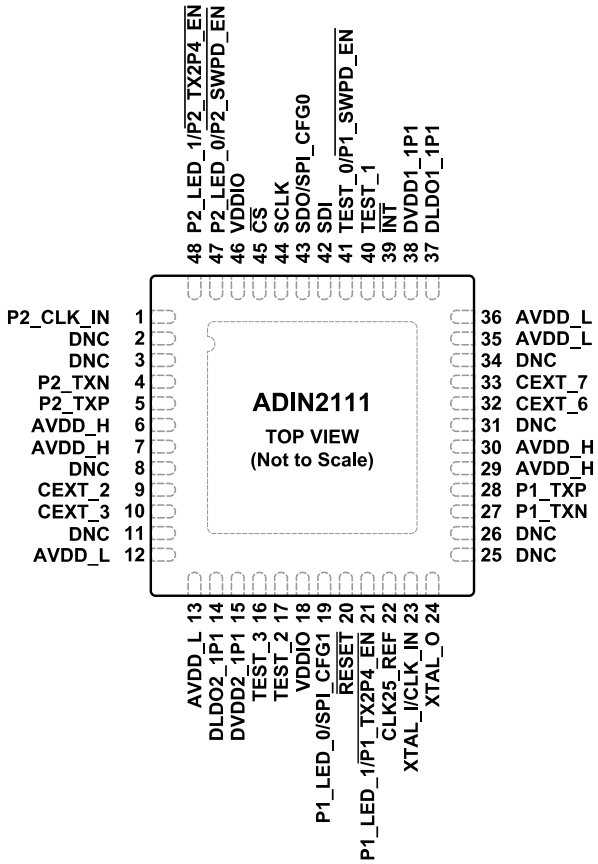
Table 7. ADIN2111, 48-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM		
P1_TXN, P1_TXP, P2_TXN, P2_TXP Pins	8000	3B
All Other Pins	2000	2
FICDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. THESE PINS MUST BE LEFT OPEN CIRCUIT.
2. EXPOSED PAD (GROUND). THE LFCSP HAS AN EXPOSED PAD THAT MUST BE CONNECTED TO GND FOR ELECTRICAL REASONS AND SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS. A 4 × 4 ARRAY OF THERMAL VIAS BENEATH THE EXPOSED GND PAD IS ALSO RECOMMENDED.

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic[1]	PU/PD[2]	Description
Clock Interface			
1	P2_CLK_IN	N/A	Single-Ended 25 MHz Reference Clock Dedicated to Port 2 PHY. This pin must be connected to an external, single-ended 25 MHz reference clock, or to the CLK25_REF pin (Pin 22), which provides a 25 MHz clock.
22	CLK25_REF	N/A	Analog Reference Clock Output. The 25 MHz reference clock from the crystal oscillator is available on the CLK25_REF pin. The 25 MHz clock output is briefly disabled (logic low) following a software reset (25 ms) or a hardware reset (70 ms). See the Reset Operations section for more details.
23	XTAL_I/CLK_IN	N/A	Main Crystal/Single-Ended 25 MHz Reference Clock Input. This pin must be connected to an external, single-ended 25 MHz reference clock. This clock source is also used by Port 1 PHY.
24	XTAL_O	N/A	Main Crystal Output. If using a single-ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open circuit. See the External 25 MHz Clock Input section.
SPI			
39	$\overline{\text{INT}}$	PU	Interrupt Pin Output. Open-drain, active low output. A low on $\overline{\text{INT}}$ indicates an unmasked management interrupt. This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
42	SDI	PD	Serial Data Input. Data is clocked in on the SDI pin on each rising edge.
43	SDO/SPI_CFG0	PD	Serial Data Output (SDO). Data is clocked out on the SDO pin on each falling edge.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic[1]	PU/PD[2]	Description
			Configure the Device to Use 8-bit CRC (generic SPI mode) or Protection Mode (OPEN Alliance Mode) on the SPI Host Interface (SPI_CFG0). Use this pin with SPI_CFG1. See Table 22 for details. The default configuration for this pin is with protection/CRC enabled. This pin is provided with an internal pull-up resistor.
44	SCLK	PD	Clock Input. Data is clocked into the shift register on each falling edge.
45	$\overline{CS}$	PD	Active Low Chip Select.
Reset			
20	$\overline{RESET}$	PU	Hardware Reset, Active Low Input. Hold low for >10 µs to reset the device. This pin can be left floating if a hardware reset is not required. See the Hardware Reset section.
Media Dependent Interface (MDI)			
4	P2_TXN	N/A	Port 2 10BASE-T1L Transmit/Receive Negative Pin.
5	P2_TXP	N/A	Port 2 10BASE-T1L Transmit/Receive Positive Pin.
27	P1_TXN	N/A	Port 1 10BASE-T1L Transmit/Receive Negative Pin.
28	P1_TXP	N/A	Port 1 10BASE-T1L Transmit/Receive Positive Pin.
Configuration/Status/Test			
16	TEST_3	PU	Test Pin 3. No function currently assigned. Do not connect.
17	TEST_2	PD	Test Pin 2. No function currently assigned. Do not connect.
19	P1_LED_0/ SPI_CFG1	PU	General-Purpose, Programmable LED Indicator 0 for Port 1 (P1_LED_0). The LED can be active high or active low. By default, P1_LED_0 is configured to turn on when a link is established and blink when there is activity. The default LED function is Tx/Rx activity. The default configuration is P1_LED_0 enabled. See the Status LEDs section. Configure the device to Use OPEN Alliance SPI Mode or Analog Devices SPI Mode (SPI_CFG1). A voltage high level on this pin enables SPI generic mode. A voltage low level on this pin enables SPI OA mode. For OPEN Alliance SPI mode, use without LED, connect an external pull-down of 4.7 kΩ or less. Use this pin with SPI_CFG0. See Table 22 for details. The default configuration is generic SPI. This pin is provided with an internal pull-up resistor.
21	P1_LED_1/$\overline{P1_TX2P4_EN}$	PD	General-Purpose, Programmable LED Indicator 1 for Port 1 (P1_LED_1). The LED can be active high or active low. The default condition is P1_LED_1 disabled. See the Status LEDs section. Port 1 Transmit Level Amplitude Hardware Configuration Pin Signal ($\overline{P1_TX2P4_EN}$). Set high for 1.0 V p-p transmit amplitude only. Set low to support both 1.0 V p-p and 2.4 V p-p transmit amplitude. See Table 19. This pin is provided with an internal pull-down resistor.
40	TEST_1	PU	Test Pin 1. This pin can be assigned to the TS_CAPT alternative function using the DIGIO_TSCAPT_PINMUX bit in the Pin Mux Configuration 1 register. Do not connect if unused.
41	TEST_0/$\overline{P1_SWPD_EN}$	PD	Test Pin 0 (TEST_0). No function currently assigned. Disable Port 1 PHY Software Power-Down After Power-Up/Reset ($\overline{P1_SWPD_EN}$). When software power-down (SWPD) is enabled, a reset or power cycle puts the chip in active mode and attempts to link up and switch forward all frames. The default configuration is SWPD enabled. To disable SWPD, connect a 4.7 kΩ or less external pull-up resistor to VDDIO. This pin is provided with an internal pull-down resistor.
47	P2_LED_0/$\overline{P2_SWPD_EN}$	PU	General-Purpose, Programmable LED Indicator 0 for Port 2 (P2_LED_0). The LED can be active high or active low. By default, P2_LED_0 is configured to turn on when a link is established and blink when there is activity. The default LED function is Tx/Rx activity. The default configuration is P2_LED_0 enabled. See the Status LEDs section. Disable Port 2 PHY Software Power-Down After Power-Up/Reset ($\overline{P2_SWPD_EN}$). When SWPD is enabled, a reset or power cycle puts the chip in active mode and attempts to link up and switch forward all frames. The default configuration is SWPD disabled. To disable SWPD, pull the pin high or leave the pin floating. This pin is provided with an internal pull-up resistor.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic[1]	PU/PD[2]	Description
48	P2_LED_1/$\overline{\text{P2_TX2P4_EN}}$	PD	General-Purpose, Programmable LED Indicator 1 for Port 2 (P2_LED_1). The LED can be active high or active low. The default configuration is P2_LED_1 disabled. See the Status LEDs section. Port 2 Transmit Level Amplitude Hardware Configuration Pin Signal ($\overline{\text{P2_TX2P4_EN}}$). Set high for 1.0 V p-p transmit amplitude only. Set low to support both 1.0 V p-p and 2.4 V p-p transmit amplitude. See Table 20. The default configuration is 1.0 V p-p and 2.4 V. This pin is provided with an internal pull-down resistor.
LDO and Reference Decoupling			
9	CEXT_2	N/A	Port 2 PHY External Decoupling for Band Gap Voltage Reference. Connect a 0.1 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
10	CEXT_3	N/A	Port 2 PHY External Decoupling for LDO Circuit. Connect a 1 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
32	CEXT_6	N/A	Port 1 PHY External Decoupling for Band Gap Voltage Reference. Connect a 0.1 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
33	CEXT_7	N/A	Port 1 PHY External Decoupling for LDO Circuit. Connect a 1.0 µF capacitor to ground as close as possible to this pin. Do not use this pin as a voltage source for an external circuit.
Power and Ground Pins			
6, 7, 29, 30	AVDD_H	N/A	Main Analog Supply Voltage for the Various Analog Circuits in the Device. This supply rail can be supplied by 1.8 V to 3.3 V depending on the transmit level configuration. If AVDD_H is 3.3 V, both the 1.0 V p-p and 2.4 V p-p transmit operating modes are supported. If AVDD_H is 1.8 V, only the 1.0 V p-p transmit operating mode is supported. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
12, 13, 35, 36	AVDD_L	N/A	Main Analog Supply Voltage for the Internal LDO Circuits. This supply rail can be supplied by 1.8 V to 3.3 V. AVDD_L can be connected directly to the AVDD_H rail in long reach applications or alternatively to the VDDIO rail when the device is configured with dual supplies for lower power consumption. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
18, 46	VDDIO	N/A	3.3 V, 2.5 V, or 1.8 V Digital Power for the SPI Host Interface. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to the pin.
14	DLDO2_1P1	N/A	Output from the Internal 1.1 V LDO Circuit 2. When using the internal LDO, connect this pin directly to the DVDD_1P1 pin. Connect a 0.68 µF capacitor to ground as close as possible to this pin.
15	DVDD2_1P1	N/A	Input for PHY 1.1 V DVDD Supply Rail 2. When using the internal LDO regulator, connect this pin directly to the DLDO2_1P1 pin. Alternatively, an external 1.1 V rail can be provided to the DVDD_1P1 pin for greater power efficiency. Connect a 0.1 µF to ground as close as possible to this pin.
37	DLDO1_1P1	N/A	Output from the 1.1 V LDO Circuit 1. When using the internal LDO, connect this pin directly to the DVDD_1P1 pin 38. Connect a 0.68 µF capacitor to ground as close as possible to this pin.
38	DVDD1_1P1	N/A	Input for PHY 1.1 V DVDD Supply Rail 1. When using the internal LDO regulator, connect this pin directly to the DLDO1_1P1 pin. Alternatively, an external 1.1 V rail can be provided to the DVDD_1P1 pin for greater power efficiency. Connect a 0.1 µF to ground as close as possible to this pin.
	EP (GND)	N/A	Exposed Pad (Ground). The LFCSP has an exposed pad that must be connected to GND for electrical reasons and soldered to a metal plate on the PCB for mechanical reasons. A 4 × 4 array of thermal vias beneath the exposed GND pad is also recommended.
Other Pins			
2, 3, 8, 11, 25, 26, 31, 34	DNC	N/A	Do Not Connect. These pins must be left open circuit.

[1] Where a pin is shared between a functional signal and a hardware configuration pin signal, the hardware configuration pin signal is listed last.

[2] PU is pull-up, and PD is pull-down. The internal pull-up or pull-down resistor is predefined and nonconfigurable. N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

All tests were performed using a 1000 m 10BASE-T1L cable between Port 1 and Port 2 and DVDD rails powered from the internal LDO regulators. Figure 5 only shows measurements for the 1.0 V p-p transmit level because AVDD_H = 3.3 V is required for the 2.4 V p-p transmit level.

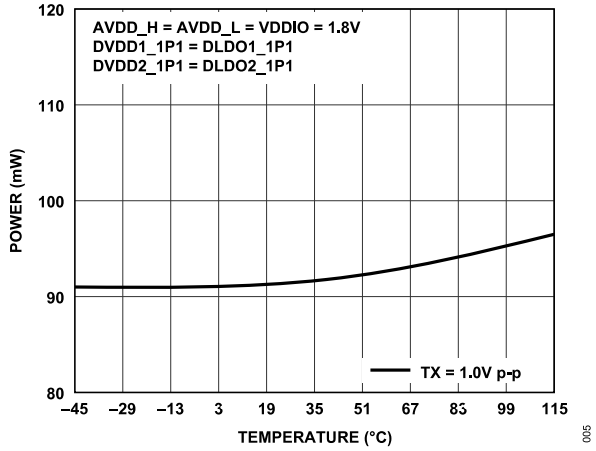


Figure 5. Power vs. Temperature, Single Supply Configuration, AVDD_H = AVDD_L = VDDIO = 1.8 V

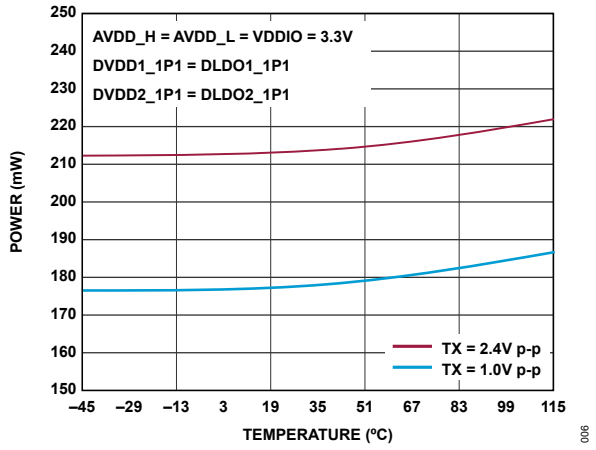


Figure 6. Power vs. Temperature, Single Supply Configuration, AVDD_H = AVDD_L = VDDIO = 3.3 V

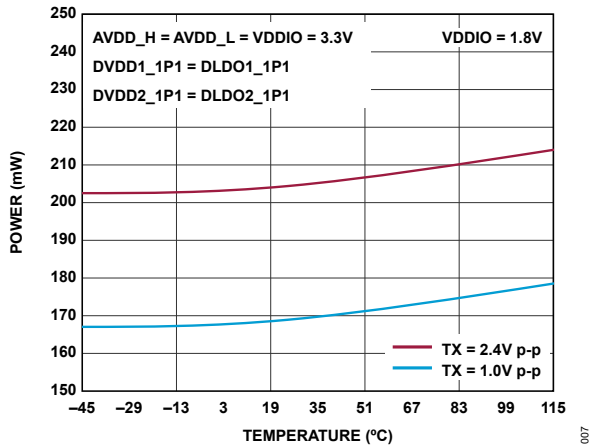


Figure 7. Power vs. Temperature, Dual Supplies Configuration, AVDD_H = AVDD_L = 3.3 V, VDDIO = 1.8 V

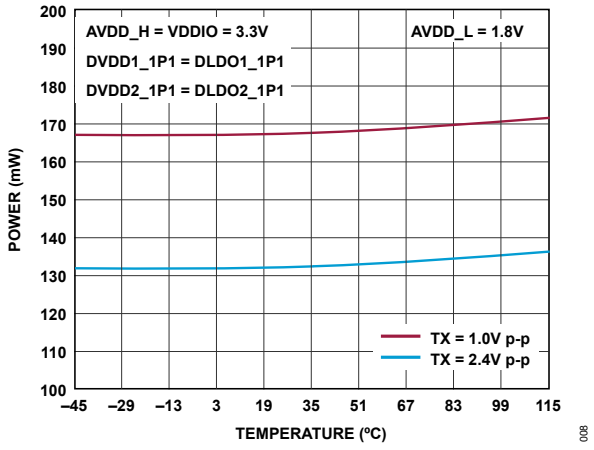


Figure 8. Power vs. Temperature, Dual Supplies Configuration, AVDD_H = VDDIO = 3.3 V, AVDD_L = 1.8 V

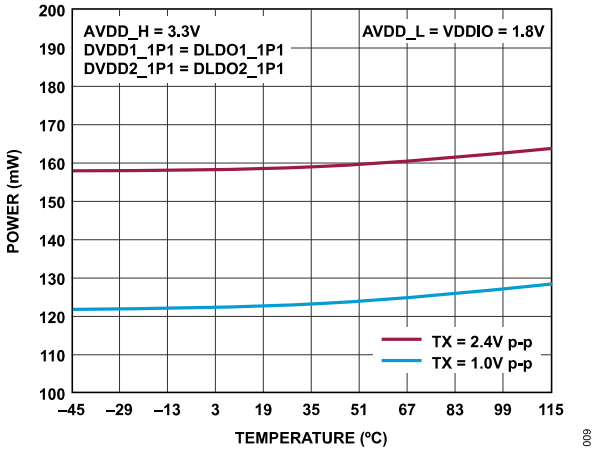


Figure 9. Power vs. Temperature, Dual Supplies Configuration, AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V

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OVERVIEW

The ADIN2111 is a low power, low complexity Ethernet switch (LES) with a dual port 10BASE-T1L transceiver designed for Ethernet applications. The chip is available on a 7 mm × 7 mm, 48-lead lead frame chip scale package (LFCSP) and includes the following features:

- Two Ethernet PHY cores with common analog circuitry
- 10 Mbps full duplex SPI for frame transfer and system register control
- MAC with support for 16 MAC addresses
- Switch with cut through or store and forward operation
- SPI to MDIO bridge to access the PHY registers
- Input and output clock buffering
- On-chip first in, first outs (FIFOs):
  - 8 kB high priority reception FIFO for the SPI host port
  - 8 kB low priority reception FIFO for the SPI host port
  - 8 kB transmission FIFO for the two Ethernet ports
  - 4 kB transmission FIFO for the SPI host
- Hardware configuration pins
- Configurable hardware interrupt pin
- Four configurable LED pins for activity monitoring

Note that two different SPI protocols are supported to communicate with the switch: a generic SPI protocol similar to protocols used in other Analog Devices products, and the OPEN Alliance MACPHY SPI protocol.

POWER SUPPLY DOMAINS

The ADIN2111 has five power supply domains and requires a minimum of one supply rail. See the following power supplies:

- AVDD_H is the analog power supply input for the analog front end (AFE) circuitry in the ADIN2111.
- AVDD_L is the analog supply voltage for the internal LDO circuits. AVDD_L can be connected to the AVDD_H rail in single-supply mode, or to an alternative lower voltage rail in dual-supply mode for lower power consumption.
- DVDD1_1P1 and DVDD2_1P1 are the 1.1 V digital core power supply inputs for Port 1 and Port 2 PHYs. DVDD_1P1 and DVDD2_1P1 can operate from the internal 1.1 V LDO outputs available on the DLDO1_1P1 and DLDO2_1P1 pins. Alternatively, DVDD1_1P1 and DVDD2_1P1 can be driven from an external 1.1 V supply for lower power consumption. Note that DLDO1_1P1 and DLDO2_1P1 must not be connected together.
- VDDIO is the digital power supply input for the ADIN2111 MAC interface, MDIO, and digital inputs/outputs (I/Os). VDDIO can be connected directly to the AVDD_L rail or to an external power rail.

The System Level Power Management section describes various application circuits that can be used as reference.

Single-Supply Applications

In a single-supply application, connect AVDD_H and AVDD_L to VDDIO and connect DVDD1_1P1 to DLDO1_1P1 and DVDD2_1P1 to DLDO2_1P1. The appropriate supply voltage used depends on the end application and cable length. A recommended circuit is shown in the Single-Supply Configuration section.

Long Reach and Trunk/Spur Applications

The 1.0 V p-p transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. The ADIN2111 in this mode supports intrinsic safety applications.

The higher transmit operating mode of 2.4 V p-p supports trunk applications and requires a higher AVDD_H supply voltage of 3.3 V. This mode can be used for longer cable lengths in industrial Ethernet environments with higher noise levels.

ANALOG FRONT-END

The AFE stage consists of a hybrid stage, 9-level DAC, line driver, analog receive filter, input buffer, and ADC.

The line driver transmits the signal onto the line via the Port 1 (respectively Port 2) MDI interface pins, P1_TXP and P1_TXN (respectively P2_TXP and P2_TXN). The hybrid stage subtracts the transmitted signal from the received signal on the Port 1 (respectively Port 2) MDI pins, thereby allowing full duplex operation on the single-pair cable.

The received signal then passes through the analog receive filter and reaches the input buffer before being sent to the ADC.

TWO PORT SWITCH

The ADIN2111 internal two port switch manages the traffic between the SPI host, Port 1 PHY, and Port 2 PHY. The following modes of operations are available for the switch:

- Store and forward (to or from the SPI host)
- Store and forward (port to port)
- Cut through (port to port or SPI host to port).

The port to port traffic is set to cut through by default. To change to store and forward operation, reset the port cut through enable bit (PORT_CUT_THRU_EN) to 0 in the Configuration Register 2.

The switch has a table of 16 MAC addresses that are used determine where to forward frames. A configurable default operation exists for frames with unknown destination addresses (DAs).

The switch integrates seven FIFOs with a total of 28 kB of buffer to support the port to port and host to port traffic:

- 4 kB host to Port 1 PHY/Port 2 PHY transmit FIFO
- 4 kB Port 1 PHY to host high priority receive FIFO
- 4 kB Port 1 PHY to host low priority receive FIFO
- 4 kB Port 2 PHY to host high priority receive FIFO

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- 4 kB Port 2 PHY to host low priority receive FIFO
- 4 kB Port 1 to Port 2 transmit FIFO
- 4 kB Port 2 to Port 1 transmit FIFO

TRANSMIT AMPLITUDE CONFIGURATION

The ADIN2111 supports two transmit amplitude modes of operation, as follows:

- 1.0 V p-p and 2.4 V p-p mode (high level)
- 1.0 V p-p only mode

The high level transmit operating mode allows the ADIN2111 to support both voltage levels. The operating level can then be automatically configured during autonegotiation (if enabled) based on the link partner capabilities. Note that in high level transmit operating mode, AVDD_H must be supplied with 2.4 V or higher for the device to work properly.

The mode of operation is configured through the $\overline{\text{P1_TX2P4_EN}}$ (Port 1) and $\overline{\text{P2_TX2P4_EN}}$ (Port 2) hardware configuration pin signals (see the Transmit Amplitude section). The ADIN2111 also configures the default value for the transmit level register bits used for the autonegotiation process based on the level configured on those two pins (see the Transmit Amplitude Advertisement section).

The ADIN2111 is configured in high level transmit operating mode by default on Port 1 (respectively Port 2) if the $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) pin is left floating (internal pull-down resistor).

MASTER/SLAVE CONFIGURATION

The 10BASE-T1L standard uses a master/slave clock scheme. This scheme is commonly used in full duplex transceiver standards with echo cancellation.

On a 10BASE-T1L link, one PHY is designated as the master, and the other PHY as the slave. Autonegotiation is used to determine which PHY is the master and which is the slave. Master and slave assignment does not generally matter.

Software Configuration

The master and slave configuration bit (CFG_MST, accessible via the MDIO bridge for each PHY) is used to configure the respective PHY role. This bit is only used when autonegotiation is disabled. Otherwise, this bit is set or reset during the autonegotiation process (see the Autonegotiation section).

Table 9. CFG_MST Settings

Bit Setting	Description
0	Prefer slave
1	Prefer master

Table 10. Port 1 and Port 2 Master/Slave Default Configuration

Port	Master/Slave Configuration

Table 10. Port 1 and Port 2 Master/Slave Default Configuration (Continued)

Port	Master/Slave Configuration
1	Prefer master
2	Prefer slave

AUTONEGOTIATION

The ADIN2111 uses the autonegotiation capability in accordance with IEEE 802.3 Clause 98, providing a mechanism for exchanging information between the local device and link partners to agree to a common mode of operation. Single twisted pair autonegotiation is performed using differential Manchester encoding (DME) pages exchanged between the local device and its link partner. At a high level, autonegotiation provides the following functions:

- Transmit
- Receive
- Half duplex
- Arbitration

During the autonegotiation process, the local device advertises its own capabilities and compares them to those received from the link partner. The arbitration mechanism defines the operating modes elected so that the transmit amplitude mode and master/slave selection are configured for the linked devices.

If the link is dropped, the autonegotiation process restarts automatically. An autonegotiation restart can also be requested by writing to the autonegotiation restart bit (AN_RESTART) in the BASE-T1 autonegotiation control register (AN_CONTROL) of the respective PHY.

The autonegotiation process can take time to complete, depending on the number of pages exchanged, but is always the fastest way to bring up a link. Clause 98 of the IEEE 802.3 standard details the sequence timers and DME pages timing related to autonegotiation.

Autonegotiation is enabled by default for both ports of the ADIN2111, and it is strongly recommended to always keep it enabled.

Transmit Amplitude Advertisement

High Voltage Transmit Ability Advertisement

The B10L_TX_LVL_HI_ABLE bit can be used on each PHY to configure the default values for the autonegotiation advertisement parameters. This bit is read only and configures Port 1 PHY (respectively Port 2 PHY) ability advertisement based on the $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) hardware configuration pin signal, as described in the Transmit Amplitude section. The transmit amplitude advertisement parameters are defined with the following bits on each of the ADIN2111 PHYs:

- AN_ADV_B10L_TX_LVL_HI_ABL: advertisement of the 10BASE-T1L high level transmit operating mode ability bit

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- AN_ADV_B10L_TX_LVL_HI_REQ: advertisement of the 10BASE-T1L high level transmit operating mode request bit
- B10L_TX_LVL_HI: 10BASE-T1L transmit voltage amplitude control bit

Table 11. AN_ADV_B10L_TX_LVL_HI_ABL Settings

Bit Setting	Description
0	Support 1.0 V p-p transmit level only
1	Support both 1.0 V p-p and 2.4 V p-p transmit level

Table 12. AN_ADV_B10L_TX_LVL_HI_REQ Settings

Bit Setting	Description
0	Request 1.0 V p-p transmit level
1	Request 2.4 V p-p transmit level

High Voltage Transmit Level Request Advertisement

The two PHYs of the ADIN2111 can be configured to advertise a request for the 2.4 V p-p transmit level using the 10BASE-T1L high level transmit operating mode ability advertisement bit (AN_ADV_B10L_TX_LVL_HI_ABL) on the respective PHY. Note that the 2.4 V p-p transmit level must be enabled using the $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) hardware configuration pin signal to enable the high voltage request advertisement on Port 1 (respectively Port 2).

Link Partner Transmit Level Advertisement

The high level transmit information advertised from the link partner can be read using the following bits on each of the ADIN2111 PHYs:

- AN_LP_ADV_B10L_TX_LVL_HI_ABL: link partner 10BASE-T1L high level transmit operating mode ability
- AN_LP_ADV_B10L_TX_LVL_HI_REQ: link partner 10BASE-T1L high level transmit operating mode request

These bits update during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) is set on the respective PHY.

Transmit Amplitude Resolution

Autonegotiation supports the following features to define the transmit amplitude to use between a local node and its link partner:

- Advertise the high voltage transmit ability from the local node
- Request to use the high voltage transmit level from the local node
- Read the link partner transmit level ability and transmit level request
- Select the autonegotiation and transmit level operating mode

If the ADIN2111 PORT1 PHY (respectively Port 2 PHY) is configured in high voltage mode, the autonegotiation process determines the level to use on the PORT1 PHY (respectively Port 2 PHY) based on the link partner capabilities.

Determination of Transmit Level Resolution

For a 10BASE-T1L link, if either the local or remote PHY advertises that it is not capable of supporting the high level (2.4 V p-p) transmit operating mode, or if neither the local nor remote PHY advertises a request for high level (2.4 V p-p) transmit operating mode, the result is operation at the 1.0 V p-p transmit level.

If both the local and remote PHYs advertise that they are capable of transmitting in the high level (2.4 V p-p) transmit operating mode, and if either the local or remote PHY advertises a request for high level (2.4 V p-p) transmit operating mode, the result is operation at the 2.4 V p-p transmit level.

Thus, a PHY can ensure that the device must operate at the 1.0 V p-p transmit level. However, it can only request operation at the 2.4 V p-p transmit level.

Software Configuration

The ADIN2111 transmit level on the Port 1 PHY (respectively Port 2 PHY) can also be configured in software using the following 10BASE-T1L autonegotiation advertisement bits on the respective PHY:

- AN_ADV_B10L_TX_LVL_HI_ABL: high level transmit operating mode ability bit
- AN_ADV_B10L_TX_LVL_HI_REQ: high level transmit operating mode request register bits

The higher transmit level must be enabled on Port 1 (respectively Port 2) with the $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) hardware configuration pin signal to configure the two autonegotiation advertisement bits through software. See the Transmit Amplitude section for details.

If it is required to only operate the Port 1 PHY (respectively Port 2 PHY) at the 1.0 V p-p transmit level operation, clear the respective AN_ADV_B10L_TX_LVL_HI_ABL bit, so that 2.4 V p-p transmit level operation is not advertised. In this case, autonegotiation can only resolve to 1.0 V p-p transmit level operation, irrespective of the setting that the remote PHY advertises.

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Table 13. Determination of Transmit Level by Autonegotiation

AN_LP_ADV_B10L_TX_LVL_HI_ABL	AN_LP_ADV_B10L_TX_LVL_HI_REQ	AN_ADV_B10L_TX_LVL_HI_ABL	AN_ADV_B10L_TX_LVL_HI_REQ	Transmit Level
0	X[1]	0	X[1]	1.0 V p-p
1	X[1]	0	X[1]	1.0 V p-p
0	X[1]	1	X[1]	1.0 V p-p
1	0	1	0	1.0 V p-p
1	0	1	1	2.4 V p-p
1	1	1	0	2.4 V p-p
1	1	1	1	2.4 V p-p

[1] X means don't care.

Master/Slave Advertisement

On a 10BASE-T1L link, a local node and its remote link partner advertise their role capabilities whether they can operate as master, slave, prefer master, or prefer slave.

Each of the ADIN2111 PHYs provides the following functions:

- Master/slave configuration advertisement
- Forced master/slave configuration advertisement
- Read link partner master/slave configuration

Master/Slave Configuration Advertisement

For each of the ADIN2111 PHYs, the master/slave configuration register bit (AN_ADV_MST) in the BASE-T1 autonegotiation advertisement register, Bits[31:16] (AN_ADV_ABILITY_M) is used to configure the PHY to advertise its master/slave configuration. Note that this bit is reset to the default role of each PHY after power-up, hardware reset, or software reset (PHY 1 = prefer master, PHY 2 = prefer slave). See the Master/Slave Configuration section for more details on the master/slave configuration.

Forced Master/Slave Configuration Advertisement

Each of the ADIN2111 PHYs can be forced to operate as a master (or slave). Forced configuration must be used with caution because a configuration fault can occur if the link partner is also set in forced mode as a master (or slave), resulting in autonegotiation failure. The ADIN2111 can be forced to operate as a master or slave on each PHY using the force master/slave configuration register bit (AN_ADV_FORCE_MS) in the BASE-T1 autonegotiation advertisement register, Bits[15:0] (AN_ADV_ABILITY_L).

Read Link Partner Master/Slave Configuration

The link partner advertised master/slave setting can be read using the following bits on each of the ADIN2111 PHYs:

- AN_LP_ADV_FORCE_MS: link partner force master/slave configuration register bit
- AN_LP_ADV_MST: link partner master/slave configuration register bit

These bits update during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) in the BASE-T1 autonegotiation status register is set on the respective PHY.

Master/Slave Resolution

The master/slave resolution between a local PHY and its remote link partner can be predefined or defined during autonegotiation. When using autonegotiation, the internal logic determines the roles so only one master is present on the link.

Each of the ADIN2111 PHYs provides the following functions:

- Master/slave configuration resolution result
- Autonegotiation complete status bit

Determination of Master/Slave Configuration

On a 10BASE-T1L link, when the local and remote PHYs have the same preferred configuration (for example, both slave or both master), autonegotiation randomly assigns compatible configurations to the local and remote PHYs. When one PHY has a forced configuration, its master/slave configuration is given priority over a PHY with a preferred setting.

Master/Slave Configuration Resolution

For each of the ADIN2111 PHYs, the master/slave configuration defined by autonegotiation can be checked using the master/slave resolution result register bits (AN_MS_CONFIG_RSLTN) in the extra autonegotiation status register. The bits indicate if the respective PHY is configured as master or slave, or if there is a configuration fault.

These bits update during the autonegotiation process and are valid when the autonegotiation complete register bit (AN_COMPLETE) in the BASE-T1 autonegotiation status register (AN_STATUS) is set on the respective PHY.

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Table 14. Determination of Master/Slave by Autonegotiation

Local[1]		Remote[1]		Local	Remote
AN_ADV_FORCE_MS	AN_ADV_MST	AN_LP_ADV_FORCE_MS	AN_LP_ADV_MST	Master/Slave Resolution	
0	0	0	0	Master/slave	Slave/master
0	0	0	1	Slave	Master
0	1	0	0	Master	Slave
0	1	0	1	Master/slave	Slave/master
0	X	1	0	Master	Slave
0	X	1	1	Slave	Master
1	0	0	X	Slave	Master
1	1	0	X	Master	Slave
1	0	1	0	Configuration fault	Configuration fault
1	0	1	1	Slave	Master
1	1	1	0	Master	Slave
1	1	1	1	Configuration fault	Configuration fault

[1] X means don't care.

Autonegotiation Fail

On a 10BASE-T1L link, autonegotiation can fail due to the following scenarios:

- Configuration fault, such as invalid master/slave configuration
- Link quality issues
- Timeout in pages transmission

If autonegotiation fails, it restarts. The link remains down until the autonegotiation process completes.

MDI

The ADIN2111 provides a two-pin MDI for each port (Port 1 and Port 2) with internal termination resistors and an internal hybrid, to connect the ADIN2111 ports to the Ethernet network via a twisted wire pair. The two ports are connected to the internal PHYs (PHY 1 and PHY 2).

SPI

The ADIN2111 can be interfaced to the host controller via the four-pin SPI, allowing frame transfer and control of the internal switch MAC registers and the internal PHYs core management registers via the SPI to MDIO bridge.

The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures (see the Register Summary: 10BASE-T1L Single Pair Ethernet PHY Core (ADIN2111) section).

The SPI is compatible with the OPEN Alliance SPI protocol and supports a generic SPI mode. The SPI operating mode is set using the SPI_CFG0 and SPI_CFG1 hardware configuration pin signals (see the Hardware Configuration Pins section).

HARDWARE INTERRUPT ($\overline{\text{INT}}$)

The ADIN2111 can generate a hardware interrupt to a host controller using the $\overline{\text{INT}}$ pin. This pin can be configured to trigger interrupts from the following sources:

- PHY 1/PHY 2 status
- PHY 1/PHY 2 data ready
- PHY 1/PHY 2 system errors
- Frame and overflow errors
- IEEE 1588 timestamp capture
- Reset interrupt
- Software requested interrupt

Switch Subsystem Interrupt

When an interrupt occurs, the system can poll the Status Register 0 (STATUS0) and the Status Register 1 (STATUS1) to determine the origin of the interrupt.

The switch subsystem interrupts can be configured to trigger the $\overline{\text{INT}}$ pin using the Interrupt Mask Register 0 (IMASK0) and the mask bits for driving the interrupt pin register (IMASK1).

PHY Subsystem Interrupts

The following conditions can be selected to generate an interrupt on each of the ADIN2111 PHYs:

- MAC interface frame checker/generator interrupt
- MAC interface buffers overflow/underflow interrupt
- Autonegotiation status change interrupt
- Link status change interrupt

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Those conditions can be set to enable an interrupt on the $\overline{INT}$ pin using the PHY subsystem interrupt mask register (PHY_SUBSYS_IRQ_MASK).

Following a hardware interrupt on the $\overline{INT}$ pin, the interrupt source can be checked using the PHY subsystem interrupt status register (PHY_SUBSYS_IRQ_STATUS).

Hardware Reset Interrupt

Each PHY of the ADIN2111 can also be configured to generate a hardware interrupt after a hardware reset ($\overline{RESET}$ pin pulled low) by setting the CRSM_HRD_RST_IRQ_EN bit in the system interrupt mask register (CRSM_IRQ_MASK) of the respective PHY.

Although both PHYs can be used to generate a hardware interrupt, it is recommended to use PHY 1 for this purpose.

Following a hardware interrupt received on the SPI host from the $\overline{INT}$ pin, the PHYINT bit (respectively P2_PHYINT bit) on the Status Register 0 (respectively Status Register 1) is also set to 1, notifying an interrupt from PHY 1 (respectively PHY 2).

The interrupt source can then be checked using the CRSM_HRD_RST_IRQ_LH bit in the system interrupt status register (CRSM_IRQ_STATUS) of the respective PHY.

Software Requested Interrupt

For system validation with an external host controller, each PHY of the ADIN2111 can be requested to generate a hardware interrupt on the $\overline{INT}$ pin using the CRSM_SW_IRQ_REQ bit in the system interrupt mask register (CRSM_IRQ_MASK).

Although both PHYs can be used to generate a hardware interrupt, it is recommended to use PHY 1 for this purpose.

Following a hardware interrupt received on the SPI host from the $\overline{INT}$ pin, the PHYINT bit (respectively P2_PHYINT bit) in the Status Register 0 (respectively Status Register 1) is also set to 1, notifying an interrupt from PHY 1 (respectively PHY 2).

The interrupt source can then be checked using the CRSM_SW_IRQ_LH bit in the system interrupt status register (CRSM_IRQ_STATUS) of the respective PHY.

PHY System Error Interrupts

Each of the ADIN2111 PHYs can also generate system errors interrupts. The interrupt flags are located within the reserved bit sections of system interrupt status register (CRSM_IRQ_STATUS) of the respective PHY.

The system interrupt mask register (CRSM_IRQ_MASK) must be configured on the respective PHY to allow system error interrupts. Refer to Table 215 for details on the interrupts mask.

The ADIN2111 must be hardware reset to recover from a system error interrupt from one of the two PHYs (CRSM_IRQ_STATUS reserved bits read as 1 on the respective PHY).

RESET OPERATIONS

The ADIN2111 supports the following chip resets:

- Power-on reset
- Hardware reset
- Software reset
- MAC subsystem reset
- PHY 1/PHY 2 subsystem reset

All of these resets put the ADIN2111, including the two PHY cores and the internal switch, into a known state.

Power-On Reset

The ADIN2111 includes a power supply monitoring circuit to ensure that the chip has the proper voltage supply before initiating the power-up sequence. During power-up, the ADIN2111 is held in hardware reset until each of the supplies crosses its minimum rising threshold value and the power is considered good.

Hardware Reset

A hardware reset is initiated by the power-on reset circuitry or by asserting the $\overline{RESET}$ pin low for a minimum of 10 µs. The ADIN2111 includes deglitch circuitry on this pin to reject pulses shorter than 1 µs.

When the $\overline{RESET}$ pin is deasserted, all the input/output (I/O) pins are held in tristate mode, the hardware configuration pins are latched, and the I/O pins are configured to their functional mode. When all the external and internal supplies are valid and stable, the crystal oscillator circuit is enabled. After the crystal starts up and stabilizes, the phase-locked loop (PLL) enables. After a delay of 90 ms (maximum) from the deassertion of the $\overline{RESET}$ pin, all the internal clocks are valid, the internal logic releases from reset, and all the internal SPI, PHY 1, and PHY 2 registers are accessible from the SPI.

The CLK25_REF clock output stays low while the $\overline{RESET}$ pin is asserted low and remains low for another 70 ms (maximum) after the $\overline{RESET}$ pin deasserts.

Software Reset

A chip software reset can be initiated by writing 1 to the SWRESET field of the software reset register (RESET). Note that the software reset does not reset PORT2 PHY. The PORT2 PHY can be reset using the hardware reset or PHY subsystem reset.

If a transmission is taking place when the SPI software reset is initiated, the frame transmission stops abruptly and a runt or a

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frame with a bad cyclic redundancy check CRC can be transmitted. Once the chip is reset, the ADIN2111 is ready to bring up links.

When this software reset is initiated, a full initialization of the chip, almost equivalent to a hardware reset, is done. The I/O pins are held in tristate mode, the hardware configuration pins are latched, and the I/O pins are configured for their functional mode. The crystal oscillator circuit is enabled, and after the crystal starts up and stabilizes, the PLL is enabled. Approximately 10 ms (maximum) after writing the RESET register, the internal logic releases from reset and the internal SPI, as well as the two PHY registers, are accessible.

The system ready bit (CRSM_SYS_RDY) in the system status register (CRSM_STAT) on each PHY indicates that the start-up sequence is complete, and the respective PHY is ready for normal operation.

The CLK25_REF clock output remains low for 25 ms (maximum) following a software reset.

PHY Subsystem Reset

A PHY subsystem reset is initiated on the ADIN2111 PHY 1 (respectively PHY 2) by setting the respective PHY subsystem reset register bit (CRSM_PHY_SUBSYS_RST) to 1 in the PHY subsystem reset register (CRSM_PHY_SUBSYS_RST). The reset is applied for typically 1.2 µs, and then this bit self clears. All of the PHY 1 (respectively PHY 2) digital circuitry is reset, and any available active link drops. The PHY 1 (respectively PHY 2) subsystem reset does not alter the values of the management registers, which remain accessible throughout the sequence. The subsystem reset is a short reset and can be used to put the device into a known state while retaining the internal register contents.

MAC Subsystem Reset

A MAC only software reset can be initiated by writing the required pair of keys to the software reset register (SOFT_RST). The reset is applied for about 1.2 µs. The MAC subsystem reset interrupts any transmit/receive packet exchange between the MAC and the two PHYs, but does not drop any existing link or prevent a link from being established. The MAC subsystem reset does not alter the values of the PHY registers.

Note that PHY 1 must be out of software power-down for the MAC subsystem reset to take effect.

STATUS LEDS

The ADIN2111 provides two configurable LED pins for each port: P1_LED_0, P1_LED_1, P2_LED_0, and P2_LED_1 (also noted as Px_LED_x).

The LED pin signals can be used to connect external LEDs to indicate the ADIN2111 link status and transmit or receive activity. The activity assigned to each LED is configurable through the LED control register (LED_CNTRL).

The LED pins are suitable for ultra low power LEDs. The maximum output current for each LED pin is 8 mA with a VDDIO = 3.3 V. For higher LED power requirements, use an external transistor, as described in the Transistor Controlled LED section.

The LED pins can also be connected to a host microcontroller general-purpose input/output (GPIO) (configured as a pulse-width modulated input or hardware interrupt). This configuration is useful in applications where the user interface must be fully handled by an external host controller (for example, an external LED module or display).

If the LED pins are directly connected to a host controller, place a low value resistance in series between the ADIN2111 LED pins and the host controller to avoid any potential current surge. The resistor value must be defined based on host controller capabilities and the ADIN2111 LED pins output current capabilities listed in Table 1.

LED Pin Multiplexing

For the Px_LED_1 pins only (P1_LED_1 and P2_LED_1), an internal multiplexer must be configured to enable the LED signal on the respective pin. Px_LED_1 signals are disabled by default and can be enabled using the DIGIO_LED1_PINMUX bits in the Pin Mux Configuration 1 register (DIGIO_PINMUX) within the respective PHY.

The Px_LED_0 pins (P1_LED_0 and P2_LED_0) do not need multiplexing.

LED Polarity

The four LED pins can be configured to support various LED circuit polarities using the LED polarity register (LED_POLARITY) on the respective PHY. Three polarity modes are available for each LED, as follows:

- Autosense (default)
- Active high
- Active low

In autosense mode, the ADIN2111 automatically senses the pin at power-up or reset to select the appropriate polarity configuration.

In active high mode, the ADIN2111 is configured to drive the LED from the anode side.

In active low mode, the ADIN2111 is configured to drive the LED from the cathode side.

Example circuits are described in the LED Circuit Examples section.

LED Function

The LED pins can be configured to display various activities of the ADIN2111 using the LED function feature. The LED function

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is configurable for each LED using the LED0_FUNCTION and LED1_FUNCTION bits in the LED control register (LED_CNTRL).

Note that the 7, 8, 9, and 10 (decimal) bit settings for LED0_FUNCTION and LED1_FUNCTION are not available in LED Mode 2.

LED Mode

For each of the ADIN2111 LED pins, the activity behavior can be configured using the two LED modes, as follows:

- LED Mode 1: blink duty cycle defined using the LED 0 on/off blink time register (LED0_BLINK_TIME_CNTRL)
- LED Mode 2: blink duty cycle automatically defined by the ADIN2111 based on activity level (%)

LED Pins Configuration Summary

See Table 15 for the configuration options of the Px_LED_x pins.

Table 15. LED Pins Configuration Summary

Parameter	Px_LED_0	Px_LED_1
Pin Number	19 (P1_LED_0), 47 (P2_LED_0)	21 (P1_LED_1), 48 (P2_LED_1)
Internal Pull-Up or Pull-Down Resistor	Pull-up	Pull-down
Status at Power-Up or Reset	Enabled	Disabled (via pin mux)
LED Pin Mux	Not applicable	DIGIO_LED1_PINMUX bits in the Pin Mux Configuration 1 register
Enable LED	LED0_EN bit in the LED control register (default: enabled)	LED1_EN bit in the LED control register (default: LED_1 output not enabled)
LED Polarity	LED0_POLARITY bits in the LED polarity register (default: autosense)	LED1_POLARITY bits in the LED polarity register (default: autosense)
LED Mode	LED0_MODE bit in the LED control register (default: LED Mode 1)	LED1_MODE bit in the LED control register (default: LED Mode 1)
LED Function[1]	LED0_FUNCTION bits in the LED control register (default: LINKUP_TXRX_ACTIVITY)	LED1_FUNCTION bits in the LED control register (default: TXRX_ACTIVITY)
LED Blink Rate	LED0_BLINK_TIME_CNTRL in the LED 0 on/off blink time register	LED1_BLINK_TIME_CNTRL in the LED 1 on/off blink time register
Maximum Current[2]	8 mA at 3.3 V	8 mA at 3.3 V

[1] The 7, 8, 9, and 10 (decimal) settings for the LEDx_FUNCTION bits are not available in Mode 2.

[2] See Table 1 for details.

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POWER-DOWN MODES

The ADIN2111 supports the following two power-down modes:

- Hardware power-down
- Software power-down

Hardware Power-Down Mode

The hardware power-down mode can be used when no operation is required on the ADIN2111 and the power consumption needs to be minimized.

The device enters hardware power-down mode when the $\overline{\text{RESET}}$ pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the clocks are gated off, and all the I/O pins are held in tristate mode.

In this mode, the ADIN2111 power consumption is equivalent to the internal circuit leakage. The internal registers are not accessible in this mode.

Software Power-Down Mode

Software power-down mode can be used on each PHY to configure the ADIN2111 registers before bringing a link up. In this mode, the PHY 1 (respectively PHY 2) analog and digital circuits are in a low power state, and the PLL is active and can provide output clocks if configured to do so. Any signals exposed to the MDI pins, P1_TXP and P1_TXN (respectively P2_TXP, P2_TXN), are ignored and any active link on the respective PHY is dropped. The SPI registers are accessible, and the device can be configured using software.

The PHY 1 (respectively PHY 2) can be configured to automatically enter software power-down mode after power-up, hardware reset, or software reset using the $\overline{\text{P1_SWPD_EN}}$ (respectively $\overline{\text{P2_SWPD_EN}}$) hardware configuration pin signal. The ADIN2111 can also be instructed to enter software power-down mode by setting the software power-down bit (CRSM_SFT_PD) in the software power-down control register (CRSM_SFT_PD_CNTRL) within the respective PHY.

The software power-down status bit (CRSM_SFT_PD_RDY) in the system status register (CRSM_STAT) indicates that the respective PHY is in software power-down mode.

The ADIN2111 PHY 1 (respectively PHY 2) exits software power-down mode when the CRSM_SFT_PD bit is cleared within the respective PHY. After exiting software power-down, and if autonegotiation is completed, the PHY 1 (respectively PHY 2) attempts to bring a link up.

Note that it is necessary to bring PHY 1 out of software power-down mode to establish a link on PHY 2.

HARDWARE CONFIGURATION PINS

OVERVIEW

The ADIN2111 can operate in unmanaged or managed configurations with the use of the hardware configuration pins.

The hardware configuration pins are standard pins with an alternate bootstrap function. The ADIN2111 reads the configuration pin level immediately after power-up, hardware reset, or software reset, and configures the two PHY settings accordingly. When active, the ADIN2111 immediately attempts to bring up a link on each PHY, and the hardware configuration pins can then be used with their main pin function. These pins can be used in unmanaged or managed configuration.

The unmanaged configuration refers to the ADIN2111 PHY parameters being configured by the hardware configuration pins. This mode can be used when the system requires a static configuration of the ADIN2111 port settings without the need for software control. In this context, the port to port operation on the ADIN2111 is configured in cut through.

The managed configuration refers to the full control of the ADIN2111 using software via the SPI. The two PHYs, MAC layer, and the store and forward switch can be configured in software. The configuration pins can be connected to the external host or hardware configured using pull-up/pull-down resistors. When active, the host controller can override any of the ADIN2111 hardware configurations set by the hardware pins after power-up, hardware reset, or software reset.

UNMANAGED APPLICATIONS

In unmanaged applications, it is possible to configure the ADIN2111 using the hardware configuration pins without any software intervention. In that case, the ADIN2111 is configured by default in cut through mode (port to port forwarding).

Software power-down after reset must be disabled on both port PHYs for unmanaged applications, or the ADIN2111 associated PHY remains in power-down indefinitely, because the device can only exit power-down from register operation using the SPI (see the Software Power-Down Mode section).

MANAGED APPLICATIONS

In managed applications, the ADIN2111 can be configured by a host controller via the SPI. The host controller can dynamically configure the device as required by the application.

In managed applications, the software power-down after reset functionality can be enabled because the host controller brings the ADIN2111 to active mode using the management interface.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions are configurable from the ADIN2111 hardware configuration pins:

- PHY 1 software power-down mode after reset
- PHY 2 software power-down mode after reset
- PHY 1 transmit amplitude configuration
- PHY 2 transmit amplitude configuration
- OPEN Alliance or generic SPI
- SPI CRC/protection

All of the hardware configuration pins have internal pull-up or pull-down resistors, as shown in Table 8. The default mode of operation is shown in Table 16. If an alternative mode of operation is required, refer to Table 17 for the suggested external pin control.

Table 16. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode (Pin Floating)
Port 1 Software Power-Down Mode After Reset	Enabled
Port 2 Software Power-Down Mode After Reset	Disabled
Port 1 Transmit Amplitude	1.0 V p-p and 2.4 V p-p
Port 2 Transmit Amplitude	1.0 V p-p and 2.4 V p-p
SPI Protocol	OPEN Alliance
SPI CRC/Protection	Enabled

Table 17. Recommended Control for Hardware Configuration Pins

Required Pin Level	Managed Configuration Options	Unmanaged Configuration Options
High	4.7 kΩ external pull-up resistor Host GPIO output high[1]	4.7 kΩ external pull-up resistor
Low	External pull-down resistor Host GPIO output low[1] Host GPIO tristated[2] Floating pin[2]	External pull-down resistor Floating pin[2]

[1] A low value series resistor is recommended.

[2] An external pull-down resistor is recommended.

Software Power-Down After Reset

The $\overline{\text{P1_SWPD_EN}}$ (respectively $\overline{\text{P2_SWPD_EN}}$) hardware configuration pin signal is used to enable or disable the software power-down after reset feature for PHY 1 (respectively PHY 2). The power-down bit (CRSM_SFT_PD) in the software power-down control register is set based on the $\overline{\text{Px_SWPD_EN}}$ signal status during power-up, hardware reset, or software reset. CRSM_SFT_PD can also be set using the SPI via the MDIO bridge to enable software power-down after reset.

The $\overline{\text{P1_SWPD_EN}}$ pin has a weak internal pull-down resistor. Therefore, by default, the ADIN2111 Port 1 is configured with software power-down after reset enabled.

The $\overline{\text{P2_SWPD_EN}}$ pin has a weak internal pull-up resistor. Therefore, by default, the ADIN2111 Port 2 is configured with software power-down after reset disabled.

HARDWARE CONFIGURATION PINS

When software power-down after reset is enabled on a port, the associated ADIN2111 PHY enters software power-down after power-up, hardware reset, or software reset. Software power-down provides a lower power mode where most of the ADIN2111 internal modules are turned off.

The ADIN2111 PHYs can be configured to exit power-down by setting the CRSM_SFT_PD bit to 0 using the SPI via the MDIO bridge.

Following a power-up, hardware reset, or software reset, and if autonegotiation is enabled and software power-down after reset is disabled, the respective ADIN2111 PHY starts autonegotiation and tries to bring up a link.

Table 18. Port 1/Port 2 Software Power-Down (Hardware Configuration)

Px_SWPD_EN	Software Power-Down Configuration
0	PHY in software power-down after reset
1	PHY not in software power-down after reset

Transmit Amplitude

The P1_TX2P4_EN (respectively P2_TX2P4_EN) hardware configuration pin signal is shared with the P1_LED_1 (respectively P2_LED_1) signal and is used to configure the default transmit amplitude mode. The transmit amplitude mode is defined by the pin status during power-up, hardware reset, or software reset as defined in Table 19 and Table 20.

The Px_TX2P4_EN hardware configuration pin signals also configure the default setting of the high voltage transmit ability bit (B10L_TX_LVL_HI_ABLE) in the 10BASE-T1L PMA status register (B10L_PMA_STAT) within the relevant PHY during power-up, hardware reset, or software reset. The B10L_TX_LVL_HI_ABLE bit reports whether the associated PHY is capable of operating in the 10BASE-T1L high transmit voltage mode, as described in Table 21.

If Px_TX2P4_EN is pulled low during power-up, hardware reset, or software reset, the 2.4 V p-p transmit operating mode is enabled and the value of B10L_TX_LVL_HI_ABLE is set to 1.

If Px_TX2P4_EN is pulled high during power-up, hardware reset, or software reset, the 2.4 V p-p transmit operating mode is disabled, and the value of B10L_TX_LVL_HI_ABLE is set to 0. In that case, the associated register on the respective PHY cannot be changed through the SPI. That is, 2.4 V p-p operation is not possible on the respective PHY if it has been configured for the 1.0 V p-p level only via the Px_TX2P4_EN pin.

The Px_TX2P4_EN pins have a weak internal pull-down resistor. Therefore, by default, the ADIN2111 is configured to support both 1.0 V p-p and 2.4 V p-p voltage levels on Port 1 and Port 2.

Table 19. Port 1 Transmit Amplitude Selection (Hardware Configuration)

P1_TX2P4_EN	Transmit Amplitude Selection
0	1.0 V p-p and 2.4 V p-p
1	1.0 V p-p

Table 20. Port 2 Transmit Amplitude Selection (Hardware Configuration)

P2_TX2P4_EN	Transmit Amplitude Selection
0	1.0 V p-p and 2.4 V p-p
1	1.0 V p-p

Table 21. B10L_TX_LVL_HI_ABLE Settings

Bit Setting	Description
0	PHY does not support 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.
1	PHY supports 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.

SPI Protocol Configuration

The ADIN2111 allows the use of a generic SPI protocol with or without the use of CRC, or the OPEN Alliance SPI protocol with or without protection.

Table 22. SPI Protocol (Hardware Configuration)

SPI Protocol	SPI_CFG1	SPI_CFG0
OPEN Alliance with Protection	0	0
OPEN Alliance Without Protection	0	1
Generic SPI with 8-bit CRC	1	0
Generic SPI Without 8-bit CRC	1	1

BRINGING UP 10BASE-T1L LINKS

OVERVIEW

The Unmanaged PHY Operation section and Managed PHY Operation section provide some recommendations on how to bring a link up between the ADIN2111 and a remote link partner. These sections cover various configurations, and some may not be relevant to the intended application. Refer to the Theory of Operation section for more detailed explanations.

UNMANAGED PHY OPERATION

For an unmanaged PHY where there is no control of the ADIN2111 over the management interface, the hardware configuration pins determine the operating mode for each PHY (see the Hardware Configuration Pins section). In this context, the device is configured to run in cut through mode (Port 1 to Port 2 forwarding)

The Disable Software Power-Down Mode After Reset section and Set Transmit Amplitude Level section describe the steps required to bring up a link in unmanaged applications.

Disable Software Power-Down Mode After Reset

Software power-down mode after reset can be disabled for PHY 1 by asserting the $\overline{\text{P1_SWPD_EN}}$ (respectively $\overline{\text{P2_SWPD_EN}}$) pin signal high during power-up, hardware reset, or software reset, so that PHY 1 does not enter software power-down mode when it exits reset.

Software power-down mode after reset is disabled on PHY 2 by default (due to the internal pull-up resistor).

See the Software Power-Down After Reset section for details on how to configure the software power-down after reset function.

Set Transmit Amplitude Level

The $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) pin signal configures the PHY 1 (respectively PHY 2) to advertise the support of both 1.0 V p-p and 2.4 V p-p transmit level operation, or to only advertise support of the 1.0 V p-p transmit level operation.

By default, PHY 1 and PHY 2 are configured to support 1.0 V p-p and 2.4 V p-p transmit levels (due to the internal pull-down resistor). Assert the relevant pin high or low to disable the support for the 2.4 V p-p transmit level on the relevant port.

See the Transmit Amplitude section for details on how to configure the transmit amplitude level.

MANAGED PHY OPERATION

In a managed PHY application, a host controller such as a microcontroller is used to configure the ADIN2111 operation in software via the SPI interface.

Similar to the unmanaged PHY operation, the hardware configuration pins can be used to set up the controlled ADIN2111 (see the Unmanaged PHY Operation section for details). Alternatively, the hardware configuration pins can directly be controlled by the host (for example, GPIO) via an external pull-up or pull-down resistor or both.

In managed applications, the software power-down after reset can be enabled. The ADIN2111 stays in software power-down mode until the software has configured the PHY to be active. When active, the PHY can start autonegotiation and try to bring up a link.

Power-Up and Reset Complete

A typical way for software to verify that the device has completed the power-up and reset sequence and is available for normal operation is to read the management register that has the IEEE organizationally unique identifier (OUI), model, and revision numbers. The value of this register is unique to each PHY vendor and is a nonzero value. If the device has not completed the power-up, the value does not read properly. In legacy BASE-T PHYs, this value is at management interface Register Address 0x2 and Register Address 0x3.

In the ADIN2111, the OUI, model number, and revision numbers can be read from the PHY identification register (PHYID). If the reset value of the register (0x283BCA1) can be read, the device exited reset and is ready for configuration. These fields can also be read at Device Address 0x1F Clause 45 only), Register Address 0x2, and Register Address 0x3 (Clause 22 and Clause 45).

The OUI Bits[3:18] are located in the Vendor Specific MMD 1 device identifier high register (MMD1_DEV_ID1).

The OUI Bits[19:24] (MMD1_DEV_ID2_OUI), the model number Bits[6:0] (MMD1_MODEL_NUM), and the revision number Bits[6:0] (MMD1_REV_NUM) are located in the Vendor Specific MMD 1 device identifier low register (MMD1_DEV_ID2).

Table 23. ADIN2111 Unique Identifier Values

Description	Bit Name	Value
Organizationally Unique Identifier, Bits[3:18]	MMD1_DEV_ID1	0x283
Organizationally Unique Identifier, Bits[19:24]	MMD1_DEV_ID2_OUI	0x2F
Model Number, Bits[6:0]	MMD1_MODEL_NUM	0x8
Revision Number, Bits[6:0]	MMD1_REV_NUM	0x1

When a valid read of the IEEE OUI is done, the system ready bit (CRSM_SYS_RDY) in the system status register (CRSM_STAT) can also be read to verify that the start-up sequence is complete and the system is ready for normal operation.

The software power-down status bit (CRSM_SFT_PD_RDY) in the system status register (CRSM_STAT) is accessible on each PHY and can be read to check if the relevant PHY is in the software power-down state. This bit is also controlled by the $\overline{\text{P1_SWPD_EN}}$

BRINGING UP 10BASE-T1L LINKS

(PHY 1) and $\overline{\text{P1_SWPD_EN}}$ (PHY 2) hardware configuration pin signals.

Switch Initialization

After power-up, hardware reset, or software reset, the ADIN2111 switch can be configured via the SPI. Configure the Interrupt Mask Register 0 (IMASK0) register and the mask bits for driving the interrupt pin (IMASK1) register to enable interrupts as required.

Write CONFIG0 and CONFIG2 to set up the required functionality of the switch. For example, set the OPEN Alliance chunk size or enable cut through, if required.

When the switch is configured, write 1 to the SYNC field in the CONFIG0 register to indicate that the switch configuration is complete.

The default frame forwarding operation of the switch can be configured via the P1_FWD_UNK2P2, P2_FWD_UNK2P1, P1_FWD_UNK2HOST, and P2_FWD_UNK2HOST bits in the Configuration Register 2 (CONFIG2). The filtering table also needs to be configured. See the Frame Forwarding on Receive section for more details.

Configuring the Device for Linking

After power-up or reset, configure the ADIN2111 for the desired operation for linking. The ADIN2111 may already be configured as required by the hardware configuration pins, but greater control is available using the management registers via the SPI.

The autonegotiation process is used to match the operating mode between a local and remote PHY. For example, autonegotiation is used to ensure that the modes agree between the two devices on which PHY operates as master and which as slave. Autonegotiation is also used to match the transmit level between the two PHYs.

Autonegotiation is enabled by default for the ADIN2111 PHYs, and it is strongly recommended to always keep autonegotiation enabled. Autonegotiation is defined by the IEEE standard and includes a number of mechanisms to ensure robust linking operation between PHYs. Autonegotiation is the fastest way to bring up a link.

Configuration of Transmit Level Mode

The ADIN2111 PHYs can support transmit level operation at either 1.0 V p-p or 2.4 V p-p if the B10L_TX_LVL_HI_ABLE bit in the 10BASE-T1L PMA status register (B10L_PMA_STAT) on the respective PHY is set to 1 and a 3.3 V supply is provided on the AVDD_H pins. The higher transmit level can support longer reach but also has higher power consumption.

The ADIN2111 PHYs can support 1.0 V p-p transmit level operation with a 1.8 V supply on the AVDD_H pins at very low power consumption.

Each PHY of the ADIN2111 can either be configured to advertise support of both 1.0 V p-p and 2.4 V p-p transmit level operation or to advertise support of only 1.0 V p-p transmit level operation. Refer to the Transmit Level Mode Advertisement section for more details.

1.0 V p-p transmit level operation is required for intrinsically safe operation.

Enable High Voltage Transmit Ability

The high voltage transmit ability is set on Port 1 (respectively Port 2) using the $\overline{\text{P1_TX2P4_EN}}$ (respectively $\overline{\text{P2_TX2P4_EN}}$) hardware configuration pin signal. This signal internally sets the high voltage transmit ability bit B10L_TX_LVL_HI_ABLE (read only), for each PHY, as described in the Transmit Amplitude section.

Enable 1.0 V p-p and 2.4 V p-p Transmit Levels

To allow both 1.0 V p-p and 2.4 V p-p transmit level operation, set the 10BASE-T1L high level transmit operating mode ability bit (AN_ADV_B10L_TX_LVL_HI_ABL) in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H) to 1 to indicate that the device is capable of 2.4 V p-p transmit level operation. A 3.3 V supply is required on the AVDD_H pins.

Set 2.4 V p-p Transmit Level as Preferred

If 2.4 V p-p transmit level operation is preferred on PHY 1 or PHY 2, set the 10BASE-T1L high level transmit operating mode request bit (AN_ADV_B10L_TX_LVL_HI_REQ) in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H) to 1 on the respective PHY. Note that autonegotiation determines the transmit level that the link operates at.

Set 1.0 V p-p Transmit Level as Preferred

If 1.0 V p-p transmit level operation is preferred on PHY 1 or PHY 2, set the AN_ADV_B10L_TX_LVL_HI_REQ bit in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_B10L_TX_LVL_HI_REQ) to 0 on the respective PHY.

Note that autonegotiation determines the transmit level at which the link operates.

Enable 1.0 V p-p Transmit Level Only

If it is required to only operate the PHY 1 or PHY 2 at the 1.0 V p-p transmit level operation, set the 10BASE-T1L high level transmit operating mode ability bit (AN_ADV_B10L_TX_LVL_HI_ABL) in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H) to 0 so that the 2.4 V p-p transmit level operation is not advertised.

In this case, autonegotiation can only resolve to the 1.0 V p-p transmit level operation, irrespective of the setting that the remote PHY advertises. For very long cable lengths, depending on the characteristics of the cable, it may not be possible to bring up a link at the 1.0 V p-p operation.

BRINGING UP 10BASE-T1L LINKS

When the high level transmit is disabled on PHY1 (respectively PHY2) through the P1_TX2P4_EN (respectively P2_TX2P4_EN) pin signal, the AVDD_H supply can be supplied from either 1.8 V or 3.3 V for the 1.0 V p-p transmit level operation.

Transmit Level Mode Advertisement

Enable High Voltage Transmit Ability

The AVDD_H power rail must be provided with a 3.3 V supply for the ADIN2111 to support the 2.4 V p-p transmit level on Port 1 and Port 2.

The high voltage transmit ability is enabled on the ADIN2111 PHY 1 (respectively PHY 2) by setting the P1_TX2P4_EN (respectively P2_TX2P4_EN) hardware configuration pin signal low during power-up, hardware reset, or software reset. The 10BASE-T1L high voltage transmit ability bit (B10L_TX_LVL_HI_ABLE) in the 10BASE-T1L PMA status register (B10L_PMA_STAT) of the respective PHY is set automatically to the defined hardware configuration as follows:

- B10L_TX_LVL_HI_ABLE = 0: 1.0 V p-p only ability
- B10L_TX_LVL_HI_ABLE = 1: 1.0 V p-p and 2.4 V p-p ability

See the Configuration of Transmit Level Mode section for more details.

Advertise High Voltage Transmit Ability

To advertise the high voltage transmit ability during autonegotiation between PHY 1 (respectively PHY 2) and a link partner, set the 10BASE-T1L high level transmit operating mode ability bit (AN_ADV_B10L_TX_LVL_HI_ABL) in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H) to 1 on PHY 1 (respectively PHY 2). This bit can only be set if the ADIN2111 PHY 1 (respectively PHY 2) has the ability to transmit in high voltage mode (B10L_TX_LVL_HI_ABLE = 1 in the 10BASE-T1L PMA status register).

High voltage transmit ability only enables the ADIN2111 PHY 1 (respectively PHY 2) to advertise support for both the 2.4 V p-p and 1.0 V p-p levels. The selected level is determined by autonegotiation with the link partner.

See the Transmit Amplitude Advertisement section for more details.

Advertise a Request for High Voltage Transmit Level

For each PHY, set the 10BASE-T1L high level transmit operating mode request bit (AN_ADV_B10L_TX_LVL_HI_REQ) in the BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H) to 1 to advertise a request for 2.4 V p-p transmit level operation during autonegotiation. This bit can only be set if the ADIN2111 respective PHY has the ability to transmit in high voltage mode (B10L_TX_LVL_HI_ABLE = 1 in the 10BASE-T1L PMA status register).

See the Transmit Amplitude Advertisement section for more details.

Read Link Partner Advertised Transmit Level

For each PHY, the link partner advertised transmit information can be read from the transmit operating mode ability bit (AN_LP_ADV_B10L_TX_LVL_HI_ABL) and the link partner high level transmit operating mode request bit (AN_LP_ADV_B10L_TX_LVL_HI_REQ) in the BASE-T1 autonegotiation link partner base page ability register, Bits[47:32] (AN_LP_ADV_ABILITY_H) of the respective PHY. These bits are valid when autonegotiation completes (AN_COMPLETE = 1 in the BASE-T1 autonegotiation status register).

See the Transmit Amplitude Advertisement section for more details.

Completion of Autonegotiation

When autonegotiation completes on PHY 1 or PHY 2, the autonegotiation complete indication register bit (AN_LINK_GOOD) in the extra autonegotiation status register (AN_STATUS_EXTRA) is set to 1 on the respective PHY. This bit indicates the completion of the autonegotiation sequence and that the enabled PHY link is setting up or active.

When autonegotiation completes and the link is up, the autonegotiation complete register bit (AN_COMPLETE in the BASE-T1 autonegotiation status register) is set to 1, and the contents of the following registers are valid on the respective PHY:

- BASE-T1 autonegotiation advertisement registers:
  - BASE-T1 autonegotiation advertisement register, Bits[15:0] (AN_ADV_ABILITY_L)
  - BASE-T1 autonegotiation advertisement register, Bits[31:16] (AN_ADV_ABILITY_M)
  - BASE-T1 autonegotiation advertisement register, Bits[47:32] (AN_ADV_ABILITY_H)
- BASE-T1 autonegotiation link partner base page ability registers:
  - BASE-T1 autonegotiation link partner base page ability register, Bits[15:0] (AN_LP_ADV_ABILITY_L)
  - BASE-T1 autonegotiation link partner base page ability register, Bits[31:16] (AN_LP_ADV_ABILITY_M)
  - BASE-T1 autonegotiation link partner base page ability register, Bits[47:32] (AN_LP_ADV_ABILITY_H)

Link Status

The status of each PHY link can be determined by reading the link status register bit (AN_LINK_STATUS) in the BASE-T1 autonegotiation status register (AN_STATUS) of the respective PHY. This bit latches low.

When read as 1, this bit indicates that a valid link is established.

If this bit reads 0, the link failed since the last time it was read. This bit latches low. Therefore, if a 0 is read, this bit must be read

BRINGING UP 10BASE-T1L LINKS

a second time to determine if the link status has come up in the interim (see the Latch Low Registers section).

If the link is dropped, the autonegotiation process restarts automatically. Autonegotiation can be restarted by a request through a write to the autonegotiation restart bit (AN_RESTART) in the BASE-T1 autonegotiation control register (AN_CONTROL) of the respective PHY.

ON-CHIP DIAGNOSTICS

LOOPBACK MODES

Each of the two PHY cores on the ADIN2111 provides the following loopback modes:

- Physical medium attachment (PMA) loopback
- Physical coding sublayer (PCS) loopback
- MAC interface loopback
- MAC interface remote loopback
- MAC loopback
- Host processor loopback

These loopback modes test and verify various functional blocks within each PHY. The use of a frame generator and frame checkers allows completely self contained in-circuit testing of the digital and analog datapaths within each PHY core.

PMA Loopback

The PHY 1 and PHY 2 can be configured in PMA loopback mode. In that case, the MDI must be left open circuit, thereby transmitting into an unterminated connector or cable. In this mode, the signal transmitted from the respective ADIN2111 PHY is echoed back from the open 10BASE-T1L MDI. This test mode is an implementation of the PMA local loopback function defined in Subclause 146.5.6 of the IEEE Standard 802.3cg. Remove any cable connected to the MDI to improve the test mode accuracy.

If configured in PMA loopback mode, the respective PHY must be configured in forced link configuration mode (autonegotiation disabled). To enable PMA loopback mode, set the 10BASE-T1L PMA loopback enable bit (B10L_LB_PMA_LOC_EN) to 1 in the 10BASE-T1L PMA control register (B10L_PMA_CNTRL) of the respective PHY.

PCS Loopback

PCS loopback mode loops the transmit data back to the receiver within the PCS block at the input stage of the PHY 1 (respectively PHY 2) digital block. Setting the B10L_LB_PCS_EN bit to 1 in the 10BASE-T1L PCS control register (B10L_PCS_CNTRL) on PHY 1 (respectively PHY 2) enables PCS loopback mode on PHY 1 (respectively PHY 2).

When the PCS loopback mode is enabled on PHY 1 (respectively PHY 2), no signal is transmitted to the PHY 1 (respectively PHY 2) MDI pins.

MAC Interface Loopback

MAC interface loopback mode loops the data received on the ADIN2111 PHY 1 (respectively PHY 2) MAC interface back to the SPI host, and can therefore be used to verify MAC interface connectivity. Set the MAC_IF_LB_EN bit in the MAC interface loopbacks configuration register (MAC_IF_LOOPBACK) to 1 on PHY 1 (respectively PHY 2) to enable MAC interface loopback mode on PHY 1 (respectively PHY 2).

If the MAC_IF_LB_TX_SUP_EN bit in MAC_IF_LOOPBACK is set (enabled by default) on PHY 1 (respectively PHY 2), the transmission of the signal received on the PHY MAC interface is not transferred to the ADIN2111 PHY 1 (respectively PHY 2) core.

MAC Interface Remote Loopback

MAC interface remote loopback mode requires a link up with a remote PHY and enables looping of the data received on the ADIN2111 PHY 1 (respectively PHY 2) to the remote PHY. This linking allows a remote PHY to verify a complete link by ensuring that the PHY receives the proper data. Set the MAC_IF_REM_LB_EN bit in the MAC interface loopbacks configuration register (MAC_IF_LOOPBACK) to 1 on PHY 1 (respectively PHY 2) to enable MAC interface remote loopback mode.

If the MAC_IF_REM_LB_RX_SUP_EN bit in MAC_IF_LOOPBACK is set (set by default), the data received by the ADIN2111 PHY 1 (respectively PHY 2) from the MDI pins is not transferred to the ADIN2111 MAC.

MAC Loopback

MAC loopback mode loops the data received on the MAC transmit channel of Port 1 or Port 2 back to the SPI host.

MAC loopback mode can be enabled on PORT1 by setting the MAC loopback bit (P1_LOOPBACK_EN) to 1 in the P1 MAC loopback enable register (P1_LOOP).

MAC loopback mode can be enabled on PORT2 by setting the MAC loopback bit (P2_LOOPBACK_EN) to 1 in the P2 MAC loopback enable register (P2_LOOP).

Host Processor Loopback

Outside of the loopback modes associated with the PHY cores within the ADIN2111, the host processor can be used to create a full MAC loopback. In a full MAC loopback, whatever frame is received from the MAC is transmitted back to the MAC, as shown in Figure 10.

ON-CHIP DIAGNOSTICS

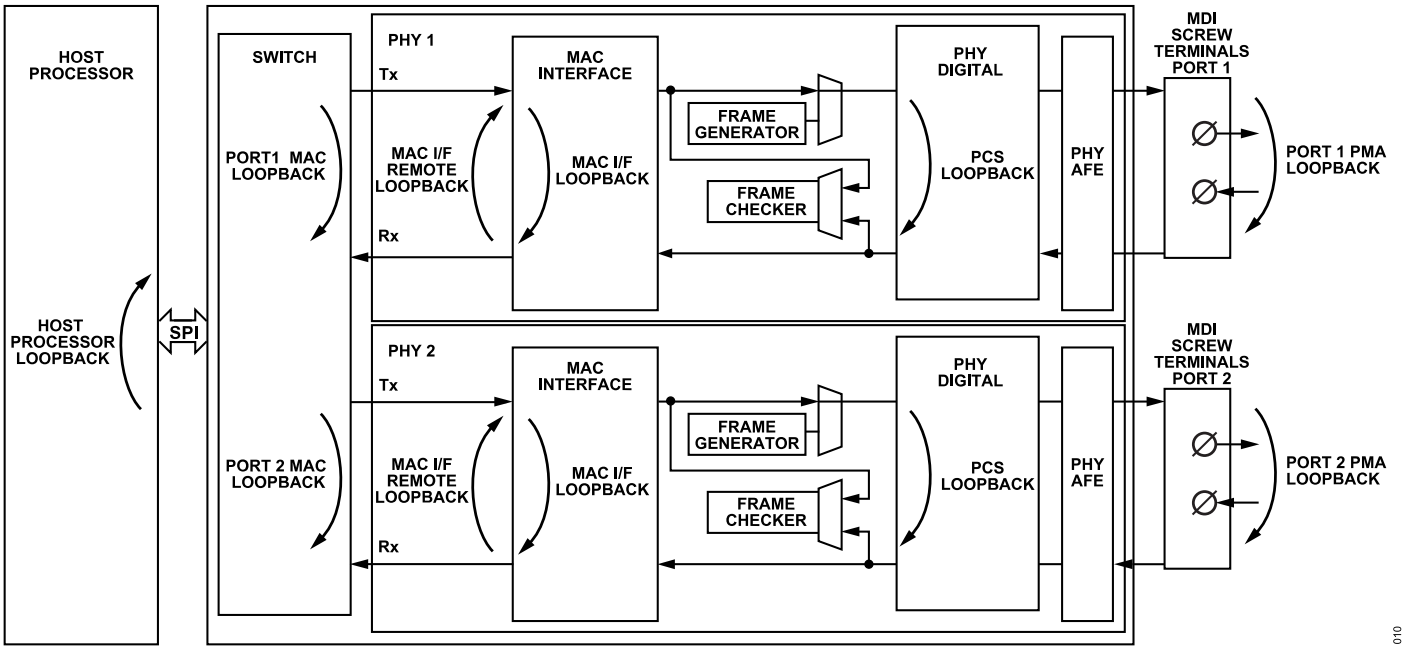

Figure 10. ADIN2111 Loopback Modes

FRAME GENERATOR AND CHECKER

The two PHYs on the ADIN2111 can be configured to generate frames and to check received frames (see Figure 11). The generating and checking functions can be used together or independently. If the ADIN2111 PHY 1 (respectively PHY 2) transmitted frames are looped back at the remote end, the frame checker on PHY 1 (respectively PH Y2) can be used to check the echoed self generated frames.

Frame Generator

When the frame generator is enabled, the MAC interface is ignored and the frame generator data is used for transmission on the MDI pins. To use the frame generator, the diagnostic clock must also be enabled using the CRSM_DIAG_CLK_EN bit in the CRSM diagnostics clock control register (CRSM_DIAG_CLK_CTRL).

The frame generator control registers configure the type of frames to be sent (for example, random data, all 1s), the frame length, and the number of frames to be generated.

The generation of the requested frames starts by enabling the frame generator by setting the FG_EN bit in the frame generator enable register (FG_EN).

When the generation of the frames completes, the frame generator done bit, FG_DONE, is set in the frame generator done register (FG_DONE).

Frame Checker

The frame checker is enabled by setting the frame checker enable bit (FC_EN) in the frame checker enable register (FC_EN). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY using the frame checker transmit select bit (FC_TX_SEL) in the frame checker transmit select register (FC_TX_SEL). The frame checker reports the number of frames received, CRC errors, and various frame errors. The frame checker frame counter registers and the frame checker error counter registers count these events.

Error Counters

The frame checker counts the number of CRC errors, and these errors are reported in the receive error count register (RX_ERR_CNT). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched copy of the receive frame counter register is available in the frame checker count higher register (FC_FRM_CNT_H) and the frame checker count low register (FC_FRM_CNT_L).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frames errors, and undersized frame errors.

The frame checker also counts frames with an odd number of nibbles in the frame, and counts packets with an odd number of nibbles in the preamble.

The frame checker also counts the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (SSD) state is entered.

ON-CHIP DIAGNOSTICS

FRAME GENERATOR AND CHECKER LINK TEST

Using two ADIN2111 devices, the user can configure a convenient, self contained validation setup of the PHY to PHY connection. Figure 11 shows an overview of how each device is configured. An external cable is connected between both devices, and PHY 1 is generating frames using the frame generator. PHY 2 has MAC interface remote loopback mode enabled using the MAC interface loopbacks configuration register (MAC_IF_REM_LB_EN).

See the following sequence for remote loopback used across two PHYs for self check purposes:

1. The ADIN2111-1 PHY 2 frames (frame generator) are sent over the 10BASE-T1L single pair cable.
2. The ADIN2111-2 PHY 1 receives frames on the MDI pins.
3. The ADIN2111-2 PHY 1 MAC interface loops the frame back.
4. The ADIN2111-2 PHY 1 frames (looped back) are sent over the 10BASE-T1L single pair cable.
5. ADIN2111-1 PHY 2 receives the ADIN2111-2 PHY 1 frames (looped back) on the MDI pins.
6. The ADIN2111-1 PHY 2 frame checker checks the received frames.

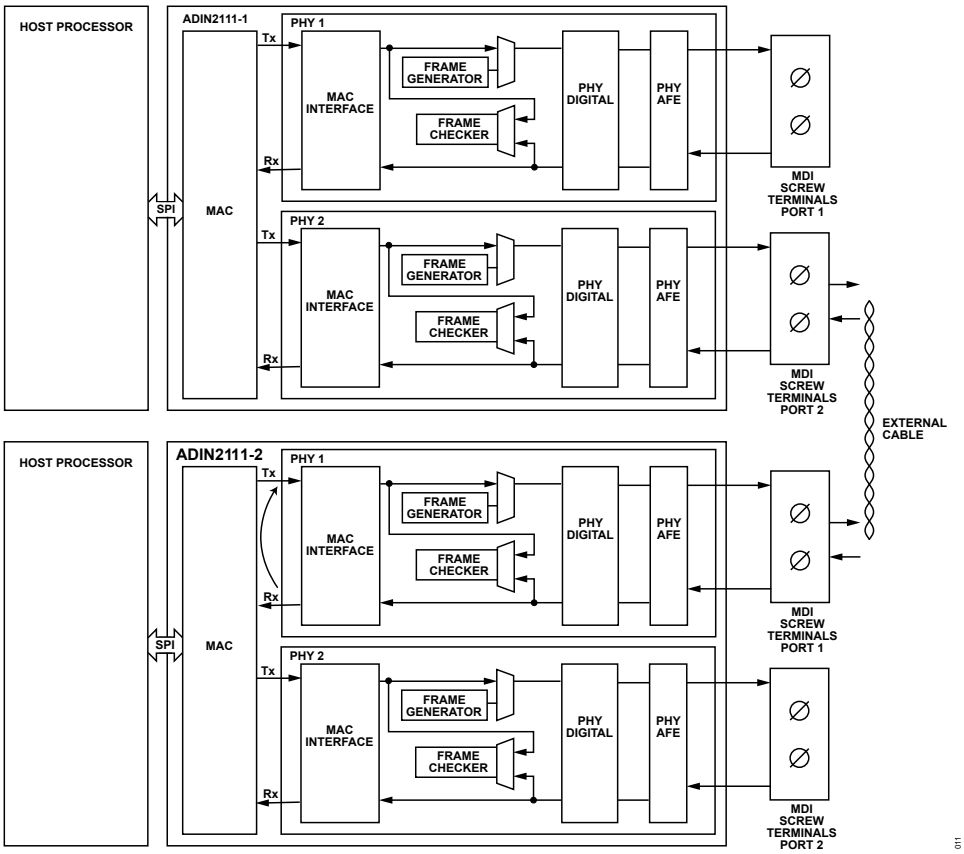

Figure 11. Remote Loopback Used Across Two PHYs for Self Check Purposes

ON-CHIP DIAGNOSTICS

TEST MODES

The ADIN2111 provides several test modes for each PHY as described in Subclause 146.5.2 from the IEEE 802.3cg-2019 standard that allows testing of the transmitter waveform, distortion, jitter, and droop. These test modes change only the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from the normal operation.

Additionally, the ADIN2111 supports the transmit disable mode as described in Subclause 45.2.1.186a.2.

Table 24. ADIN2111 Test Modes Summary

Test Mode	Description
PMA Test Modes (Subclause 146.5.2)	
Test Mode 1	Transmitter output voltage and timing jitter test mode. When this mode is selected, the ADIN2111 repeatedly transmits the data symbol sequence (+1, –1).
Test Mode 2	Transmitter output droop test mode. In this mode, the ADIN2111 transmits ten +1 symbols followed by ten −1 symbols. This sequence is repeated indefinitely.
Test Mode 3	Normal operation in idle mode test mode. In this mode, the ADIN2111 transmits as in a nontest operation and in the master data mode with the data set to normal interframe idle signals.
Transmit Disable Mode (Subclause 45.2.1.186a.2)	Both transmit and receive paths act like in normal operation mode, but only transmit 0 symbols. This mode can be used to measure the MDI return loss specified in Subclause 146.8.3.

Enable the PMA Test Mode 1 to Test Mode 3

Each of the ADIN2111 PHYs can be configured in one of the PMA test modes (Test Mode 1 to Test Mode 3) using the following procedure:

1. Enter software power-down mode by writing a 1 to the CRSM_SFT_PD bit in the software power-down control register (CRSM_SFT_PD_CNTRL).
2. Check that the ADIN2111 has entered software power-down mode by reading the CRSM_SFT_PD_RDY bit in the system status register (CRSM_STAT).
3. Disable autonegotiation by writing a 0 to the AN_EN bit in the BASE-T1 autonegotiation control register (AN_CONTROL).
4. Set autonegotiation forced mode by writing a 1 to the AN_FRC_MODE_EN bit in the autonegotiation force mode enable register (AN_FRC_MODE_EN).
5. Select the desired test mode by writing the appropriate value to the B10L_TX_TEST_MODE bits in the 10BASE-T1L test mode control register (B10L_TEST_MODE_CNTRL).
6. Exit software power-down mode by writing 0 to the CRSM_SFT_PD bit in the software power-down control register (CRSM_SFT_PD_CNTRL).

Table 25. PMA Test Modes Configuration

PMA Test Mode	B10L_TX_TEST_MODE, Bits[15:13] (Binary)
Test Mode 1	001
Test Mode 2	010
Test Mode 3	011

Enable Transmit Disable Mode

Each of the ADIN2111 PHYs can be configured in transmit disable mode using the following procedure:

1. Enter software power-down mode by writing a 1 to the CRSM_SFT_PD bit in the software power-down control register (CRSM_SFT_PD_CNTRL).
2. Check that the ADIN2111 has entered the software power-down mode by reading the CRSM_SFT_PD_RDY bit in the system status register (CRSM_STAT).
3. Disable autonegotiation by writing a 0 to the AN_EN bit in the BASE-T1 autonegotiation control register (AN_CONTROL).
4. Set autonegotiation forced mode by writing a 1 to the AN_FRC_MODE_EN bit in the autonegotiation force mode enable register (AN_FRC_MODE_EN).
5. Set the transmit disable mode by writing a 1 to the B10L_TX_DIS_MODE_EN bit in the 10BASE-T1L PMA control register (B10L_PMA_CNTRL).
6. Exit software power-down mode by writing 0 to the CRSM_SFT_PD bit in the software power-down control register (CRSM_SFT_PD_CNTRL).

TIME DOMAIN REFLECTOMETRY (TDR)

Given that the 10BASE-T1L compliant PHY enables communication over long cables, debugging a faulty cable can become costly and difficult without the right tools. To help with this, Analog Devices 10BASE-T1L products provide a TDR engine that enables cable fault detection, distance to fault, and cable length estimation.

The diagnostics solution is the combination of a highly accurate on-chip TDR engine and a set of algorithms that run on a host microcontroller, allowing maximum flexibility for a wide variety of cables and more advanced cable diagnostic capabilities.

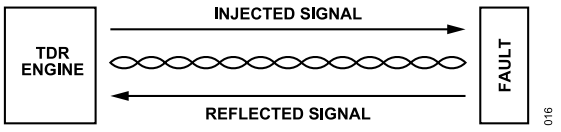

Figure 12. ADIN2111 TDR Engine

ON-CHIP DIAGNOSTICS

Fault Detection with the TDR Engine

The Analog Devices algorithm has a time resolution of 8.3 ns, which translates to a length resolution of less than 1 m and a maximum of 1600 m, with an accuracy of 2%.

This fault detector algorithm is capable of finding open and short fault conditions even when the ADIN2111 is physically connected to another PHY through their MDI, which implies that the link partner PHY is potentially transmitting DME pages. Traditional TDR methods struggle to find faults if other signal sources or noise is also present in the same link. This is not the case of the Analog Devices solution, which makes it suitable for debugging when there is no control over the remote end.

The fault detector algorithm is provided as a C-code library containing the high-level functions required for diagnostics. These functions have been optimized to not utilize any advanced processing so that they can be executed by any low-power microcontroller.

A single function call is sufficient to execute the fault detector. The function returns the type of fault and the distance to the fault in meters from the MDI connector.

TDR Offset Calibration

The library includes a function to calibrate the offset of the TDR measurement. This particular function in the library is useful given that different MDI circuits may introduce variable delays in the signal path, which can contribute to the offset of the length measurement. For instance, an isolation transformer on the MDI is highly likely to introduce a signal delay that corresponds to a couple of meters in length.

This calibration is not required to run the fault detector, and an average value is provided by default. However, it is recommended for short cables if accuracy is required. If this calibration is required, it can be done once in the lab for a specific MDI circuit implementation, and the offset value can then be stored in nonvolatile memory for future use.

To perform this calibration, the MDI port must be left open or shorted. No load or cable can be connected to the MDI port.

Cable Calibration

By default, the algorithm is optimized to support long reach cables compliant with the IEEE 802.3cg standard. However, given the wide variety of cable types, which have different insertion loss, return loss, and signal delay characteristics, the library includes a calibration function that optimizes the algorithm to operate with any cable, and estimates its nominal velocity of propagation (NVP) for more accurate length estimations. The length accuracy mainly depends on the accuracy of the NVP value.

To run this calibration, a cable with a known length must be attached to the MDI port, and its end must be left open or shorted. NVP values are generally between 0.5 and 0.9 and are a property of the construction of the cable. In general, an average NVP value of approximately 0.65 can be assumed. This calibration is not required to run the fault detector, unless higher length accuracy is needed or if nonstandard cables are utilized. This calibration can be done once in the laboratory for a given cable, and the values can be stored in nonvolatile memory.

Refer to the C-code driver for more information related to the usage of these functions.

Length/Distance to Fault Accuracy

The accuracy of the distance to a fault, or length measurements, mainly depends on the NVP value, which is determined by the accuracy of the cable length used to perform the NVP calibration.

Table 26 provides results for induced faults and distance-to-fault measurements for different cables and lengths. In all cases, the algorithm was successful finding the open or short conditions induced during the test. The NVP value for the Profibus PA cable used in this test was roughly estimated, and the same was used for the Cat5E and Cat6 cables.

Table 26. Length Estimation Error for Different Cables

Cable Type	Estimated Length (m)	Length Error (%)	Note
Fieldbus Type A - AWG 18	50.2	0.7	NVP calibrated
Fieldbus Type A - AWG 18	102.1	2.1	NVP calibrated
Fieldbus Type A - AWG 18	403.4	0.8	NVP calibrated
Fieldbus Type A - AWG 18	807.6	0.8	NVP calibrated
Fieldbus Type A - AWG 18	1045.3	1.0	NVP calibrated
Fieldbus Type A - AWG 18	1462.9	2.0	NVP calibrated
Cat5E	133.1	2.4	NVP not calibrated
Cat5E	244.4	1.8	NVP not calibrated
Cat6	73.6	5.1	NVP not calibrated
Cat6	137.2	5.6	NVP not calibrated

APPLICATIONS INFORMATION

SYSTEM LEVEL POWER MANAGEMENT

Transmit Level = 1.0 V p-p

The 1.0 V p-p transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. This mode supports intrinsic safe applications.

For applications where the ADIN2111 PHY 1 (respectively PHY 2) must operate in 1.0 V p-p transmit operating mode, the P1_TX2P4_EN (respectively P2_TX2P4_EN) pin signal must be tied high via a 4.7 kΩ resistor (see Figure 13). This configuration forces the ADIN2111 to only operate in 1.0 V p-p transmit operating mode and enables the ADIN2111 PHY 1 (respectively PHY 2) to operate from a signal supply voltage at a lower voltage rail (for example, 1.8 V), allowing the user to minimize power dissipation in the system.

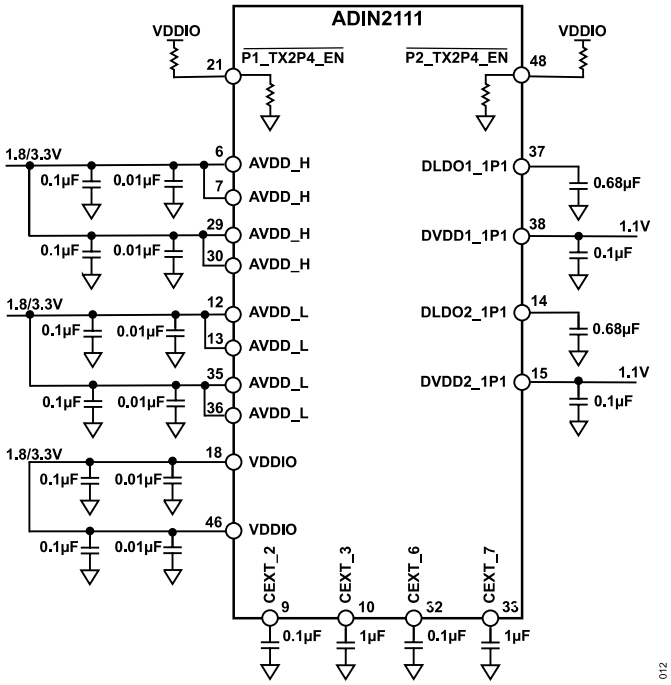

Figure 13. Supplies and Capacitors for Forced 1 V p-p Transmit Mode

Transmit Level = 2.4 V p-p

The higher transmit operating mode of 2.4 V p-p supports trunk applications and requires a higher AVDD_H supply voltage of 3.3 V. This mode can be used for longer cable lengths in industrial Ethernet environments with high noise levels.

For the ADIN2111 PHY 1 (respectively PHY 2) to be able to operate at 2.4 V p-p, the P1_TX2P4_EN (respectively P2_TX2P4_EN) pin signal must be held low (the pin has an internal pull-down resistor). This mode of operation still allows the 1.0 V p-p operating mode to be selected via SPI or autonegotiation.

Multiple Supplies Configuration

Figure 14 shows an overview of the proposed power configuration. Note that this configuration requires that AVDD_H = 3.3 V even if the link is established in 1.0 V p-p transmit operating mode via SPI or autonegotiation.

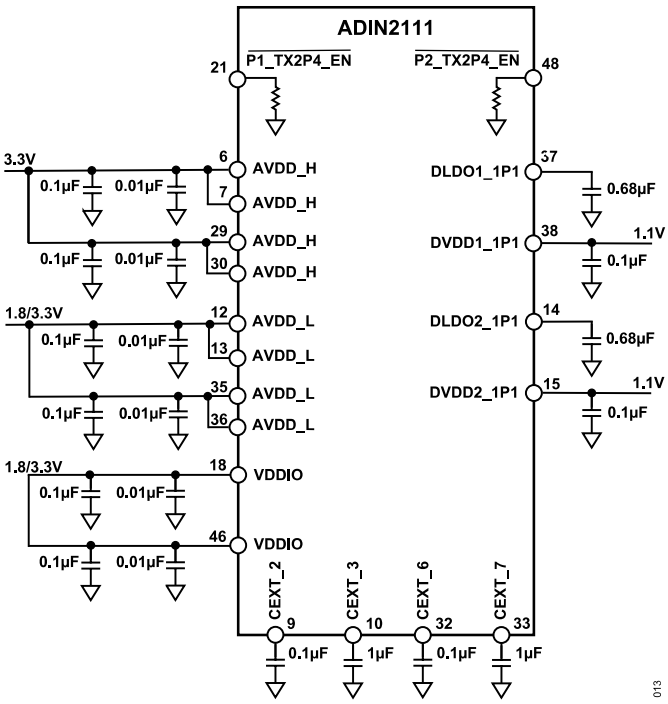

Figure 14. Supplies and Capacitors for Multiple Supply 2.4 V p-p and 1.0 V p-p Transmit Mode

Single-Supply Configuration

For single-supply operation, the same rail can be used to supply the ADIN2111 AVDD_H, AVDD_L, and VDDIO supply rails. The DVDDx_1P1 1.1 V rails can be derived internally or alternatively provided by an external 1.1 V rail. This configuration is shown in Figure 15.

APPLICATIONS INFORMATION

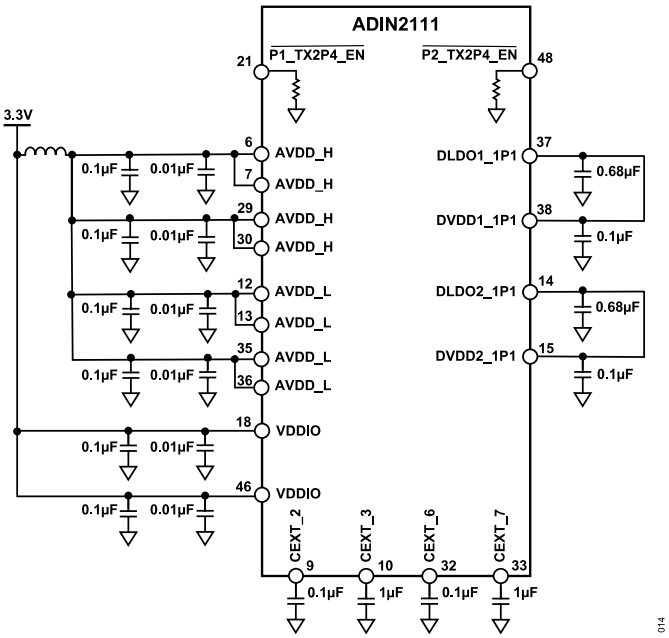

Figure 15. Supplies and Capacitors for Single-Supply 2.4 V p-p Transmit Mode

ETHERNET DAISY CHAIN, LINE, AND RING NETWORK TOPOLOGIES

The ADIN2111 is targeted at building automation and factory automation applications that deploy 10BASE-T1L in a daisy chain, line, or ring network topology. These network topologies significantly reduce the amount of cabling required when compared to a star network.

The ADIN2111 integrates two 10BASE-T1L PHY and a store and forward switch to provide a single chip, low power solution for adding devices to a daisy chain, line, or ring network topology. The ADIN2111 provides an industry standard SPI for the device connection. Using SPI eases the requirements for the host processor and gives the user more choices to optimize a device for power, cost, and performance.

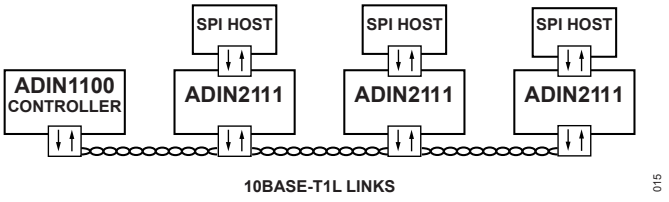

Figure 16. Daisy Chain Topology Using ADIN2111

LED CIRCUIT EXAMPLES

The LED_0 and LED_1 pins can be used in various circuit configurations depending on the LED polarity mode defined in the LED polarity register (LED_POLARITY). The circuits described in the Active High LED Polarity, Active Low LED Polarity, and Autosense Polarity sections provide examples for the following three polarity modes that are available for each LED:

- Active high
- Active low
- Autosense (default)

The output current for the LED_0 and LED_1 pins is 8 mA with VDDIO = 3.3 V (see the Specifications section for details). For higher current requirements, consider using the circuit described in the Transistor Controlled LED section.

Active High LED Polarity

In the active high configuration, the Px_LED_x pin can drive an external LED from the anode side. Select the R0 and R1 resistors to control the LED current (refer to the LED specifications in Table 1 for information). External pull-down resistors (R_{PD0} and R_{PD1}) with a value of 4.7 kΩ are recommended.

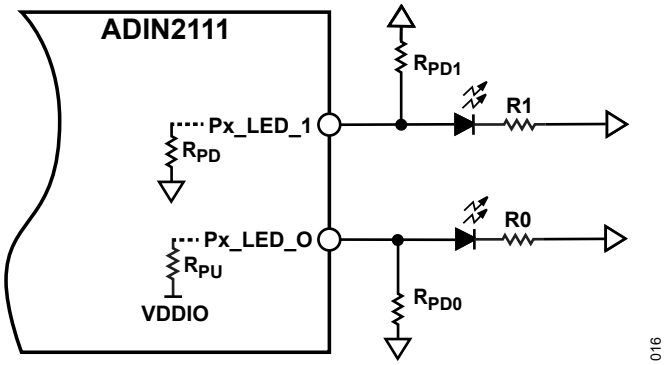

Figure 17. Active High LED Polarity Configuration

Active Low LED Polarity

In the active low configuration, the Px_LED_x pin can drive an external LED from the cathode side. Select the R0 and R1 resistors to control the LED current (refer to the LED specifications in Table 1 for information). External pull-up resistors (R_{PU0} and R_{PU1}) with a value of 4.7 kΩ are recommended.

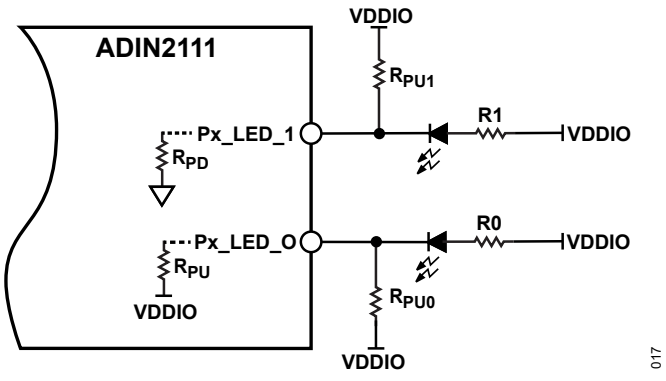

Figure 18. Active Low LED Polarity Configuration

APPLICATIONS INFORMATION

Transistor Controlled LED

Figure 19 displays a typical configuration where the LED current required is higher than what the Px_LED_0 and Px_LED_1 pins can supply. The circuit operates using the active high LED mode. An external transistor, such as an N channel metal-oxide semiconductor field effect transistor (MOSFET), can be used. The transistor must be selected so that the gate input capacitance is not sinking current above the maximum rating of the Px_LED_x pin during the actuation. Refer to the transistor technical specifications for information. If required, the inrush current can be reduced by placing a resistance between the transistor gate and the ADIN2111 pin, and/or adding a parallel capacitor between the GND and the Px_LED_x pin. The additional resistor and capacitor values must be defined based on the transistor selection.

Select the R0 and R1 resistors to control the LED current (refer to the selected LED and transistor specifications of the manufacturer for information).

External pull-down resistors (R_{PD0} and R_{PD1}) with a value of 4.7 kΩ are recommended. In Figure 19, VCC is the power supply used to supply the LEDs.

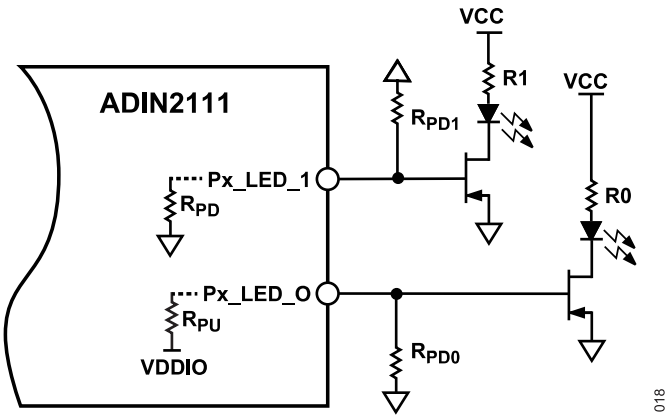

Figure 19. Transistor Controlled LED Configuration

Autosense Polarity

In autosense mode, the polarity of the LED is automatically detected during power-up, hardware reset, or software reset. LED_0 (internal pull-up) and LED_1 (internal pull-down) have different autosense behaviors due to their internal pull-up and pull-down configurations. Use one of the configurations described in the Active High LED Polarity, Active Low LED Polarity, and Transistor Controlled LED sections so that the two LEDs can be controlled the same way.

COMPONENT RECOMMENDATIONS

The ADIN2111 requires an external 25 MHz clock, which can be sourced from an external crystal oscillator or an external single-ended clock.

The signal voltage on the XTAL_I/CLK_IN pin (V_{CLK_IN}) must be a sine or filtered square wave signal with a peak-to-peak voltage range from 0.8 V to 2.5 V. For the single-ended clock option, a V_{CLK_IN} with a 1.0 V p-p swing is recommended to achieve best performance.

Various circuit configurations are proposed in the following sections. A common circuit topology can be used across these options with a change to the passive component values.

Note that during normal operation, a 25 MHz reference clock generated from the external clock source input (a crystal or 25 MHz external single-ended clock) is provided on the CLK25_REF output pin. This pin can be used as a reference clock for other circuits, such as another 10BASE-T1L device. CLK25_REF is disabled in reset mode.

External Crystal Oscillator

The typical connection for an external crystal (XTAL) is shown in Figure 20.

To ensure minimum current consumption and minimize stray capacitance, make connections between the crystal, capacitors, and ground as close to the ADIN2111 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

The crystal load capacitance (C_L) is defined by the crystal vendor. C_{PCB1} and C_{PCB2} are the parasitic capacitance between the XTAL_I/CLK_IN and XTAL_O and the ground plan beneath, respectively. C_{X1} and C_{X2} are the two external load capacitors required for the oscillator to operate.

Assuming the following:

- $C_{PCB1} \approx C_{PCB2} \approx C_{PCBx}$
- $C_{X1} \approx C_{X2} \approx C_{Xx}$

Then, $C_{Xx} = 2 \times C_L - C_{PCBx} - 3$ pF

Choose precision capacitors for C_{Xx} with low appreciable temperature coefficient to minimize frequency errors.

To ensure minimum current consumption and to minimize stray capacitance, make the connections between the crystal, capacitors, and ground as close to the ADIN2111 as possible.

APPLICATIONS INFORMATION

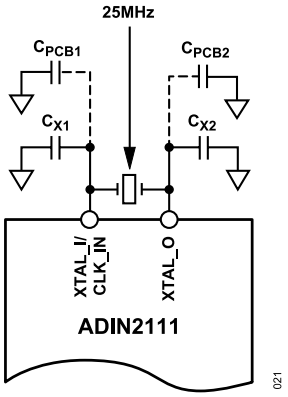

Figure 20. Crystal Oscillator Connection

External 25 MHz Clock Input

The clock source must be a dc-coupled with the ADIN2111 XTAL_I/CLK_IN pin input, and the XTAL_O pin must be left open circuit.

With 0.8 V ≤ V_{CLK_IN} p-p ≤ 2.5 V, the following results:

- For 0.8 V ≤ V_S p-p ≤ 1.0 V, the following is true:
  - R1 = 50 Ω
  - R2 is not required
- For 1.0 V < V_S p-p < 1.8 V, the following is true:
  - For best performance, set V_{CLK_IN} to 1.0 V p-p
  - 500 Ω ≤ R1 ≤ 2 kΩ
  - 1 kΩ ≤ R2 ≤ 2 kΩ
  - V_S p-p – V_{CLK_IN} p-p > 0.2 V
  - $R2 = \frac{V_{CLK_IN}\,p-p \times R1}{V_S\,p-p - V_{CLK_IN}\,p-p}$
- For 1.8 V ≤ V_S p-p, the following is true:
  - R1 = 2 kΩ
  - R2 = 2 kΩ

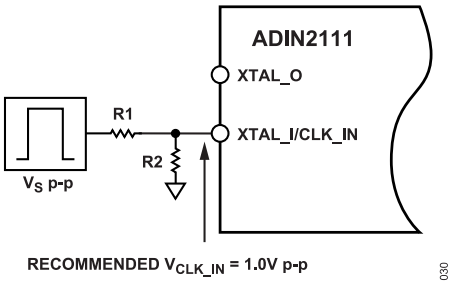

Figure 21. External 25 MHz Clock Input Circuit

Table 27. R1 and R2 Values for Different V_S p-p Values with V_{CLK_IN} = 1 V p-p

V_S (V p-p)	R1	R2
1.0	50 Ω	Not applicable
1.2	500 Ω	2.5 kΩ
1.8	2 kΩ	2 kΩ
2.2	2 kΩ	2 kΩ

Table 27. R1 and R2 Values for Different V_S p-p Values with V_{CLK_IN} = 1 V p-p (Continued)

V_S (V p-p)	R1	R2
2.5	2 kΩ	2 kΩ
2.8	2 kΩ	2 kΩ
3.0	2 kΩ	2 kΩ
3.3	2 kΩ	2 kΩ

ELECTROMAGNETIC COMPATIBILITY (EMC) AND ELECTROMAGNETIC IMMUNITY (EMI)

The ADIN2111 was tested at the system level for EMC and EMI. Table 28 summarizes the results.

Table 28. EMC/EMI Tests Conducted on ADIN2111 at System Level

EMC/EMI Test	Withstand Threshold/Class
IEC 61000-4-4 EFT	±4 kV
IEC 61000-4-2 ESD (contact discharge)	±4 kV
IEC 61000-4-2 ESD (air discharge)	±8 kV
IEC 61000-4-5 Surge	±4 kV
IEC 61000-4-6 Conducted Immunity	10 V/m
IEC 61000-4-3 Radiated Immunity	Class A
EN 55032 Radiated Emissions	Class B

SWITCH SPI

SPI

Overview

The ADIN2111 register interface is via a 4-wire SPI consisting of the following pins: SCLK, $\overline{CS}$, SDI, and SDO/SPI_CFG0.

The possible access permissions of the registers are as follows:

- R/W: read/write
- R: read only
- W: write only
- R/W1C: read/write 1 to clear

The ADIN2111 also allows access to the PHY registers via an SPI to MDIO master bridge. See the SPI Access to the PHY Registers section.

The following registers have additional access permissions:

- R LL: read only, latch low
- R LH: read only, latch high
- R/W SC: read/write, self clear

Generic SPI Protocol

The generic SPI protocol is detailed in Table 29 to Table 36. The protocol is determined by the hardware configuration pins. The register map is organized as a 32-bit map, and all accesses are in multiples of 32-bit words. Both single and burst access in multiples of 32-bit words is supported. The MSB of the data is transmitted first.

The R/W and TA fields are defined as follows:

- R/W: read/write
  - 0: read
  - 1: write
- TA: turn around

Burst writes and reads must be in multiples of 4 bytes. The last word (4 bytes) written can contain between one byte and four bytes of valid data. However, TX_FSIZE is still written with the original frame size + 2 bytes for the frame header (see Figure 22). For example, to transmit a 65-byte frame that is prepended with a 2-byte header, 67 is written to TX_FSIZE, but 68 bytes are transferred over SDI. The last byte is not used.

It is possible to enable a CRC on the SPI protocol via a hardware configuration pin on power-up. This 8-bit CRC uses the polynomial $x^8 + x^2 + x + 1$ seeded with 0x0, and provides up to 3-bit error detection. The 8-bit CRC is included for every control and data transaction after the ADDR bits, and then after every 32-bit data-word for every control transaction. There is no 8-bit CRC after each 32-bit data-word in data transactions because Ethernet frames include their own 32-bit CRC.

Table 29. Control Write Transaction

	MSB							LSB
	D47	**D46**	**D45**	**D44 to D32**	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**
SDI	1	0	R/W	ADDR[12:0]	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]

Table 30. Control Read Transaction

	MSB								LSB
	D55	**D54**	**D53**	**D52 to D40**	**D39 to D32**	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**
SDI	1	0	R/W	ADDR[12:0]	TA[7:0]	0	0	0	0
SDO						DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]

Table 31. Burst Write Transaction (Control or Data)

	MSB											LSB
	D79	**D78**	**D77**	**D76 to D64**	**D63 to D56**	**D55 to D48**	**D47 to D40**	**D39 to D32**	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**
SDI	1	0	R/W	ADDR[12:0]	DATA0[31:24]	DATA0[23:16]	DATA0[15:8]	DATA0[7:0]	DATA1[31:24]	DATA1[23:16]	DATA1[15:8]	DATA1[7:0]

Table 32. Burst Read Transaction (Control or Data)

	MSB												LSB
	D87	**D86**	**D85**	**D84 to D72**	**D71 to D64**	**D63 to D56**	**D55 to D48**	**D47 to D40**	**D39 to D32**	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**
SDI	1	0	R/W	ADDR[12:0]	TA[7:0]	0	0	0	0	0	0	0	0
SDO						DATA0 [31:24]	DATA0 [23:16]	DATA 0 [15:8]	DATA0 [7:0]	DATA1 [31:24]	DATA1 [23:16]	DATA1 [15:8]	DATA1 [7:0]

SWITCH SPI

Table 33. Control Write Transaction with CRC

	MSB								LSB
	D102	D101	D101	D100 to D89	D88 to D80	D79 to D48	D47 to D40	D39 to D8	D7 to D0
SDI	1	0	R/W	ADDR[12:0]	CRC[7:0]	DATA0[31:0]	CRC[7:0]	DATA1[31:0]	CRC[7:0]

Table 34. Control Read Transaction with CRC

	MSB									LSB
	D110	D109	D108	D107 to D96	D95 to D88	D87 to D80	D79 to D48	D47 to D40	D39 to D8	D7 to D0
SDI	1	0	R/W	ADDR[12:0]	CRC[7:0]	TA[7:0]	0	0	0	0
SDO							DATA0[31:0]	CRC[7:0]	DATA1[31:0]	CRC[7:0]

Table 35. Data Write Transaction with CRC

	MSB						LSB
	D86	D85	D84	D83 to D71	D71 to D64	D63 to D32	D31 to D0
SDI	1	0	R/W	ADDR[12:0]	CRC[7:0]	DATA0[31:0]	DATA1[31:0]

Table 36. Data Read Transaction with CRC

	MSB								LSB
	D94	D93	D92	D91 to D80	D79 to D72	D71 to D64	D63 to D32	D31 to 0	
SDI	1	0	R/W	ADDR[12:0]	CRC[7:0]	TA[7:0]	0	0	
SDO							DATA0[31:0]	DATA1[31:0]	

The generic SPI protocol is half duplex. Therefore, it is not possible to write frame data into the MAC_TX register and read from the MAC_RX register at the same time. Because of this, the SPI SCLK frequency must be 25 MHz to achieve full duplex transmissions on Ethernet at 10 Mbps.

MAC Frame: Transmit and Receive

The 2-byte frame header shown in Table 37 is appended to all transmitted and received frames. This frame header always precedes the frame data (see Figure 22).

Time Stamp Capture

On receive, if TIME_STAMP_PRESENT is asserted, an additional 4-byte or 8-byte time stamp is provided after the 2-byte header in Table 37 and before the data frame. This time stamp can then be stored or discarded by software when reading the receive FIFO.

On transmit, if EGRESS_CAPTURE is set other than 00, the ADIN2111 captures the time stamp of the transmitted frame into the respective TTSCxH and TTSCxL registers for Port 1, and P2_TTSCxH and P2_TTSCxL for Port 2.

To enable the time stamp capture signal pin, enable the P1_LED_0 or TEST_1 pins to be muxed as the time stamp input pin using the DIGIO_TSCAPT_PINMUX bits field in the Pin Mux Configuration 1 register (DIGIO_PINMUX).

The time stamp counter can be enabled by setting TS_EN (TS_CFG register) to 1 and setting FTSE (CONFIG0 register) to 1.

Time Stamp Timer Output

The ADIN2111 supports a TS_TIMER output signal. TS_TIMER can be started at a defined time relative to the nanoseconds counter. The TS_TIMER counter start time register (TS_TIMER_START) is used to set the start time. TS_TIMER then toggles based on the high and low times configured in high period for the TS_TIMER register (TS_TIMER_HI) and low period for the TS_TIMER register (TS_TIMER_LO).

Use the following sequence to enable the TS_TIMER output:

1. Configure the P1_LED_0 pin to the TS_TIMER function using the LED control register (LED_CNTRL).
2. To change the default value of the TS_TIMER from 0 to 1, write 1 to TS_TIMER_DEF in the timer configuration register (TS_CFG). TS_TIMER immediately toggles from 0 to 1.
3. Write to the TS_TIMER_HI and TS_TIMER_LO bits to set the required high time and low time for the TS_TIMER output.
4. Configure the quantization error correction register (TS_TIMER_QE_CORR) to set the required quantization error correction.

SWITCH SPI

5. Write a start time to the TS_TIMER_START register. When the nanoseconds counter matches this value, TS_TIMER starts to toggle.
6. To stop TS_TIMER, write 1 to the TS_TIMER_STOP bit in TS_CFG. TS_TIMER returns to the default value as set by TS_TIMER_DEF bit in TS_CFG. To start the timer again, write to the TS_TIMER_START register.

Note that If P1_LED_0 is used as the TS_TIMER output, the default value is dependent on the P1_LED_0 polarity set by the LED0_POLARITY bit field.

Transmit Frame over SPI

The following sequence must be followed when using the generic SPI protocol in store and forward mode (the ADIN2111 operates in cut through mode on the SPI by default):

1. Verify that there is space for the frame by reading the transmit FIFO space register. The internal MAC internally appends a 2-byte size field to the frame in the FIFO. Therefore, ensure that there is sufficient space for the Ethernet frame plus the 2-byte header and 2-byte size field.
2. Write the size of the frame in bytes, including the 2-byte header to the MAC transmit frame size register. If the host appended a frame check sequence (FCS) to the frame, this is also included in the size.
3. Write the frame data including the 2-byte frame header to the transmit FIFO using the MAC transmit register. The first byte for transmission is written to TXD, Bits[31:24]. The full frame can be written in a single burst or split up into multiple smaller burst writes. The burst write data must always be in multiples of four bytes. That is, the last word (four bytes) can contain between one byte and four bytes of valid data.
4. When the end of frame (EOF) byte of a frame is read from the transmit FIFO, the bit transmit ready asserts, and an interrupt triggers if the TX_RDY_MASK is set.

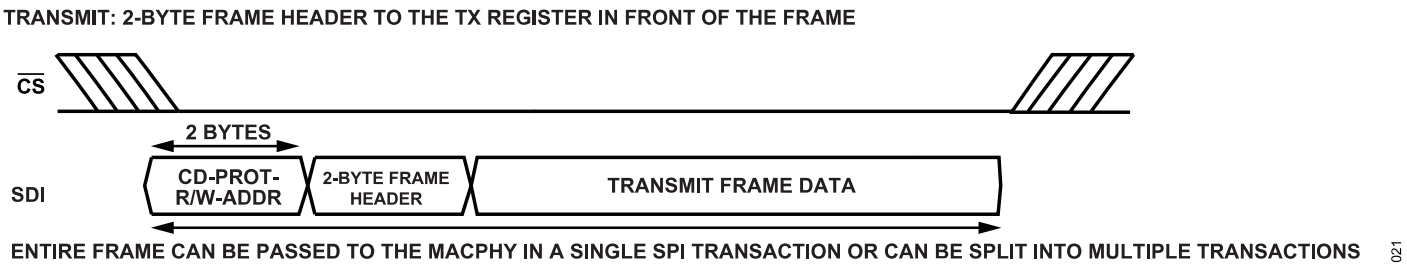

Figure 22. MAC Frame: Transmit

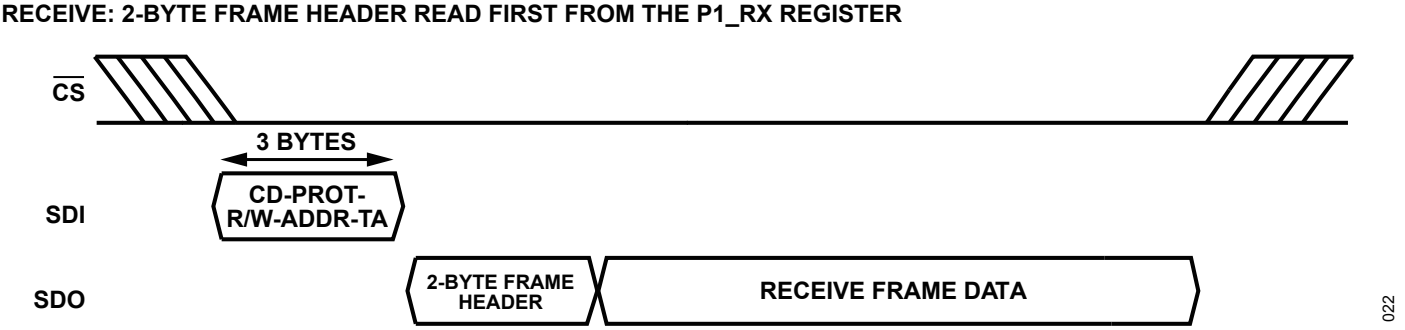

Figure 23. MAC Frame: Receive

SWITCH SPI

Table 37. Frame Header

D15 to D11	D10	D9 to D8	D7 to D6	D5 to D4	D3	D2	D1	D0
Reserved	Priority	Reserved	EGRESS_CAPTURE	Reserved	TIME_STAMP_PARITY	TIME_STAMP_PRESENT	Reserved	Port

See the following definitions:

- Priority: indicates which priority queue the frame was received from. Not used on transmit. Set 0 in transmitted frames.
- EGRESS_CAPTURE: capture an egress time stamp into the host readable egress time registers, as follows:
  - 00: no action.
  - 01: capture in the pair of the TTSCAL and TTSCAH registers. The TTSCAA bits in the STATUS0 register assert when captured.
  - 10: capture in the pair of the TTSCBL and TTSCBH registers. The TTSCAB bits in the STATUS0 register assert when captured.
  - 11: capture in the pair of the TTSCCL and TTSCCH registers. The TTSCAC bits in the STATUS0 register assert when captured.
- TIME_STAMP_PARITY: odd parity for the appended time stamp. Not used on transmit. Set to 0 in transmitted frames.
- TIME_STAMP_PRESENT: on receive, the first four bytes or eight bytes of data contain the time stamp for the frame. Not used on transmit. Set to 0 in transmitted frames.
- Port: on transmit, this bit indicates the destination port of the frame to be transmitted. On receive, it indicates the source port.
  - 0: Port 1
  - 1: Port 2
- Reserved: always set to 0.

Receive Frame over SPI

The following procedure (which applies to Port 1 and Port 2) must be followed to receive an Ethernet frame when using the generic SPI protocol in store and forward mode (the ADIN2111 operates in store and forward mode by default):

1. Set the Px_RX_RDY_MASK bit to 0 to enable an interrupt when a full frame is received.
2. If the Px_RX_RDY bit is asserted, read the MAC receive frame size register to determine the size of the received frame.
3. Read the frame via the MAC receive register. It is possible to burst read the entire frame or split it up into multiple smaller burst reads. The first byte of the received frame is returned in Px_RX, Bits[31:24]. The burst read transaction must be a multiple of four bytes. Some of the last four bytes are padded with 0s if the frame is not a multiple of four bytes in size.
4. Read Px_RX_RDY again. If the value of the bit is 1, another frame is available to read. Repeat from Step 3.

Cut Through

The generic SPI protocol supports cut through mode for transmit operations.

Before transmitting any frames, write 1 to the transmit cut through enable bits.

The threshold at which the frame transmit starts can be modified via the host transmit start threshold in cut through bit (HOST_TX_THRESH) in the transmit threshold register (TX_THRESH). This bit a default value of 1. Therefore, by default, transmit starts immediately on writing to the host transmit FIFO.

To ensure that the frame transmission does not under run, the host transmit FIFO has to be written at a rate greater than 10 Mbps. If the frame under runs, the host transmit under run error bit asserts.

Generic SPI Errors
Generic SPI CRC Error

If an SPI CRC error occurs on a write to a register, the register is not written.

If the write is to the transmit register, the transmit FIFO is missing data and must be cleared by the host. Similarly, a read of the receive register has missing data in the receive frame, and the FIFO must be cleared.

If the errored transaction was a write to a configuration register, the SPI host must issue the write again. If the software does not know which configuration, reset the MAC by writing the RST_MAC_ONLY keys to the SOFT_RST register.

Generic SPI Transmit Protocol Error (TXPE)

TXPE asserts when the TX_FSIZE register is written, but the MAC still expects further writes to the transmit register related to the previous frame size written to the TX_FSIZE register. This error does not occur in the normal operation and indicates an issue with the software driver, for example, two consecutive writes to the TX_FSIZE register without any writes to the transmit register.

In response to the assertion of TXPE, the host must clear the transmit FIFO.

OPEN Alliance SPI Protocol

The OPEN Alliance SPI protocol Version 1.0 can transfer data over the SPI using full duplex operation, achieving a 10-Mbps bidirectional frame transfer with an SPI clock frequency in the region of 12 MHz to 16 MHz or greater.

SWITCH SPI

The ADIN2111 supports the following OPEN Alliance SPI capabilities. See the supported capabilities register (CAPABILITY) for more details:

- Transmit FCS validation
- Cut through
- IEEE 1588 time stamp capture on transmit and receive
- Minimum supported chunk size is 8 bytes

The OPEN Alliance SPI protocol defines two types of transactions: data transactions for Ethernet frame transfers, and control transactions for register read/write operations.

A chunk is the basic element of data transactions, and it is composed of four bytes of overhead plus the configured payload size.

Data transactions consist of an equal number of transmit and receive chunks. Chunks in both transmit and receive directions may or may not contain valid frame data independent from each other, allowing for the simultaneous transmission and reception of different length frames. The data header of the chunk in transmit frames, and the data footer in receive frames, indicate which bytes of the payload contain valid frame data. For full information on the OPEN Alliance SPI protocol used by the ADIN2111, refer to OPEN Alliance 10BASE-T1x MACPHY serial interface Version 1.0.

Note that $\overline{CS}$ must be deasserted between data transactions and control transactions, as shown in Figure 24.

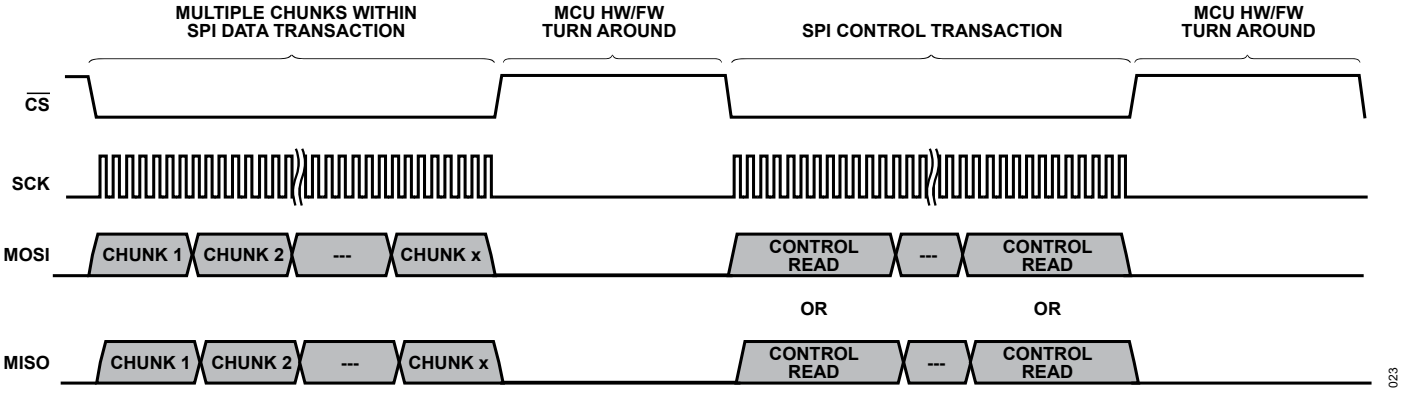

Figure 24. Ethernet Data Frame Transfer Followed by Control Transfer

SWITCH SPI

Data Chunks

Transmit data chunks consist of a 4-byte header followed by the transmit data chunk payload, as shown in Figure 25.

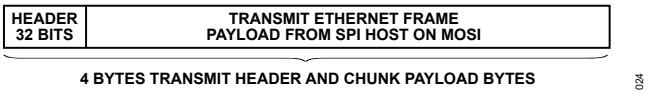

Figure 25. Transmit Data Chunk

Receive data chunks consist of the receive data chunk payload followed by a 4-byte footer, as shown in Figure 26.

Figure 26. Receive Data Chunk

The default size of the data chunk payload is 64 bytes. This size can be configured to 8 bytes, 16 bytes, 32 bytes, or 64 bytes via the chunk payload selector bits. The data chunk size must be configured before enabling data transmission or reception. Therefore, when the data chunk size is configured, it must not be changed without resetting the ADIN2111.

Data Chunk Transactions

Data transactions consist of 1 to N chunks on SDO and SDI. The 4-byte data header occurs at the beginning of each transmit data chunk on SDO, and the 4-byte data footer occurs at the end of each data chunk on SDI. These headers and footers contain the information needed to determine the validity and location of the transmitted and received frames within the data chunk payload. The Ethernet frames start at any 32-bit aligned word within the payloads, as shown in Figure 27 and Figure 28.

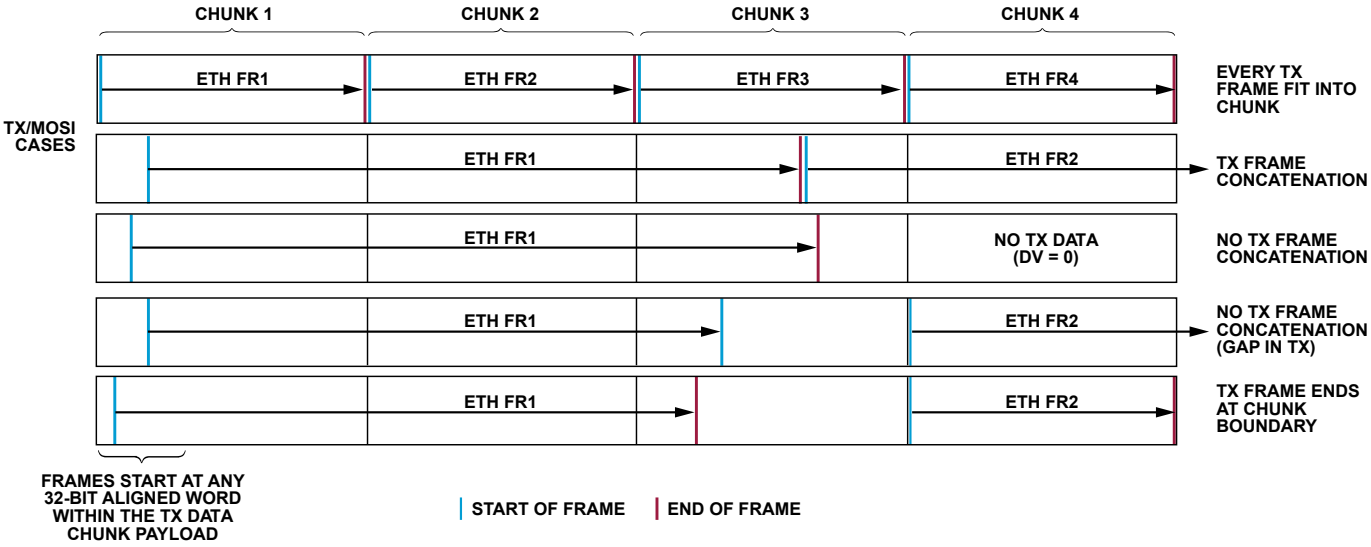

Figure 27. Transmit Data Chunk Cases

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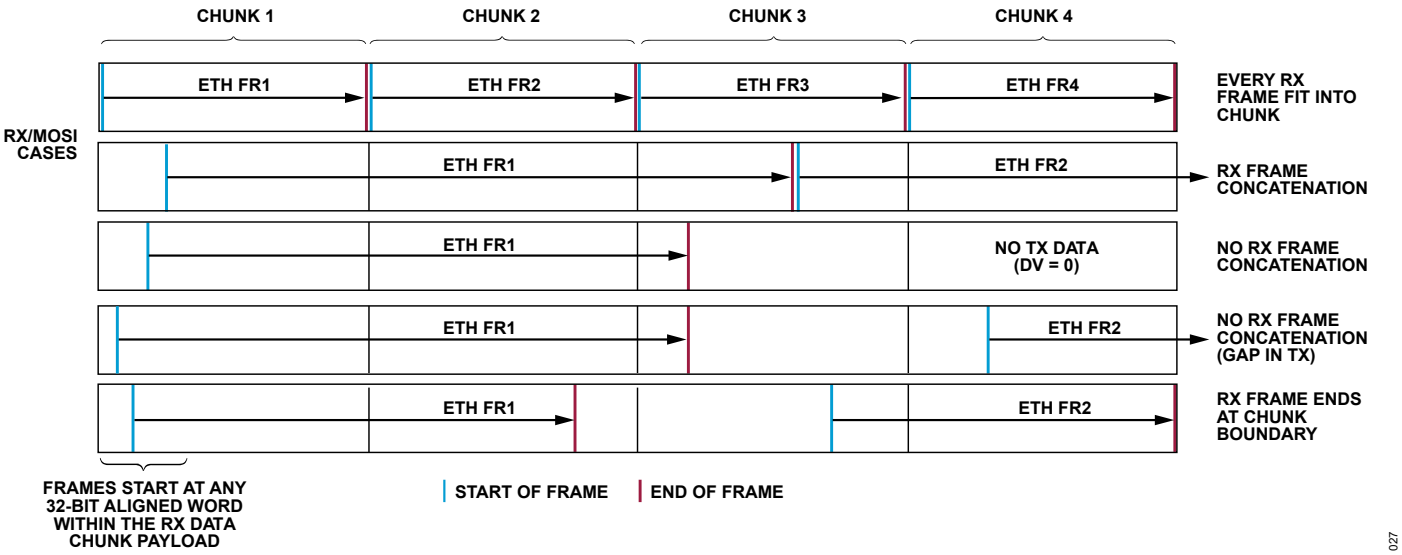

Figure 28. Receive Data Chunk Cases

Transmit Data Header

Table 38. Transmit Data Header

D31	D30	D29	D28 to D24	D23 to D22	D21	D20	D19 to D16	D15	D14	D13 to D8	D7 to D6	D5 to D1	D0
1	SEQ	NORX	RSVD	VS	DV	SV	SWO	RSVD	EV	EBO	TSC	RSVD	P

See the following definitions:

- SEQ: data chunk sequence. The sequence functionality is not supported by the ADIN2111. This bit must be set to 0.
- NORX: no receive flag. The SPI host can set this bit to indicate to the ADIN2111 that it does not process receive frame data that is in the current receive data chunk. For normal operation, set NORX to 0 to indicate that it accepts and processes any receive frame data within the current chunk.
- VS: vendor specific bits.
  - VS[1]: unused, to be set to 0 by the host.
  - VS[0]: frame destination port.
    - 0: frame destination is Port 1.
    - 1: frame destination is Port 2.
- DV: data valid flag. The SPI host uses this bit to indicate if the current chunk contains valid transmit data (DV = 1) or not. When this bit is 0, the ADIN2111 ignores the chunk payload.
- SV: start valid flag. When this bit is 1, the beginning of an Ethernet frame is present in the current transmit data chunk payload. Do not confuse the SV bit with the start of frame delimiter (SFD) byte described in IEEE Standard 802.3.
- SWO: start word offset. When SV is 1, this field contains the 32-bit word offset into the transmit data chunk payload that points to the start of the new Ethernet frame. If SV is 0, the host must write this field as 0.
- EV: end valid flag. When this bit is 1, the end of an Ethernet frame is present in the current transmit data chunk payload.
- EBO: end byte offset. When EV is 1, this field contains the byte offset into the transmit data chunk payload that points to the last byte of the Ethernet frame to transmit. If EV is 0, the host must write this field as 0.
- TSC: time stamp capture. Request a time stamp capture when the frame is transmitted onto the network. See the following:
  - 00: no action.
  - 01: capture in the pair of the TTSCAL and TTSCAH registers. The TTSCAA bits in the STATUS0 register assert when captured.
  - 10: capture in the pair of the TTSCBL and TTSCBH registers. The TTSCAB bits in the STATUS0 register assert when captured.
  - 11: capture in the pair of the TTSCCL and TTSCCH registers. The TTSCAC bits in the STATUS0 register assert when captured.
- P: parity. The parity bit is calculated over the transmit data header. The method is odd parity.
- RSVD: reserved. Always set to 0.

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Receive Data Footer

Table 39. Receive Data Footer

D31	D30	D29	D28 to D24	D23 to D22	D21	D20	D19 to D16	D15	D14	D13 to D8	D7	D6	D5 to D1	D0
EXST	HDRB	SYNC	RCA	VS	DV	SV	SWO	FD	EV	EBO	RTSA	RTSP	TXC	P

See the following definitions:

- EXST: extended status. This bit is set when any bit in the STATUS0 or STATUS1 registers is set and not masked.
- HDRB: received header bad. When this bit is set, the ADIN2111 has received a control or data header with a parity error.
- SYNC: configuration synchronized flag. This field reflects the state of the SYNC bit in the CONFIG0 register. When 0, this bit indicates that the ADIN2111 configuration may not be as expected by the SPI host. Following configuration, the SPI host sets the corresponding bit in the configuration register, which is reflected in this field.
- RCA: receive chunks available. The RCA field indicates the minimum number of additional receive data chunks of frame data that are available for reading beyond the current one. This field is 0 when there is no more receive frame data pending in the buffer of the ADIN2111 to be read.
- VS: vendor specific.
  - VS[1]: priority of the received frame.
    - 0: frame received via the low priority queue.
    - 1: frame received via the high priority queue.
  - VS[0]: port number for received frame.
    - 0: frame received from Port 1.
    - 1: frame received from Port 2.
- DV: data valid flag. The SPI host uses this bit to indicate if the current chunk contains valid transmit data (DV = 1) or not. When this bit is 0, the SPI host ignores the chunk payload.
- SV: start valid flag. When this bit is 1, the beginning of an Ethernet frame is present in the current transmit data chunk payload. Do not confuse the SV bit with the SFD byte described in IEEE Standard 802.3.
- SWO: start word offset. When SV is 1, this field contains the 32-bit word offset into the receive data chunk payload that points to the start of the new Ethernet frame. When a receive time stamp is added to the beginning of the received frame (RTSA = 1), SWO points to the most significant byte of the time stamp. If SV is 0, the host must write this field as 0.
- FD: frame drop. When set, this bit indicates that the ADIN2111 MAC has detected a condition for which the SPI host must drop the received Ethernet frame. This bit is only valid at the end of a received frame (EV = 1), and must be 0 at all other times.
- EV: end valid flag. When this bit is 1, the end of an Ethernet frame is present in the current receive data chunk payload.
- EBO: end byte offset. When EV is 1, this field contains the byte offset into the receive data chunk payload that points to the last byte of the received Ethernet frame. This field is 0 when EV = 0.
- RTSA: receive time stamp added. This bit is set when a 32-bit or 64-bit time stamp is added to the beginning of the SPI frame. This bit must be 0 when SV = 0.
- TXC: transmit credits. This field contains the minimum number of transmit data chunks of frame data that the SPI host can write in a single transaction without incurring a transmit buffer overflow.
- P: parity. The parity bit is calculated over the receive data header. The method is odd parity.

OPEN Alliance SPI Cut Through Mode

If cut through mode from or to the host is enabled, the method to transfer frames remains the same as when using store and forward mode. However, the frame receive starts when sufficient frame data to fill a chunk is received, and the frame transmit starts when a configured transmit threshold is reached. See the transmit threshold register (TX_THRESH) for details.

The cut through mode can be enabled via the receive cut through enable bits (RXCTE) and transmit cut through enable bits (TXCTE) in the Configuration Register 0 (CONFIG0).

On receive, the MAC returns data as it becomes available. Unlike in store and forward mode, there may be empty chunks (DV = 0) between a start of frame (SOF) chunk and an EOF chunk.

If the host does not read frames fast enough to keep the receive FIFO empty, the frames are then buffered in the receive FIFO as if it is operating in store and forward mode. When all the frames are read, the FIFO returns to operating in cut through mode.

On transmit, the host must provide frame data at a rate fast enough (>10 Mbps) to ensure that the frame does not under run on transmit. If the MAC under runs, TXBUE in the Status Register 0 (STATUS0) asserts and the MAC stops transmitting the frame in progress and appends a bad CRC to the frame.

Cut Through Transmit Latency

The time interval between the start of an SPI data transaction with a transmit header SWO of 0 (frame starts immediately in the chunk), and the time TX_EN rises on the media independent interface (MII) with an SPI frequency of 16 MHz and TX_THRESH = 1 is 4 µs. The PHY transmit latency is 3.2 µs. This makes a total transmit latency of 7.2 µs.

Cut Through Receive Latency

The receive latency varies based on the chunk size and the SPI frequency. Table 40 indicates the latency for an SPI frequency of 16 MHz and all supported chunk sizes.

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Table 40. Receive Latency for 16 MHz for All Supported Chunk Sizes

Chunk Size (Bytes)	PHY Rx Latency (µs)	Time to Receive a Chunk of Data on the Ethernet Wire (µs) [1]	Time to Start of Frame Transfer over SPI (µs) [2]	Total Rx Latency onto Wire (µs)	Total Rx Latency to End of First Chunk Transfer (µs) [3]
64	6.4	57.6	17	81	98
32	6.4	32	9	47.4	56.4
16	6.4	19.2	5	30.6	35.6
8	6.4	12.8	3	22.2	25.2

[1] Enough frame data to fill a chunk must be received before a transfer starts on the SPI. The time to receive the frame preamble is also included in this chunk.

[2] Assuming that the µC is not waiting for an interrupt and that it is providing back to back OPEN Alliance data transactions on the SPI. The frame transfers start in the middle of the chunk on average.

[3] Realistically, the µC cannot use the data until it receives the receive header at the end of the chunk.

Control Transactions

Table 41. Control Command Header

D31	D30	D29	D28	D27 to D24	D23 to D8	D7 to D1	D0
0	HDRB	WNR	AID	MMS	ADDR [15:0]	LEN [6:0]	P

Control transactions consist of one or more control commands. These commands are used by the SPI host to read and write registers within the ADIN2111, and each one is composed of a 32-bit control command header followed by register data. See Table 41.

See the following definitions:

- HDRB: received header bad. When set by the ADIN2111, HDRB indicates that a header was received with a parity error. The SPI host must always clear this bit. The ADIN2111 ignores this value.
- WNR: write not read. If 1, data is written to registers. Otherwise, data is read.
- AID: address increment disable. When clear, the address is automatically post incremented by one following each register read or write.
- MMS: memory map selector. This field selects the specific register memory map to access. See Table 42.
- ADDR: address of the first register within the selected memory map to access.
- LEN: length. Specifies the number of registers to read or write. This field is interpreted as the number of registers − 1. Therefore, a length of 0 reads or writes a single register.
- P: parity. Parity bit calculated over the control command header. Method used is odd parity.

Table 42. Register Memory Maps (MMS)

MMS	Memory Map Description
0	Standard control and status (SPI Address 0x00 to Address 0x20)
1	MAC (from SPI Address 0x30)

Control Write

The ADIN2111 ignores the final 32 bits of data from the SPI host at the end of the control write command. The write command and data is also echoed from the ADIN2111 back to the SPI so it can identify which register write failed in the case of any bus errors.

Control write commands can write either a single register or multiple registers. When multiple registers are written, the address is automatically post incremented.

When a control write command is followed by another control command, the new control header must immediately follow the last word of the echoed register write data. The SPI host must deassert $\overline{CS}$ following the last word of the echoed register write data when the write command is the last command of the transaction.

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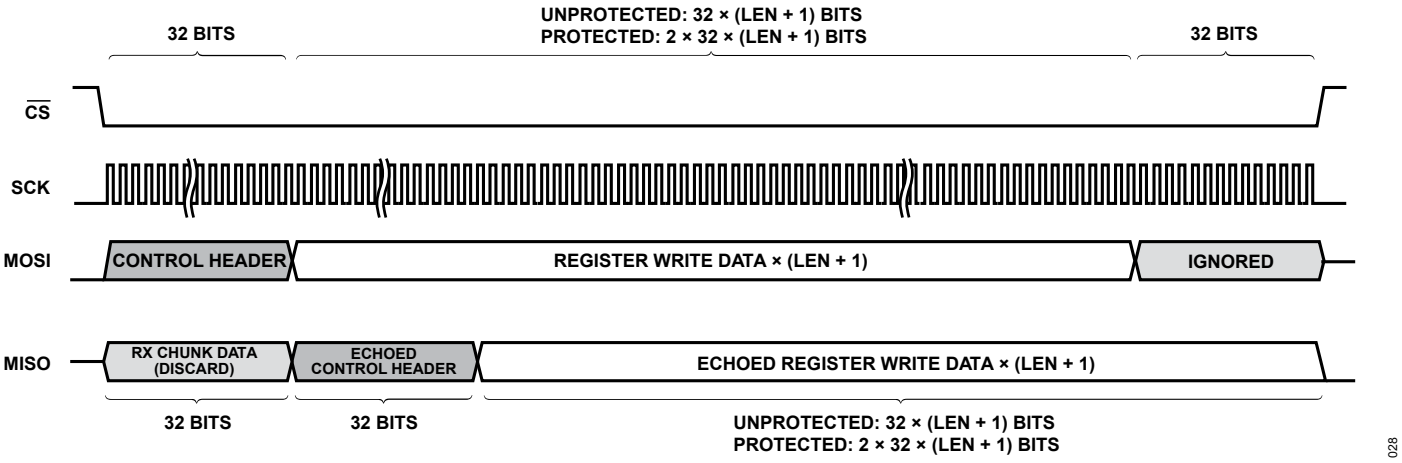

Figure 29. OPEN Alliance Control Transaction

Control Read

The MACPHY ignores all data from the SPI host following the control header for the rest of the control read command. Control read commands can read either a single register or multiple registers. When multiple registers are read, the address is automatically post incremented, according to the address increment disable bit in the control header.

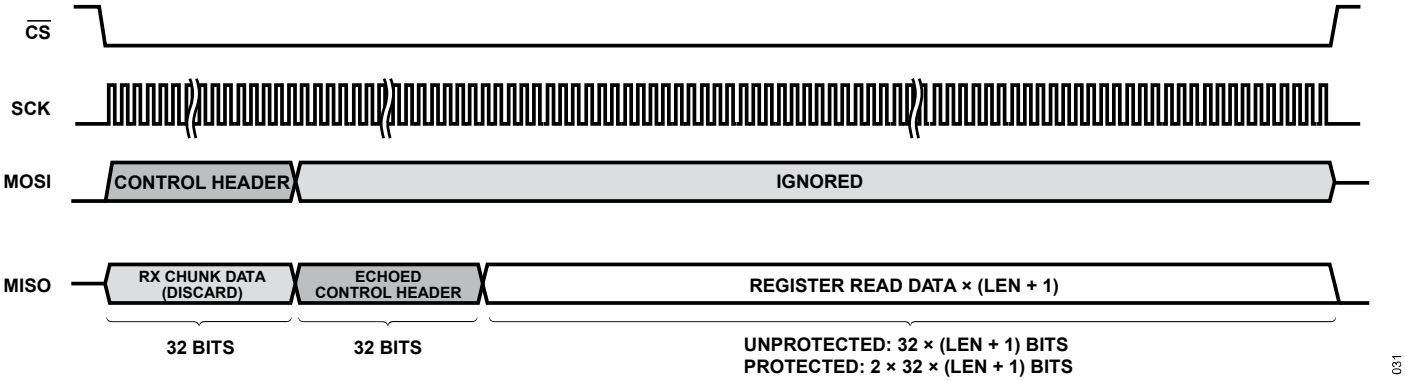

Figure 30. Control Read Transaction

OPEN Alliance SPI Errors

See the following OPEN Alliance SPI errors:

- SPI header parity error. If a parity error is detected on a transmit header and there is a transmit frame in the process of transferring over the SPI, this frame drops. If the switch is operating in cut through mode, the frame transmit stops and a bad CRC is appended to the frame.

  The ADIN2111 returns a fixed value of 0x4000_0000 in every word until $\overline{CS}$ goes high. The ADIN2111 responds with DV = 1, EV = 1, EBO = 0, and FD = 1 in the first data footer following a new assertion of $\overline{CS}$.

  If there is a parity error on a control transaction, the operation does not complete. Software can determine which transaction caused the error as the ADIN2111 returns a fixed 0x4000_0000 on SDO for the duration of the SPI transaction. Software can then resend the corrupted control transaction after clearing the header error bit.
- Transmit protocol error. Occurs when the ADIN2111 detects protocol errors in the transfer of transmit data chunks. These errors are usually due to SPI host firmware issues and do not occur in normal operation. The transmit protocol error bit is set when a data header received by the ADIN2111 indicates data valid (DV = 1) without a prior start of frame indication (SV = 1), in which case the data chunk is ignored. Or, when the ADIN2111 receives two data headers indicating a start of frame (SV = 1) without an end of frame (EV = 1), the ADIN2111 drops the frame data from the previous start of frame indicator and begins accepting the frame data from the second start of frame indicator.
- Transmit buffer overflow. Occurs when attempting to write transmit frame data to the ADIN2111 when there is no transmit buffer

space available as indicated by the transmit credit field (TXC) of the previous data footer. In this condition, the ADIN2111 ignores the transmit data chunk and sets the host transmit FIFO overflow bit, and the frame data already in the buffer is dropped.

- Transmit buffer under run. This error can only occur in cut through mode. The SPI host must always send frame data to the ADIN2111 faster than the network to avoid this error. When this error occurs, the host transmit FIFO under run error bit is set, and the ADIN2111 terminates the frame being transmitted in a way that invalidates the frame. Additionally, the ADIN2111 ignores any additional frame data received from the SPI host until it receives an end of frame indication (EV = 1).
- Loss of framing error. This error occurs when the $\overline{CS}$ signal is deasserted before the expected end of the data chunk or control command. When this error occurs, any transmit frame in progress is dropped, and any receive frame in progress of being sent to the SPI host is terminated.
- Receive buffer overflow. This error occurs when the SPI host does not read frame data from the ADIN2111 fast enough. This error can occur both in store and forward and cut through modes. When this error occurs, the ADIN2111 terminates the frame being received from the internal PHYs. In store and forward mode, no portion of the frame is transferred to the SPI host. In cut through mode, the ADIN2111 terminates the frame (EV = 1) with frame drop set (FD = 1).
- Control data protection error. The control data protection error (CDPE) and the loss of frame error (LOFE) bits assert when protection is enabled on the OPEN Alliance SPI and there is an error on write data received from the host. The write does not complete in this case. If possible, the software executes the write again. If software does not know which configuration register was written, the device may not be configured properly. In this case, reset the ADIN2111 MAC by writing the RST_MAC_ONLY keys to the software reset register.

SPI Access to the PHY Registers

The ADIN2111 provides indirect access to the two PHY management registers via the internal SPI to MDIO bridge. The eight MDIOACCn registers in the SPI register map are used to access the PHY management registers. Each MDIOACCn register corresponds to an MDIO transaction.

The MDC default speed is 2.5 MHz. Either a 2.5 MHz or 4.166 MHz management data clock (MDC) frequency can be selected via the MSPEED bits in the CONFIG2 register.

The MDIO master polls the TRDONE bits of the eight MDIOACCn registers in round robin mode. When the MDIO master detects that one of the TRDONE fields is 0, the MDIO master starts an MDIO transaction. When the MDIO transaction completes, the TRDONE bits are set to 1, and the master proceeds to check the TRDONE bits of the next MDIOACCn register.

Each of the two PHYs has a fixed MDIO PHY address, as follows:

- PHY 1 MDIO address: 0x1
- PHY 2 MDIO address: 0x2

Note that MDIO_DEVAD is always written with the device ID of the register being accessed. MDIO_PRTAD is set to the respective PHY MDIO address, and MDIO_ST is written to 0x0 for Clause 45 access (this applies to all of the following Clause 45 examples).

MDIO PHY Address Determination

The ADIN2111 allows access to the two PHY registers via an SPI to MDIO master bridge.

Each of the two PHYs has a fixed MDIO PHY address, as follows:

- MDIO PHY Address 1: PHY 1
- MDIO PHY Address 2: PHY 2

Clause 45 MDIO Operation Examples

Example write to PHY 1 Register XYZ:

1. Write MDIOACC0 with MDIO_DATA = the address of Register XYZ, MDIO_DEVAD = the device ID of Register XYZ, MDIO_PRTAD = 0x1, MDIO_OP = 0x0(ADDR), MDIO_ST = 0x0, and TRDONE = 0x0.
2. Write MDIOACC1 with MDIO_DATA = the value to be written to Register XYZ, MDIO_OP = 0x1(WR) and TRDONE = 0x0.
3. Optionally, poll MDIOACC0. TRDONE = 0x1 to determine that the write address operation has completed.
4. Poll MDIOACC1. TRDONE = 0x1 to determine that the write data operation completed.

Example read of PHY 1 Register XYZ:

1. Write MDIOACC0 with MDIO_DATA = the address of Register XYZ, MDIO_OP = 0x0(ADDR), and TRDONE = 0x0.
2. Write MDIOACC1 with MDIO_OP = 0x3(RD) and TRDONE = 0x0.
3. Poll MDIOACC1. TRDONE = 0x1 to determine that the write data operation completed. MDIOACC1. MDIO_DATA reflects the content of MDIO Register XYZ.

Example write operation followed by a read to verify the write operation:

1. Write MDIOACC0 with MDIO_DATA = the address of register ABC and TRDONE = 0x0.
2. Write MDIOACC1 with MDIO_DATA = the value to be written to register ABC, MDIO_OP = 0x1(WR), and TRDONE = 0x0.
3. Write MDIOACC2 MDIO_OP = 0x3(RD) and TRDONE = 0x0.
4. Poll MDIOACC2. TRDONE = 0x1 to verify that all operations completed. MDIO_DATA reflects the content of register ABC.

Example of four consecutive writes. It is possible to write a command to all eight registers before checking any.

1. Write MDIOACC0 with MDIO_DATA = the address of Register ABC and TRDONE = 0x0.

2. Write MDIOACC1 with the write data for register ABC, MDIO_OP = 0x1, and TRDONE = 0x0.
3. Write MDIOACC2 with MDIO_DATA = the address of Register DEF and TRDONE = 0x0.
4. Write MDIOACC3 with the write data for register DEF, MDIO_OP = 0x1, and TRDONE = 0x0.
5. Write MDIOACC4 with MDIO_DATA = the address of Register GHJ and TRDONE = 0x0.
6. Write MDIOACC5 with the write data for register GHJ, MDIO_OP = 0x1, and TRDONE = 0x0.
7. Write MDIOACC6 with MDIO_DATA = the address of Register XYZ and TRDONE = 0x0.
8. Write MDIOACC7 with the write data for Register XYZ, MDIO_OP = 0x1, and TRDONE = 0x0.
9. Host polls MDIOACC7. TRDONE = 0x1 to verify that all write data operations are complete.

Example burst read starting from Register XYZ:

1. Write MDIOACC0 with MDIO_DATA = the address of the Register XYZ, MDIO_OP = 0x0(ADDR), and TRDONE = 0x0
2. Write MDIOACC1 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
3. Write MDIOACC2 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
4. Write MDIOACC3 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
5. Write MDIOACC4 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
6. Write MDIOACC5 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
7. Write MDIOACC6 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
8. Write MDIOACC7 with MDIO_OP = 0x2(INC_RD) and TRDONE = 0x0.
9. Poll MDIOACC7. TRDONE = 1 to verify that all read data operations are complete.
10. Read MDIOACC1. MDIO_DATA, reflects the content of Register XYZ.
11. Read MDIOACC2. MDIO_DATA, reflects the content of Register XYZ. ADDR + 1.
12. Read MDIOACC3. MDIO_DATA, reflects the content of Register XYZ. ADDR + 2.
13. Read MDIOACC4. MDIO_DATA, reflects the content of Register XYZ. ADDR + 3.
14. Read MDIOACC5. MDIO_DATA, reflects the content of Register XYZ. ADDR + 4.
15. Read MDIOACC6. MDIO_DATA, reflects the content of Register XYZ. ADDR + 5.
16. Read MDIOACC7. MDIO_DATA, reflects the content of Register XYZ. ADDR + 6.

Clause 22 MDIO Operations Examples

Example of Clause 22 write of Register XYZ:

1. Write MDIOACC0 with MDIO_DATA = write data, MDIO_DEV_AD = the address of the Register XYZ, MDIO_PRTAD = 0x1, MDIO_OP = 0x1(WR), MDIO_ST = 0x1(Clause 22), and TRDONE = 0x0.
2. Poll MDIOACC0. TRDONE= 0x1 to determine that the write data operation is complete.

Example of Clause 22 read of Register XYZ:

1. Write MDIOACC0 with MDIO_DEV_AD = the address of the Register XYZ, MDIO_PRTAD = 0x1, MDIO_OP = 0x3(RD), MDIO_ST = 0x1(Clause 22), and TRDONE = 0x0.
2. Poll MDIOACC0. TRDONE = 0x1 to determine that the read operation is complete. MDIO_DATA reflects the contents of MDIO Register XYZ.

Example of Clause 22 write and read back of Register XYZ:

1. Write MDIOACC0 with MDIO_DATA = write data, MDIO_DEV_AD = the address of the Register XYZ, MDIO_PRTAD = 0x1, MDIO_OP = 0x1(WR), MDIO_ST = 0x1(Clause 22), and TRDONE = 0x0.
2. Write MDIOACC1 with MDIO_DEV_AD = the address of the Register XYZ, MDIO_PRTAD = 0x1, MDIO_OP = 0x3(RD), MDIO_ST = 0x1(Clause 22), and TRDONE = 0x0.
3. Poll MDIOACC1. TRDONE = 0x1 to determine that the read operation is complete. MDIO_DATA reflects the contents of MDIO Register XYZ.

Contents of PHY Registers

The PHY registers provide access to control and status information in the management registers.

The registers of the PHY Clause 45 register map are made up of four device address groupings (see Table 43) based on the MDIO manageable device (MMD). Within each device address space, IEEE standard registers are located in register addresses between 0x0000 and 0x7FFF, and vendor specific registers are located in register addresses from 0x8000 to 0xFFFF.

Table 43. Clause 45 Register Groupings

Device Address	MMD Name
0x01	PMA/physical medium dependent (PMD)
0x03	PCS
0x07	Autonegotiation
0x1E	Vendor Specific 1

Clause 45 can access to up to 32 PHYs consisting of up to 32 MMDs through a single MDIO interface.

The default value of some of the registers is determined by the value of the hardware configuration pins, which are read just after the $\overline{\text{RESET}}$ pin is deasserted. In these cases, the reset value in the

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register table is listed as pin dependent, which allows the default operation of the ADIN2111 to be configured without having to write to it over the SPI.

Recommended Register Operation

Many of the PHY registers in the ADIN2111 are defined in the IEEE Standard 802.3, and the exact behavior of these registers follows the standard. This behavior is not always obvious and is described in this section, in addition to the recommended operation and use of the registers.

Latch Low Registers

The IEEE Standard 802.3-2018 requires certain MDIO accessible registers to exhibit latch low behavior. The idea is to allow software that only intermittently reads these registers to detect conditions that can be transitory or short lived. For example, the AN_LINK_STATUS bit is required to latch low. When the device exits from a reset or power-down state, the latching condition is not active and the value of the AN_LINK_STATUS bit reflects the current status of the link. However, if the link comes up and drops, the latching condition is active. In this case, the AN_LINK_STATUS bit reads as 0 even if the link has come back up again in the interim. The latching condition is only cleared when the AN_LINK_STATUS bit is read, ensuring the software had the opportunity to observe that the link dropped.

One implication of this latch low behavior is that, if software wishes to determine the current status of the link, it must perform two reads of the AN_LINK_STATUS bit back to back. The first read is needed to clear any active latching condition.

Another implication is that it is important that software take account of the interaction between MDIO accessible bits that share a register address. For example, the AN_PAGE_RX bits and AN_LINK_STATUS bits reside at the same register address. As a result, reading the AN_PAGE_RX bits clears any active latching condition associated with the AN_LINK_STATUS bits.

IEEE Duplicated Registers

The IEEE Standard 802.3-2018 covers a very wide range of standards and speeds, from 10 Mbps to 40 Gbps and higher, and includes a large number of clauses. There are registers associated with many clauses, and different PHYs can include different clauses and combinations of clauses. Therefore, registers for common functions like software reset, software power-down, loopback, and so on, tend to be implemented in multiple clauses.

In the ADIN2111, the physical implementation of these registers is in a single location, but they can be accessed at multiple addresses. For example, the software reset bit, can be read or written in all the following IEEE MMD locations and vendor specific register locations:

- PMA_SFT_RST
- B10L_PMA_SFT_RST
- PCS_SFT_RST
- B10L_PCS_SFT_RST
- CRSM_SFT_RST

In this example, these are the PMA/PMD, PCS, autonegotiation, and Vendor Specific MMD 1 device address locations (per Table 43).

Having multiple address locations for the same register makes the use of the device more complex than necessary, particularly in relation to registers that have latch low or self clear access permissions. This is an unavoidable consequence of the IEEE standard.

The ADIN2111 data sheet only calls out a single recommended address location for each of these IEEE registers to simplify the operation and use of the device. In general, the registers introduced in the 802.3cg (10BASE-T1L) section of the standard are recommended over older (equivalent) registers. Often, registers in a vendor specific address are recommended, particularly where a register brings a number of useful IEEE register bits into a single register address. The ADIN2111 responds to register accesses to all the IEEE register address locations covered by the 10BASE-T1L standard when the start up completes after a power-on reset, hardware reset, or software reset.

PHY Subsystem Registers Read Modify Write Operation

All PHY subsystems register write operations must be performed as read modify write operations. If this process is not followed, the value of the register bits can inadvertently change.

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Frame Forwarding on Receive

By default, the device drops all frames received. To receive frames, set up the address filtering table, or change the default operation for all receive frames.

Note that frames can be forwarded from one port to two destinations: the other port and the host SPI port.

The device can be configured to forward up to 16 different MAC addresses based on the MAC destination address (DA).

To receive frames with a particular DA, that DA has to be programmed to one of the 16 ADDR_FILT_x registers. Each register is 32 bits wide. Therefore, for example, to program a DA of 08:00:00:5A:64:68 to ADDR_FILT_x0, write:

- 0x0800 to ADDR_FILT_UPR0
- 0x005A6468 to ADDR_FILT_LWR0

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To forward frames with this DA to the host, set the TO_HOST bit field within the ADDR_FILT_UPRn register to 1. To apply this rule, set APPLY2PORT1 or APPLY2PORT2 to 1, accordingly.

MAC addresses can be masked using the ADDR_MSK_x registers. For example, to receive all the MAC addresses in the range 0x8000005A64xx, write:

- 0xFFFF to ADDR_MSK_UPR0
- 0XFFFFFF00 to ADDR_MSK_LWR0

Frames that do not match any of the 16 ADDR_FILT_x registers are dropped by default. The user can select to forward packages from unknown DAs to either the other port or the host with the bit fields P2_FWD_UNK2P1, P1_FWD_UNK2P2, P2_FWD_UNK2HOST, and P1_FWD_UNK2HOST in the MAC configuration register (CONFIG2). Figure 31 shows the forwarding algorithm. Frames received with a bad CRC or with RX_ERR asserted from the PHYs, as well as runt and jabber frames, are dropped and counted.

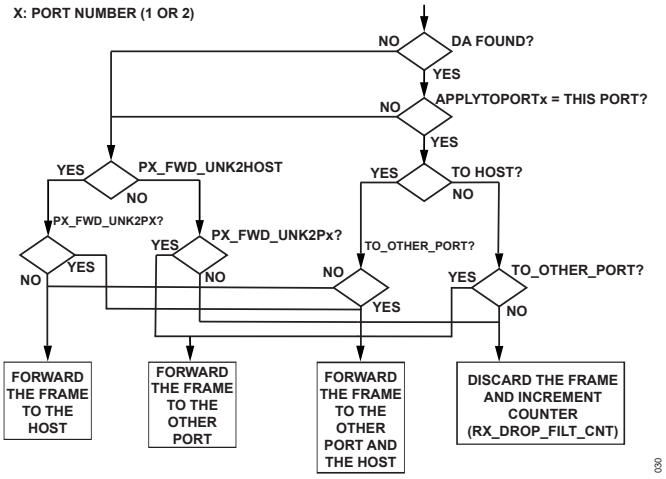

Figure 31. Frame Forwarding Algorithm

Receive Priority Queues

Each of the ADIN2111 PHYs has two different FIFOs on receive: a high priority FIFO and a low priority FIFO.

By default, the low priority FIFO is configured to 12 kB, and the high priority FIFO is configured to 8 kB. The sizes of these FIFOs can be changed before receiving or transmitting any frames via the P1_RX_LO_SIZE and P1_RX_HI_SIZE (Port 1) and P2_RX_LO_SIZE and P2_RX_HI_SIZE (Port 2) fields in the FIFO_SIZE register.

Statistics Counters

The ADIN2111 has fifteen 16-bit counters on each port that increment on frame transmit and receive. They roll over to 0 when the maximum value of 65535 is reached and they are not cleared on reading. Therefore, the counters must be read every four seconds to ensure that the counters do not roll over the last value read by the host.

Table 44. Port 1 and Port 2 Statistics Counters

Name[1]	Description
Px_RX_FRM_CNT	PORT Rx frame count
Px_RX_UCAST_CNT	PORT Rx unicast frame count
Px_RX_MCAST_CNT	PORT Rx multicast frame count
Px_RX_BCAST_CNT	PORT Rx broadcast frame count
Px_RX_CRC_ERR_CNT	PORT Rx CRC errored frame count
Px_RX_ALGN_ERR_CNT	PORT Rx alignment error count
Px_RX_PHY_ERR_CNT	PORT Rx PHY error count
Px_RX_LS_ERR_CNT	PORT Rx long and short frame error count
Px_TX_FRM_CNT	PORT Tx frame count
Px_TX_UCAST_CNT	PORT Tx unicast frame count
Px_TX_MCAST_CNT	PORT Tx multicast frame count
Px_TX_BCAST_CNT	PORT Tx broadcast frame count
Px_RX_DROP_FULL_CNT	PORT Rx frames dropped due to FIFO full
Px_RX_DROP_FILT_CNT	PORT Rx frames dropped due to filtering
Px_RX_IFG_ERR_CNT	PORT Rx frames received with interframe gap (IFG) errors

[1] One set of counters for each port. X represents the port number.

Receive Drop FIFO Full Counter

Before the first byte of a received frame is written into the appropriate receive FIFO on Port 1 (respectively Port 2), the space in the FIFO is checked. If there is no space for at least 256 bytes, the frame is dropped and the P1_RX_DROP_FULL_CNT (respectively P2_RX_DROP_FULL_CNT) counter increments. If there is space for at least 256 bytes in the FIFO, the logic writes the frame to the receive FIFO. If the received frame exceeds 256 bytes and the receive FIFO fills, the frame is dropped and the P1_RX_DROP_FULL_CNT (respectively P2_RX_DROP_FULL_CNT) counter increments.

Note that if a frame is destined for both the host and the other port, and the frame is not forwarded in one of the destination FIFOs because it is full, the frame is not counted as a dropped frame.

Frame Receive and Transmit Errors

By default, received errored frames do not generate interrupts. These frames are dropped and counted, and the software must monitor the statistics counters. The static random-access memory (SRAM) error correction code (ECC) error and transmit overflow error are reported in the error status register (ERR_STATUS). These errors result in the $\overline{INT}$ pin asserting an interrupt, unless an error is masked using the error status mask register (ERR_STATUS_MASK). See the SRAM ECC Error section and Transmit Overflow Error section.

SWITCH SPI

SRAM ECC Error

When writing a frame to one of the ADIN2111 PHY FIFOs, the size of the frame is inserted in a 16-bit word at the front of the frame and written to the FIFO. A 5-bit ECC is placed alongside the size field.

When this location is read from the SRAM, the ECC is checked. If a double bit error is detected, the RX_ECC_ERR or TX_ECC_ERR bits of the STATUS1 register are set to 1. If a double bit error is detected on reading a frame header from the receive FIFO, the frame is not transmitted.

In response to an ECC error, a FIFO automatically clears. All frames in the FIFO are lost, transmission stops, and a bad CRC is appended to the frame that transmitted. The next frame received is written to a FIFO.

Transmit Overflow Error

If the host attempts to write to the transmission FIFO but there is not enough space, the host transmission FIFO overflow bit field asserts (TXBOE). The software checks the space available in the transmission FIFO by reading the transmission FIFO space register (TX_SPACE) before attempting to write to it.

If this error occurs, the frame is automatically dumped, and the software has no other requirement than to clear the TXBOE status bit. Note that frames dropped because of a transmission FIFO overflow are not counted in the statistics counters.

REGISTERS

SPI REGISTER MAP

Register Summary: Host MAC Interface Register Map (MAC)

Table 45. MAC Register Summary

Address	Name	Description	Reset	Access
0x00	IDVER	Identification Version Register.	0x00000010	R
0x01	PHYID	PHY Identification Register.	0x0283BCA1	R
0x02	CAPABILITY	Supported Capabilities Register.	0x000006C3	R
0x03	RESET	Reset Control and Status Register.	0x00000000	W
0x04	CONFIG0	Configuration Register 0.	0x00000006	R/W
0x06	CONFIG2	Configuration Register 2.	0x00000800	R/W
0x08	STATUS0	Status Register 0.	0x00000040	R/W
0x09	STATUS1	Status Register 1.	0x00000000	R/W
0x0B	BUFSTS	Buffer Status Register.	0x00003B00	R
0x0C	IMASK0	Interrupt Mask Register 0.	0x00001FBF	R/W
0x0D	IMASK1	Mask Bits for Driving the Interrupt Pin Register.	0x43FA1F1A	R/W
0x10	TTSCAH	Transmit Time Stamp Capture Register A (High).	0x00000000	R
0x11	TTSCAL	Transmit Time Stamp Capture Register A (Low).	0x00000000	R
0x12	TTSCBH	Transmit Time Stamp Capture Register B (High).	0x00000000	R
0x13	TTSCBL	Transmit Time Stamp Capture Register B (Low).	0x00000000	R
0x14	TTSCCH	Transmit Time Stamp Capture Register C (High).	0x00000000	R
0x15	TTSCCL	Transmit Time Stamp Capture Register C (Low).	0x00000000	R
0x20 to 0x27 by 1	MDIOACCn	MDIO Access Registers.	0x8C000000	R/W
0x30	TX_FSIZE	MAC Tx Frame Size Register.	0x00000000	R/W
0x31	TX	MAC Transmit Register.	0x00000000	W
0x32	TX_SPACE	Tx FIFO Space Register.	0x000007FF	R
0x34	TX_THRESH	Transmit Threshold Register.	0x00000041	R/W
0x35	TX_PRI	LES Tx Priority Register.	0x00000000	R/W
0x36	FIFO_CLR	MAC FIFO Clear Register.	0x00000000	W
0x37 to 0x3A by 1	SCRATCHn	Scratch Registers.	0x00000000	R/W
0x3B	MAC_RST_STATUS	MAC Reset Status.	0x00000003	R
0x3C	SOFT_RST	Software Reset Register.	0x00000000	W
0x3D	SPI_INJ_ERR	Inject an Error on MISO from the Device Under Test (DUT).	0x00000000	R/W
0x3E	FIFO_SIZE	FIFO Sizes Register.	0x02222222	R/W
0x3F	TFC	Tx FIFO Frame Count Register.	0x00000000	R
0x40	TXSIZE	Tx FIFO Valid Half Words Register.	0x00000000	R
0x41	HTX_OVF_FRM_CNT	Host Tx Frames Dropped Due to FIFO Overflow.	0x00000000	R
0x42	MECC_ERR_ADDR	Address of a Detected ECC Error in Memory.	0x00000000	R
0x43 to 0x49 by 1	CECC_ERRn	Corrected ECC Error Counters.	0x00000000	R
0x50 to 0x6E by 2	ADDR_FILT_UPRn	MAC Address Rule and DA Filter Upper 16 Bits Registers.	0x00000000	R/W
0x51 to 0x6F by 2	ADDR_FILT_LWRn	MAC Address DA Filter Lower 32 Bits Registers.	0x00000000	R/W
0x70 to 0x72 by 2	ADDR_MSK_UPRn	Upper 16 Bits of the MAC Address Mask.	0x0000FFFF	R/W
0x71 to 0x73 by 2	ADDR_MSK_LWRn	Lower 32 Bits of the MAC Address Mask.	0xFFFFFFFF	R/W

REGISTERS

Table 45. MAC Register Summary (Continued)

Address	Name	Description	Reset	Access
0x80	TS_ADDEND	Time Stamp Accumulator Addend Register.	0x85555555	R/W
0x81	TS_1SEC_CMP	Timer Update Compare Register.	0x3B9ACA00	R/W
0x82	TS_SEC_CNT	Seconds Counter Register.	0x00000000	R/W
0x83	TS_NS_CNT	Nanoseconds Counter Register.	0x00000000	R/W
0x84	TS_CFG	Timer Configuration Register.	0x00000000	R/W
0x85	TS_TIMER_HI	High Period for TS_TIMER Register.	0x00000000	R/W
0x86	TS_TIMER_LO	Low Period for TS_TIMER Register.	0x00000000	R/W
0x87	TS_TIMER_QE_CORR	Quantization Error Correction Register.	0x00000000	R/W
0x88	TS_TIMER_START	TS_TIMER Counter Start Time Register.	0x00000000	R/W
0x89	TS_EXT_CAPT0	TS_CAPT Pin 0 Time Stamp Register.	0x00000000	R
0x8A	TS_EXT_CAPT1	TS_CAPT Pin 1 Time Stamp Register.	0x00000000	R
0x8B	TS_FREECNT_CAPT	TS_CAPT Free Running Counter Register.	0x00000000	R
0x90	P1_RX_FSIZE	Port 1 (P1) MAC Rx Frame Size Register.	0x00000000	R
0x91	P1_RX	P1 MAC Receive Register.	0x00000000	R
0xA0	P1_RX_FRM_CNT	P1 Rx Frame Count Register.	0x00000000	R
0xA1	P1_RX_BCAST_CNT	P1 Rx Broadcast Frame Count Register.	0x00000000	R
0xA2	P1_RX_MCAST_CNT	P1 Rx Multicast Frame Count Register.	0x00000000	R
0xA3	P1_RX_UCAST_CNT	P1 Rx Unicast Frame Count Register.	0x00000000	R
0xA4	P1_RX_CRC_ERR_CNT	P1 Rx CRC Errored Frame Count Register.	0x00000000	R
0xA5	P1_RX_ALGN_ERR_CNT	P1 Rx Align Error Count Register.	0x00000000	R
0xA6	P1_RX_LS_ERR_CNT	P1 Rx Long/Short Frame Error Count Register.	0x00000000	R
0xA7	P1_RX_PHY_ERR_CNT	P1 Rx PHY Error Count Register.	0x00000000	R
0xA8	P1_TX_FRM_CNT	P1 Tx Frame Count Register.	0x00000000	R
0xA9	P1_TX_BCAST_CNT	P1 Tx Broadcast Frame Count Register.	0x00000000	R
0xAA	P1_TX_MCAST_CNT	P1 Tx Multicast Frame Count Register.	0x00000000	R
0xAB	P1_TX_UCAST_CNT	P1 Tx Unicast Frame Count Register.	0x00000000	R
0xAC	P1_RX_DROP_FULL_CNT	P1 Rx Frames Dropped Due to FIFO Full Register.	0x00000000	R
0xAD	P1_RX_DROP_FILT_CNT	P1 Rx Frames Dropped Due to Filtering Register.	0x00000000	R
0xAE	P1_RX_IFG_ERR_CNT	Frame Received on Port 1 with IFG Errors.	0x00000000	R
0xB0	P1_TX_IFG	P1 Transmit Interframe Gap Register.	0x0000000B	R/W
0xB3	P1_LOOP	P1 MAC Loopback Enable Register.	0x00000000	R/W
0xB4	P1_RX_CRC_EN	P1 CRC Check Enable on Receive Register.	0x00000001	R/W
0xB5	P1_RX_IFG	P1 Receive Interframe Gap Register.	0x0000000A	R/W
0xB6	P1_RX_MAX_LEN	P1 Maximum Receive Frame Length Register.	0x00000618	R/W
0xB7	P1_RX_MIN_LEN	P1 Minimum Receive Frame Length Register.	0x00000040	R/W
0xB8	P1_LO_RFC	P1 Rx Low Priority FIFO Frame Count Register.	0x00000000	R
0xB9	P1_HI_RFC	P1 Rx High Priority FIFO Frame Count Register.	0x00000000	R
0xBA	P1_LO_RXSIZE	P1 Low Priority Rx FIFO Valid Half Words Register.	0x00000000	R
0xBB	P1_HI_RXSIZE	P1 High Priority Rx FIFO Valid Half Words Register.	0x00000000	R
0xBC	P1TOP2_TXSIZE	P1 to Port 2 (P2) Tx Size.	0x00000000	R
0xC0	P2_RX_FSIZE	P2 MAC Rx Frame Size Register.	0x00000000	R
0xC1	P2_RX	P2 MAC Receive Register.	0x00000000	R
0xD0	P2_RX_FRM_CNT	P2 Rx Frame Count Register.	0x00000000	R

REGISTERS

Table 45. MAC Register Summary (Continued)

Address	Name	Description	Reset	Access
0xD1	P2_RX_BCAST_CNT	P2 Rx Broadcast Frame Count Register.	0x00000000	R
0xD2	P2_RX_MCAST_CNT	P2 Rx Multicast Frame Count Register.	0x00000000	R
0xD3	P2_RX_UCAST_CNT	P2 Rx Unicast Frame Count Register.	0x00000000	R
0xD4	P2_RX_CRC_ERR_CNT	P2 Rx CRC Errored Frame Count Register.	0x00000000	R
0xD5	P2_RX_ALGN_ERR_CNT	P2 Rx Align Error Count Register.	0x00000000	R
0xD6	P2_RX_LS_ERR_CNT	P2 Rx Long/Short Frame Error Count Register.	0x00000000	R
0xD7	P2_RX_PHY_ERR_CNT	P2 Rx PHY Error Count Register.	0x00000000	R
0xD8	P2_TX_FRM_CNT	P2 Tx Frame Count Register.	0x00000000	R
0xD9	P2_TX_BCAST_CNT	P2 Tx Broadcast Frame Count Register.	0x00000000	R
0xDA	P2_TX_MCAST_CNT	P2 Tx Multicast Frame Count Register.	0x00000000	R
0xDB	P2_TX_UCAST_CNT	P2 Tx Unicast Frame Count Register.	0x00000000	R
0xDC	P2_RX_DROP_FULL_CNT	P2 Rx Frames Dropped Due to FIFO Full Register.	0x00000000	R
0xDD	P2_RX_DROP_FILT_CNT	P2 Rx Frames Dropped Due to Filtering Register.	0x00000000	R
0xDE	P2_RX_IFG_ERR_CNT	Frames Received on Port 2 with IFG Errors.	0x00000000	R
0xE0	P2_TX_IFG	P2 Transmit Interframe Gap Register.	0x0000000B	R/W
0xE3	P2_LOOP	P2 MAC Loopback Enable Register.	0x00000000	R/W
0xE4	P2_RX_CRC_EN	P2 CRC Check Enable on Receive Register.	0x00000001	R/W
0xE5	P2_RX_IFG	P2 Receive Interframe Gap Register.	0x0000000A	R/W
0xE6	P2_RX_MAX_LEN	P2 Maximum Receive Frame Length Register.	0x00000618	R/W
0xE7	P2_RX_MIN_LEN	P2 Minimum Receive Frame Length Register.	0x00000040	R/W
0xE8	P2_LO_RFC	P2 Rx Low Priority FIFO Frame Count Register.	0x00000000	R
0xE9	P2_HI_RFC	P2 Rx High Priority FIFO Frame Count Register.	0x00000000	R
0xEA	P2_LO_RXSIZE	P2 Low Priority Rx FIFO Valid Half Words Register.	0x00000000	R
0xEB	P2_HI_RXSIZE	P2 High Priority Rx FIFO Valid Half Words Register.	0x00000000	R
0xEC	P2TOP1_TXSIZE	P2 to P1 Tx Size.	0x00000000	R
0xF0	P2_TTSCAH	Transmit Time Stamp Capture Register A (High).	0x00000000	R
0xF1	P2_TTSCAL	Transmit Time Stamp Capture Register A (Low).	0x00000000	R
0xF2	P2_TTSCBH	Transmit Time Stamp Capture Register B (High).	0x00000000	R
0xF3	P2_TTSCBL	Transmit Time Stamp Capture Register B (Low).	0x00000000	R
0xF4	P2_TTSCCH	Transmit Time Stamp Capture Register C (High).	0x00000000	R
0xF5	P2_TTSCCL	Transmit Time Stamp Capture Register C (Low).	0x00000000	R

Identification Version Register

Address: 0x00, Reset: 0x00000010, Name: IDVER

Table 46. Bit Descriptions for IDVER

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:4]	MAJVER	OA Major Version. Major version identifier of the OPEN Alliance serial 10BASE-T1x MACPHY interface specification supported by this device.	0x1	R
[3:0]	MINVER	OA Minor Version. Minor version identifier of the OPEN Alliance serial 10BASE-T1x MACPHY interface specification supported by this device.	0x0	R

REGISTERS

PHY Identification Register

Address: 0x01, Reset: 0x0283BCA1, Name: PHYID

Table 47. Bit Descriptions for PHYID

Bits	Bit Name	Description	Reset	Access
[31:10]	OUI	Organizationally Unique Identifier (OUI) (Bits[23:2]). The 22 bits in the OUI field correspond to the 22 MSBs of the manufacturer's assigned 24-bit OUI. The OUI is arranged into the PHYID register such that OUI, Bit 2 is located at PHYID, Bit 31, and OUI, Bit 23 is located at PHYID, Bit 10.	0xA0EF	R
[9:4]	MODEL	Manufacturer's Model Number. The manufacturer's model number is used to identify the device.	0xA	R
[3:0]	REVISION	Manufacturer's Revision Number. The manufacturer's product revision number is used to indicate a revision level of the device.	0x1	R

Supported Capabilities Register

Address: 0x02, Reset: 0x000006C3, Name: CAPABILITY

Table 48. Bit Descriptions for CAPABILITY

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
10	TXFCSVC	Transmit Frame Check Sequence Validation Capability. Indicates the ability to validate the FCS appended by and received from the SPI host. When this bit is set it also indicates the ability of the MAC to be configured to accept egress frames with padding and FCS appended by the SPI host, and send ingress frames to the SPI host with the received FCS. 0: transmit FCS validation is not supported. 1: transmit FCS validation is supported.	0x1	R
9	IPRAC	Indirect PHY Register Access Capability. Indicates if PHY registers are directly accessible within the SPI register memory space. 0: PHY registers are not indirectly accessible. 1: PHY registers are indirectly accessible.	0x1	R
8	DPRAC	Direct PHY Register Access Capability. Indicates if PHY registers are directly accessible within the SPI register memory space. 0: PHY registers are not directly accessible. 1: PHY registers are directly accessible.	0x0	R
7	CTC	Cut Through Capability. Indicates if the MACPHY device supports cut through transfer of frames through the MACPHY to and from the network. 0: cut through not supported. 1: cut through supported.	0x1	R
6	FTSC	Frame Time Stamp Capability. Indicates if the MACPHY device supports the capturing of IEEE 1588 time stamps on frame receive from or transmit to the network. 1: IEEE 1588 time stamp capture on frame Tx/Rx is supported. 0: IEEE 1588 time stamp capture on frame Tx/Rx is not supported.	0x1	R
5	AIDC	Address Increment Disable Capability. Indicates if the MACPHY device supports the disabling of the automatic post-incrementing of the register address in control command reads and writes through the AID bit in the control command header. Address increment disable is not supported. This field is only used with the Open Alliance SPI protocol.	0x0	R
4	SEQC	TX Data Chunk Sequence and Retry Capability. Tx data chunk sequence and retry capability. Indicates if the MACPHY supports monitoring the SEQ bit sent by the SPI host in the Tx data chunk header and the retry of Tx data chunks.	0x0	R

REGISTERS

Table 48. Bit Descriptions for CAPABILITY (Continued)

Bits	Bit Name	Description	Reset	Access
		This field is only used with the OPEN Alliance SPI protocol. 1: Tx data chunk sequence and retry is supported. 0: Tx data chunk sequence and retry is not supported.		
3	RESERVED	Reserved.	0x0	R
[2:0]	MINCPS	Minimum Supported Chunk Payload Size. Minimum supported chunk payload size. Indicates the minimum size chunk payload that may be configured into the CPS field of the CONFIG0 register. The minimum supported chunk payload Size is 2^N, where N is the value of this bit field. This field is only used with the OPEN Alliance SPI protocol. 110: minimum supported chunk payload size is 64 bytes. 101: minimum supported chunk payload size is 32 bytes. 100: minimum supported chunk payload size is 16 bytes. 011: minimum supported chunk payload size is 8 bytes.	0x3	R

Reset Control and Status Register

Address: 0x03, Reset: 0x00000000, Name: RESET

Table 49. Bit Descriptions for RESET

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	SWRESET	MACPHY Software Reset. Writing a 1 to this bit fully resets the MACPHY, including the integrated PHY, to an initial state including but not limited to resetting all state machines and registers to their default value. When this bit is set, the reset does not occur until $\overline{CS}$ is deasserted to allow for the control command write to complete. $\overline{CS}$ must be held asserted for at least 100 ns for the reset to take effect. This bit is self clearing.	0x0	W

Configuration Register 0

Address: 0x04, Reset: 0x00000006, Name: CONFIG0

Table 50. Bit Descriptions for CONFIG0

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
15	SYNC	Configuration Synchronization. The state of this bit is reflected in the Rx footer SYNC bit. This bit defaults to 0 upon reset. Once written to a 1 by the SPI host, writing 0 does not clear this bit. Immediately after any reset the SYNC bit clears to 0, RESETC is set to 1, and the interrupt pin asserts. 0: the MACPHY reset and is not configured. 1: the MACPHY is configured.	0x0	R/W1S
14	TXFCSVE	Transmit Frame Check Sequence Validation Enable. When set, the final four octets of all Ethernet frames received are validated. CRC_APPEND must be 0 if this bit is set. That is, the MAC must not be configured to append a CRC to each transmitted frame.	0x0	R/W
13	CSARFE	$\overline{CS}$ Align Receive Frame Enable. When set, all receive Ethernet frames data starts only at the beginning of the first receive chunk payload following $\overline{CS}$ assertion. The start word offset (SWO) is always zero. Receive frames can begin within any receive chunk when this bit is clear. Only applies to the OA SPI protocol.	0x0	R/W
12	ZARFE	Zero Align Receive Frame Enable. When set, all receive Ethernet frames data is aligned to start at the beginning of the receive chunk payload with an SWO of zero. Receive frames can begin anywhere within the receive chunk payload when this bit is clear. Only applies to the Open Alliance SPI protocol.	0x0	R/W

REGISTERS

Table 50. Bit Descriptions for CONFIG0 (Continued)

Bits	Bit Name	Description	Reset	Access
[11:10]	TXCTHRESH	Transmit Credit Threshold. This field configures the number of transmit credits (TXC) of free buffer that must be available for writing before $\overline{INT}$ asserts. Only applies to the OA SPI Protocol. 00: ≥ 1 credit. 01: ≥ 4 credits. 10: ≥ 8 credits. 11: ≥ 16 credits.	0x0	R/W
9	TXCTE	Transmit Cut Through Enable. This bit enables the cut through mode of the frame transfer through the MACPHY device from the SPI host to the network. When cut through on Tx is enabled the host must ensure that data is provided to the device at a rate of > 10 Mbps to ensure frame transmission does not under run.	0x0	R/W
8	RXCTE	Receive Cut Through Enable. This bit enables the cut through mode of the frame transfer through the LES device from the network to the SPI host. Cut through must be enabled on device configuration before receiving frames is enabled. That is, enable cut through before setting Px_FWD_UNK2HOST or Px_FWD_UNK2Px or writing to the ADDR_FILT_x registers. RXCTE must be 0 when using the generic SPI protocol.	0x0	R/W
7	FTSE	Frame Time Stamp Enable. This bit enables IEEE 1588 receive and transmit frame time stamps. 0: frame receive/transmit time stamps are disabled. 1: frame receive/transmit time stamps are enabled.	0x0	R/W
6	FTSS	Receive Frame Time Stamp Select. When supported by this MACPHY device and enabled by FTSE = 1, this bit configures the size and format of the time stamps appended to received frames and captures on request of transmit frames. 0: 32-bit time stamps. 1: 64-bit time stamps.	0x0	R/W
5	PROTE	Enable Control Data Read Write Protection. When set and using the OPEN Alliance SPI protocol, all control data written to and read from the MACPHY is transferred with its complement for detection of bit errors. When set and using the generic SPI protocol, a CRC8 must be provided on SDI, and read data on SDO provides a CRC8. Note this bit cannot be written. Its value is set via sensing a pin on power-up.	0x0	R
4	SEQE	Enable Tx Data Chunk Sequence and Retry. When supported by this MACPHY device, this bit enables MACPHY monitoring of the SEQ bit transmitted in the Tx data chunk header by the SPI host and TX data chunk retries. Not supported. Only applies to the OA SPI Protocol.	0x0	R/W
		0: Support for Tx data chunk sequence and retry is disabled. The MACPHY ignores the Tx header SEQ bit.		
		1: Support for Tx data chunk sequence and retry is enabled. The MACPHY monitors the SEQ bit in the Tx header and allows the rewriting of Tx data chunks when the SEQ bit does not change.		
3	RESERVED	Reserved.	0x0	R
[2:0]	CPS	Chunk Payload Selector (N). Chunk payload size is 2^N. N = 3 minimum and 6 maximum. Default is 64 bytes. This field must be set on device configuration before frame transmission from the host starts and before enabling receiving frames into the Rx FIFOs. This field cannot be modified while transmitting a frame from the host or while sending a received frame to the host. Once the configuration synchronization (SYNC) bit is set, the chunk payload size must not be changed without a reset of the MACPHY. The minimum supported chunk payload size for this MACPHY device is indicated in the CPSMIN field of the CAPABILITY register. Only applies to the OA SPI protocol. 011: chunk size is 8 bytes. 100: chunk size is 16 bytes. 101: chunk size is 32 bytes. 110: chunk size is 64 bytes.	0x6	R/W

Configuration Register 2

Address: 0x06, Reset: 0x00000800, Name: CONFIG2

REGISTERS

Vendor specific.

Table 51. Bit Descriptions for CONFIG2

Bits	Bit Name	Description	Reset	Access
[31:17]	RESERVED	Reserved.	0x0	R
16	P2_RCV_IFG_ERR_FRM	Admit Frames with IFG Errors on Port 2. If enabled, the MAC admits frames with IFG errors on Port 2. Enables reception of frames that violate the minimum IFG requirement on Port 2.	0x0	R/W
15	RX_RD_ORDER	Rx Ports Read Order for the OPEN Alliance Data Protocol. On LES, there are two receive FIFOs on each port. When using the OPEN Alliance SPI protocol and there are frames in the FIFOs of both ports, the Rx FIFO from which a frame is read/returned to the host can be controlled via this field. 0: Fill level. When using the SPI Data protocol, frames from the FIFO of the port containing the most data for a particular priority level are returned first. By default, frames from the high priority FIFO containing the most data are returned first. If the high priority FIFOs are empty, the frames from the low priority FIFO containing the most data are returned first. . 1: Ping pong. When using the SPI data protocol, a single frame is read from each port in turn, that is, ping pong between the two ports on a per frame basic. Again by default frames from the high priority FIFOs are returned first. For example, if Port 1 contains high priority frames and Port 2 contains only low priority frames, all the high priority frames from Port 1 are read first.	0x0	R/W
14	P2_FWD_UNK2P1	Forward Frames from Port 2 Not Matching a MAC Address to Port 1. Determines the default rule for forwarding unknown frames. If a frame has a destination address that does not match a MAC address, the frame is dropped if this field is 0 and P2_UNK_TO_HOST is 0.	0x0	R/W
13	P1_FWD_UNK2P2	Forward Frames from Port 1 Not Matching a MAC Address to Port 2. Determines the default rule for forwarding unknown frames. If a frame has a destination address that does not match a MAC address, the frame is dropped if this field is 0 and P1_UNK_TO_HOST is 0.	0x0	R/W
12	P2_FWD_UNK2HOST	Forward Frames Not Matching Any MAC Address to the Host. Determines the default rule for forwarding unknown frames. Frames with an unknown destination address are placed in the low priority FIFO.	0x0	R/W
11	PORT_CUT_THRU_EN	Enable Cut Through from Port to Port. Cut through must be enabled on device configuration before receiving of frames is enabled. That is, enable cut through before setting Px_FWD_UNK2HOST or Px_FWD_UNK2Px or writing to the ADDR_FILT_x registers.	0x1	R/W
[10:9]	RESERVED	Reserved.	0x0	R/W
8	TX_RDY_ON_EMPTY	Assert TX_RDY When the Tx FIFO is Empty. By default, TX_RDY asserts when a frame transmits. If this bit is set, TX_RDY asserts when the Tx FIFO is empty. This field is only used with the generic SPI protocol.	0x0	R/W
7	SFD_DETECT_SRC	Determines If the SFD is Detected in the PHY or MAC. 0: select the SFD from the PHY. This option provides the least jitter as the SFD is detected in the same 120 MHz clock domain as is used in 1588 timer logic. 1: select the SFD from the MAC. The SFD from the MAC is from the 25 MHz clock domain and results in additional jitter on the SFD detection.	0x0	R/W
6	STATS_CLR_ON_RD	Statistics Clear on Reading. This field determines if the following registers/counters are cleared on reading: Px_RX_FRM_CNT, Px_RX_BCAST_CNT, Px_RX_MCAST_CNT, Px_RX_UCAST_CNT, Px_RX_CRC_ERR_CNT, Px_RX_ALGN_ERR_CNT, Px_RX_LS_ERR_CNT, Px_RX_PHY_ERR_CNT, Px_TX_FRM_CNT, Px_TX_BCAST_CNT, Px_TX_MCAST_CNT, Px_TX_UCAST_CNT, Px_RX_DROP_FULL_CNT, Px_RX_DROP_FILT_CNT, Px_RX_IFG_ERR_CNT, CECC_ERRn. 0: statistic counter is not cleared on reading. When the maximum value is reached, the counters roll over to 0x0.	0x0	R/W

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Table 51. Bit Descriptions for CONFIG2 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: clear statistics counters on reading. If a counter reaches its maximum value, the counter holds at its maximum until read. When using the generic SPI protocol, the status counters must be burst read in one SPI transaction to ensure all counters are cleared correctly in sequence. If a single SPI register/counter is read, it clears and the next counter (address location) also clears when using the generic SPI protocol.		
5	CRC_APPEND	Enable CRC Append in the MAC Tx Path. Enables (1) or disables (0) CRC appendage by the MAC. If this field is set to 0, the MAC assumes that the host is providing a frame with a valid CRC header at the end. It is recommended that the host always appends a CRC32 with the frame as this provides errors detection over the SPI for transmitted frames. The CRC32 is checked as the frame is transmitted. If an error is detected, TXFCSE asserts. Similarly on receive, the CRC32 is forwarded with the frame to the host where the host verifies it is correct.	0x0	R/W
4	P1_RCV_IFG_ERR_FRM	Admit Frames with IFG Errors on Port 1. If enabled, the MAC admits frames with IFG errors on Port 1. Enables reception of frames that violate the minimum IFG requirement on Port 1.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	P1_FWD_UNK2HOST	Forward Frames Not Matching Any MAC Address to the Host. Determines the default rule for forwarding unknown frames. Frames with an unknown destination address are placed in the low priority FIFO.	0x0	R/W
[1:0]	MSPEED	SPI to MDIO Bridge MDC Clock Speed. 00: 2.5 MHz. 01: 4.166 MHz.	0x0	R/W

Status Register 0

Address: 0x08, Reset: 0x00000040, Name: STATUS0

Table 52. Bit Descriptions for STATUS0

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved.	0x0	R
12	CDPE	Control Data Protection Error. When control data read/write protection is enabled, this bit indicates that the MACPHY detected an error in protected control write data received from the host. When not implemented, this bit is reserved with a read-only value of zero. This field is only used with the OPEN Alliance SPI protocol.	0x0	R/W1C
11	TXFCSE	Transmit Frame Check Sequence Error. This bit indicates that a frame was received over SPI from the host with an invalid FCS appended. The frame is still forwarded from the device as the FCS is checked as the frame is being transmitted.	0x0	R/W1C
10	TTSCAC	Transmit Time Stamp Capture Available C.	0x0	R/W1C
9	TTSCAB	Transmit Time Stamp Capture Available B.	0x0	R/W1C
8	TTSCAA	Transmit Time Stamp Capture Available A.	0x0	R/W1C
7	PHYINT	PHY Interrupt for Port 1. Host software must read the MDIO Interrupt Status registers (PHY_SUBSYS_IRQ_STATUS or CRSM_IRQ_STATUS) to determine the source of the interrupt. When exiting power-on reset or pin reset this bit is asserted, but this field is masked from asserting an interrupt by default.	0x0	R
6	RESETC	Reset Complete. This bit is set when the MACPHY reset is complete and ready for configuration. When it is set, it generates a nonmaskable interrupt assertion on $\overline{\text{INT}}$ to alert the SPI host. Additionally, setting the RESETC bit also sets EXST = 1 in the first Rx footer, or until this bit is cleared by action of the SPI host writing a 1.	0x1	R/W1C
5	HDRE	Header Error. When set, this bit indicates that the MACPHY detected an invalid header received from the SPI host. The invalid header is due to a parity check error. This field is only used with the OPEN Alliance SPI protocol.	0x0	R/W1C

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Table 52. Bit Descriptions for STATUS0 (Continued)

Bits	Bit Name	Description	Reset	Access
4	LOFE	Loss of Frame Error. When set, this bit indicates that the MACPHY detected an early deassertion of $\overline{CS}$ prior to the expected end of a data chunk or command control transaction. Note that this bit field also asserts if CDPE asserts.	0x0	R/W1C
3	RXBOE	Receive Buffer Overflow Error. When set, this bit indicates that the receive buffer (from the network) overflowed and the receive frame data was lost.	0x0	R/W1C
2	TXBUE	Host Tx FIFO Under Run Error. This error can only assert when cut through from the host is enabled. The host software ensures this bit never asserts by writing frame data to the MAC at a rate greater than 10 Mbps. If an under run error occurs, transmit of the current packet stops.	0x0	R/W1C
1	TXBOE	Host Tx FIFO Overflow. The host software ensures this bit never asserts by checking the space available in the Tx FIFO before writing to the Tx FIFO. If using the OPEN Alliance SPI Data protocol, the space in the Tx FIFO is indicated in the TXC field of the Rx footer. If using the generic SPI protocol, the TX_SPACE register indicates the remaining space in the Tx FIFO. If the host Tx FIFO overflows, the frame being written is dumped and software can chose to resend the entire frame. Writes to the FIFO commence at the next SOF. There is always room for more than one frame in the host Tx FIFO as it is 4 kB (or greater) in size. Therefore, a frame currently being transmitted is not interrupted by an overflow on the write side of the FIFO.	0x0	R/W1C
0	TXPE	Transmit Protocol Error. When set, this bit indicates that a Tx data chunk protocol error occurred. Data chunk received with DV = 1 but without a prior SV = 1. Data chunk received with SV = 1 but with no EV = 1 (repeated SV = 1 received). When using the generic SPI protocol, this bit indicates that the previous frame was not fully written. A write of the TX_FSIZE register was detected, but the MAC still expects further writes to the Tx register related to the previous frame size written to the TX_FSIZE register.	0x0	R/W1C

Status Register 1

Address: 0x09, Reset: 0x00000000, Name: STATUS1

Table 53. Bit Descriptions for STATUS1

Bits	Bit Name	Description	Reset	Access
[31:25]	RESERVED	Reserved.	0x0	R/W1C
24	P2_TXFCSE	CRC Mismatch on a Tx Frame on Port 2.	0x0	R/W1C
23	P2_RX_IFG_ERR	Rx MAC Interframe Gap Error. If the IFG is too short, the frame is dropped on receive. The threshold used for measuring the IFG on receive can be set in the P2_RX_IFG register.	0x0	R/W1C
22	P2_TTSCAC	Transmit Time Stamp Capture Available C.	0x0	R/W1C
21	P2_TTSCAB	Transmit Time Stamp Capture Available B.	0x0	R/W1C
20	P2_TTSCAA	Transmit Time Stamp Capture Available A.	0x0	R/W1C
19	P2_PHYINT	PHY Interrupt for Port 2. Host software must read the MDIO Interrupt Status registers (PHY_SUB-SYS_IRQ_STATUS or CRSM_IRQ_STATUS) on PORT2 PHY to determine the source of the interrupt.	0x0	R
18	P2_RX_RDY_HI	Port 2 Rx Ready High Priority. Indicates that there is a high priority frame available on Port 2. See P1_RX_RDY_HI. This field does not drive the interrupt pin. This field is only used with the generic SPI protocol.	0x0	R
17	P2_RX_RDY	Port 2 Rx FIFO Contains Data. In store and forward mode, this field indicates that there is one or more frames in Port 2 Rx FIFO. In cut through mode, this field indicates that the receive threshold (RX_THRESH) is reached or the EOF byte of a frame is received. If there are frames in both the Rx high and low priority FIFOs, the frame from the high priority FIFO is read first by default. This default operation can be changed using the RX_LOW_PRI_1ST field. This field is only used with the generic SPI protocol.	0x0	R
[16:13]	RESERVED	Reserved.	0x0	R
12	TX_ECC_ERR	ECC Error on Reading the Frame Size from a Tx FIFO. An uncorrectable ECC error was detected on a read of the size field from the Tx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and any other frames in the Tx FIFO is lost/dropped.	0x0	R/W1C

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Table 53. Bit Descriptions for STATUS1 (Continued)

Bits	Bit Name	Description	Reset	Access
11	RX_ECC_ERR	ECC Error on Reading the Frame Size from an Rx FIFO. An uncorrectable ECC error was detected on a reading the frame size field from an Rx FIFO. The FIFO is automatically cleared and the frame associated with the ECC error and other frames in the Rx FIFO is not lost/dropped.	0x0	R/W1C
10	SPI_ERR	Detected an Error on an SPI Transaction. When using the generic SPI protocol, this field indicates that a CRC error was detected. This field is not used with the OPEN Alliance Protocol. See HDRE and CDPE in STATUS0 for OPEN Alliance SPI errors.	0x0	R/W1C
9	RESERVED	Reserved.	0x0	R/W1C
8	P1_RX_IFG_ERR	Rx MAC Interframe Gap Error. If the IFG is too short, the frame is dropped on receive. The threshold used for measuring the IFG on receive can be set in the P1_RX_IFG register.	0x0	R/W1C
[7:6]	RESERVED	Reserved.	0x0	R
5	P1_RX_RDY_HI	Port 1 Rx Ready High Priority. Indicates that there is a high priority frame available on Port 1. When using the generic SPI protocol, this field can be used on LES to determine which port's receive FIFO is read next in the case where frames are available on both ports. If P1_RX_RDY_HI is 1 and P2_RX_RDY_HI is 0, the next frame is read from Port 1 because Port 1 has a high priority frame. If P1_RX_RDY_HI is 0 and P2_RX_RDY_HI is 1, the next frame is read from Port 2 because Port 2 has a high priority frame. This field does not drive the interrupt pin. This field is only used with the generic SPI protocol on LES.	0x0	R
4	P1_RX_RDY	Port 1 Rx FIFO Contains Data. In store and forward mode, this field indicates that there is one or more frames in Port 1 Rx FIFO. In cut through mode, this field indicates that the receive threshold (RX_THRESH) is reached or the EOF byte of a frame is received. If there are frames in both the Rx high and low priority FIFOs, the frame from the high priority FIFO is read first by default. This field is only used with the generic SPI protocol.	0x0	R
3	TX_RDY	Tx Ready. If TX_RDY_ON_EMPTY is 0, TX_RDY asserts when frame transmission completes. If TX_RDY_ON_EMPTY is 1, TX_RDY asserts when the Tx FIFO is empty and frame transmission completes. This bit is cleared by writing 1 to this field. This field is only used with the generic SPI protocol.	0x0	R/W1C
[2:0]	RESERVED	Reserved.	0x0	R

Buffer Status Register

Address: 0x0B, Reset: 0x00003B00, Name: BUFSTS

Table 54. Bit Descriptions for BUFSTS

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:8]	TXC	Transmit Credits Available. Number of chunk buffers of transmit data currently available for the SPI host to write. Reading this field allows the SPI host to queue up the number of transmit chunks available into a single DMA, if desired. The value in this field is saturated to 31 and sent in the 5-bit TXC field of every RX data footer. The default (maximum) number of transmit buffer credits available is implementation specific. This field is only used with the OPEN Alliance SPI protocol.	0x3B	R
[7:0]	RCA	Receive Chunks Available. Number of chunks of receive data currently available for the SPI host to read. Reading this field allows the SPI host to queue up the number of receive chunks available into a single DMA, if desired. This field is only used with the OPEN Alliance SPI protocol.	0x0	R

Interrupt Mask Register 0

Address: 0x0C, Reset: 0x00001FBF, Name: IMASK0

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Table 55. Bit Descriptions for IMASK0

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved.	0x0	R
12	CDPEM	Control Data Protection Error Mask. Setting this bit to 1 prevents the control data protection error status bit in STATUS0 from asserting the footer EXST bit. This field is only used with the OPEN Alliance SPI protocol.	0x1	R/W
11	TXFCSEM	Transmit Frame Check Sequence Error Mask. Setting this bit to 1 prevents the transmit frame check sequence error status bit in STATUS0 from asserting the interrupt pin.	0x1	R/W
10	TTSCACM	Transmit Time Stamp Capture Available C Mask. Setting this bit to 1 prevents the Transmit Time stamp Capture Available C status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
9	TTSCABM	Transmit Time Stamp Capture Available B Mask. Setting this bit to 1 prevents the Transmit Time Stamp Capture Available B status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
8	TTSCAAM	Transmit Time Stamp Capture Available A Mask. Setting this bit to 1 prevents the Transmit Time Stamp Capture Available A status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
7	PHYINTM	Physical Layer Interrupt Mask. Setting this bit to 1 prevents the physical layer interrupt (PHYINT) status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
6	RESETCM	RESET Complete Mask. This bit is reserved as a mask for the reset complete (RESETC) status bit. This bit is read only and always zero as the RESETC status bit is a nonmaskable interrupt that causes $\overline{\text{INT}}$ to always assert when RESETC is set.	0x0	R
5	HDREM	Header Error Mask. Setting a 1 to this bit prevents the header error (HDRE) status bit in STATUS0 from asserting the footer EXST bit. This field is only used with the OPEN Alliance SPI protocol.	0x1	R/W
4	LOFEM	Loss of Frame Error Mask. Setting a 1 to this bit prevents the loss of frame error (LOFE) status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
3	RXBOEM	Receive Buffer Overflow Error Mask. Setting a 1 to this bit prevents the receive buffer overflow error (RXBOE) status bit in STATUS0 from the footer EXST bit.	0x1	R/W
2	TXBUEM	Transmit Buffer Underflow Error Mask. Setting a 1 to this bit prevents the transmit buffer underflow error (TXBUE) status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
1	TXBOEM	Transmit Buffer Overflow Error Mask. Setting a 1 to this bit prevents the transmit buffer overflow error (TXBOE) status bit in STATUS0 from asserting the footer EXST bit.	0x1	R/W
0	TXPEM	Transmit Protocol Error Mask. Setting a 1 to this bit prevents the transmit protocol error (TXPE) status bit in STATUS0 from asserting $\overline{\text{INT}}$.	0x1	R/W

Mask Bits for Driving the Interrupt Pin Register

Address: 0x0D, Reset: 0x43FA1F1A, Name: IMASK1

Table 56. Bit Descriptions for IMASK1

Bits	Bit Name	Description	Reset	Access
[31:25]	RESERVED	Reserved.	0x21	R
24	P2_TXFCSEM	Transmit Frame Check Sequence Error Mask for P2_TXFCSE.	0x1	R/W
23	P2_RX_IFG_ERR_MASK	Mask Bit for RX_IFG_ERR.	0x1	R/W
22	P2_TTSCACM	Transmit Time Stamp Capture Available C Mask.	0x1	R/W
21	P2_TTSCABM	Transmit Time Stamp Capture Available B Mask.	0x1	R/W
20	P2_TTSCAAM	Transmit Time Stamp Capture Available A Mask.	0x1	R/W
19	P2_PHYINT_MASK	Mask Bit for P2_PHYINT.	0x1	R/W
18	RESERVED	Reserved.	0x0	R
17	P2_RX_RDY_MASK	Mask Bit for P2_RX_RDY. This field is only used with the generic SPI protocol.	0x1	R/W
[16:13]	RESERVED	Reserved.	0x0	R
12	TX_ECC_ERR_MASK	Mask Bit for TXF_ECC_ERR.	0x1	R/W

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Table 56. Bit Descriptions for IMASK1 (Continued)

Bits	Bit Name	Description	Reset	Access
11	RX_ECC_ERR_MASK	Mask Bit for RXF_ECC_ERR.	0x1	R/W
10	SPI_ERR_MASK	Mask Bit for SPI_ERR. This field is only used with the generic SPI protocol.	0x1	R/W
9	RESERVED	Reserved.	0x1	R/W
8	P1_RX_IFG_ERR_MASK	Mask Bit for RX_IFG_ERR.	0x1	R/W
[7:5]	RESERVED	Reserved.	0x0	R
4	P1_RX_RDY_MASK	Mask Bit for P1_RX_RDY. This field is only used with the generic SPI protocol.	0x1	R/W
3	TX_RDY_MASK	Mask Bit for TX_FRM_DONE. This field is only used with the generic SPI protocol.	0x1	R/W
2	RESERVED	Reserved.	0x0	R
1	LINK_CHANGE_MASK	Mask Bit for LINK_CHANGE.	0x1	R/W
0	RESERVED	Reserved.	0x0	R

Transmit Time Stamp Capture Register A (High)

Address: 0x10, Reset: 0x00000000, Name: TTSCAH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 57. Bit Descriptions for TTSCAH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_A	Transmit Time Stamp A, Bits[63:32].	0x0	R

Transmit Time Stamp Capture Register A (Low)

Address: 0x11, Reset: 0x00000000, Name: TTSCAL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 58. Bit Descriptions for TTSCAL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_A	Transmit Time Stamp A, Bits[31:0].	0x0	R

Transmit Time Stamp Capture Register B (High)

Address: 0x12, Reset: 0x00000000, Name: TTSCBH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 59. Bit Descriptions for TTSCBH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_B	Transmit Time Stamp B, Bits[63:32].	0x0	R

Transmit Time Stamp Capture Register B (Low)

Address: 0x13, Reset: 0x00000000, Name: TTSCBL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

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Table 60. Bit Descriptions for TTSCBL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_B	Transmit Time Stamp B, Bits[31:0].	0x0	R

Transmit Time Stamp Capture Register C (High)

Address: 0x14, Reset: 0x00000000, Name: TTSCCH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 61. Bit Descriptions for TTSCCH

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCH_C	Transmit Time Stamp C Bits, [63:32].	0x0	R

Transmit Time Stamp Capture Register C (Low)

Address: 0x15, Reset: 0x00000000, Name: TTSCCL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 62. Bit Descriptions for TTSCCL

Bits	Bit Name	Description	Reset	Access
[31:0]	TTSCL_C	Transmit Time Stamp C, Bits[31:0].	0x0	R

MDIO Access Registers

Address: 0x20 to 0x27 (Increments of 1), Reset: 0x8C000000, Name: MDIOACCn

Use this register to access the PHY registers via the SPI to MDIO bridge.

Table 63. Bit Descriptions for MDIOACCn

Bits	Bit Name	Description	Reset	Access
31	MDIO_TRDONE	Transaction Done. This bit must be written to 0 by the SPI host to initiate an MDIO transaction. The MACPHY sets this bit to 1 when the MDIO transaction completes.	0x1	R/W
30	MDIO_TAERR	Turnaround Error. The MACPHY sets this bit to 1 when a turnaround error occurs during the MDIO transaction. If this occurs, the contents of the DATA field for read and read-post-increment-address operations must be ignored.	0x0	R
[29:28]	MDIO_ST	Start of Frame. This field selects between Clause 45 and Clause 22 MDIO access. 00: Clause 45. 01: Clause 22.	0x0	R/W
[27:26]	MDIO_OP	Operation Code. 00: MD address command. 01: write command. 11: read command. 10: incremental read command.	0x3	R/W
[25:21]	MDIO_PRTAD	MDIO Port Address. This is the address of target port (PHY). This is called port address (PRTAD) for Clause 45, and called PHY address (PHYAD) for Clause 22.	0x0	R/W
[20:16]	MDIO_DEVAD	MDIO Device Address. When using Clause 45, this is the device address. When using Clause 22, this is the register address.	0x0	R/W

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Table 63. Bit Descriptions for MDIOACCn (Continued)

Bits	Bit Name	Description	Reset	Access
[15:0]	MDIO_DATA	Data/Address Value. For a write operation (Clause 45 or Clause 22), the SPI host must set this to the 16-bit value to be written. For an address operation (Clause 45), the SPI host must set this to the 16-bit register address value. For a read operation (Clause 45 or Clause 22), or for a read-post-increment-address operation (Clause 45), the SPI host must set this value to 0. On completion of the MDIO transaction (as indicated by TRDONE), the MACPHY sets this to the 16-bit value read.	0x0	R/W

MAC Tx Frame Size Register

Address: 0x30, Reset: 0x00000000, Name: TX_FSIZE

Table 64. Bit Descriptions for TX_FSIZE

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
[10:0]	TX_FRM_SIZE	Transmit Frame Size. This field indicates the size of the frame that is written to the transmit FIFO in bytes when using the generic SPI protocol. The size must include the 2-byte frame header. This is used on the SPI side of the Tx FIFO to determine when the full frame is written. When the full frame byte count is reached, subsequent writes to MAC_TX register are ignored until the MAC_TXF_SIZE is written again. This field is only used with the generic SPI protocol.	0x0	R/W

MAC Transmit Register

Address: 0x31, Reset: 0x00000000, Name: TX

The transmit FIFO is written via this register.

Table 65. Bit Descriptions for TX

Bits	Bit Name	Description	Reset	Access
[31:0]	TDR	Transmit Data Register. Writing to this register adds four bytes to the Host Tx FIFO. Note that the last word of a frame can only contain less than four bytes of data. The hardware uses MAC_TXF_SIZE to determine if there is one, two, three, or four bytes valid in the last SPI write of a frame. Only used with the generic SPI protocol.	0x0	W

Tx FIFO Space Register

Address: 0x32, Reset: 0x000007FF, Name: TX_SPACE

Table 66. Bit Descriptions for TX_SPACE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SPACE	Transmit FIFO Space Available in Half Words (16 Bits). This is used by the host software to determine if there is space in the Tx FIFO for a frame. Note that the software can queue two frames for transmission and simply wait for a TX_RDY interrupt, or it can fill the Tx FIFO with multiple frames and use TX_SPACE to determine if there is space for the next frame. Note that an extra two words of space is needed per frame in the host TX FIFO to store the frame size and header. For example, if TX_SPACE is 64, the maximum size frame that can be written is (64 − 2) × 2 bytes = 124 bytes. Only used with the generic SPI protocol.	0x7FF	R

Transmit Threshold Register

Address: 0x34, Reset: 0x00000041, Name: TX_THRESH

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Table 67. Bit Descriptions for TX_THRESH

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved.	0x0	R
[11:6]	P2P_TX_THRESH	Port to Port Transmit Start Threshold in Cut Through. If port to port cut through (PORT_CUT_THRU_EN) is enabled, this field determines the threshold in half words (16 bits) at which frame transmission starts when the frames are forwarded from one port to the other. The range of valid values for this field is 1 to 26 half words.	0x1	R/W
[5:0]	HOST_TX_THRESH	Host Transmit Start Threshold in Cut Through. When cut through on Tx is enabled (TX_CUT_THRU_EN = 1), this field is used to set the threshold in half words (16 bits) at which frame transmission starts for frames coming from the host. The range of valid values for this field is 1 to 26 half words.	0x1	R/W

LES Tx Priority Register

Address: 0x35, Reset: 0x00000000, Name: TX_PRI

Table 68. Bit Descriptions for TX_PRI

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved.	0x0	R
[2:0]	TX_HOST_PRI	Host Transmit Priority. When frames are queued to egress a port from both the host and the other port at the same time, this field determines the ratio of access to the port. For example, if there is a stream of 128-byte frames from Port 1 to Port 2, and the host is transmitting a stream of 128-byte frames on Port 2, and this field is set to H50_P50, 50% of the frames transmitted are from the host. The ratio is based on comparing the recent number of bytes transmitted from the host and the other port. 3 options are available: H50_P50, H100_P0, or H0_P100. Values outside of those listed below are reserved. 000: 50/50 host/port. 101: 100/0 host/port. The host is always guaranteed access to wire. 110: 0/100 host/port. Port to port traffic always gets priority.	0x0	R/W

MAC FIFO Clear Register

Address: 0x36, Reset: 0x00000000, Name: FIFO_CLR

Table 69. Bit Descriptions for FIFO_CLR

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved.	0x0	R
3	LES_P2P_FIFOS_CLR	Clear the Port to Port FIFOs on LES. If a frame is being transmitted from a Tx FIFO, transmission stops and a bad CRC is appended to the frame. Writes to Rx FIFOs resume at the start of the next received frame.	0x0	W
2	LES_FIFOS_CLR	Clear All FIFOs. If a frame is being transmitted from a Tx FIFO, transmission stops and a bad CRC is appended to the frame. Writes to Rx FIFOs resume at the start of the next received frame.	0x0	W
1	RESERVED	Reserved.	0x0	W
0	MAC_RXF_CLR	Clear the Receive FIFOs. Writes to the Rx FIFOs resume at the start of the next frame.	0x0	W

Scratch Registers

Address: 0x37 to 0x3A (Increments of 1), Reset: 0x00000000, Name: SCRATCHn

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Table 70. Bit Descriptions for SCRATCHn

Bits	Bit Name	Description	Reset	Access
[31:0]	SCRATCH_DATA	Scratch Data.	0x0	R/W

MAC Reset Status Register

Address: 0x3B, Reset: 0x00000003, Name: MAC_RST_STATUS

If this register returns 0x00000000_00000001 when read, the oscillator clock is active but the 25 MHz crystal clock is not active.

If this register returns 0x00000000_00000003 when read, both the oscillator clock and the 25 MHz crystal clock are active.

If this register returns 0x00000000_00000000 (SDO output pad is enabled as $\overline{CS}$ is low), the SPI slave and MAC core are both still in reset.

Only single SPI reads of this register are supported. An SPI burst read must not increment into this register.

Table 71. Bit Descriptions for MAC_RST_STATUS

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved.	0x0	R
1	MAC_CRYSL_CLK_RDY	MAC Crystal Clock Ready. If 0, this field indicates that the MAC core has released from reset. If 1, this field indicates that the MAC core released from reset. The MAC core is released from reset when the crystal clock (25 MHz) is ready.	0x1	R
0	MAC_OSC_CLK_RDY	MAC Oscillator Clock Ready.	0x1	R

Software Reset Register

Address: 0x3C, Reset: 0x00000000, Name: SOFT_RST

Table 72. Bit Descriptions for SOFT_RST

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	RST_KEY	Software Reset. Write a pair of keys in order and back to back on the SPI to trigger a reset. 0x4F1C: Key 1 to reset the MAC logic only. 0xC1F4: Key 2 to reset the MAC logic only. Reset does not take effect until $\overline{CS}$ is brought high and $\overline{CS}$ must be held asserted for at least 100 ns for the reset to take effect. If the MACPHY is in software power-down, the MAC_ONLY reset has no effect. That is, CRSM_SFT_P_CNTRL.CRSM_SFT_PD must be 0. 0x6F1A: Key 1 to request release of reset to the MAC core logic. Use MAC_RST_EXIT_REQ_KEYx to request a release of reset to the MAC core logic when the 25 MHz crystal clock is not available. This brings the MAC out of reset using the oscillator clock (12.5 MHz to 25.7 MHz). SPI accesses can then proceed at 15 MHz to allow debug access to MAC and PHY registers. 0xA1F6: Key 2 to request release of reset to the MAC core logic.	0x0	W

Inject an Error on MISO from the DUT Register

Address: 0x3D, Reset: 0x00000000, Name: SPI_INJ_ERR

Table 73. Bit Descriptions for SPI_INJ_ERR

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	TEST_SPI_INJ_ERR	Inject an Error on the SPI MISO Path. This function allows software to test that errors received on MISO are properly detected in software.	0x0	R/W

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Table 73. Bit Descriptions for SPI_INJ_ERR (Continued)

Bits	Bit Name	Description	Reset	Access
		If set and using the OPEN Alliance SPI protocol for data transaction, the parity bit in the Rx footer is inverted. Also, the time stamp parity bit in the in Rx footer is inverted. If set and using the OPEN Alliance SPI protocol for protected control burst write transactions, starting from the second word in a burst, the MSB of each echoed 32-bit word is inverted. If set and using the OPEN Alliance SPI protocol for protected control read transactions, the MSB of each 32-bit complement word is inverted. If set and using the generic SPI protocol with protection enabled, the CRC8 returned on a register read is inverted.		

FIFO Sizes Register

Address: 0x3E, Reset: 0x02222222, Name: FIFO_SIZE

Before modifying the FIFO sizes, frame reception and transmission must be stopped and the FIFOs must be empty.

Configure ADDR_RULE to drop all frames and set Px_UNK2HOST and Px_UNK2Px to 0 to ensure all received frames are dropped.

Use LES_FIFO_CLR to reset the FIFOs. Then the FIFO sizes can be modified.

The total FIFO size must be less than or equal to 28 kB.

Table 74. Bit Descriptions for FIFO_SIZE

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved.	0x0	R
[27:24]	P2_TX_SIZE	Port 1 to Port 2 Transmit FIFO Size. 0000: 0 bytes. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.	0x2	R/W
[23:20]	P1_TX_SIZE	Port 2 to Port 1 Transmit FIFO Size. 0000: 0 Bytes. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.	0x2	R/W
[19:16]	P2_RX_HI_SIZE	Port 2 Rx High Priority FIFO Size. 0000: 0 kB. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB.	0x2	R/W

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Table 74. Bit Descriptions for FIFO_SIZE (Continued)

Bits	Bit Name	Description	Reset	Access
		0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.		
[15:12]	P2_RX_LO_SIZE	Port 2 Rx Low Priority FIFO Size. 0000: 0 kB. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.	0x2	R/W
[11:8]	P1_RX_HI_SIZE	Port 1 Rx High Priority FIFO Size. 0000: 0 kB. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.	0x2	R/W
[7:4]	P1_RX_LO_SIZE	Port 1 Rx Low Priority FIFO Size. 0000: 0 kB. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB. 1000: 16 kB.	0x2	R/W
[3:0]	HTX_SIZE	Host Transmit FIFO Size. 0000: 0 kB. 0001: 2 kB. 0010: 4 kB. 0011: 6 kB. 0100: 8 kB. 0101: 10 kB. 0110: 12 kB. 0111: 14 kB.	0x2	R/W

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Table 74. Bit Descriptions for FIFO_SIZE (Continued)

Bits	Bit Name	Description	Reset	Access
		1000: 16 kB.		

Tx FIFO Frame Count Register

Address: 0x3F, Reset: 0x00000000, Name: TFC

For debug only. Number of frames in the transmit FIFO.

Table 75. Bit Descriptions for TFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	TFC	Number of Frames in the Tx FIFO.	0x0	R

Tx FIFO Valid Half Words Register

Address: 0x40, Reset: 0x00000000, Name: TXSIZE

Number of Valid Half Words (16 Bits) in the Host Tx FIFO.

Table 76. Bit Descriptions for TXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SIZE	Data in the Tx FIFO. Number of Half Words (16 Bits).	0x0	R

Host Tx Frames Dropped Due to FIFO Overflow Register

Address: 0x41, Reset: 0x00000000, Name: HTX_OVF_FRM_CNT

Table 77. Bit Descriptions for HTX_OVF_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	HTX_OVF_FRM_CNT	Counts Host Tx Frames Dropped Due to FIFO Overflow.	0x0	R

Address of a Detected ECC Error in Memory Register

Address: 0x42, Reset: 0x00000000, Name: MECC_ERR_ADDR

Table 78. Bit Descriptions for MECC_ERR_ADDR

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	MECC_ERR_ADDR	Address of an Uncorrectable ECC Error in Memory. This is the address of the first uncorrectable ECC error detected. That is when either RX_ECC_ERR or TX_ECC_ERR assert. When RX_ECC_ERR and TX_ECC_ERR are cleared, the register is opened to catch the address of the next ECC error. SRAM is 16 bits wide and this address points to a location in SRAM.	0x0	R

Corrected ECC Error Counters Register

Address: 0x43 to 0x49 (Increments of 1), Reset: 0x00000000, Name: CECC_ERRn

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Table 79. Bit Descriptions for CECC_ERRn

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved.	0x0	R
[9:0]	CECC_ERR_CNT	Corrected ECC Error Count. The seven counters map to FIFOs is as follows: CECC_ERR0: low priority Rx FIFO for Port 1. CECC_ERR1: high priority Rx FIFO for Port 2. CECC_ERR2: low priority Rx FIFO for Port 2 (LES only). CECC_ERR3: high priority Rx FIFO for Port 2 (LES only). CECC_ERR4: Tx FIFO from the host. CECC_ERR5: Port 1 to Port 2 Tx FIFO (LES only). CECC_ERR6: Port 2 to Port 1 Tx FIFO (LES only).	0x0	R

MAC Address Rule and DA Filter Upper 16 Bits Registers

Address: 0x50 to 0x6E (Increments of 2), Reset: 0x00000000, Name: ADDR_FILT_UPRn

Contains the upper 16 bits of a MAC address and the forwarding rules associated with the MAC address.

When writing the ADDR_FILT_x* registers, two register locations must be written in order for a given table entry.

For example to write table entry 0, the registers must be written in the following order:

1: ADDR_FILT_UPR0.

2: ADDR_FILT_LWR0.

Table 80. Bit Descriptions for ADDR_FILT_UPRn

Bits	Bit Name	Description	Reset	Access
31	APPLY2PORT2	Apply to Port 2. 0: do not apply to Port 2. Do not apply this table entry/rule to frames received on Port 2. 1: apply to Port 2. Apply this table entry/rule to frames received on Port 2.	0x0	R/W
30	APPLY2PORT1	Apply to Port 1. 0: do not apply to Port 1. Do not apply this table entry/rule to frames received on Port 1. 1: apply to Port 1. Apply this table entry/rule to frames received on Port 1.	0x0	R/W
[29:20]	RESERVED	Reserved.	0x0	R
19	HOST_PRI	Host Rx Port Priority. On the receive port to the host, there are two FIFOs, a low priority FIFIO and a high priority FIFO. This field determines which FIFO the frame is placed in. Note that by default memory resources are provided for a high priority FIFO. However if the memory assigned to the high priority FIFO is moved to another FIFO by writing to the FIFO_SIZE register, this field must not be set to 1. 0: low priority. 1: high priority.	0x0	R/W
18	RESERVED	Reserved.	0x0	R
17	TO_OTHER_PORT	Forward Frames Matching this MAC Address to the Other Port.	0x0	R/W
16	TO_HOST	Forward Frames Matching This MAC Address to the Host. If APPLY2PORT1 or APPLY2PORT2 is set to 1 and TO_HOST is 1, the frames matching this DA from the corresponding port are forwarded to the host. If TO_HOST is 0 and TO_OTHER_PORT is 0, frames matching the DA for this entry are dropped.	0x0	R/W
[15:0]	MAC_ADDR, Bits[47:32]	MAC Address.	0x0	R/W

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MAC Address DA Filter Lower 32 Bits Registers

Address: 0x51 to 0x6F (Increments of 2), Reset: 0x00000000, Name: ADDR_FILT_LWRn

Contains the lower 32 bits of a MAC address in the DA filter table.

A write to one of these registers must be preceded by a write to the corresponding ADDR_FILT_UPRn register.

Table 81. Bit Descriptions for ADDR_FILT_LWRn

Bits	Bit Name	Description	Reset	Access
[31:0]	MAC_ADDR, Bits[31:0]	MAC Address.	0x0	R/W

Upper 16 Bits of the MAC Address Mask Register

Address: 0x70 to 0x72 (Increments of 2), Reset: 0x0000FFFF, Name: ADDR_MSK_UPRn

The upper 16 bits of a MAC address mask in the DA mask table.

When writing the ADDR_MSK_x registers, all two register locations must be written in order for a given table entry. They must be written in order with the UPR register written first and the LWR register written last.

Table 82. Bit Descriptions for ADDR_MSK_UPRn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	MAC_ADDR_MASK, Bits[47:32]	MAC Address Bit Mask for the Address Table.	0xFFFF	R/W

Lower 32 Bits of the MAC Address Mask Register

Address: 0x71 to 0x73 (Increments of 2), Reset: 0xFFFFFFFF, Name: ADDR_MSK_LWRn

The lower 32 bits of a MAC address mask in the DA mask table.

When writing the ADDR_MSK_x registers, all two register locations must be written in order for a given table entry. They must be written in order with the UPR register written first and the LWR register written last.

Table 83. Bit Descriptions for ADDR_MSK_LWRn

Bits	Bit Name	Description	Reset	Access
[31:0]	MAC_ADDR_MASK, Bits[31:0]	MAC Address Bit Mask for the Address Table.	0xFFFFFFFF	R/W

Time Stamp Accumulator Addend Register

Address: 0x80, Reset: 0x85555555, Name: TS_ADDEND

Table 84. Bit Descriptions for TS_ADDEND

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_ADDEND	Time Stamp Accumulator Addend.	0x85555555	R/W

Timer Update Compare Register

Address: 0x81, Reset: 0x3B9ACA00, Name: TS_1SEC_CMP

Table 85. Bit Descriptions for TS_1SEC_CMP

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_1SEC_CMP	Time Stamp 1 Second Compare Value.	0x3B9ACA00	R/W

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Seconds Counter Register

Address: 0x82, Reset: 0x00000000, Name: TS_SEC_CNT

Use this register to write to the seconds counter.

Table 86. Bit Descriptions for TS_SEC_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_SEC_CNT	Write to the Seconds Counter.	0x0	R/W

Nanoseconds Counter Register

Address: 0x83, Reset: 0x00000000, Name: TS_NS_CNT

Use this register to write to the nanoseconds counter.

Table 87. Bit Descriptions for TS_NS_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_NS_CNT	Write to the Nanoseconds Counter. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 120 MHz clock and increment in steps of 16.	0x0	R/W

Timer Configuration Register

Address: 0x84, Reset: 0x00000000, Name: TS_CFG

Table 88. Bit Descriptions for TS_CFG

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved.	0x0	R
4	TS_CAPT_FREE_CNT	Capture the Free Running Counter. When this bit is 1 and FTSS is 0, time stamps are captured from the 32-bit free running counter. If this bit is 0 and FTSS is 0, 32-bit time stamps as defined in the OPEN Alliance MACPHY specification are captured. If FTSS is 1, 64- bit time stamps as defined in the OPEN Alliance MACPHY specification are captured.	0x0	R/W
3	TS_TIMER_STOP	Stop Toggling the TS_TIMER Output. Write 1 to this bit to stop the TS_TIMER output toggling and return it to its default value. Write to the TS_TIMER_START registers to start the TS_TIMER output signal again. This bit automatically clears to 0.	0x0	W
2	TS_TIMER_DEF	Default Value for the TS_TIMER Output. To change the default value of the TS_TIMER from 0, write 1 to this field before enabling the TS_TIMER (it is enabled when TS_TSTART is written). Note that on writing 1 to this register, the TS_TIMER output immediately toggles from 0 to 1. Writing to this field has no effect if the TS_TIMER is already enabled. If P1_LED_0 is used as the TS_TIMER output, the default value is dependent on the P1_LED_0 polarity set by the LED0_POLARITY bit field.	0x0	R/W
1	TS_CLR	Clear the 1588 Time Stamp Counters. Write to 1 to reset the time stamp counters to 0. This field automatically clears to 0 after it is written to 1. Four counters are cleared, the accumulator, the nanoseconds counter, the seconds counter, and the free running counter.	0x0	W
0	TS_EN	Enable the 1588 Time Stamp Counter. When this bit is 1, the time stamp counter is enabled and time stamps are captured for all received frames. The counters are not cleared when TS_EN is 0. Instead, the counters freeze. Therefore, it is recommended to write to use TS_CLR after disabling the counters to get them to a known state before starting again.	0x0	R/W

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High Period for TS_TIMER Register

Address: 0x85, Reset: 0x00000000, Name: TS_TIMER_HI

Table 89. Bit Descriptions for TS_TIMER_HI

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TIMER_HI	TS_TIMER High Period. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 120 MHz clock and increment in steps of 16. The minimum value that can be written to this field is 16 decimal.	0x0	R/W

Low Period for TS_TIMER Register

Address: 0x86, Reset: 0x00000000, Name: TS_TIMER_LO

Table 90. Bit Descriptions for TS_TIMER_LO

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TIMER_LO	TS_TIMER Low Period. Note that this register must be programmed with a value that is divisible by 16 decimal. This is because the counters are driven by a 120 MHz clock and increment in steps of 16. The minimum value that can be written to this field is 16 decimal.	0x0	R/W

Quantization Error Correction Register

Address: 0x87, Reset: 0x00000000, Name: TS_TIMER_QE_CORR

Table 91. Bit Descriptions for TS_TIMER_QE_CORR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:0]	TS_TIMER_QE_CORR	TS_TIMER Quantization Error Correction Value. If the required TS_TIMER low and high periods are not directly divisible by 16, program this field with a value between 0 and 15 to compensate for the TS_TIMER quantization error.	0x0	R/W

TS_TIMER Counter Start Time Register

Address: 0x88, Reset: 0x00000000, Name: TS_TIMER_START

Point in time at which to start the TS_TIMER counter.

Table 92. Bit Descriptions for TS_TIMER_START

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_TSTART	Point in Time at Which to Start the TS_TIMER Counter. Writing to this register starts the TS_TIMER output. To start the TS_TIMER output, this field must be written to a value greater than or equal to 16. After the TS_TIMER starts, writing to TS_TIMER_STOP stops the timer and return the TS_TIMER output to its default value.	0x0	R/W

TS_CAPT Pin 0 Time Stamp Register

Address: 0x89, Reset: 0x00000000, Name: TS_EXT_CAPT0

Time stamp captured on the assertion of the TS_CAPT pin.

Table 93. Bit Descriptions for TS_EXT_CAPT0

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_EXT_CAPTD, Bits[31:0]	Time Stamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

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TS_CAPT Pin 1 Time Stamp Register

Address: 0x8A, Reset: 0x00000000, Name: TS_EXT_CAPT1

Time Stamp Captured on the Assertion of the TS_CAPT Pin.

Table 94. Bit Descriptions for TS_EXT_CAPT1

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_EXT_CAPTD, Bits[63:32]	Time Stamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

TS_CAPT Free Running Counter Register

Address: 0x8B, Reset: 0x00000000, Name: TS_FREECNT_CAPT

Capture of the free running counter when TS_CAPT asserts.

Table 95. Bit Descriptions for TS_FREECNT_CAPT

Bits	Bit Name	Description	Reset	Access
[31:0]	TS_CNT_CAPTD	Captured Free Running Counter. This 32-bit counter is captured on the assertion of TS_CAPT pin, as is TS_EXT_CAPT.	0x0	R

P1 MAC Rx Frame Size Register

Address: 0x90, Reset: 0x00000000, Name: P1_RX_FSIZE

Table 96. Bit Descriptions for P1_RX_FSIZE

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
[10:0]	P1_RX_FRM_SIZE	Receive Frame Size. The size of the frame at the head of the Rx FIFO in bytes. The size includes the appended header. When using the generic SPI protocol this register must be read before reading a frame from a receive FIFO via P1_RX.	0x0	R

P1 MAC Receive Register

Address: 0x91, Reset: 0x00000000, Name: P1_RX

The receive FIFO is read via this register. It is possible to burst read data from the Rx FIFO over SPI.

Table 97. Bit Descriptions for P1_RX

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RDR	Receive Data Register. This field is only used with the generic SPI protocol. Reading this register returns the four bytes at the top of the receive FIFO and pops these four bytes from the FIFO. The upper 8 bits contain the first byte, the next 8 bits contain the second byte, and so on. When a complete frame is read out, no further data is returned from the P1 Rx FIFOs until the P1_RX_FRM_SIZE register is read first. Only used with the generic SPI protocol.	0x0	R

P1 Rx Frame Count Register

Address: 0xA0, Reset: 0x00000000, Name: P1_RX_FRM_CNT

Table 98. Bit Descriptions for P1_RX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_FRM_CNT	Rx Frame Count. This counter increments for received good and bad frames.	0x0	R

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P1 Rx Broadcast Frame Count Register

Address: 0xA1, Reset: 0x00000000, Name: P1_RX_BCAST_CNT

Table 99. Bit Descriptions for P1_RX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_BCAST_CNT	Rx Broadcast Frame Count. This counter increments for received good and bad frames.	0x0	R

P1 Rx Multicast Frame Count Register

Address: 0xA2, Reset: 0x00000000, Name: P1_RX_MCAST_CNT

Table 100. Bit Descriptions for P1_RX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_MCAST_CNT	Rx Multicast Frame Count. This counter increments for received good and bad frames.	0x0	R

P1 Rx Unicast Frame Count Register

Address: 0xA3, Reset: 0x00000000, Name: P1_RX_UCAST_CNT

Table 101. Bit Descriptions for P1_RX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_UCAST_CNT	Rx Unicast Frame Count.	0x0	R

P1 Rx CRC Errored Frame Count Register

Address: 0xA4, Reset: 0x00000000, Name: P1_RX_CRC_ERR_CNT

Table 102. Bit Descriptions for P1_RX_CRC_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_CRC_ERR_CNT	Rx CRC Errored Frame Count.	0x0	R

P1 Rx Align Error Count Register

Address: 0xA5, Reset: 0x00000000, Name: P1_RX_ALGN_ERR_CNT

Table 103. Bit Descriptions for P1_RX_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_ALGN_ERR_CNT	Rx Align Error Count.	0x0	R

P1 Rx Long/Short Frame Error Count Register

Address: 0xA6, Reset: 0x00000000, Name: P1_RX_LS_ERR_CNT

Table 104. Bit Descriptions for P1_RX_LS_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_LS_ERR_CNT	Rx Long/Short Frame Error Count.	0x0	R

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P1 Rx PHY Error Count Register

Address: 0xA7, Reset: 0x00000000, Name: P1_RX_PHY_ERR_CNT

Table 105. Bit Descriptions for P1_RX_PHY_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_PHY_ERR_CNT	Rx PHY Error Count.	0x0	R

P1 Tx Frame Count Register

Address: 0xA8, Reset: 0x00000000, Name: P1_TX_FRM_CNT

Table 106. Bit Descriptions for P1_TX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_TX_FRM_CNT	Tx Frame Count.	0x0	R

P1 Tx Broadcast Frame Count Register

Address: 0xA9, Reset: 0x00000000, Name: P1_TX_BCAST_CNT

Table 107. Bit Descriptions for P1_TX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_TX_BCAST_CNT	Tx Broadcast Frame Count.	0x0	R

P1 Tx Multicast Frame Count Register

Address: 0xAA, Reset: 0x00000000, Name: P1_TX_MCAST_CNT

Table 108. Bit Descriptions for P1_TX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_TX_MCAST_CNT	Tx Multicast Frame Count.	0x0	R

P1 Tx Unicast Frame Count Register

Address: 0xAB, Reset: 0x00000000, Name: P1_TX_UCAST_CNT

Table 109. Bit Descriptions for P1_TX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_TX_UCAST_CNT	Tx Unicast Frame Count.	0x0	R

P1 Rx Frames Dropped Due to FIFO Full Register

Address: 0xAC, Reset: 0x00000000, Name: P1_RX_DROP_FULL_CNT

Table 110. Bit Descriptions for P1_RX_DROP_FULL_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_DROP_FULL_CNT	Rx Frames Dropped Due to FIFO Full. Note that on LES, if a received frame is destined for both the host and other port (a flooded frame), and the frame is not forwarded to one of the destination FIFOs because it is full, the frame is not counted as a dropped frame.That is, if the frame is flooded, P1_RX_DROP_FULL_CNT only increments if both FIFOs are full.	0x0	R

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P1 Rx Frames Dropped Due to Filtering Register

Address: 0xAD, Reset: 0x00000000, Name: P1_RX_DROP_FILT_CNT

Table 111. Bit Descriptions for P1_RX_DROP_FILT_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_DROP_FILT_CNT	Rx Frames Dropped Due to Filtering.	0x0	R

Frame Received on Port 1 with IFG Errors Register

Address: 0xAE, Reset: 0x00000000, Name: P1_RX_IFG_ERR_CNT

Table 112. Bit Descriptions for P1_RX_IFG_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P1_RX_IFG_ERR_CNT	IFG Error Counter for Port 1 Received Frames.	0x0	R

P1 Transmit Interframe Gap Register

Address: 0xB0, Reset: 0x0000000B, Name: P1_TX_IFG

Table 113. Bit Descriptions for P1_TX_IFG

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:0]	P1_TX_IFG	Interframe Gap. Generates an IFG of ((P1_TX_IFG + 1) × 8 bit times between frames on Tx.	0xB	R/W

P1 MAC Loopback Enable Register

Address: 0xB3, Reset: 0x00000000, Name: P1_LOOP

Table 114. Bit Descriptions for P1_LOOP

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	P1_LOOPBACK_EN	MAC Loopback. Enable loopback on the MII to the PHY. 0: normal operation. Loopback disabled. 1: loopback enabled.	0x0	R/W

P1 CRC Check Enable on Receive Register

Address: 0xB4, Reset: 0x00000001, Name: P1_RX_CRC_EN

Table 115. Bit Descriptions for P1_RX_CRC_EN

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	P1_CRC_CHK_EN	CRC Check Enable on Receive.	0x1	R/W

P1 Receive Interframe Gap Register

Address: 0xB5, Reset: 0x0000000A, Name: P1_RX_IFG

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Table 116. Bit Descriptions for P1_RX_IFG

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	P1_RX_IFG	Interframe Gap. The receive MAC checks that the IFG is greater than P1_RX_IFG × 8 bit times. If the received IFG is too small, the MAC drops the received frame and asserts P1_RX_IFG_ERR. The maximum value supported in this field is 63 decimal.	0xA	R/W

P1 Maximum Receive Frame Length Register

Address: 0xB6, Reset: 0x00000618, Name: P1_RX_MAX_LEN

Maximum receive frame length in bytes.

Table 117. Bit Descriptions for P1_RX_MAX_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	P1_MAX_FRM_LEN	Maximum Frame Length on Receive.	0x618	R/W

P1 Minimum Receive Frame Length Register

Address: 0xB7, Reset: 0x00000040, Name: P1_RX_MIN_LEN

Minimum receive frame length in bytes.

Table 118. Bit Descriptions for P1_RX_MIN_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	P1_MIN_FRM_LEN	Minimum Frame Length on Receive.	0x40	R/W

P1 Rx Low Priority FIFO Frame Count Register

Address: 0xB8, Reset: 0x00000000, Name: P1_LO_RFC

The number of frames in the receive FIFO.

Table 119. Bit Descriptions for P1_LO_RFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	P1_LO_RFC	Receive Frame Count for the Low Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward mode, the host software only needs to know that there is at least one frame available. See P1_RX_RDY.	0x0	R

P1 Rx High Priority FIFO Frame Count Register

Address: 0xB9, Reset: 0x00000000, Name: P1_HI_RFC

The number of frames in the receive FIFO.

Table 120. Bit Descriptions for P1_HI_RFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R

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Table 120. Bit Descriptions for P1_HI_RFC (Continued)

Bits	Bit Name	Description	Reset	Access
[8:0]	P1_HI_RFC	Receive Frame Count for the High Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward mode, the host software only needs to know that there is at least one frame available. See P1_RX_RDY.	0x0	R

P1 Low Priority Rx FIFO Valid Half Words Register

Address: 0xBA, Reset: 0x00000000, Name: P1_LO_RXSIZE

Number of valid half words (16 bits) in the low priority Rx FIFO.

Table 121. Bit Descriptions for P1_LO_RXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	P1_LO_RXSIZE	Data in the Rx FIFO. Number of half words (16 Bits).	0x0	R

P1 High Priority Rx FIFO Valid Half Words Register

Address: 0xBB, Reset: 0x00000000, Name: P1_HI_RXSIZE

Number of valid half words (16 bits) in the high priority Rx FIFO.

Table 122. Bit Descriptions for P1_HI_RXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	P1_HI_RXSIZE	Data in the Rx FIFO. Number of half words (16 Bits).	0x0	R

P1 to P2 Tx Size Register

Address: 0xBC, Reset: 0x00000000, Name: P1TOP2_TXSIZE

Number of valid half words (16 Bits) in Port 1 Tx FIFO to be transmitted to Port 2.

Table 123. Bit Descriptions for P1TOP2_TXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	P1TOP2_TXSIZE	Data in Port 1 Tx FIFO. Number of 16-bit words to transmit to Port 1.	0x0	R

P2 MAC Rx Frame Size Register

Address: 0xC0, Reset: 0x00000000, Name: P2_RX_FSIZE

Table 124. Bit Descriptions for P2_RX_FSIZE

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved.	0x0	R
[10:0]	P2_RX_FRM_SIZE	Receive Frame Size. The size of the frame at the head of the Rx FIFO in bytes. The size includes the appended header. This register must be read before starting a frame transfer from a receive FIFO via P2_RX. Only used with the generic SPI protocol.	0x0	R

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P2 MAC Receive Register

Address: 0xC1, Reset: 0x00000000, Name: P2_RX

The receive FIFO is read via this register. It is possible to burst read data from the Rx FIFO over SPI.

Table 125. Bit Descriptions for P2_RX

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RDR	Receive Data Register. This field is only used with the generic SPI protocol. Reading this register returns the four bytes at the top of the receive FIFO and pops these four bytes from the FIFO. The upper 8 bits contain the first byte, the next 8 bits contain the second byte, and so on. When a complete frame is read out, no further data is returned from the Port 2 Rx FIFOs until the P2_RX_FRM_SIZE register is read first.	0x0	R

P2 Rx Frame Count Register

Address: 0xD0, Reset: 0x00000000, Name: P2_RX_FRM_CNT

Table 126. Bit Descriptions for P2_RX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_FRM_CNT	Rx Frame Count. This register increments for received good and bad frames.	0x0	R

P2 Rx Broadcast Frame Count Register

Address: 0xD1, Reset: 0x00000000, Name: P2_RX_BCAST_CNT

Table 127. Bit Descriptions for P2_RX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_BCAST_CNT	Rx Broadcast Frame Count. This counter increments for received good and bad frames.	0x0	R

P2 Rx Multicast Frame Count Register

Address: 0xD2, Reset: 0x00000000, Name: P2_RX_MCAST_CNT

Table 128. Bit Descriptions for P2_RX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_MCAST_CNT	Rx Multicast Frame Count. This counter increments for received good and bad frames.	0x0	R

P2 Rx Unicast Frame Count Register

Address: 0xD3, Reset: 0x00000000, Name: P2_RX_UCAST_CNT

Table 129. Bit Descriptions for P2_RX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_UCAST_CNT	Rx Unicast Frame Count. This counter increments for received good and bad frames.	0x0	R

P2 Rx CRC Errored Frame Count Register

Address: 0xD4, Reset: 0x00000000, Name: P2_RX_CRC_ERR_CNT

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Table 130. Bit Descriptions for P2_RX_CRC_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_CRC_ERR_CNT	Rx CRC Errored Frame Count.	0x0	R

P2 Rx Align Error Count Register

Address: 0xD5, Reset: 0x00000000, Name: P2_RX_ALGN_ERR_CNT

Table 131. Bit Descriptions for P2_RX_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_ALGN_ERR_CNT	Rx Align Error Count.	0x0	R

P2 Rx Long/Short Frame Error Count Register

Address: 0xD6, Reset: 0x00000000, Name: P2_RX_LS_ERR_CNT

Table 132. Bit Descriptions for P2_RX_LS_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_LS_ERR_CNT	Rx Long/Short Frame Error Count.	0x0	R

P2 Rx PHY Error Count Register

Address: 0xD7, Reset: 0x00000000, Name: P2_RX_PHY_ERR_CNT

This counter does not increment on LES because a PHY error cannot be determined via the reduced media independent interface (RMII). Instead, PHY errors are seen as CRC errored frames in the MAC. The PHY error counter on the PHY must be read to determine if there are PHY errors on Port 2.

Table 133. Bit Descriptions for P2_RX_PHY_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_PHY_ERR_CNT	Rx PHY Error Count.	0x0	R

P2 Tx Frame Count Register

Address: 0xD8, Reset: 0x00000000, Name: P2_TX_FRM_CNT

Table 134. Bit Descriptions for P2_TX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TX_FRM_CNT	Tx Frame Count.	0x0	R

P2 Tx Broadcast Frame Count Register

Address: 0xD9, Reset: 0x00000000, Name: P2_TX_BCAST_CNT

Table 135. Bit Descriptions for P2_TX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TX_BCAST_CNT	Tx Broadcast Frame Count.	0x0	R

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P2 Tx Multicast Frame Count Register

Address: 0xDA, Reset: 0x00000000, Name: P2_TX_MCAST_CNT

Table 136. Bit Descriptions for P2_TX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TX_MCAST_CNT	Tx Multicast Frame Count.	0x0	R

P2 Tx Unicast Frame Count Register

Address: 0xDB, Reset: 0x00000000, Name: P2_TX_UCAST_CNT

Table 137. Bit Descriptions for P2_TX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TX_UCAST_CNT	Tx Unicast Frame Count.	0x0	R

P2 Rx Frames Dropped Due to FIFO Full Register

Address: 0xDC, Reset: 0x00000000, Name: P2_RX_DROP_FULL_CNT

Table 138. Bit Descriptions for P2_RX_DROP_FULL_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_DROP_FULL_CNT	Rx Frames Dropped Due to FIFO Full. Note that on LES, if a received frame is destined for both the host and other port (a flooded frame), and the frame is not forwarded to one of the destination FIFOs because it is full, the frame is not counted as a dropped frame. That is, if the frame is flooded, the P2_RX_DROP_FULL_CNT only increments if both FIFOs are full.	0x0	R

P2 Rx Frames Dropped Due to Filtering Register

Address: 0xDD, Reset: 0x00000000, Name: P2_RX_DROP_FILT_CNT

Table 139. Bit Descriptions for P2_RX_DROP_FILT_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_DROP_FILT_CNT	Rx Frames Dropped Due to Filtering.	0x0	R

Frames Received on Port 2 with IFG Errors Register

Address: 0xDE, Reset: 0x00000000, Name: P2_RX_IFG_ERR_CNT

Table 140. Bit Descriptions for P2_RX_IFG_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_RX_IFG_ERR_CNT	IFG Error Counter for Port 2 Received Frames.	0x0	R

P2 Transmit Interframe Gap Register

Address: 0xE0, Reset: 0x0000000B, Name: P2_TX_IFG

Table 141. Bit Descriptions for P2_TX_IFG

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
[7:0]	P2_TX_IFG	Interframe Gap. Generates an IFG of (P2_TX_IFG + 1) × 8 bit times between frames on Tx.	0xB	R/W

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P2 MAC Loopback Enable Register

Address: 0xE3, Reset: 0x00000000, Name: P2_LOOP

Table 142. Bit Descriptions for P2_LOOP

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	P2_LOOPBACK_EN	MAC Loopback. Enable loopback on the MII to the PHY. 0: normal operation. Loopback disabled. 1: loopback enabled.	0x0	R/W

P2 CRC Check Enable on Receive Register

Address: 0xE4, Reset: 0x00000001, Name: P2_RX_CRC_EN

Table 143. Bit Descriptions for P2_RX_CRC_EN

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved.	0x0	R
0	P2_CRC_CHK_EN	CRC Check Enable on Receive.	0x1	R/W

P2 Receive Interframe Gap Register

Address: 0xE5, Reset: 0x0000000A, Name: P2_RX_IFG

Table 144. Bit Descriptions for P2_RX_IFG

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
[5:0]	P2_RX_IFG	Interframe Gap. The receive MAC checks that the IFG is greater than P2_RX_IFG × 8 bit times. If the received IFG is too small, the MAC drops the received frame and asserts P2_RX_IFG_ERR. The maximum value supported in this field is 63 decimal.	0xA	R/W

P2 Maximum Receive Frame Length Register

Address: 0xE6, Reset: 0x00000618, Name: P2_RX_MAX_LEN

Maximum receive frame length in bytes.

Table 145. Bit Descriptions for P2_RX_MAX_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	P2_MAX_FRM_LEN	Maximum Frame Length on Receive in Bytes.	0x618	R/W

P2 Minimum Receive Frame Length Register

Address: 0xE7, Reset: 0x00000040, Name: P2_RX_MIN_LEN

Minimum receive frame length in bytes.

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Table 146. Bit Descriptions for P2_RX_MIN_LEN

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	P2_MIN_FRM_LEN	Minimum Frame Length on Receive in Bytes.	0x40	R/W

P2 Rx Low Priority FIFO Frame Count Register

Address: 0xE8, Reset: 0x00000000, Name: P2_LO_RFC

The number of frames in the receive FIFO.

Table 147. Bit Descriptions for P2_LO_RFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	P2_LO_RFC	Receive Frame Count for the Low Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward mode, the host software only needs to know that there is at least one frame available. See P2_RX_RDY.	0x0	R

P2 Rx High Priority FIFO Frame Count Register

Address: 0xE9, Reset: 0x00000000, Name: P2_HI_RFC

The number of frames in the receive FIFO.

Table 148. Bit Descriptions for P2_HI_RFC

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved.	0x0	R
[8:0]	P2_HI_RFC	Receive Frame Count for the High Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward mode, the host software only needs to know that there is at least one frame available. See P2_RX_RDY.	0x0	R

P2 Low Priority Rx FIFO Valid Half Words Register

Address: 0xEA, Reset: 0x00000000, Name: P2_LO_RXSIZE

Number of valid half words (16 bits) in the low priority Rx FIFO.

Table 149. Bit Descriptions for P2_LO_RXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	P2_LO_RXSIZE	Data in the Rx FIFO. Number of half words (16 bits).	0x0	R

P2 High Priority Rx FIFO Valid Half Words Register

Address: 0xEB, Reset: 0x00000000, Name: P2_HI_RXSIZE

Number of valid half words (16 bits) in the high priority Rx FIFO.

Table 150. Bit Descriptions for P2_HI_RXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R

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Table 150. Bit Descriptions for P2_HI_RXSIZE (Continued)

Bits	Bit Name	Description	Reset	Access
[13:0]	P2_HI_RXSIZE	Data in the Rx FIFO. Number of half words (16 bits).	0x0	R

P2 to P1 Tx Size Register

Address: 0xEC, Reset: 0x00000000, Name: P2TOP1_TXSIZE

Number of valid half words (16 bits) in Port 2 Tx FIFO to be transmitted to Port 1.

Table 151. Bit Descriptions for P2TOP1_TXSIZE

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved.	0x0	R
[13:0]	P2TOP1_TXSIZE	Data in Port 2 Tx FIFO. Number of 16-bit words to transmit to Port 2.	0x0	R

Transmit Time Stamp Capture Register A (High)

Address: 0xF0, Reset: 0x00000000, Name: P2_TTSCAH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 152. Bit Descriptions for P2_TTSCAH

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCH_A	Port 2 Transmit Time Stamp A, Bits[63:32].	0x0	R

Transmit Time Stamp Capture Register A (Low)

Address: 0xF1, Reset: 0x00000000, Name: P2_TTSCAL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 153. Bit Descriptions for P2_TTSCAL

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCL_A	Port 2 Transmit Time Stamp A, Bits[31:0].	0x0	R

Transmit Time Stamp Capture Register B (High)

Address: 0xF2, Reset: 0x00000000, Name: P2_TTSCBH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 154. Bit Descriptions for P2_TTSCBH

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCH_B	Port 2 Transmit Time Stamp B, Bits[63:32].	0x0	R

Transmit Time Stamp Capture Register B (Low)

Address: 0xF3, Reset: 0x00000000, Name: P2_TTSCBL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

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Table 155. Bit Descriptions for P2_TTSCBL

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCL_B	Port 2 Transmit Time Stamp B, Bits[31:0].	0x0	R

Transmit Time Stamp Capture Register C (High)

Address: 0xF4, Reset: 0x00000000, Name: P2_TTSCCH

This field contains the upper 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 156. Bit Descriptions for P2_TTSCCH

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCH_C	Port 2 Transmit Time Stamp C, Bits[63:32].	0x0	R

Transmit Time Stamp Capture Register C (Low)

Address: 0xF5, Reset: 0x00000000, Name: P2_TTSCCL

This field contains the lower 32 bits of the captured time stamp for when the requested frame was transmitted.

Table 157. Bit Descriptions for P2_TTSCCL

Bits	Bit Name	Description	Reset	Access
[31:0]	P2_TTSCL_C	Port 2 Transmit Time Stamp C, Bits[31:0].	0x0	R

PHY CLAUSE 22 REGISTER DETAILS

Register Summary: 10BASE-T1L Single Pair Ethernet PHY Core (ADIN2111)

Table 158. ADIN2111 Register Summary

Address	Name	Description	Reset	Access
0x0	MI_CONTROL	MII Control Register.	0x1100	R/W
0x1	MI_STATUS	MII Status Register.	0x1009	R
0x2	MI_PHY_ID1	PHY Identifier 1 Register.	0x0283	R
0x3	MI_PHY_ID2	PHY Identifier 2 Register.	0xBC01	R
0xD	MMD_ACCESS_CNTRL	MMD Access Control.	0x0000	R/W
0xE	MMD_ACCESS	MMD Access.	0x0000	R/W

MII Control Register

Address: 0x0, Reset: 0x1100, Name: MI_CONTROL

This address corresponds to the MII control register specified in Clause 22.2.4.1 of Standard 802.3.

Table 159. Bit Descriptions for MI_CONTROL

Bits	Bit Name	Description	Reset	Access
15	MI_SFT_RST	Software Reset. The software reset bit allows a software reset cycle to be initiated. Mirrors CRSM_SFT_RST.	0x0	R/W SC
14	MI_LOOPBACK	Local Loopback (PCS). The loopback bit allows the PHY loopback mode to be engaged. Mirrors LB_PCS_EN.	0x0	R/W
13	MI_SPEED_SEL_LSB	MII Speed Selection LSB. See MI_SPEED_SEL_MSB.	0x0	R

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Table 159. Bit Descriptions for MI_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
12	MI_AN_EN	Autonegotiation Enable. Use the AN_FRC_MODE_EN bit to enable forced link configuration mode. Mirrors AN_EN. 1 = enable autonegotiation. 0 = disable autonegotiation.	0x1	R
11	MI_SFT_PD	Software Power-Down. The software power-down bit allows the PHY to be placed in software power-down mode. In this mode, most of the PHY circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via the RX_DV/RX_CTL/$\overline{\text{SWPD_EN}}$ pin, which allows the PHY to be held in reset until an appropriate software initialization has been performed. Mirrors CRSM_SFT_PD.	Pin Dependent	R/W
10	MI_ISOLATE	MII Isolate. This bit field allows the PHY to be isolated from the MII.	0x0	R/W
9	RESERVED	Reserved.	0x0	R/W SC
8	MI_FULL_DUPLEX	MII Full Duplex. The duplex mode register cannot be written and always reads as 1 because the PHY is only able to operate in full duplex mode.	0x1	R
7	MI_COLTEST	MII Collision Test. The collision test bit cannot be written and always reads as 0 because the PHY is only able to operate in full duplex mode, and does not have a collision detect MII (COL) pin.	0x0	R
6	MI_SPEED_SEL_MSB	MII Speed Selection MSB. The speed selection MSB and LSB bits cannot be written and always reads as 00 because the PHY is only able to operate at 10 Mbps.	0x0	R
5	MI_UNIDIR_EN	MII Unidirectional Enable. The unidirectional enable bit cannot be written and always reads as 0 because the PHY does not have the ability to transmit data from the MII regardless of whether it has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

MII Status Register

Address: 0x1, Reset: 0x1009, Name: MI_STATUS

This address corresponds to the MII status register specified in Clause 22.2.4.2 of Standard 802.3.

Table 160. Bit Descriptions for MI_STATUS

Bits	Bit Name	Description	Reset	Access
15	MI_T4_SPRT	100BASE-T4 Ability. The 100BASE-T4 ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
14	MI_FD100_SPRT	Full Duplex 100BASE-X Ability. The 100BASE-X full duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
13	MI_HD100_SPRT	Half-Duplex 100BASE-X Ability. The 100BASE-X half-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
12	MI_FD10_SPRT	Full Duplex 10 Mbps Ability. The 10 Mbps full duplex ability bit indicates that the PHY supports this technology.	0x1	R
11	MI_HD10_SPRT	Half Duplex 10 Mbps Ability. The 10 Mbps half duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
10	MI_FD_T2_SPRT	Full Duplex 100BASE-T2 Ability. The 100BASE-T2 full duplex ability bits always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
9	MI_HD_T2_SPRT	Half Duplex 100BASE-T2- Ability. The 100BASE-T2 half duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
8	MI_EXT_STAT_SPRT	Extended Status Support. The extended status support bit always reads as 0 to indicate that the PHY does not provide extended status information in Register 0xF.	0x0	R
7	MI_UNIDIR_ABLE	Unidirectional Ability. The unidirectional ability register always reads as 0 to indicate that the PHY can only transmit data from the MII when it determines that a valid link is established.	0x0	R

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Table 160. Bit Descriptions for MI_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
6	MI_MF_PREAM_SUP_ABLE	Management Preamble Suppression Ability. The management frame preamble suppression ability bit always reads as 0 to indicate that the PHY is not able to receive management frames that are not preceded by the preamble pattern.	0x0	R
5	MI_AN_COMPLETE	Autonegotiation Complete. The autonegotiation complete bit indicates that the autonegotiation process completed and the PHY link is up. Mirrors AN_COMPLETE.	0x0	R
4	MI_REM_FLT	Remote Fault. The remote fault bit always reads as 0 because the PHY has no provision for remote fault detection.	0x0	R LH
3	MI_AN_ABLE	Autonegotiation Ability. The autonegotiation ability bit always reads as 1 indicating that the PHY has the ability to perform autonegotiation. Mirrors AN_ABLE.	0x1	R
2	MI_LINK_STAT_LAT	Link Status. This bit uses a latch low functionality as described in IEEE Standard 802.3 Subclause 45.2.7.20.5. If the link status value is fail, this register stays cleared and remains cleared until the latching is cleared when the register is read. Mirrors AN_LINK_STATUS.	0x0	R LL
1	MI_JABBER_DET	MII Jabber Detect. The jabber detect bit always reads as 0 because the 10BASE-T1L PHY does not incorporate a jabber detect function.	0x0	R LH
0	MI_EXT_CAPABLE	MII Extended Capability. The extended capability bit always reads as 1 indicating that the PHY provides an extended set of capabilities that can be accessed through the extended register set. The extended register set consists of all of the management registers except 0x0, 0x1, and 0xF.	0x1	R

PHY Identifier 1 Register

Address: 0x2, Reset: 0x0283, Name: MI_PHY_ID1

The PHY Identifier 1 address allows 16 bits of the OUI to be observed.

Table 161. Bit Descriptions for MI_PHY_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MI_PHY_ID1	The PHY Identifier 1 address allows 16 bits of the OUI to be observed.	0x283	R

PHY Identifier 2 Register

Address: 0x3, Reset: 0xBC01, Name: MI_PHY_ID2

The PHY Identifier 2 address allows six bits of the OUI, and the model and revision number to be observed.

Table 162. Bit Descriptions for MI_PHY_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MI_PHY_ID2_OUI	OUI, Bits[7:2].	0x2F	R
[9:4]	MI_MODEL_NUM	Model Number.	Pin dependent	R
[3:0]	MI_REV_NUM	Revision Number.	0x1	R

MMD Access Control Register

Address: 0xD, Reset: 0x0000, Name: MMD_ACCESS_CNTRL

This address corresponds to the MMD access control register specified in Clause 22.2.4.3.11 of IEEE Standard 802.3-2018.

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Table 163. Bit Descriptions for MMD_ACCESS_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD_ACR_FUNCTION	Function. The function bits select the type of MMD access on accesses to the MMD_ACCESS register. 00: address. 01: data, no post increment. 10: data, post increment on reads and writes. 11: data, post increment on writes only.	0x0	R/W
[13:5]	RESERVED	Reserved.	0x0	R
[4:0]	MMD_ACR_DEVAD	Device Address. The value in this bit directs any accesses to the MMD_ACCESS register to the selected MMD.	0x0	R/W

MMD Access Register

Address: 0xE, Reset: 0x0000, Name: MMD_ACCESS

This address corresponds to the MMD access address data register specified in Clause 22.2.4.3.12 of IEEE Standard 802.3-2018.

The MMD_ACCESS register is used in conjunction with the MMD_ACCESS_CNTRL register to provide access to the MMD address space using the interface and mechanisms defined in Clause 22.2.4.

Table 164. Bit Descriptions for MMD_ACCESS

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD_ACCESS	Access Address. This address corresponds to the MMD access address data register specified in Clause 22.2.4.3.12 of IEEE Standard 802.3-2018. The MMD_ADDR_DATA register is used with the MMD_ACCESS_CNTRL register to provide access to the MMD address space using the interface and mechanisms defined in Clause 22.2.4.	0x0	R/W

PHY CLAUSE 45 REGISTER DETAILS

Register Summary: 10BASE-T1L Single Pair Ethernet PHY Core (ADIN2111)

Table 165. ADIN2111 Register Summary

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x0000	PMA_PMD_CNTRL1	PMA/PMD Control 1 Register.	0x0000	R/W
0x01	0x0001	PMA_PMD_STAT1	PMA/PMD Status 1 Register.	0x0002	R
0x01	0x0005	PMA_PMD_DEVS_IN_PKG1	PMA/PMD MMD Devices in Package 1.	0x008B	R
0x01	0x0006	PMA_PMD_DEVS_IN_PKG2	PMA/PMD MMD Devices in Package 2 Register.	0xC000	R
0x01	0x0007	PMA_PMD_CNTRL2	PMA/PMD Control 2 Register.	0x003D	R/W
0x01	0x0008	PMA_PMD_STAT2	PMA/PMD Status 2.	0x8301	R
0x01	0x0009	PMA_PMD_TX_DIS	PMA/PMD Transmit Disable Register.	0x0000	R/W
0x01	0x000B	PMA_PMD_EXT_ABILITY	PMA/PMD Extended Abilities Register.	0x0800	R
0x01	0x0012	PMA_PMD_BT1_ABILITY	BASE-T1 PMA/PMD Extended Ability Register.	0x0004	R
0x01	0x0834	PMA_PMD_BT1_CONTROL	BASE-T1 PMA/PMD Control Register.	0x8002	R/W

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Table 165. ADIN2111 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x08F6	B10L_PMA_CNTRL	10BASE-T1L PMA Control Register.	0x0000	R/W
0x01	0x08F7	B10L_PMA_STAT	10BASE-T1L PMA Status Register.	0x2800	R
0x01	0x08F8	B10L_TEST_MODE_CNTRL	10BASE-T1L Test Mode Control Register.	0x0000	R/W
0x01	0x8302	B10L_PMA_LINK_STAT	10BASE-T1L PMA Link Status Register.	0x0000	R
0x01	0x830B	MSE_VAL	Mean Squared Error (MSE) Value Register.	0x0000	R
0x03	0x0000	PCS_CNTRL1	PCS Control 1 Register.	0x0000	R/W
0x03	0x0001	PCS_STAT1	PCS Status 1 Register.	0x0002	R
0x03	0x0005	PCS_DEVS_IN_PKG1	PCS MMD Devices in Package 1 Register.	0x008B	R
0x03	0x0006	PCS_DEVS_IN_PKG2	PCS MMD Devices in Package 2 Register.	0xC000	R
0x03	0x0008	PCS_STAT2	PCS Status 2 Register.	0x8000	R
0x03	0x08E6	B10L_PCS_CNTRL	10BASE-T1L PCS Control Register.	0x0000	R/W
0x03	0x08E7	B10L_PCS_STAT	10BASE-T1L PCS Status Register.	0x0000	R
0x07	0x0005	AN_DEVS_IN_PKG1	Autonegotiation MMD Devices in Package 1 Register.	0x008B	R
0x07	0x0006	AN_DEVS_IN_PKG2	Autonegotiation MMD Devices in Package 2 Register.	0xC000	R
0x07	0x0200	AN_CONTROL	BASE-T1 Autonegotiation Control Register.	0x1000	R/W
0x07	0x0201	AN_STATUS	BASE-T1 Autonegotiation Status Register.	0x0008	R
0x07	0x0202	AN_ADV_ABILITY_L	BASE-T1 Autonegotiation Advertisement Register, Bits[15:0].	0x0001	R/W
0x07	0x0203	AN_ADV_ABILITY_M	BASE-T1 Autonegotiation Advertisement Register, Bits[31:16].	0x4000	R/W
0x07	0x0204	AN_ADV_ABILITY_H	BASE-T1 Autonegotiation Advertisement Register, Bits[47:32].	0x0000	R/W
0x07	0x0205	AN_LP_ADV_ABILITY_L	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[15:0].	0x0000	R
0x07	0x0206	AN_LP_ADV_ABILITY_M	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[31:16].	0x0000	R
0x07	0x0207	AN_LP_ADV_ABILITY_H	BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[47:32].	0x0000	R
0x07	0x0208	AN_NEXT_PAGE_L	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[15:0].	0x2001	R/W
0x07	0x0209	AN_NEXT_PAGE_M	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[31:16].	0x0000	R/W

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Table 165. ADIN2111 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x07	0x020A	AN_NEXT_PAGE_H	BASE-T1 Autonegotiation Next Page Transmit Register, Bits[47:32].	0x0000	R/W
0x07	0x020B	AN_LP_NEXT_PAGE_L	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[15:0].	0x0000	R
0x07	0x020C	AN_LP_NEXT_PAGE_M	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[31:16].	0x0000	R
0x07	0x020D	AN_LP_NEXT_PAGE_H	BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[47:32].	0x0000	R
0x07	0x020E	AN_B10_ADV_ABILITY	10BASE-T1 Autonegotiation Control Register.	0x8000	R/W
0x07	0x020F	AN_B10_LP_ADV_ABILITY	10BASE-T1 Autonegotiation Status Register.	0x0000	R
0x07	0x8000	AN_FRC_MODE_EN	Autonegotiation Force Mode Enable Register.	0x0000	R/W
0x07	0x8001	AN_STATUS_EXTRA	Extra Autonegotiation Status Register.	0x0000	R
0x07	0x8030	AN_PHY_INST_STATUS	PHY Instantaneous Status.	0x0010	R
0x1E	0x0002	MMD1_DEV_ID1	Vendor Specific MMD 1 Device Identifier High Register.	0x0283	R
0x1E	0x0003	MMD1_DEV_ID2	Vendor Specific MMD 1 Device Identifier Low Register.	0xBC01	R
0x1E	0x0005	MMD1_DEVS_IN_PKG1	Vendor Specific 1 MMD Devices in Package Register.	0x008B	R
0x1E	0x0006	MMD1_DEVS_IN_PKG2	Vendor Specific 1 MMD Devices in Package Register.	0xC000	R
0x1E	0x0008	MMD1_STATUS	Vendor Specific MMD 1 Status Register.	0x8000	R
0x1E	0x0010	CRSM_IRQ_STATUS	System Interrupt Status Register.	0x1000	R
0x1E	0x0020	CRSM_IRQ_MASK	System Interrupt Mask Register.	0x1BFE	R/W
0x1E	0x8810	CRSM_SFT_RST	Software Reset Register.	0x0000	R/W
0x1E	0x8812	CRSM_SFT_PD_CNTRL	Software Power-down Control Register.	0x0000	R/W
0x1E	0x8814	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset Register.	0x0000	R/W
0x1E	0x8815	CRSM_MAC_IF_RST	PHY MAC Interface Reset Register.	0x0000	R/W
0x1E	0x8818	CRSM_STAT	System Status Register.	0x0000	R
0x1E	0x8819	CRSM_PMG_CNTRL	Clock, Reset, and State Machine (CRSM) Power Management Control Register.	0x0000	R/W
0x1E	0x882C	CRSM_DIAG_CLK_CTRL	CRSM Diagnostics Clock Control.	0x0002	R/W
0x1E	0x8C22	MGMT_PRT_PKG	Package Configuration Values Register.	0x0000	R
0x1E	0x8C30	MGMT_MDIO_CNTRL	MDIO Control Register.	0x0000	R/W

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Table 165. ADIN2111 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x1E	0x8C56	DIGIO_PINMUX	Pin Mux Configuration 1 Register.	0x00FE	R/W
0x1E	0x8C80	LED0_BLINK_TIME_CNTRL	LED_0 On/Off Blink Time Register.	0x3636	R/W
0x1E	0x8C81	LED1_BLINK_TIME_CNTRL	LED_1 On/Off Blink Time Register.	0x3636	R/W
0x1E	0x8C82	LED_CNTRL	LED Control Register.	0x8E80	R/W
0x1E	0x8C83	LED_POLARITY	LED Polarity Register.	0x0000	R/W
0x1F	0x0002	MMD2_DEV_ID1	Vendor Specific MMD 2 Device Identifier High Register.	0x0283	R
0x1F	0x0003	MMD2_DEV_ID2	Vendor Specific MMD 2 Device Identifier Low Register.	0xBC01	R
0x1F	0x0005	MMD2_DEVS_IN_PKG1	Vendor Specific 2 MMD Devices in Package Register.	0x008B	R
0x1F	0x0006	MMD2_DEVS_IN_PKG2	Vendor Specific 2 MMD Devices in Package Register.	0xC000	R
0x1F	0x0008	MMD2_STATUS	Vendor Specific MMD 2 Status Register.	0x8000	R
0x1F	0x0011	PHY_SUBSYS_IRQ_STATUS	PHY Subsystem Interrupt Status Register.	0x0000	R
0x1F	0x0021	PHY_SUBSYS_IRQ_MASK	PHY Subsystem Interrupt Mask Register.	0x2402	R/W
0x1F	0x8001	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x1F	0x8004	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x1F	0x8005	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x1F	0x8008	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x1F	0x8009	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x1F	0x800A	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x1F	0x800B	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R
0x1F	0x800C	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R
0x1F	0x800D	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Count Register.	0x0000	R
0x1F	0x800E	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R
0x1F	0x800F	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x1F	0x8010	FC_ODD_CNT	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x1F	0x8011	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x1F	0x8013	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x1F	0x8020	FG_EN	Frame Generator Enable Register.	0x0000	R/W

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Table 165. ADIN2111 Register Summary (Continued)

Device Address	Register Address	Name	Description	Reset	Access
0x1F	0x8021	FG_CNTRL_RSTRT	Frame Generator Control/Restart Register.	0x0001	R/W
0x1F	0x8022	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x1F	0x8023	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x1F	0x8025	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x1F	0x8026	FG_IFG_LEN	Frame Generator Interframe Gap Length Register.	0x000C	R/W
0x1F	0x8027	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W
0x1F	0x8028	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x1F	0x8029	FG_DONE	Frame Generator Done Register.	0x0000	R
0x1F	0x8055	MAC_IF_LOOPBACK	MAC Interface Loopbacks Configuration Register.	0x000A	R/W
0x1F	0x805A	MAC_IF_SOP_CNTRL	MAC Start of Packet (SOP) Generation Control Register.	0x001B	R/W

PMA/PMD Control 1 Register

Device Address: 0x01; Register Address: 0x0000, Reset: 0x0000, Name: PMA_PMD_CNTRL1

This address corresponds to the PMA/PMD Control Register 1 specified in Clause 45.2.1.1 of Standard 802.3. Note that the reset value of this register is dependent on the hardware configuration pin settings.

Table 166. Bit Descriptions for PMA_PMD_CNTRL1

Bits	Bit Name	Description	Reset	Access
15	PMA_SFT_RST	PMA Software Reset. The PMA software reset bit allows the chip to be reset. When this bit is set, the chip fully initializes, almost equivalent to a hardware reset. This bit is self clearing and returns a value of 1 when a reset is in progress. Otherwise, it returns a value of 0.	0x0	R/W SC
[14:12]	RESERVED	Reserved.	0x0	R
11	PMA_SFT_PD	PMA Software Power-Down. The PMA software power-down bit puts the chip in a lower power mode. In this mode, most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this bit is configurable via the $\overline{\text{Px_SWPD_EN}}$ pin, which allows the chip to be held in power-down mode until an appropriate software initialization is performed.	0x0	R/W
[10:1]	RESERVED	Reserved.	0x0	R
0	LB_PMA_LOC_EN	Enables PMA Local Loopback. When this bit is set to 1, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PMA works in normal mode.	0x0	R/W

PMA/PMD Status 1 Register

Device Address: 0x01; Register Address: 0x0001, Reset: 0x0002, Name: PMA_PMD_STAT1

This address corresponds to the PMA/PMD Status Register 1 specified in Clause 45.2.1.2 of Standard 802.3.

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Table 167. Bit Descriptions for PMA_PMD_STAT1

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	PMA_LINK_STAT_OK_LL	PMA Link Status. When read as 1, this bit indicates that the link is up. When read as 0, it indicates that the link has dropped since the last time the bit was read.	0x0	R LL
1	PMA_SFT_PD_ABLE	PMA Software Power-Down Able. Indicates that the PMA supports software power-down.	0x1	R
0	RESERVED	Reserved.	0x0	R

PMA/PMD MMD Devices in Package 1 Register

Device Address: 0x01; Register Address: 0x0005, Reset: 0x008B, Name: PMA_PMD_DEVS_IN_PKG1

Table 168. Bit Descriptions for PMA_PMD_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	PMA_PMD_DEVS_IN_PKG1	PMA/PMD MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

PMA/PMD MMD Devices in Package 2 Register

Device Address: 0x01; Register Address: 0x0006, Reset: 0xC000, Name: PMA_PMD_DEVS_IN_PKG2

Table 169. Bit Descriptions for PMA_PMD_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	PMA_PMD_DEVS_IN_PKG2	PMA/PMD MMD Devices in Package 2. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

PMA/PMD Control 2 Register

Device Address: 0x01; Register Address: 0x0007, Reset: 0x003D, Name: PMA_PMD_CNTRL2

Table 170. Bit Descriptions for PMA_PMD_CNTRL2

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:0]	PMA_PMD_TYPE_SEL	PMA/PMD Type Selection. See IEEE Standard 802.3. PMA_PMD_TYPE_SEL is used only when autonegotiation is disabled and forced link configuration mode is enabled. If autonegotiation is enabled, the PHY type is determined by the autonegotiation process itself. Note that for ADIN2111, the only valid value for this bit field is for BASE-T1 PMA/PMD. 0000000: TS_10GBASE_CX4_PMA_PMD. 0000001: TS_10GBASE_EW_PMA_PMD. 0000010: TS_10GBASE_LW_PMA_PMD. 0000011: TS_10GBASE_SW_PMA_PMD. 0000100: TS_10GBASE_LX4_PMA_PMD. 0000101: TS_10GBASE_ER_PMA_PMD. 0000110: TS_10GBASE_LR_PMA_PMD. 0000111: TS_10GBASE_SR_PMA_PMD. 0001000: TS_10GBASE_LRM_PMA_PMD. 0001001: TS_10GBASE_T_PMA. 0001010: TS_10GBASE_KX4_PMA_PMD. 0001011: TS_10GBASE_KR_PMA_PMD.	0x3D	R/W

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Table 170. Bit Descriptions for PMA_PMD_CNTRL2 (Continued)

Bits	Bit Name	Description	Reset	Access
		0001100: TS_1000BASE_T_PMA_PMD. 0001101: TS_1000BASE_KX_PMA_PMD. 0001110: TS_100BASE_TX_PMA_PMD. 0001111: TS_10BASE_T_PMA_PMD. 0010000: TS_10_1GBASE_PRX_D1. 0010001: TS_10_1GBASE_PRX_D2. 0010010: TS_10_1GBASE_PRX_D3. 0010011: TS_10GBASE_PR_D1. 0010100: TS_10GBASE_PR_D2. 0010101: TS_10GBASE_PR_D3. 0010110: TS_10_1GBASE_PRX_U1. 0010111: TS_10_1GBASE_PRX_U2. 0011000: TS_10_1GBASE_PRX_U3. 0011001: TS_10GBASE_PR_U1. 0011010: TS_10GBASE_PR_U3. 0011011: TS_RESERVED. 0011100: TS_10GBASE_PR_D4. 0011101: TS_10_1GBASE_PRX_D4. 0011110: TS_10GBASE_PR_U4. 0011111: TS_10_1GBASE_PRX_U4. 0100000: TS_40GBASE_KR4_PMA_PMD. 0100001: TS_40GBASE_CR4_PMA_PMD. 0100010: TS_40GBASE_SR4_PMA_PMD. 0100011: TS_40GBASE_LR4_PMA_PMD. 0100100: TS_40GBASE_FR_PMA_PMD. 0100101: TS_40GBASE_ER4_PMA_PMD. 0100110: TS_40GBASE_T_PMA. 0101000: TS_100GBASE_CR10_PMA_PMD. 0101001: TS_100GBASE_SR10_PMA_PMD. 0101010: TS_100GBASE_LR4_PMA_PMD. 0101011: TS_100GBASE_ER4_PMA_PMD. 0101100: TS_100GBASE_KP4_PMA_PMD. 0101101: TS_100GBASE_KR4_PMA_PMD. 0101110: TS_100GBASE_CR4_PMA_PMD. 0101111: TS_100GBASE_SR4_PMA_PMD. 0110000: TS_2_5GBASE_T_PMA. 0110001: TS_5GBASE_T_PMA. 0110010: TS_10GPASS_XR_D_PMA_PMD. 0110011: TS_10GPASS_XR_U_PMA_PMD. 0110100: TS_BASE_H_PMA_PMD. 0110101: TS_25GBASE_LR_PMA_PMD. 0110110: TS_25GBASE_ER_PMA_PMD. 0110111: TS_25GBASE_T_PMA. 0111000: TS_25GBASE_CR_OR_25GBASE_CR_S_PMA_PMD.		

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Table 170. Bit Descriptions for PMA_PMD_CNTRL2 (Continued)

Bits	Bit Name	Description	Reset	Access
		0111001: TS_25GBASE_KR_OR_25GBASE_KR_S_PMA_PMD. 0111010: TS_25GBASE_SR_PMA_PMD. 0111101: TS_BASE_T1_PMA_PMD. 1010011: TS_200GBASE_DR4_PMA_PMD. 1010100: TS_200GBASE_FR4_PMA_PMD. 1010101: TS_200GBASE_LR4_PMA_PMD. 1011001: TS_400GBASE_SR16_PMA_PMD. 1011010: TS_400GBASE_DR4_PMA_PMD. 1011011: TS_400GBASE_FR8_PMA_PMD. 1011100: TS_400GBASE_LR8_PMA_PMD.		

PMA/PMD Status 2 Register

Device Address: 0x01; Register Address: 0x0008, Reset: 0x8301, Name: PMA_PMD_STAT2

Table 171. Bit Descriptions for PMA_PMD_STAT2

Bits	Bit Name	Description	Reset	Access
[15:14]	PMA_PMD_PRESENT	PMA/PMD Present. Indicates that the PMA is present and responding.	0x2	R
[13:10]	RESERVED	Reserved.	0x0	R
9	PMA_PMD_EXT_ABLE	PHY Extended Abilities Support. Indicates that the PHY supports extended abilities as listed in PMA_PMD_EXT_ABILITY.	0x1	R
8	PMA_PMD_TX_DIS_ABLE	PMA/PMD Tx Disable. Indicates that the PMA supports transmit disable.	0x1	R
[7:1]	RESERVED	Reserved.	0x0	R
0	LB_PMA_LOC_ABLE	PMA Local Loopback Able. Indicates that the PMA supports local loopback.	0x1	R

PMA/PMD Transmit Disable Register

Device Address: 0x01; Register Address: 0x0009, Reset: 0x0000, Name: PMA_PMD_TX_DIS

This address corresponds to the PMD transmit disable register specified in Clause 45.2.1.8 of Standard 802.3.

Table 172. Bit Descriptions for PMA_PMD_TX_DIS

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	PMA_TX_DIS	PMD Transmit Disable. When this bit is set to 1, the PMD disables the output on the transmit path. Otherwise, the PMD enables the output on the transmit path.	0x0	R/W

PMA/PMD Extended Abilities Register

Device Address: 0x01; Register Address: 0x000B, Reset: 0x0800, Name: PMA_PMD_EXT_ABILITY

PMA/PMD extended abilities.

Table 173. Bit Descriptions for PMA_PMD_EXT_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	PMA_PMD_BT1_ABLE	PHY Supports BASE-T1. Indicates that the PHY supports BASE-T1 extended abilities as listed in PMA_PMD_BT1_ABILITY.	0x1	R

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Table 173. Bit Descriptions for PMA_PMD_EXT_ABILITY (Continued)

Bits	Bit Name	Description	Reset	Access
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 PMA/PMD Extended Ability Register

Device Address: 0x01; Register Address: 0x0012, Reset: 0x0004, Name: PMA_PMD_BT1_ABILITY

This address corresponds to the BASE-T1 PMA/PMD extended ability register specified in Clause 45.2.1.16 of Standard 802.3. This register is read only and writes have no effect.

Table 174. Bit Descriptions for PMA_PMD_BT1_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	B10S_ABILITY	10BASE-T1S Ability. This bit always reads as 0 because the PMA/PMD does not support 10BASE-T1S.	0x0	R
2	B10L_ABILITY	10BASE-T1L Ability. This bit always reads as 1 because the PMA/PMD supports 10BASE-T1L.	0x1	R
1	B1000_ABILITY	1000BASE-T1 Ability. This bit always reads as 0 because the PMA/PMD does not support 1000BASE-T1.	0x0	R
0	B100_ABILITY	100BASE-T1 Ability. This bit always reads as 0 because the PMA/PMD does not support 100BASE-T1.	0x0	R

BASE-T1 PMA/PMD Control Register

Device Address: 0x01; Register Address: 0x0834, Reset: 0x8002, Name: PMA_PMD_BT1_CONTROL

This address corresponds to the BASE-T1 PMA/PMD control register specified in Clause 45.2.1.185 of Standard 802.3.

Table 175. Bit Descriptions for PMA_PMD_BT1_CONTROL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x1	R
14	CFG_MST	Master and Slave Configuration. CFG_MST is used only when autonegotiation is disabled. Otherwise, this value is determined by the autonegotiation process itself. When this bit is set as 1, the device is configured as a master. Otherwise, the device is configured as a slave.	0x1 (PORT1), 0x0 (PORT2)	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	BT1_TYPE_SEL	BASE-T1 Type Selection. See IEEE Standard 802.3 for the following control register bit definitions (where X means don't care): 1XXX: Reserved. 01XX: Reserved. 0011: 10BASE-T1S. 0010: 10BASE-T1L. 0001: 1000BASE-T1. 0000: 100BASE-T1. BT1_TYPE_SEL is used only when autonegotiation is disabled and forced link configuration mode is enabled. If autonegotiation is enabled, the PHY type is determined by the autonegotiation process itself. Note that for ADIN2111, the only valid value is for 10BASE-T1L. 0010: 10BASE-T1L.	0x2	R/W

10BASE-T1L PMA Control Register

Device Address: 0x01; Register Address: 0x08F6, Reset: 0x0000, Name: B10L_PMA_CNTRL

This address corresponds to the 10BASE-T1L PMA control register specified in Clause 45.2.1.186a of Standard 802.3cg

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Table 176. Bit Descriptions for B10L_PMA_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_TX_DIS_MODE_EN	10BASE-T1L Transmit Disable Mode. When this bit is set to 1, it disables output on the transmit path. Otherwise, it enables output on the transmit path.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
12	B10L_TX_LVL_HI	10BASE-T1L Transmit Voltage Amplitude Control. This configuration is only used when autonegotiation is disabled. Otherwise, the configuration is decided by the autonegotiation process. When this bit is set as 1, the device works in the 2.4 V p-p operating mode. Otherwise, the device works in the 1.0 V p-p operating mode.	Pin dependent	R/W
11	RESERVED	Reserved.	0x0	R/W
10	B10L_EEE	10BASE-T1L EEE Enable.	0x0	R/W
[9:1]	RESERVED	Reserved.	0x0	R
0	B10L_LB_PMA_LOC_EN	10BASE-T1L PMA Loopback. When this bit is set to 1, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PMA works in normal mode.	0x0	R/W

10BASE-T1L PMA Status Register

Device Address: 0x01; Register Address: 0x08F7, Reset: 0x2800, Name: B10L_PMA_STAT

This address corresponds to the 10BASE-T1L PMA status register specified in Clause 45.2.1.186b of Standard 802.3cg

Table 177. Bit Descriptions for B10L_PMA_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_LB_PMA_LOC_ABLE	10BASE-T1L PMA Loopback Ability. This bit always reads as 1 because the PMA has loopback ability.	0x1	R
12	B10L_TX_LVL_HI_ABLE	10BASE-T1L High Voltage Tx Ability. Indicates that the PHY supports 10BASE-T1L high voltage (2.4 V p-p) transmit level operating mode.	Pin dependent	R
11	B10L_PMA_SFT_PD_ABLE	PMA Supports Power-Down. Indicates that the PMA supports software power-down.	0x1	R
10	B10L_EEE_ABLE	10BASE-T1L EEE Ability. Indicates if the PHY supports 10BASE-T1L EEE.	0x0	R
[9:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L Test Mode Control Register

Device Address: 0x01; Register Address: 0x08F8, Reset: 0x0000, Name: B10L_TEST_MODE_CNTRL

This address corresponds to the 10BASE-T1L PMA test mode control register specified in Clause 45.2.1.186c of Standard 802.3cg. The default value of this register selects normal operation without management intervention as the initial state of the device.

Table 178. Bit Descriptions for B10L_TEST_MODE_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:13]	B10L_TX_TEST_MODE	10BASE-T1L Transmitter Test Mode. 000: normal operation. 001: Test Mode 1—transmitter output voltage and timing jitter test mode. When Test Mode 1 is enabled, the PHY repeatedly transmits the data symbol sequence (+1, −1). 010: Test Mode 2—transmitter output droop test mode. When Test Mode 2 is enabled, the PHY transmits ten +1 symbols followed by ten −1 symbols.	0x0	R/W

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Table 178. Bit Descriptions for B10L_TEST_MODE_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
		011: Test Mode 3—normal operation in idle mode. When Test Mode 3 is enabled, the PHY transmits as in nontest operation and in the master data mode with data set to normal interframe idle signals.		
[12:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PMA Link Status Register

Device Address: 0x01; Register Address: 0x8302, Reset: 0x0000, Name: B10L_PMA_LINK_STAT

This address can be read to determine the 10BASE-T1L PMA link status. Reading B10L_PMA_LINK_STAT clears the latching condition of these bits.

Table 179. Bit Descriptions for B10L_PMA_LINK_STAT

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
9	B10L_REM_RCVR_STAT_OK_LL	10BASE-T1L Remote Receiver Status OK Latch Low. Latched low version of B10L_REM_RCVR_STAT_OK.	0x0	R LL
8	B10L_REM_RCVR_STAT_OK	10BASE-T1L Remote Receiver Status OK. When read as 1, this bit indicates that the remote receiver status is OK.	0x0	R
7	B10L_LOC_RCVR_STAT_OK_LL	10BASE-T1L Local Receiver Status OK Latch Low. Latched low version of B10L_LOC_RCVR_STAT_OK.	0x0	R LL
6	B10L_LOC_RCVR_STAT_OK	10BASE-T1L Local Receiver Status OK. When read as 1, this bit indicates that the local receiver status is OK.	0x0	R
5	B10L_DSCR_STAT_OK_LL	BASE-T1L Descrambler Status OK Latch Low. When read as 1, this bit indicates that the descrambler status is OK.	0x0	R LL
4	B10L_DSCR_STAT_OK	10BASE-T1L Descrambler Status OK. When read as 1, this bit indicates that the descrambler status is OK.	0x0	R
[3:2]	RESERVED	Reserved.	0x0	R
1	B10L_LINK_STAT_OK_LL	Link Status OK Latch Low. When read as 1, this bit indicates that the link status is OK.	0x0	R LL
0	B10L_LINK_STAT_OK	Link Status OK. When read as 1, this bit indicates that the link status is OK.	0x0	R

MSE Value Register

Device Address: 0x01; Register Address: 0x830B, Reset: 0x0000, Name: MSE_VAL

Table 180. Bit Descriptions for MSE_VAL

Bits	Bit Name	Description	Reset	Access
[15:0]	MSE_VAL	MSE Value. Note that the LSB weight is 2^{-18}. When computing a signal-to-noise ratio (SNR) value, the mean 10BASE-T1L idle symbol power is 0.64422.	0x0	R

PCS Control 1 Register

Device Address: 0x03; Register Address: 0x0000, Reset: 0x0000, Name: PCS_CNTRL1

This address corresponds to the PCS Control Register 1 specified in Clause 45.2.3.1 of Standard 802.3.

Table 181. Bit Descriptions for PCS_CNTRL1

Bits	Bit Name	Description	Reset	Access
15	PCS_SFT_RST	PCS Software Reset. Mirrors PMA_SFT_RST.	0x0	R/W SC

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Table 181. Bit Descriptions for PCS_CNTRL1 (Continued)

Bits	Bit Name	Description	Reset	Access
14	LB_PCS_EN	PCS Loopback Enable. When this bit is set to 1, the PCS accepts data on the transmit path and returns it on the receive path. When this bit is set to 0, the PCS works in normal mode.	0x0	R/W
[13:12]	RESERVED	Reserved.	0x0	R
11	PCS_SFT_PD	PCS Software Power-Down. Mirrors PMA_SFT_PD.	0x0	R/W
[10:0]	RESERVED	Reserved.	0x0	R

PCS Status 1 Register

Device Address: 0x03; Register Address: 0x0001, Reset: 0x0002, Name: PCS_STAT1

Table 182. Bit Descriptions for PCS_STAT1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	PCS_SFT_PD_ABLE	PCS Software Power-Down Able. Indicates that the PCS supports software power-down.	0x1	R
0	RESERVED	Reserved.	0x0	R

PCS MMD Devices in Package 1 Register

Device Address: 0x03; Register Address: 0x0005, Reset: 0x008B, Name: PCS_DEVS_IN_PKG1

Table 183. Bit Descriptions for PCS_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	PCS_DEVS_IN_PKG1	PCS MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

PCS MMD Devices in Package 2 Register

Device Address: 0x03; Register Address: 0x0006, Reset: 0xC000, Name: PCS_DEVS_IN_PKG2

Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.

Table 184. Bit Descriptions for PCS_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	PCS_DEVS_IN_PKG2	PCS MMD Devices in Package 2. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

PCS Status 2 Register

Device Address: 0x03; Register Address: 0x0008, Reset: 0x8000, Name: PCS_STAT2

Table 185. Bit Descriptions for PCS_STAT2

Bits	Bit Name	Description	Reset	Access
[15:14]	PCS_PRESENT	PCS Present. Indicates that the PCS is present and responding.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PCS Control Register

Device Address: 0x03; Register Address: 0x08E6, Reset: 0x0000, Name: B10L_PCS_CNTRL

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This address corresponds to the 10BASE-T1L PCS control register specified in Clause 45.2.3.68a of Standard 802.3cg.

Table 186. Bit Descriptions for B10L_PCS_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_LB_PCS_EN	PCS Loopback Enable. When set to 1, this bit enables the 10BASE-T1L PCS loopback.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PCS Status Register

Device Address: 0x03; Register Address: 0x08E7, Reset: 0x0000, Name: B10L_PCS_STAT

This address corresponds to the 10BASE-T1L PCS status register specified in Clause 45.2.3.68b of Standard 802.3cg.

Table 187. Bit Descriptions for B10L_PCS_STAT

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	B10L_PCS_DSCR_STAT_OK_LL	PCS Descrambler Status. When read as 1, this bit indicates that the 10BASE-T1L descrambler is locked. When read as 0, this bit indicates that the 10BASE-T1L descrambler has unlocked since the last time the bit was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

Autonegotiation MMD Devices in Package 1 Register

Device Address: 0x07; Register Address: 0x0005, Reset: 0x008B, Name: AN_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 188. Bit Descriptions for AN_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_DEVS_IN_PKG1	Autonegotiation MMD Devices in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Autonegotiation MMD Devices in Package 2 Register

Device Address: 0x07; Register Address: 0x0006, Reset: 0xC000, Name: AN_DEVS_IN_PKG2

Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.

Table 189. Bit Descriptions for AN_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_DEVS_IN_PKG2	Autonegotiation MMD Devices in Package 2. Vendor Specific Device 1 and Vendor Specific Device 2 MMDs are present.	0xC000	R

BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x0200, Reset: 0x1000, Name: AN_CONTROL

This address corresponds to the BASE-T1 autonegotiation control register specified in Clause 45.2.7.19 of Standard 802.3.

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Table 190. Bit Descriptions for AN_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R/W SC
12	AN_EN	Autonegotiation Enable. When this bit is set to 1, autonegotiation is enabled. Autonegotiation is enabled by default and it is strongly recommended that it is always enabled.	0x1	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	AN_RESTART	Autonegotiation Restart. Setting this bit to 1 restarts the autonegotiation process. This bit is self clearing and it returns a value of one until the autonegotiation process is initiated.	0x0	R/W SC
[8:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x0201, Reset: 0x0008, Name: AN_STATUS

This address corresponds to the BASE-T1 autonegotiation status register specified in Clause 45.2.7.20 of Standard 802.3.

Table 191. Bit Descriptions for AN_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AN_PAGE_RX	Page Received. This bit is set to indicate that a new link codeword has been received and stored in the AN_LP_ADV_ABILITY_x register or the AN_LP_NEXT_PAGE register. The contents of the AN_LP_ADV_ABILITY_x are valid when this bit is set the first time during autonegotiation. This bit resets to 0 on a read of the AN_STATUS register.	0x0	R LH
5	AN_COMPLETE	Autonegotiation Complete. When this bit is read as 1, the autonegotiation process is complete, the PHY link is up, and that the contents of the AN_ADV_ABILITY_x and AN_LP_ADV_ABILITY_x registers are valid. This bit returns 0 if the autonegotiation is disabled, clearing the AN_EN bit.	0x0	R
4	AN_REMOTE_FAULT	Autonegotiation Remote Fault. Remote fault set in base page received from link partner.	0x0	R LH
3	AN_ABLE	Autonegotiation Ability. When this bit is read as 1, it indicates that the PHY is able to perform autonegotiation.	0x1	R
2	AN_LINK_STATUS	Link Status. When read as 1, this bit indicates that a valid link is established. If this bit reads 0, the link failed since the last time it was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0202, Reset: 0x0001, Name: AN_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits[15:0], specified in Clause 45.2.7.21 of Standard 802.3.

Table 192. Bit Descriptions for AN_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_ADV_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R/W
14	AN_ADV_ACK	Acknowledge (ACK). This bit indicates that the device has received the link codeword of its link partner. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_ADV_REMOTE_FAULT	Remote Fault. See IEEE Standard 802.3 Subclause 98.2.1.2.7.	0x0	R/W
12	AN_ADV_FORCE_MS	Force Master/Slave Configuration. This bit allows the PHY to force its master/slave configuration. When this bit is set as 0, the master/slave configuration is a preferred mode. (The configuration in AN_ADV_MST is a preferred configuration.) If this bit is set to 1,	0x0	R/W

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Table 192. Bit Descriptions for AN_ADV_ABILITY_L (Continued)

Bits	Bit Name	Description	Reset	Access
		the master/slave configuration is a forced mode. (The configuration in AN_ADV_MST is a forced configuration.) See IEEE Standard 802.3 Subclause 98.2.1.2.5 for more details.		
[11:10]	AN_ADV_PAUSE	Pause Ability. This bit field advertises support for asymmetric and symmetric pause functions on full duplex links. See IEEE Standard 802.3 Subclause 98.2.1.2.6 for more details.	0x0	R/W
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_ADV_SELECTOR	Selector. The value of this bit field is fixed at 00001, which is the IEEE 802.3 selector value. See IEEE Standard 802.3 Subclause 98.2.1.2.1.	0x1	R

BASE-T1 Autonegotiation Advertisement Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0203, Reset: 0x4000, Name: AN_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits [31:16], specified in Clause 45.2.7.21 of Standard 802.3.

Table 193. Bit Descriptions for AN_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_ADV_B10L	10BASE-T1L Ability. This bit indicates that the device is compatible with 10BASE-T1L.	0x1	R/W
[13:5]	RESERVED	Reserved.	0x0	R
4	AN_ADV_MST	Master/slave Configuration. This bit advertises the master/slave configuration, as follows: 0: slave, 1: master. See also the AN_ADV_FORCE_MS bit, which determines whether this bit expresses a preference or a forced value. See IEEE Standard 802.3 Subclause 98.2.1.2.3 (master/slave configuration is Bit 4 of the transmitted nonce field).	Pin Dependent	R/W
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x0204, Reset: 0x0000, Name: AN_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation advertisement register, Bits[47:32], specified in Clause 45.2.7.21 of Standard 802.3.

Table 194. Bit Descriptions for AN_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	AN_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This bit advertises that the PHY is capable of transmitting in the high level (2.4 V p-p) transmit operating mode. This bit is used with AN_ADV_B10L_TX_LVL_HI_REQ to configure the 10BASE-T1L transmission level (2.4 V p-p or 1.0 V p-p). See the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	Pin dependent	R/W
12	AN_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This bit advertises that the PHY is requesting that high level (2.4 V p-p) transmit operating mode be used. The transmit level is resolved as follows: If either PHY is not capable of high level transmission (and has AN_ADV_B10L_TX_LVL_HI_ABL = 0), both PHYs must use the low voltage (1.0 V p-p) transmit operating mode. Otherwise, if either PHY requests high level transmission (and has AN_ADV_B10L_TX_LVL_HI_REQ = 1), both PHYs must use the high volt-	Pin dependent	R/W

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Table 194. Bit Descriptions for AN_ADV_ABILITY_H (Continued)

Bits	Bit Name	Description	Reset	Access
		age (2.4 V p-p) transmit operating mode. See IEEE P802.cg Subclause 146.6.4 for more details.		
[11:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0205, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[15:0], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of the AN_LP_ADV_ABILITY_M and AN_LP_ADV_ABILITY_H registers is latched when AN_LP_ADV_ABILITY_L is read.

Table 195. Bit Descriptions for AN_LP_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_ADV_NEXT_PAGE_REQ	Link Partner Next Page Request. This bit indicates that the link partner PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R
14	AN_LP_ADV_ACK	Link Partner Acknowledge (ACK). This bit indicates that the device has received the link codeword of its link partner. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_LP_ADV_REMOTE_FAULT	Link Partner Remote Fault. See IEEE Standard 802.3 Subclause 98.2.1.2.7.	0x0	R
12	AN_LP_ADV_FORCE_MS	Link Partner Force Master/Slave Configuration. This bit reports the forced master/slave configuration of the link partner, with values as follows. See IEEE Standard 802.3 Subclause 98.2.1.2.5 for more details. 0: preferred mode (AN_LP_ADV_MST is a preferred configuration). 1: forced mode (AN_LP_ADV_MST is a forced configuration).	0x0	R
[11:10]	AN_LP_ADV_PAUSE	Link Partner Pause Ability. This bit field reports the support of the link partner for asymmetric and symmetric pause functions on full duplex links. See IEEE Standard 802.3 Subclause 98.2.1.2.6 for more details.	0x0	R
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_LP_ADV_SELECTOR	Link Partner Selector. The value of this field reads 00001, which is the IEEE 802.3 selector value. See IEEE Standard 802.3 Subclause 98.2.1.2.1.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0206, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[31:16], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 196. Bit Descriptions for AN_LP_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L	Link Partner 10BASE-T1L Ability. This bit indicates if the link partner has 10BASE-T1L ability.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
7	AN_LP_ADV_B1000	Link Partner 1000BASE-T1 Ability. This bit indicates if the link partner has 1000BASE-T1 ability.	0x0	R
6	AN_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This bit indicates if the link partner has 10BASE-T1S ability.	0x0	R
5	AN_LP_ADV_B100	Link Partner 100BASE-T1 Ability. This bit indicates if the link partner has 100BASE-T1 ability.	0x0	R

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Table 196. Bit Descriptions for AN_LP_ADV_ABILITY_M (Continued)

Bits	Bit Name	Description	Reset	Access
4	AN_LP_ADV_MST	Link Partner Master/Slave Configuration. This bit reports the master/slave configuration of the link partner, as follows: 0: slave, 1: master. See also the AN_LP_ADV_FORCE_MS bit, which determines whether this bit expresses a preference or a forced value. See IEEE Standard 802.3 Subclause 98.2.1.2.3 (master/slave configuration is Bit 4 of the transmitted nonce field).	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x0207, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation base page ability register, Bits[47:32], of the link partner specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 197. Bit Descriptions for AN_LP_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L_EEE	Link Partner 10BASE-T1L EEE Ability. This bit reports if the link partner is capable of using 10BASE-T1L energy efficient Ethernet.	0x0	R
13	AN_LP_ADV_B10L_TX_LVL_HI_ABL	Link Partner 10BASE-T1L High Level Transmit Operating Mode Ability. This bit reports whether the link partner is capable of transmitting in the high level (2.4 V p-p) transmit operating mode. This bit is used with AN_LP_ADV_B10L_TX_LVL_HI_REQ to configure the 10BASE-T1L transmission level (2.4 V p-p or 1.0 V p-p); see the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	0x0	R
12	AN_LP_ADV_B10L_TX_LVL_HI_REQ	Link Partner 10BASE-T1L High Level Transmit Operating Mode Request. This bit reports whether the link partner is requesting that the high level (2.4 V p-p) transmit operating mode be used. See the AN_ADV_B10L_TX_LVL_HI_REQ bit for more details.	0x0	R
11	AN_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half-Duplex Ability. This bit reports if the link partner is capable of using 10BASE-T1S half duplex.	0x0	R
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x0208, Reset: 0x2001, Name: AN_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[15:0], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 198. Bit Descriptions for AN_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R/W
14	AN_NP_ACK	Next Page Acknowledge. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_NP_MESSAGE_PAGE	Next Page Encoding. Indicates encoding of next page, as follows: 0: unformatted next page. 1: message next page.	0x1	R/W

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Table 198. Bit Descriptions for AN_NEXT_PAGE_L (Continued)

Bits	Bit Name	Description	Reset	Access
12	AN_NP_ACK2	Acknowledge 2. Indicates whether the PHY can comply with the message. See IEEE Standard 802.3 Subclause 28.2.3.4.6.	0x0	R/W
11	AN_NP_TOGGLE	Toggle Bit. The toggle bit is used to synchronize pages between the PHYs. This always read as 0 (the toggle bit is set automatically by the arbitration state machine).	0x0	R
[10:0]	AN_NP_MESSAGE_CODE	Message/Unformatted Code Field. For a message page (AN_NP_MESSAGE_PAGE = 1), the valid values are defined in IEEE Standard 802.3. 1: null message. 5: organizationally unique identifier tagged message. 6: autonegotiation device identifier tag code.	0x1	R/W

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x0209, Reset: 0x0000, Name: AN_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[31:16], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 199. Bit Descriptions for AN_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED1	Unformatted Code Field 1.	0x0	R/W

BASE-T1 Autonegotiation Next Page Transmit Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x020A, Reset: 0x0000, Name: AN_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation next page transmit register, Bits[47:42], specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represents a message page with the message code set to null. Write AN_NEXT_PAGE_M and AN_NEXT_PAGE_H before AN_NEXT_PAGE_L.

Table 200. Bit Descriptions for AN_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED2	Unformatted Code Field 2.	0x0	R/W

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[15:0]

Device Address: 0x07; Register Address: 0x020B, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation next page ability register, Bits[15:0], of the link partner specified in Clause 45.2.7.24 of Standard 802.3. The values of AN_LP_NEXT_PAGE_M and AN_LP_NEXT_PAGE_H are latched when this register is read.

Table 201. Bit Descriptions for AN_LP_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Standard 802.3 Subclause 98.2.1.2.9.	0x0	R
14	AN_LP_NP_ACK	Link Partner Next Page Acknowledge. See IEEE Standard 802.3 Subclause 98.2.1.2.8.	0x0	R
13	AN_LP_NP_MESSAGE_PAGE	Link Partner Next Page Encoding. Indicates encoding of link partner next page, as follows: 0: unformatted next page. 1: message next page.	0x0	R

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Table 201. Bit Descriptions for AN_LP_NEXT_PAGE_L (Continued)

Bits	Bit Name	Description	Reset	Access
12	AN_LP_NP_ACK2	Link Partner Acknowledge 2. See AN_NP_ACK2 for more details.	0x0	R
11	AN_LP_NP_TOGGLE	Link Partner Toggle Bit. Link partner toggle bit.	0x0	R
[10:0]	AN_LP_NP_MESSAGE_CODE	Link Partner Message/Unformatted Code Field. See AN_NP_MESSAGE_PAGE for more details. 1: null message. 5: organizationally unique identifier tagged message. 6: autonegotiation device identifier tag code.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[31:16]

Device Address: 0x07; Register Address: 0x020C, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page ability register, Bits[31:16], of the link partner specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 202. Bit Descriptions for AN_LP_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED1	Link Partner Unformatted Code Field 1.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability Register, Bits[47:32]

Device Address: 0x07; Register Address: 0x020D, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register, Bits[47:32], specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 203. Bit Descriptions for AN_LP_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED2	Link Partner Unformatted Code Field 2.	0x0	R

10BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x020E, Reset: 0x8000, Name: AN_B10_ADV_ABILITY

This address corresponds to the 10BASE-T1 autonegotiation control register specified in Clause 45.2.7.25 of Standard 802.3cg.

Table 204. Bit Descriptions for AN_B10_ADV_ABILITY

Bits	Bit Name	Description	Reset	Access
15	AN_B10_ADV_B10L	10BASE-T1L Ability. This is a duplicate of the AN_ADV_B10L bit.	0x1	R/W
14	AN_B10_ADV_B10L_EEE	10BASE-T1L EEE Ability. This is a duplicate of the AN_ADV_B10L_EEE bit.	0x0	R
13	AN_B10_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This is a duplicate of the AN_ADV_B10L_TX_LVL_HI_ABL bit.	Pin dependent	R/W
12	AN_B10_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This is a duplicate of the AN_ADV_B10L_TX_LVL_HI_REQ bit.	Pin dependent	R/W
[11:0]	RESERVED	Reserved.	0x0	R

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10BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x020F, Reset: 0x0000, Name: AN_B10_LP_ADV_ABILITY

This address corresponds to the 10BASE-T1 autonegotiation status register specified in Clause 45.2.7.26 of Standard 802.3cg.

Table 205. Bit Descriptions for AN_B10_LP_ADV_ABILITY

Bits	Bit Name	Description	Reset	Access
15	AN_B10_LP_ADV_B10L	10BASE-T1L Ability. This is a duplicate of the AN_LP_ADV_B10L bit.	0x0	R
14	AN_B10_LP_ADV_B10L_EEE	10BASE-T1L EEE Ability. This is a duplicate of the AN_LP_ADV_B10L_EEE bit.	0x0	R
13	AN_B10_LP_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This is a duplicate of the AN_LP_ADV_B10L_TX_LVL_HI_ABL bit.	0x0	R
12	AN_B10_LP_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This is a duplicate of the AN_LP_ADV_B10L_TX_LVL_HI_REQ bit.	0x0	R
[11:8]	RESERVED	Reserved.	0x0	R
7	AN_B10_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This is a duplicate of the AN_LP_ADV_B10S_FD bit.	0x0	R
6	AN_B10_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half Duplex Ability. This is a duplicate of the AN_LP_ADV_B10S_HD bit.	0x0	R
[5:0]	RESERVED	Reserved.	0x0	R

Autonegotiation Force Mode Enable Register

Device Address: 0x07; Register Address: 0x8000, Reset: 0x0000, Name: AN_FRC_MODE_EN

Note that the effect of this register is superseded by the AN_EN bit, which enables the autonegotiation process. If autonegotiation is disabled (AN_EN = 0), forced mode is engaged if AN_FRC_MODE_EN is 1.

Table 206. Bit Descriptions for AN_FRC_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	AN_FRC_MODE_EN	Autonegotiation Forced Mode. Enables forced mode functionality.	0x0	R/W

Extra Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x8001, Reset: 0x0000, Name: AN_STATUS_EXTRA

This register is provided in addition to AN_STATUS.

Table 207. Bit Descriptions for AN_STATUS_EXTRA

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	AN_LP_NP_RX	Next Page Request Received from Link Partner.	0x0	R LH
9	AN_INC_LINK	Incompatible Link Indication. This corresponds to the incompatible link state of IEEE Standard 802.3 Subclause 98.5.1. Its value is set by the priority resolution function run on entering the autonegotiation good check state.	0x0	R
[8:7]	AN_TX_LVL_RSLTN	Autonegotiation Tx Level Result. Transmit level high/low resolution result, determined as per IEEE Standard 802.3cg Subclause 146.6.4. This is encoded as follows: 0: not run. 2: success, low transmit levels (1.0 V p-p) selected. 3: success, high transmit levels (2.4 V p-p) selected.	0x0	R

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Table 207. Bit Descriptions for AN_STATUS_EXTRA (Continued)

Bits	Bit Name	Description	Reset	Access
[6:5]	AN_MS_CONFIG_RSLTN	Master/Slave Resolution Result. Determined as per master/slave configuration of IEEE Standard 802.3. This is encoded as follows: 0: not run. 1: configuration fault. 2: success, PHY is configured as slave. 3: success, PHY is configured as master.	0x0	R
[4:1]	AN_HCD_TECH	Highest Common Denominator (HCD) PHY Technology. As selected by the priority resolution function of IEEE Standard 802.3 Subclause 98.2.4.2. Consider all values that are not shown to be reserved. 0: null (not run). 1: 10BASE-T1L.	0x0	R
0	AN_LINK_GOOD	Autonegotiation Complete Indication. This corresponds to the an_link_good state of IEEE Standard 802.3 Subclause 98.5.1. This signal indicates completion of the autonegotiation transmission, and that the enabled PHY technology is either bringing up its link or that it has brought up its link. See also AN_COMPLETE, which is similar, but also indicates that the PHY link is up.	0x0	R

PHY Instantaneous Status Register

Device Address: 0x07; Register Address: 0x8030, Reset: 0x0010, Name: AN_PHY_INST_STATUS

This register address provides access to instantaneous status indications. These values are not latched. The set of indications returned by this register is a consistent set, that is, a set of values in effect at the time the register address is read.

Table 208. Bit Descriptions for AN_PHY_INST_STATUS

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
4	IS_AN_TX_EN	Autonegotiation Tx Enable Status. Autonegotiation transmit enable. This bit indicates that the autonegotiation is active and controlling the transmitter, and arbitration has not yet reached the autonegotiation (AN) good check state or the AN good state. That is, the link_control signals have not been set to enable.	0x1	R
3	IS_CFG_MST	Master Status. If link_control = enable (for example, B10L_LINK_CTRL_EN = 1), this indicates whether the PHY is operating as master (and not slave).	0x0	R
2	IS_CFG_SLV	Slave Status. If link_control = enable (for example, B10L_LINK_CTRL_EN = 1), this indicates whether the PHY is operating as slave (and not master).	0x0	R
1	IS_TX_LVL_HI	Tx Level High Status. Indicates that the PHY is operating with high transmit levels (2.4 V), and not low transmit levels (1.0 V).	0x0	R
0	IS_TX_LVL_LO	Tx Level Low Status. Indicates that the PHY is operating with low transmit levels (1.0 V), and not low transmit levels (2.4 V).	0x0	R

Vendor Specific MMD 1 Device Identifier High Register

Device Address: 0x1E; Register Address: 0x0002, Reset: 0x0283, Name: MMD1_DEV_ID1

This address corresponds to the Vendor Specific 1 MMD identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

Table 209. Bit Descriptions for MMD1_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEV_ID1	Organizationally Unique Identifier, Bits[3:18].	0x283	R

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Vendor Specific MMD 1 Device Identifier Low Register

Device Address: 0x1E; Register Address: 0x0003, Reset: 0xBCA1, Name: MMD1_DEV_ID2

This address corresponds to the Vendor Specific 1 MMD identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows six bits of the OUI along with the model number and revision number to be observed.

Table 210. Bit Descriptions for MMD1_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD1_DEV_ID2_OUI	Organizationally Unique Identifier, Bits[19:24].	0x2F	R
[9:4]	MMD1_MODEL_NUM	Model Number.	0xA	R
[3:0]	MMD1_REV_NUM	Revision Number.	0x1	R

Vendor Specific 1 MMD Devices in Package Register

Device Address: 0x1E; Register Address: 0x0005, Reset: 0x008B, Name: MMD1_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 211. Bit Descriptions for MMD1_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEVS_IN_PKG1	Vendor Specific 1 MMDs in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Device Address: 0x1E; Register Address: 0x0006, Reset: 0xC000, Name: MMD1_DEVS_IN_PKG2

Vendor-specific device 1 and Vendor-specific device 2 MMDs present

Table 212. Bit Descriptions for MMD1_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEVS_IN_PKG2	Vendor Specific 1 MMDs in Package 2. Vendor Specific 1 and Vendor Specific 2 MMDs are present.	0xC000	R

Vendor Specific MMD 1 Status Register

Device Address: 0x1E; Register Address: 0x0008, Reset: 0x8000, Name: MMD1_STATUS

This address corresponds to the Vendor Specific 1 MMD status register specified in Clause 45.2.11.2 of Standard 802.3.

Table 213. Bit Descriptions for MMD1_STATUS

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD1_STATUS	Vendor Specific 1 MMD Status. 10: device responding at this address. 11: no device responding at this address. 01: no device responding at this address. 00: no device responding at this address.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

System Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0010, Reset: 0x1000, Name: CRSM_IRQ_STATUS

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This address can be used to check which interrupt requests have been triggered since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of CRSM_IRQ_STATUS go high even when the associated interrupts are not enabled. A reserved interrupt being triggered indicates a fatal error in the system.

Table 214. Bit Descriptions for CRSM_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_LH	Software Requested Interrupt Event.	0x0	R LH
[14:13]	RESERVED	Reserved.	0x0	R
12	CRSM_HRD_RST_IRQ_LH	Hardware Reset Interrupt.	0x1	R LH
[11:0]	RESERVED	Reserved.	0x0	R LH

System Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0020, Reset: 0x1BFE, Name: CRSM_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 215. Bit Descriptions for CRSM_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_REQ	Software Interrupt Request. Software can set this bit to generate an interrupt for system level testing. This bit always reads as 0 because it is self clearing.	0x0	R/W SC
[14:13]	RESERVED	Reserved.	0x0	R
12	CRSM_HRD_RST_IRQ_EN	Enable Hardware Reset Interrupt. Note that writing a 0 to this bit does not mask the interrupt because this bit is initialized when a hardware reset occurs.	0x1	R/W
[11:0]	RESERVED	Reserved.	0xBFE	R/W

Software Reset Register

Device Address: 0x1E; Register Address: 0x8810, Reset: 0x0000, Name: CRSM_SFT_RST

Table 216. Bit Descriptions for CRSM_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_RST	Software Reset Register. The software reset bit allows the chip to be reset. When this bit is set, the chip fully initializes, almost equivalent to a hardware reset.	0x0	R/W SC

Software Power-Down Control Register

Device Address: 0x1E; Register Address: 0x8812, Reset: 0x0000, Name: CRSM_SFT_PD_CNTRL

Table 217. Bit Descriptions for CRSM_SFT_PD_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_PD	Software Power-down. The software power-down register puts the chip in a lower power mode. In this mode, most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via the $\overline{\text{Px_SWPD_EN}}$ pin. This allows the chip to be held in power-down mode until an appropriate software initialization is performed.	Pin Dependent	R/W

PHY Subsystem Reset Register

Device Address: 0x1E; Register Address: 0x8814, Reset: 0x0000, Name: CRSM_PHY_SUBSYS_RST

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Table 218. Bit Descriptions for CRSM_PHY_SUBSYS_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset. The PHY subsystem reset register allows a managed subsystem reset to be initiated. When the PHY subsystem is reset, normal operation resumes, and the bit self clears.	0x0	R/W SC

PHY MAC Interface Reset Register

Device Address: 0x1E; Register Address: 0x8815, Reset: 0x0000, Name: CRSM_MAC_IF_RST

Table 219. Bit Descriptions for CRSM_MAC_IF_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_MAC_IF_RST	PHY MAC Interface Reset. The PHY MAC interface reset register allows a managed PHY MAC interface reset to be initiated. When the PHY MAC interface is reset, normal operation resumes, and the bit self clears.	0x0	R/W SC

System Status Register

Device Address: 0x1E; Register Address: 0x8818, Reset: 0x0000, Name: CRSM_STAT

Table 220. Bit Descriptions for CRSM_STAT

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	CRSM_SFT_PD_RDY	Software Power-down Status. This bit indicates that the system is in the software power-down state.	0x0	R
0	CRSM_SYS_RDY	System Ready. This bit indicates that the start-up sequence is complete and the system is ready for normal operation.	0x0	R

CRSM Power Management Control Register

Device Address: 0x1E; Register Address: 0x8819, Reset: 0x0000, Name: CRSM_PMG_CNTRL

Table 221. Bit Descriptions for CRSM_PMG_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_FRC_OSC_EN	Force Digital Boot Oscillator Clock Enable.	0x0	R/W

CRSM Diagnostics Clock Control Register

Device Address: 0x1E; Register Address: 0x882C, Reset: 0x0002, Name: CRSM_DIAG_CLK_CTRL

CRSM diagnostics clock control.

Table 222. Bit Descriptions for CRSM_DIAG_CLK_CTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x1	R
0	CRSM_DIAG_CLK_EN	Enable the Diagnostics Clock.	0x0	R/W

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Package Configuration Values Register

Device Address: 0x1E; Register Address: 0x8C22, Reset: 0x0000, Name: MGMT_PRT_PKG

The MGMT_CFG_VAL address allows reading of the package configuration values.

Table 223. Bit Descriptions for MGMT_PRT_PKG

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	MGMT_PRT_PKG_VAL	Package Type. 0 = 40-lead LFCSP.	0x0	R

MDIO Control Register

Device Address: 0x1E; Register Address: 0x8C30, Reset: 0x0000, Name: MGMT_MDIO_CNTRL

Table 224. Bit Descriptions for MGMT_MDIO_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	MGMT_GRP_MDIO_EN	Enable MDIO PHY/Port Group Address Mode. In this mode, the PHY responds to any write or address operation to the 5-bit PHY/Port Address 31 (decimal) regardless of its own PHY/port address. This feature is only intended for initialization sequences in multiport applications, must only be set in those cases, and cleared immediately after the initialization is complete.	0x0	R/W

Pin Mux Configuration 1 Register

Device Address: 0x1E; Register Address: 0x8C56, Reset: 0x00FE, Name: DIGIO_PINMUX

Table 225. Bit Descriptions for DIGIO_PINMUX

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:6]	DIGIO_TSTIMER_PINMUX	Pin Mux Select for TS_TIMER. 00: Reserved 01: LED_0 10: $\overline{\text{INT}}$ 11: TS_TIMER not assigned.	0x3	R/W
[5:4]	DIGIO_TSCAPT_PINMUX	Pin Mux Select for TS_CAPT. 00: Reserved. 01: LED_1. 10: TEST_1. 11: TS_CAPT not assigned.	0x3	R/W
[3:1]	DIGIO_LED1_PINMUX	Pin Mux Select for LED_1. 000: LED_1. 001: TX_ER. 010: TX_EN. 011: TX_CLK. 100: TXD_0. 101: TXD_2. 110: LINK_ST. 111: LED_1 output not enabled.	0x7	R/W
0	DIGIO_LINK_ST_POLARITY	LINK_ST Polarity.	0x0	R/W

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Table 225. Bit Descriptions for DIGIO_PINMUX (Continued)

Bits	Bit Name	Description	Reset	Access
		0: ASSERT_HIGH. 1: ASSERT_LOW.		

LED_0 On/Off Blink Time Register

Device Address: 0x1E; Register Address: 0x8C80, Reset: 0x3636, Name: LED0_BLINK_TIME_CNTRL

LED on blink time = LED0_ON_N4MS × 4 ms.

LED off blink time = LED0_OFF_N4MS × 4 ms.

If LEDx_MODE = 0 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED off sequence, followed by an LED on sequence, and then repeats.

If LEDx_MODE = 1 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED on sequence, followed by an LED off sequence, and then repeats.

If LEDx_OFF_N4MS = LEDx_ON_N4MS = 0, this is a special case whereby the internal activity signal as selected by LEDx_FUNCTION can be monitored live.

If LEDx_FUNCTION is programmed to a combination of a link and activity signal, the LED is on while the link is up and with no activity. The LED switches off for either loss of link or receipt of activity.

If LEDx_FUNCTION is programmed to an activity signal, the LED is off with no activity. The LED switches on upon receipt of activity.

Table 226. Bit Descriptions for LED0_BLINK_TIME_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	LED0_ON_N4MS	LED_0 On Blink Time. LED_0 on blink time is calculated by 4 ms × LED0_ON_N4MS bit field. Recommended value is greater than 3.	0x36	R/W
[7:0]	LED0_OFF_N4MS	LED_0 Off Blink Time. LED_0 off blink time is calculated by 4 ms × LED0_OFF_N4MS bit field. Recommended value is greater than 3.	0x36	R/W

LED_1 On/Off Blink Time Register

Device Address: 0x1E; Register Address: 0x8C81, Reset: 0x3636, Name: LED1_BLINK_TIME_CNTRL

LED on blink time = LED1_ON_N4MS × 4 ms.

LED off blink time = LED1_OFF_N4MS × 4 ms.

If LEDx_MODE = 0 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED off sequence followed by an LED on sequence, and then repeats.

If LEDx_MODE = 1 and LEDx_FUNCTION is set to blink, the LED activity starts with an LED on sequence, followed by an LED Off sequence, and then repeats.

If LEDx_OFF_N4MS = LEDx_ON_N4MS = 0, this is a special case whereby the internal activity signal as selected by LEDx_FUNCTION can be monitored live.

If LEDx_FUNCTION is programmed to a combination of a link and activity signal, the LED is on while the link is up and with no activity. The LED switches off for either loss of link or receipt of activity.

If LEDx_FUNCTION is programmed to an activity signal, the LED is off with no activity. The LED switches on upon receipt of activity.

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Table 227. Bit Descriptions for LED1_BLINK_TIME_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	LED1_ON_N4MS	LED_1 On Blink Time. LED_1 on blink time is calculated by 4 ms × LED1_ON_N4MS bit field. Recommended value is greater than 3.	0x36	R/W
[7:0]	LED1_OFF_N4MS	LED_1 Off Blink Time. LED_1 off blink time is calculated by 4 ms × LED1_OFF_N4MS bit field. Recommended value is greater than 3.	0x36	R/W

LED Control Register

Device Address: 0x1E; Register Address: 0x8C82, Reset: 0x8E80, Name: LED_CNTRL

LED control register.

Table 228. Bit Descriptions for LED_CNTRL

Bits	Bit Name	Description	Reset	Access
15	LED1_EN	LED 1 Enable. A disabled LED is off. An enabled LED can be on or blinking depending on LED1_FUNCTION selection and activity.	0x1	R/W
14	LED1_LINK_ST_QUALIFY	Qualify Certain LED 1 Options with link_status. 0: TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave not qualified by link_status. 1: TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave are qualified by link_status.	0x0	R/W
13	LED1_MODE	LED 1 Mode Selection. 0: LED Mode 1. If there is activity, blink at the rate defined by MMR LED1_BLINK_TIME_CNTRL. 1: LED Mode 2. The LED blink frequency is set depending on the level of activity. The activity level is graded in steps of 10%, and the frequency of the LED adjusts accordingly. A higher activity level means a longer off duration and shorter on duration. The activity level is reevaluated after a window period that varies between 640 ms and 1.5 sec.	0x0	R/W
[12:8]	LED1_FUNCTION	LED_1 Pin Function. Determines the source activity for the LED_1 pin. The CLK25_REF, TX_TCLK, and CLK_120MHZ options are clock out features with the LED controller bypassed. The waveform transmitted off chip is dependent on the selected clock source frequency. The following LED1_FUNCTION settings are not qualified with link_status: LED1_FUNCTION = on, off, blink, INCOMPATIBLE_LINK_CFG, AN_LINK_GOOD, AN_COMPLETE, LOC_RCVR_STATUS, REM_RCVR_STATUS, CLK25_REF, TX_TCLK, and CLK_120MHz. The TX_LEVEL_2P4, TX_LEVEL_1P0, master, and slave options are optionally qualified by link_status and this is controlled via the LED1_LINK_ST_QUALIFY MMR. The TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave, MSTR_SLV_FAULT, AN_LINK_GOOD, AN_COMPLETE, and TS_TIMER options are considered status indicators and the LED controller is not used. If the programmed signal is high, the LED is static on and if the programmed signal is low, the LED is static off. 0: LINKUP_TXRX_ACTIVITY. 1: LINKUP_TX_ACTIVITY. 2: LINKUP_RX_ACTIVITY. 3: LINKUP_ONLY. 4: TXRX_ACTIVITY. 5: TX_ACTIVITY. 6: RX_ACTIVITY. 7: LINKUP_RX_ER. 8: LINKUP_RX_TX_ER. 9: RX_ER. 10: RX_TX_ER. 11: TX_SOP. 12: RX_SOP.	0xE	R/W

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Table 228. Bit Descriptions for LED_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
		13: on. 14: off. 15: blink. 16: TX_LEVEL_2P4. 17: TX_LEVEL_1P0. 18: master. 19: slave. 20: INCOMPATIBLE_LINK_CFG. 21: AN_LINK_GOOD. 22: AN_COMPLETE. 23: TS_TIMER. 24: LOC_RCVR_STATUS. 25: REM_RCVR_STATUS. 26: CLK25_REF. 27: TX_TCLK. 28: CLK_120MHZ.		
7	LED0_EN	LED 0 Enable. A disabled LED is off. An enabled LED can be on or blinking depending on LED0_FUNCTION selection and activity.	0x1	R/W
6	LED0_LINK_ST_QUALIFY	Qualify Certain LED 0 Options with link_status. 0: TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave not qualified by link_status. 1: TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave are qualified by link_status.	0x0	R/W
5	LED0_MODE	LED 0 Mode Selection. 0: LED Mode 1. If activity, blink at the rate defined by MMR LED0_BLINK_TIME_CNTRL. 1: LED Mode 2. The LED blink frequency is set depending on the level of activity. The activity level is graded in steps of 10%, and the frequency of the LED adjusts accordingly. A higher activity level means a longer off duration and shorter on duration. The activity level is reevaluated after a window period that varies between 640 ms and 1.5 sec.	0x0	R/W
[4:0]	LED0_FUNCTION	LED 0 Pin Function. Determines the source activity for the LED pin. The CLK25_REF, TX_TCLK, CLK_120MHZ options are clock out features with the LED controller bypassed. The waveform transmitted off chip is dependent on the selected clock source frequency. The following LED_FUNCTION settings are not qualified with link_status: LED_FUNCTION = on, off, blink, INCOMPATIBLE_LINK_CFG, AN_LINK_GOOD, AN_COMPLETE, LOC_RCVR_STATUS, REM_RCVR_STATUS, CLK25_REF, TX_TCLK and CLK_120MHz. Options TX_LEVEL_2P4, TX_LEVEL_1P0, master, and slave are optionally qualified by link status and this is controlled via the LED0_LINK_ST_QUALIFY MMR. The TX_LEVEL_2P4, TX_LEVEL_1P0, master, slave, MSTR_SLV_FAULT, AN_LINK_GOOD, AN_COMPLETE, and TS_TIMER. These options are considered status indicators and the LED controller is not used. If the programmed signal is high, the LED is static on and if the programmed signal is low, the LED is static off. 0: LINKUP_TXRX_ACTIVITY. 1: LINKUP_TX_ACTIVITY. 2: LINKUP_RX_ACTIVITY. 3: LINKUP_ONLY. 4: TXRX_ACTIVITY. 5: TX_ACTIVITY. 6: RX_ACTIVITY. 7: LINKUP_RX_ER.	0x0	R/W

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Table 228. Bit Descriptions for LED_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
		8: LINKUP_RX_TX_ER. 9: RX_ER. 10: RX_TX_ER. 11: TX_SOP. 12: RX_SOP. 13: on. 14: off. 15: blink. 16: TX_LEVEL_2P4. 17: TX_LEVEL_1P0. 18: master. 19: slave. 20: INCOMPATIBLE_LINK_CFG. 21: AN_LINK_GOOD. 22: AN_COMPLETE. 23: TS_TIMER. 24: LOC_RCVR_STATUS. 25: REM_RCVR_STATUS. 26: CLK25_REF. 27: TX_TCLK. 28: CLK_120MHZ.		

LED Polarity Register

Device Address: 0x1E; Register Address: 0x8C83, Reset: 0x0000, Name: LED_POLARITY

Allows the LED polarity to be automatically sensed by the internal logic or allows reconfiguration by the user.

Table 229. Bit Descriptions for LED_POLARITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:2]	LED1_POLARITY	LED 1 Polarity. 0: LED autosense. LED active high or low as per autosense. 1: LED active high. 2: LED active low.	0x0	R/W
[1:0]	LED0_POLARITY	LED 0 Polarity. 0: LED autosense. LED active high or low as per autosense. 1: LED active high. 2: LED active low.	0x0	R/W

Vendor Specific MMD 2 Device Identifier High Register

Device Address: 0x1F; Register Address: 0x0002, Reset: 0x0283, Name: MMD2_DEV_ID1

Table 230. Bit Descriptions for MMD2_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEV_ID1	Vendor Specific MMD 2 Device Identifier.	0x283	R

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Vendor Specific MMD 2 Device Identifier Low Register

Device Address: 0x1F; Register Address: 0x0003, Reset: 0xBC01, Name: MMD2_DEV_ID2

Table 231. Bit Descriptions for MMD2_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD2_DEV_ID2_OUI	OUI Bits.	0x2F	R
[9:4]	MMD2_MODEL_NUM	Model Number.	0xA	R
[3:0]	MMD2_REV_NUM	Revision Number.	0x1	R

Vendor Specific 2 MMD Devices in Package Register

Device Address: 0x1F; Register Address: 0x0005, Reset: 0x008B, Name: MMD2_DEVS_IN_PKG1

Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.

Table 232. Bit Descriptions for MMD2_DEVS_IN_PKG1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEVS_IN_PKG1	Vendor Specific 2 MMDs in Package 1. Clause 22 registers and PMA/PMD, PCS, and autonegotiation MMDs are present.	0x8B	R

Device Address: 0x1F; Register Address: 0x0006, Reset: 0xC000, Name: MMD2_DEVS_IN_PKG2

Vendor Specific 1 and Vendor Specific 2 MMDs are present.

Table 233. Bit Descriptions for MMD2_DEVS_IN_PKG2

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD2_DEVS_IN_PKG2	Vendor Specific 2 MMDs in Package 2. Vendor Specific 1 and Vendor Specific 2 MMDs are present.	0xC000	R

Vendor Specific MMD 2 Status Register

Device Address: 0x1F; Register Address: 0x0008, Reset: 0x8000, Name: MMD2_STATUS

This address corresponds to the Vendor Specific MMD 2 status register.

Table 234. Bit Descriptions for MMD2_STATUS

Bits	Bit Name	Description	Reset	Access
[15:14]	MMD2_STATUS	Vendor specific 2 MMD Status. 10: device responding at this address. 11: no device responding at this address. 01: no device responding at this address. 00: no device responding at this address.	0x2	R
[13:0]	RESERVED	Reserved.	0x0	R

PHY Subsystem Interrupt Status Register

Device Address: 0x1F; Register Address: 0x0011, Reset: 0x0000, Name: PHY_SUBSYS_IRQ_STATUS

This address can be read to check which interrupt events have occurred since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of PHY_SUBSYS_IRQ_STATUS go high even when the associated bits in PHY_SUBSYS_IRQ_MASK are not set. A reserved interrupt being triggered indicates a fatal error in the system.

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Table 235. Bit Descriptions for PHY_SUBSYS_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R LH
14	MAC_IF_FC_FG_IRQ_LH	MAC Interface Frame Checker/Generator Interrupt.	0x0	R LH
13	MAC_IF_EBUF_ERR_IRQ_LH	MAC Interface Buffers Overflow/Underflow Interrupt.	0x0	R LH
12	RESERVED	Reserved.	0x0	R LH
11	AN_STAT_CHNG_IRQ_LH	Autonegotiation Status Change Interrupt.	0x0	R LH
[10:2]	RESERVED	Reserved.	0x0	R LH
1	LINK_STAT_CHNG_LH	Link Status Change.	0x0	R LH
0	RESERVED	Reserved.	0x0	R LH

PHY Subsystem Interrupt Mask Register

Device Address: 0x1F; Register Address: 0x0021, Reset: 0x2402, Name: PHY_SUBSYS_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 236. Bit Descriptions for PHY_SUBSYS_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	MAC_IF_FC_FG_IRQ_EN	Enable MAC Interface Frame Checker/Generator Interrupt.	0x0	R/W
13	MAC_IF_EBUF_ERR_IRQ_EN	Enable MAC Interface Buffers Overflow/Underflow Interrupt.	0x1	R/W
12	RESERVED	Reserved.	0x0	R/W
11	AN_STAT_CHNG_IRQ_EN	Enable Autonegotiation Status Change Interrupt.	0x0	R/W
[10:2]	RESERVED	Reserved.	0x100	R/W
1	LINK_STAT_CHNG_IRQ_EN	Enable Link Status Change Interrupt.	0x1	R/W
0	RESERVED	Reserved.	0x0	R/W

Frame Checker Enable Register

Device Address: 0x1F; Register Address: 0x8001, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 237. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	Frame Checker Enable. Set to 1 to enable the frame checker.	0x1	R/W

Frame Checker Interrupt Enable Register

Device Address: 0x1F; Register Address: 0x8004, Reset: 0x0001, Name: FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register.

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Table 238. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	Frame Checker Interrupt Enable. When set, this bit enables the frame checker interrupt.	0x1	R/W

Frame Checker Transmit Select Register

Device Address: 0x1F; Register Address: 0x8005, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received from the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (see the MAC_IF_REM_LB_EN bit in the MAC_IF_LOOPBACK register) because it can be used to check the received data after it is looped back at the MAC interface.

Table 239. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	Frame Checker Transmit Select. When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Receive Error Count Register

Device Address: 0x1F; Register Address: 0x8008, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY.

Table 240. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	Receive Error Count. This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self clearing upon reading.	0x0	R SC

Frame Checker Count High Register

Device Address: 0x1F; Register Address: 0x8009, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits[31:16] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and the receive frame count are synchronized.

Table 241. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits[31:16] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Count Low Register

Device Address: 0x1F; Register Address: 0x800A, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits[15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and receive frame count are synchronized.

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Table 242. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits[15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Length Error Count Register

Device Address: 0x1F; Register Address: 0x800B, Reset: 0x0000, Name: FC_LEN_ERR_CNT

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized.

Table 243. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Alignment Error Count Register

Device Address: 0x1F; Register Address: 0x800C, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT) is read, the alignment error counter is latched, which ensures that the frame alignment error count and the receive frame count are synchronized.

Table 244. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Count Register

Device Address: 0x1F; Register Address: 0x800D, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT) is read, the symbol error count is latched, which ensures that the symbol error count and the frame receive count are synchronized.

Table 245. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYMB_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Oversized Frame Count Register

Device Address: 0x1F; Register Address: 0x800E, Reset: 0x0000, Name: FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of receiver frames with a length greater than 1522 bytes. When the receive error counter (RX_ERR_CNT) is read, the oversized frame counter register is latched, which ensures that the oversized error count and the receive frame count are synchronized.

Table 246. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched Copy of the Overisized Frame Error Counter.	0x0	R

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Frame Checker Undersized Frame Count Register

Device Address: 0x1F; Register Address: 0x800F, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with less than 64 bytes. When the receive error counter (RX_ERR_CNT) is read, the undersized frame error counter is latched, which ensures that the undersized frame error count and the receive frame count are synchronized.

Table 247. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Device Address: 0x1F; Register Address: 0x8010, Reset: 0x0000, Name: FC_ODD_CNT

This register is a latched copy of the odd nibble frame register. This register is a count of received frames with an odd number of nibbles in the frame. When the receive error counter (RX_ERR_CNT) is read, the odd nibble frame counter register is latched, which ensures that the odd nibble frame count and the receive frame count are synchronized.

Table 248. Bit Descriptions for FC_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_CNT	Latched Copy of the Odd Nibble Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Device Address: 0x1F; Register Address: 0x8011, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received packets with an odd number of nibbles in the preamble. When the receive error counter (RX_ERR_CNT) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and the receive frame count are synchronized.

Table 249. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_PRE_CNT	Latched Copy of the Odd Preamble Packet Counter.	0x0	R

Frame Checker False Carrier Count Register

Device Address: 0x1F; Register Address: 0x8013, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This register is a count of the number of times the bad SSD state is entered. When the receive error counter (RX_ERR_CNT) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and the receive frame count are synchronized.

Table 250. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Device Address: 0x1F; Register Address: 0x8020, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled (CRSM_DIAG_CLK_EN).

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Table 251. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_EN	Frame Generator Enable.	0x0	R/W

Frame Generator Control/Restart Register

Device Address: 0x1F; Register Address: 0x8021, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register controls the frame generator. The FG_CNTRL bit field specifies data field type used by the frame generator, for example, random or all zeros. The FG_RSTRT bit restarts the frame generator.

Table 252. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	Frame Generator Restart. When set, this bit restarts the frame generator. This bit is self clearing.	0x0	R/W SC
[2:0]	FG_CNTRL	Frame Generator Control. 000: no frames after completion of current frame. 001: random number data frame. 010: all zeros data frame. 011: all ones data frame. 100: alternative 0x55 data field. 101: data field decrementing from 255 (decimal) to 0.	0x1	R/W

Frame Generator Continuous Mode Enable Register

Device Address: 0x1F; Register Address: 0x8022, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H and FG_NFRM_L registers.

Table 253. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable. This bit is used to put the frame generator into continuous mode or burst mode. 1: frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames is determined by the FG_NFRM_H and FG_NFRM_L registers.	0x0	R/W

Frame Generator Interrupt Enable Register

Device Address: 0x1F; Register Address: 0x8023, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The interrupt status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register

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Table 254. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	Frame Generator Interrupt Enable. When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

Frame Generator Frame Length Register

Device Address: 0x1F; Register Address: 0x8025, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the data field frame length in bytes. In addition to the data field, six bytes are added for the source address, six bytes for the destination address, two bytes for the length field, and four bytes for the frame check sequence (FCS). The total length is the data field length plus 18.

Table 255. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Interframe Gap Length Register

Device Address: 0x1F; Register Address: 0x8026, Reset: 0x000C, Name: FG_IFG_LEN

This register specifies the length in bytes of the interframe gap to be inserted between frames by the frame generator.

Table 256. Bit Descriptions for FG_IFG_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_IFG_LEN	Frame Generator Interframe Gap Length. This register specifies the length in bytes of the interframe gap to be inserted between frames by the frame generator.	0xC	R/W

Frame Generator Number of Frames High Register

Device Address: 0x1F; Register Address: 0x8027, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits[31:16] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 257. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits[31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Device Address: 0x1F; Register Address: 0x8028, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits[15:0] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 258. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits[15:0] of the Number of Frames to be Generated.	0x100	R/W

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Frame Generator Done Register

Device Address: 0x1F; Register Address: 0x8029, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H and FG_NFRM_L registers.

Table 259. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	Frame Generator Done. This bit reads as 1 to indicate that the generation of frames has completed. When set, this bit goes high and it latches high until it is unlatched by reading.	0x0	R LH

MAC Interface Loopbacks Configuration Register

Device Address: 0x1F; Register Address: 0x8055, Reset: 0x000A, Name: MAC_IF_LOOPBACK

MAC interface loopbacks configuration.

Table 260. Bit Descriptions for MAC_IF_LOOPBACK

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	MAC_IF_REM_LB_RX_SUP_EN	Suppress RX Enable. Suppress receiver to the MAC when MAC_IF_REM_LB_EN is set.	0x1	R/W
2	MAC_IF_REM_LB_EN	MAC Interface Remote Loopback Enable. Receive data is looped back to the transmitter.	0x0	R/W
1	MAC_IF_LB_TX_SUP_EN	Suppress Transmission Enable. Suppress transmission to the PHY when MAC_IF_LB_EN is set.	0x1	R/W
0	MAC_IF_LB_EN	MAC Interface Loopback Enable. Transmit data is looped back to the receiver.	0x0	R/W

MAC Start Of Packet (SOP) Generation Control Register

Device Address: 0x1F; Register Address: 0x805A, Reset: 0x001B, Name: MAC_IF_SOP_CNTRL

Table 261. Bit Descriptions for MAC_IF_SOP_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	MAC_IF_TX_SOP_LEN_CHK_EN	Enable Tx SOP Preamble Length Check.	0x0	R/W
4	MAC_IF_TX_SOP_SFD_EN	Enable Tx SOP Signal Indication on SFD.	0x1	R/W
3	MAC_IF_TX_SOP_DET_EN	Enable the Generation of the Tx SOP Indication Signal.	0x1	R/W
2	MAC_IF_RX_SOP_LEN_CHK_EN	Enable RX SOP Preamble Length Check. If this bit is set and no SFD is received, the RX SOP signal indication is set after eight bytes. Otherwise, the RX SOP is not set if no SFD is received in the first eight bytes.	0x0	R/W
1	MAC_IF_RX_SOP_SFD_EN	Enable RX SOP Signal Indication on SFD Reception. If both MAC_IF_RX_SOP_DET_EN and MAC_IF_RX_SOP_SFD_EN are set, the RX SOP signal is set when the SFD is received. Otherwise, the RX SOP is set when RX_DV is set. The RX SOP signal remains set until the end of the frame.	0x1	R/W
0	MAC_IF_RX_SOP_DET_EN	Enable the Generation of the Rx SOP Indication Signal.	0x1	R/W

PCB LAYOUT RECOMMENDATIONS

LAND PATTERN

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical, electrical, and thermal reasons.

For thermal impedance performance and to maximize heat transfer to the PCB, the use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended. Via tenting is also recommended.

COMPONENT PLACEMENT AND ROUTING

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout. The critical components are the crystal and load capacitors, the CEXT_2, CEXT_3, CEXT_6, and CEXT_7 capacitors, and all bypass capacitors local to the ADIN2111 device. Prioritize these components for placement and routing, as follows:

- Place the decoupling capacitor as close as possible to their input pins.
- Minimize traces turns, and use a 45° corner.
- Avoid traces crossing power planes on adjacent layers.
- Avoid stubs.
- Keep the MDI traces (P1_TXP, P1_TXN, P2_TXP, and P2_TXN) as short as possible.
- Use matched length differential lines for each port with a differential impedance of 100 Ω.
- Avoid vias on a high speed signal. Place ground vias next to the signal vias to improve the return current path.

CRYSTAL PLACEMENT AND ROUTING

Particular attention is required on the crystal placement and routing to ensure minimum current consumption, reduce stray capacitance, and improve noise immunity.

Follow these recommendations:

- Place the crystal, capacitors as close as possible to the ADIN2111 XTAL_I/CLK_IN and XTAL_O pins.
- Place the load capacitors close to each other.
- Use a local GND plane (copper island) for the crystal and load capacitors with a single point connection to the main GND.
- Reduce parasitic capacitance by keeping the XTAL_I and XTAL_O traces away from each other.
- Adding a copper keepout on the layer beneath the crystal can also reduce the parasitic capacitance.

PCB STACK

Follow these recommendations for the PCB stack:

- Use a PCB stack with a minimum of four layers. Consider six layers or more with external layers used as ground planes to improve EMI issues (optional).
- Define copper layer thickness based on the application and power requirements.
- Use internal layers for the power and ground planes.
- Use external layers for the signal traces.
- Use via stitching to improve ground and reduce EMI. The stitching pattern and via to via gaps are defined based on the application.

OUTLINE DIMENSIONS

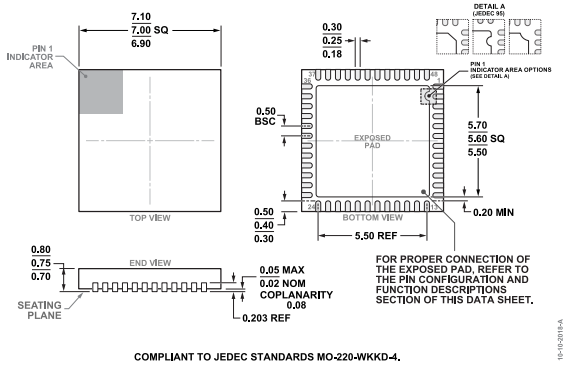

Figure 32. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-13)
Dimensions shown in millimeters

Updated: December 18, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADIN2111BCPZ	-40°C to +85°C	48-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)		CP-48-13
ADIN2111BCPZ-R7	-40°C to +85°C	48-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)	Reel, 750	CP-48-13
ADIN2111CCPZ	-40°C to +105°C	48-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)		CP-48-13
ADIN2111CCPZ-R7	-40°C to +105°C	48-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)	Reel, 750	CP-48-13

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Package Description
EVAL-ADIN2111EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ADIN2111CCPZ on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management