THE DATASHEET OF

LT8491IUKJ#PBF

High Voltage Buck-Boost Battery Charge Controller with Maximum Power Point Tracking (MPPT) and I²C

FEATURES

- **V_{IN} Range: 6V to 80V**
- **V_{BAT} Range: 1.3V to 80V**
- **Single Inductor Allows V_{IN} Above, Below, or Equal to V_{BAT}**
- **Automatic MPPT for Solar Powered Charging**
- **Automatic Temperature Compensation**
- **I²C Telemetry and Configuration**
- **Internal EEPROM for Configuration Storage**
- **Operation from Solar Panel or DC Supply**
- **Four Integrated Feedback Loops**
- Synchronizable Fixed Frequency: 100kHz to 400kHz
- 64-Lead (7mm × 11mm × 0.75mm) QFN Package

APPLICATIONS

- Solar Powered Battery Chargers
- Multiple Types of Lead-Acid Battery Charging
- Li-Ion Battery Charger
- Battery Equipped Industrial or Portable Military Equipment

DESCRIPTION

The LT®8491 is a buck-boost switching regulator battery charger that implements a constant-current constant-voltage (CCCV) charging profile used for most battery types, including sealed lead-acid (SLA), flooded, gel and lithium-ion.

The device operates from input voltages above, below or equal to the output voltage and can be powered by a solar panel or a DC power supply. On-chip logic provides automatic maximum power point tracking (MPPT) for solar powered applications. The LT8491 can perform automatic temperature compensation by sensing an external thermistor thermally coupled to the battery. The STATUS pin can be used to drive an LED indicator lamp. The device is available in a low profile (0.75mm) 7mm × 11mm 64-lead QFN package.

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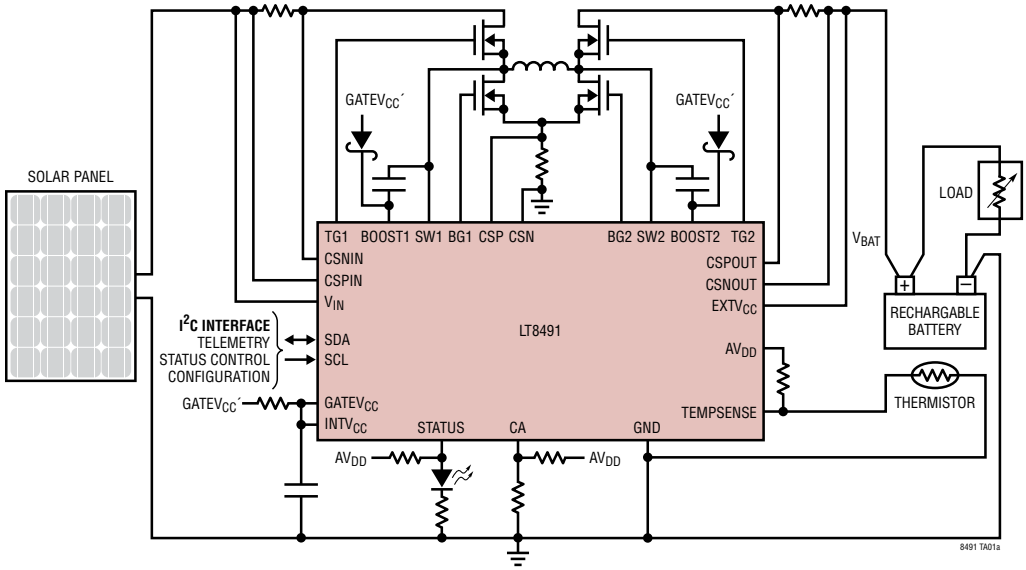
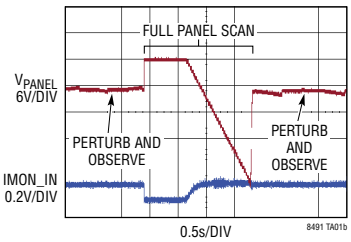
TYPICAL APPLICATION

Simplified Solar Powered Battery Charger Schematic



Maximum Power Point Tracking



Rev. 0

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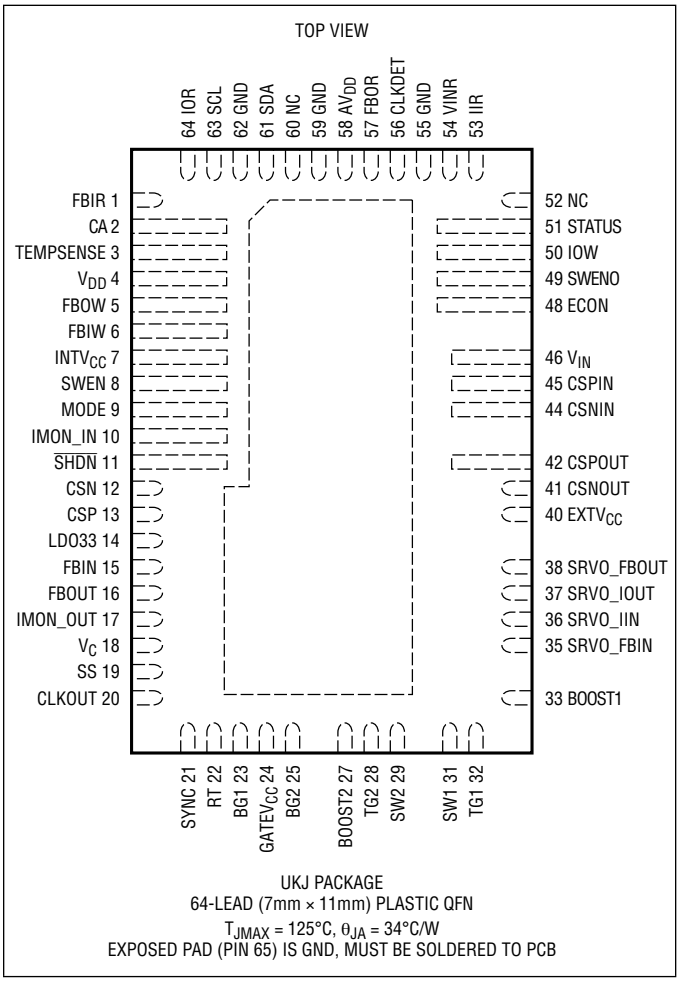
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CSP} – V_{CSN}$, $V_{CSPIN} – V_{CSNIN}$,
$V_{CSPOUT} – V_{CSNOUT}$ ..... –0.3V to 0.3V
SS, CLKOUT, CSP, CSN Voltage ..... –0.3V to 3V
V_C Voltage (Note 2) ..... –0.3V to 2.2V
LDO33, V_{DD}, AV_{DD}, Voltage ..... –0.3V to 5V
RT, FBOUT Voltage ..... –0.3V to 5V
IMON_IN, IMON_OUT Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage ..... –0.3V to 7V
$V_{BOOST1} – V_{SW1}$, $V_{BOOST2} – V_{SW2}$ ..... –0.3V to 7V
SWEN, MODE Voltage ..... –0.3V to 7V
SRVO_FBIN, SRVO_FBOUT Voltage ..... –0.3V to 30V
SRVO_IIN, SRVO_IOUT Voltage ..... –0.3V to 30V
FBIN, $\overline{SHDN}$ Voltage ..... –0.3V to 30V
CSNIN, CSPIN, CSPOUT,
CSNOUT Voltage ..... –0.3V to 80V
V_{IN}, $EXTV_{CC}$ Voltage ..... –0.3V to 80V
SW1, SW2 Voltage ..... 81V (Note 5)
BOOST1, BOOST2 Voltage ..... –0.3V to 87V
BG1, BG2, TG1, TG2 ..... (Note 4)
IOW, ECON, CLKDET Voltage ..... –0.3V to V_{DD} + 0.5V
SWENO, STATUS Voltage ..... –0.3V to V_{DD} + 0.5V
FBOW, FBIW, Voltage ..... –0.3V to V_{DD} + 0.5V
VINR, FBOR, IIR, IOR Voltage ..... –0.3V to V_{DD} + 0.5V
TEMPSENSE Voltage ..... –0.3V to V_{DD} + 0.5V
SDA, SCL, CA Voltage ..... –0.3V to V_{DD} + 0.5V
Operating Junction Temperature Range
LT8491E (Notes 1, 3) ..... –40°C to 125°C
LT8491I (Notes 1, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8491EUKJ#PBF	LT8491EUKJ#TRPBF	LT8491UKJ	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 125°C
LT8491IUKJ#PBF	LT8491IUKJ#TRPBF	LT8491UKJ	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supply and Regulators						
V_{IN} Operating Voltage Range (Note 7)		●	6		80	V
V_{IN} Quiescent Current	Not Switching, V_{EXTVCC} = 0, V_{DD} = AV_{DD} = Float			2.65	4.2	mA
V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
V_{DD} Quiescent Current	I_{AVDD} + I_{VDD}, V_{DD} = AV_{DD} = 3.3V	●	2.5	4	6.5	mA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.18		V
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit		●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device	●	1.184	1.234	1.284	V
$\overline{SHDN}$ Input Voltage High Hysteresis				50		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current	●			0.35	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 11	1 22	µA µA
SWEN Rising Threshold Voltage		●	1.156	1.206	1.256	V
SWEN Threshold Voltage Hysteresis				22		mV
MODE Pin Thresholds	Discontinuous Mode Automatic DCM/CCM Mode	● ●	 0.4		2.3	V V
IMON_OUT Rising threshold for CCM Operation	MODE = 0V		168	195	224	mV
IMON_OUT Falling threshold for DCM	MODE = 0V		95	122	150	mV
Voltage Regulation						
Regulation Voltage for FBOUT	V_C = 1.2V, $EXTV_{CC}$ = 0	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	V_C = 1.2V, $EXTV_{CC}$ = 0	●	1.184	1.205	1.226	V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBIN Pin Bias Current	Current Out of Pin			10		nA
Current Regulation						
Regulation Voltage for IMON_IN and IMON_OUT	VC = 1.2V, $EXTV_{CC}$ = 0	●	1.187	1.208	1.229	V
IMON_IN Output Current	V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSPIN} = 5.025V V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSPIN} = 5.025V V_{CSPIN} – V_{CSNIN} = 0mV, V_{CSPIN} = 5V	 ● ●	54 53 2.5	57 57 7	60 61 11.5	µA µA µA
IMON_IN Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_OUT Output Current	V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V	 ● ●	47.5 47 3.25 2.75	50 50 5 5	52.5 54.25 6.75 8	µA µA µA µA
IMON_OUT Overvoltage Threshold		●	1.55	1.61	1.67	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Oscillator (OSC1)						
Switch Frequency Range	Syncing or Free Running		100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365kΩ R_T = 215kΩ R_T = 124kΩ	● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Min SYNC Ratio, f_{SYNC}/f_{OSC}				¾		f/f
CLKOUT Output Voltage HIGH	1mA Out of CLKOUT Pin		2.3	2.45	2.55	V
CLKOUT Output Voltage LOW	1mA into CKLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %
Charging Control						
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output Low Voltage	I_{OL} = 5mA	●		0.22	0.5	V
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output High Voltage	I_{OH} = –5mA	●	2.7	3		V
Power Supply Mode Detection Threshold (Note 6)	VINR Pin Falling	●	155	174		mV
Power Supply Mode Detection Threshold Hysteresis (Note 6)				29		mV
Minimum VINR Voltage for Startup (Note 6)	Not in Power Supply Mode Low Power Mode Enabled Low Power Mode Disabled	 ● ●	 380 213	 395 225	 410 237	 mV mV
High Charging Current Threshold on IOR (Note 6)	IOR Rising → ECON Rising	●	168	195	224	mV
Low Charging Current Threshold on IOR (Note 6)	IOR Falling → ECON Falling	●	95	122	150	mV
Minimum TEMPSENSE % of AV_{DD} to Detect Battery Disconnected (Note 6)		●	94.5	96	97.5	%
V_{CSPOUT} – V_{CSNOUT} Threshold for C/5 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		9	10	11	mV
V_{CSPOUT} – V_{CSNOUT} Threshold for C/10 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, IOR Falling, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		4.25	5	5.75	mV
FBIW, FBOW PWM Frequency (OSC2)				31.25		kHz
FBIW, FBOW PWM Resolution				8		bits
Internal A/D Resolution				10		bits

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EEPROM Characteristics						
Endurance (Note 8)	0°C < T_J < 85°C During EEPROM Write Operations		100,000			Cycles
Digital Input/Output SCL, SDA						
SDA Input Voltage High (V_{SDA_VIH})		●	2.25			V
SDA Input Voltage Low (V_{SDA_VIL})		●			0.65	V
SCL Input Voltage High (V_{SCL_VIH})		●	2.25			V
SCL Input Voltage Low (V_{SCL_VIL})		●			0.65	V
SDA Input Leakage Current (I_{LEAK_SDA})	SDA = 0V and 3.3V	●		<0.05	±1	µA
SCL Input Leakage Current (I_{LEAK_SCL})	SCL = 0V and 3.3V	●		<0.05	±1	µA
SDA Output Low Voltage (V_{SDA_OL})	3mA into SDA Pin	●			0.4	V
I^2C Timing Characteristics						
Serial Clock Frequency (f_{SCL})		●			100	kHz
Serial Clock Low Period (t_{LOW})		●	4.7			µs
Serial Clock High Period (t_{HIGH})		●	4			µs
Bus Free Time Between Stop and Start (t_{BUF})		●	4.7			µs
Start Condition Hold Time ($t_{HD,STA}$)		●	4			µs
Start Condition Setup Time ($t_{SU,STA}$)		●	4.7			µs
Stop Condition Setup Time ($t_{SU,STO}$)		●	4			µs
Data Hold Time ($t_{HD,DAT}$) (Note 9)		●	0			ns
Data Setup Time ($t_{SU,DAT}$)		●	250			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8491E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8491I is guaranteed over the full –40°C to 125°C junction temperature range.

Note 4: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only; otherwise permanent damage may occur.

Note 5: Negative voltages on the SW1 and SW2 pins are limited in the applications by the body diodes of the external NMOS devices M2 and M3 or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages more than one diode drop below ground, guaranteed by design.

Note 6: These thresholds are measured by the internal A/D converter. The A/D reference voltage is AV_{DD}. AV_{DD}, V_{DD} and an additional 2.8mA load are regulated by LDO33 to create the AV_{DD} reference for these measurements. The absolute threshold voltages will shift with corresponding changes in the AV_{DD} voltage.

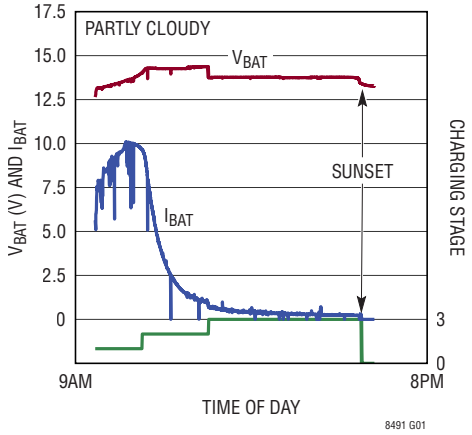
Note 7: 10V minimum V_{IN} required for solar powered start-up if low power mode is enabled.

Note 8: The EEPROM has an endurance of at least 100,000 write/erase cycles. Data retention of 20 years at 85°C, 100 years at 25°C. These statements are based on published information from vendor.

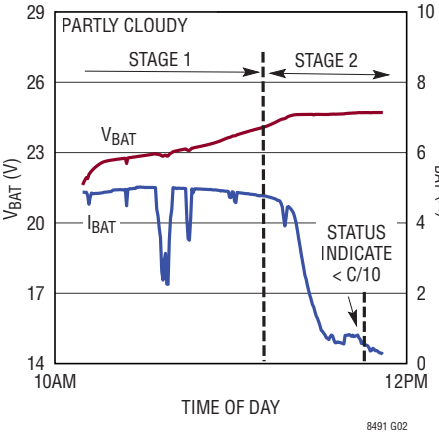
Note 9: A master device must provide a hold time of at least 300ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the SCL falling edge.

TYPICAL PERFORMANCE CHARACTERISTICS

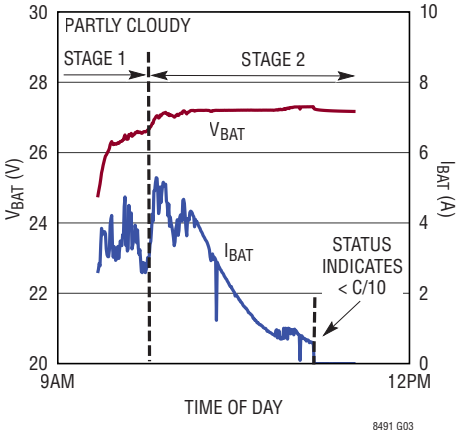
Solar Powered Charging Lead-Acid Battery



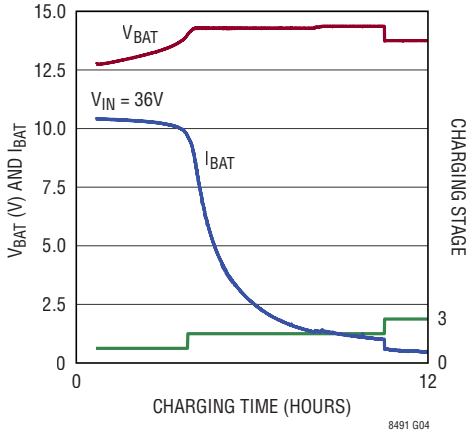
Solar Powered Charging Lithium-Ion Battery



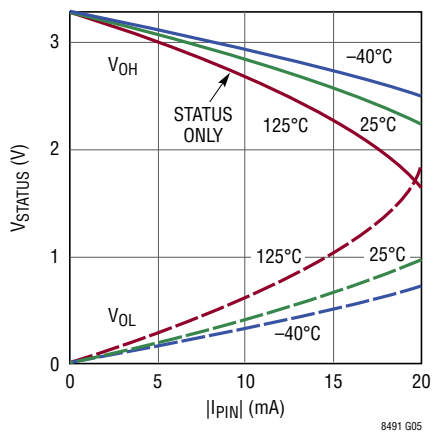
Solar Powered Charging Lithium-Ion Battery – C/10 Termination



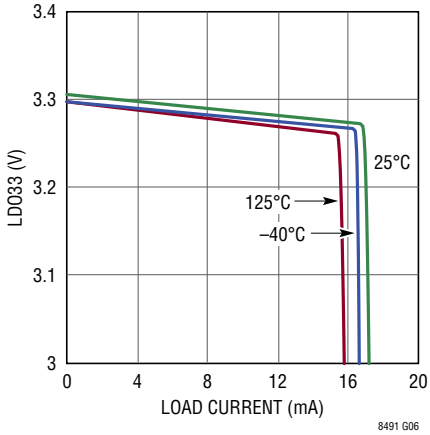
Power Supply Mode Charging Lead-Acid Battery



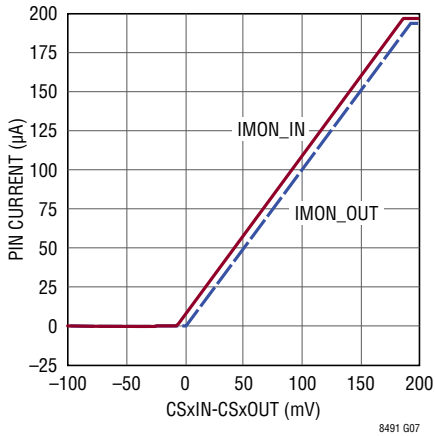
STATUS, SDA, SCL V_{OH} and V_{OL} (V_{DD} = AV_{DD} = 3.3V)



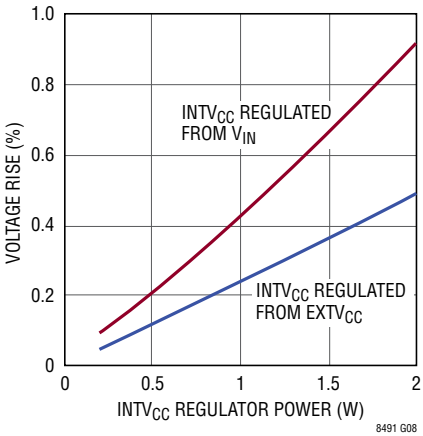
LDO33 Load Regulation (Not Connected to AV_{DD} and V_{DD})



IMON Output Currents



FBOUT, FBIN, IMONIN, IMONOUT Voltage Rise vs Power



TYPICAL PERFORMANCE CHARACTERISTICS

Max Power Point Tracking

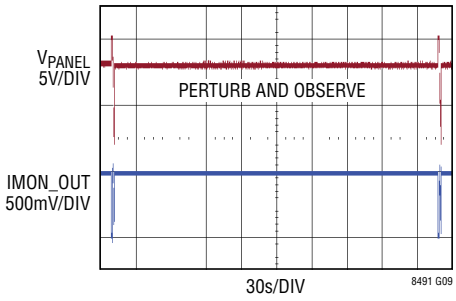


FIGURE 37 APPLICATION

Perturb and Observe

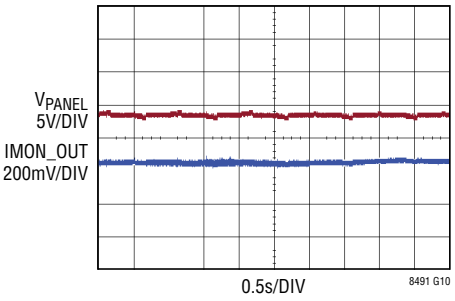


FIGURE 37 APPLICATION

Perturb and Observe

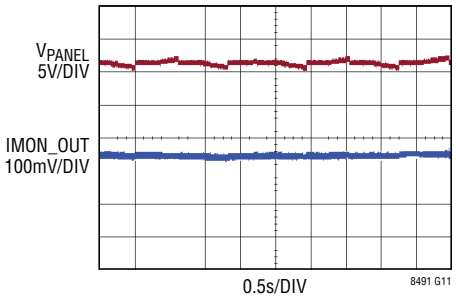


FIGURE 37 APPLICATION

Perturb and Observe Max Power Point Tracking

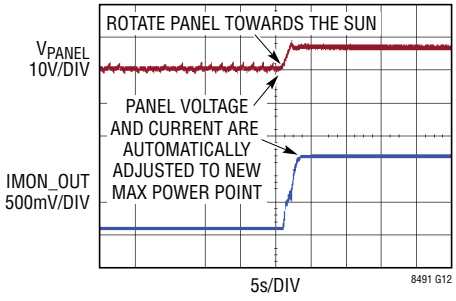


FIGURE 37 APPLICATION

Full Panel Scan Single Power Peak

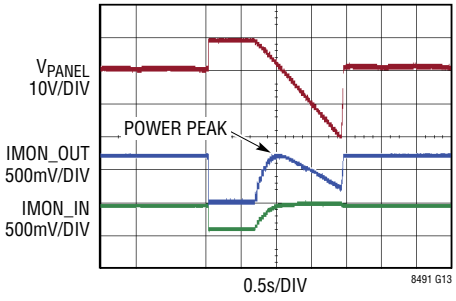


FIGURE 37 APPLICATION

Full Panel Scan – Partially Shaded with Dual Power Peaks

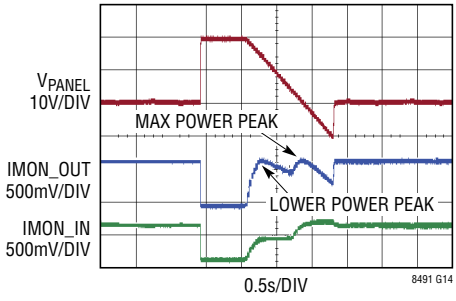


FIGURE 37 APPLICATION

Panel Voltage in Low Power Mode

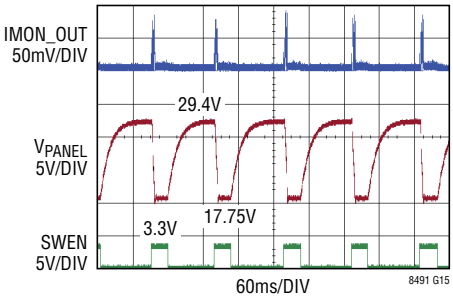


FIGURE 37 APPLICATION

Panel Voltage in Low Power Mode

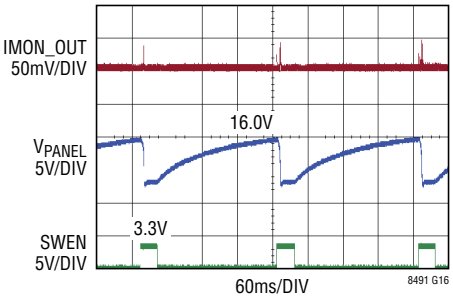


FIGURE 37 APPLICATION

PIN FUNCTIONS

FBIR (Pin 1): A/D Input Pin. Connects to FBIN pin to measure input voltage.

CA (Pin 2): A/D Input Pin. Connects to a resistor divider to program the I^2C address. This pin is measured during the power up sequence.

TEMPSENSE (Pin 3): A/D Input Pin. Connects to a thermistor divider network for sensing battery temperature or a resistor divider if unused. This pin is frequently monitored for temperature compensation and enforcing temperature limits.

V_{DD} (Pin 4): I^2C and Control Logic Power Supply Pin. Connect this pin to LDO33 and AV_{DD}.

FBOW (Pin 5): PWM Digital Output Pin. Connects to FBOUT through an RCR network to temperature compensate the battery voltage.

FBIW (Pin 6): PWM Digital Output Pin. Connects to FBIN through an RCR network to adjust the solar panel voltage for MPPT.

$INTV_{CC}$ (Pin 7): Internal 6.35V Regulator Output Pin. Connects to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{IN}. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor. See HW Config: MODE Pin - Current Conduction Mode for additional details.

SWEN (Pin 8): Switch Enable Pin. Tie to the SWENO pin.

MODE (Pin 9): Mode Pin. The voltage applied to this pin sets the operating mode of the switching regulator. Tie this pin to $INTV_{CC}$ to make discontinuous current mode active. Tie this pin to ground to operate in discontinuous current mode for low battery charging currents and continuous current mode for high battery charging currents. Do not float this pin. See HW Config: MODE Pin - Current Conduction Mode for additional details.

IMON_IN (Pin 10): Input Current Monitor and Limit Pin. The current out of this pin is proportional to the input current. See the Applications Information section for more information.

$\overline{SHDN}$ (Pin 11): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip. Do not float this pin.

CSN (Pin 12): The (–) Input to the Inductor Current Sense and Reverse Current Detect Amplifier.

CSP (Pin 13): The (+) Input to the Inductor Current Sense and Reverse Current Detect Amplifier. The V_C pin voltage and built-in offsets between the CSP and CSN pins set the inductor current trip threshold.

LDO33 (Pin 14): 3.3V Regulator Output. This pin provides power to the V_{DD} and AV_{DD} pins. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

FBIN (Pin 15): Input Feedback Pin. This pin is connected to the input error amplifier input.

FBOUT (Pin 16): Output Feedback Pin. This pin connects the error amplifier input to an external resistor divider from the output.

IMON_OUT (Pin 17): Output Current Monitor and Limit Pin. The current out of this pin is proportional to the average output current. See the Applications Information section for more information.

V_C (Pin 18): Error Amplifier Output Pin. Tie the external compensation network to this pin.

SS (Pin 19): Soft-Start Pin. Place 100nF of capacitance from this pin to ground. Upon start-up, this pin will be charged by an internal resistor to 2.5V.

CLKOUT (Pin 20): Switching Regulator Clock Output Pin. CLKOUT will toggle at the same frequency as the switching regulator oscillator (OSC1 on the Block Diagram) or as the SYNC pin but is approximately 180° out-of-phase. CLKOUT can also be used as a temperature monitor of the switching regulator since the CLKOUT duty cycle varies linearly with the junction temperature of the switching regulator. It is connected to the CLKDET pin through an RC filter. The CLKOUT pin can drive capacitive loads up to 200pF.

PIN FUNCTIONS

SYNC (Pin 21): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock (OSC1 in the Block Diagram).

RT (Pin 22): Timing Resistor Pin. Adjusts the switching regulator frequency (OSC1) when SYNC is not driven by a clock. Place a resistor from this pin to ground to set the free-running frequency of OSC1. Do not float this pin.

BG1, BG2 (Pin 23/Pin 25): Bottom Gate Drive. Drives the gates of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 24): Power Supply for Gate Drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to ground.

BOOST1, BOOST2 (Pin 33/Pin 27): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{BAT} + $GATEV_{CC}$.

SW1, SW2 (Pin 31/Pin 29): Switch Nodes. The (–) terminal of the bootstrap capacitors connect here.

TG1, TG2 (Pin 32/Pin 28): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SRVO_FBIN (Pin 35): Open-Drain Logic Output. This pin is pulled to ground when the input voltage feedback loop is active. This pin is unused for most LT8491 applications and can be floated.

SRVO_IIN (Pin 36): Open-Drain Logic Output. This pin is pulled to ground when the input current feedback loop is active. This pin is unused for most LT8491 applications and can be floated.

SRVO_IOUT (Pin 37): Open-Drain Logic Output. This pin is pulled to ground when the output current feedback loop is active. This pin is unused for most LT8491 applications and can be floated.

SRVO_FBOUT (Pin 38): Open-Drain Logic Output. This pin is pulled to ground when the output voltage feedback loop is active. This pin is unused for most LT8491 applications and can be floated.

$EXTV_{CC}$ (Pin 40): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.22V (typical), $INTV_{CC}$ will be powered from V_{IN}. See HW Config: MODE Pin - Current Conduction Mode for additional details.

CSNOUT (Pin 41): The (–) Input to the Output Current Sense Amplifier.

CSPOUT (Pin 42): The (+) Input to the Output Current Sense Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor to provide the output current signals.

CSNIN (Pin 44): The (–) Input to the Input Current Sense Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor to provide the instantaneous input current signals.

CSPIN (Pin 45): The (+) Input to the Input Current Sense Amplifier.

V_{IN} (Pin 46): Main Input Supply Pin. Must be bypassed to local ground plane.

ECON (Pin 48): Digital Output Pin. Optional control output signal used to disconnect $EXTV_{CC}$ from the battery when the average charge current drops below a predetermined threshold.

SWENO (Pin 49): Digital Output Pin. Connect to SWEN. Enables the switching regulator. A 200k pull-down resistor is required from this pin to ground.

IOW (Pin 50): Digital Output Pin. Connects to IMON_OUT through a resistor. By switching the pin between logic low and high impedance, the total R_{IMON_OUT} changes, which changes the output current limit.

STATUS (Pin 51): Digital Output Pin. When used with an LED, this signal provides a visual indication of the progress of the charging algorithm.

PIN FUNCTIONS

NC (Pins 52, 60): Not connected.

IIR (Pin 53): A/D Input Pin. Connects to IMON_IN to read input current. Used to manage MPPT and for telemetry.

VINR (Pin 54): A/D Input Pin. Connects to resistive divider on V_{IN} to measure input voltage. Used for telemetry and to manage MPPT and startup.

CLKDET (Pin 56): A/D Input Pin. Connects to CLKOUT through an RC filter to detect the duty cycle of CLKOUT. Used to manage startup.

FBOR (Pin 57): A/D Input Pin. Connects to FBOUT pin to read charger output voltage. Used to manage the charging algorithm.

AV_{DD} (Pin 58): A/D Positive Reference Pin. Tie this pin to V_{DD} and LDO33.

SDA (Pin 61): I^2C Bidirectional Data Pin.

SCL (Pin 63): I^2C Clock Input Pin (100kHz Maximum).

IOR (Pin 64): A/D Input Pin. Connects to IMON_OUT pin to read the charger output current. Used for telemetry and to manage the charging algorithm.

GND (Pins 55, 59, 62, Exposed Pad 65): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM

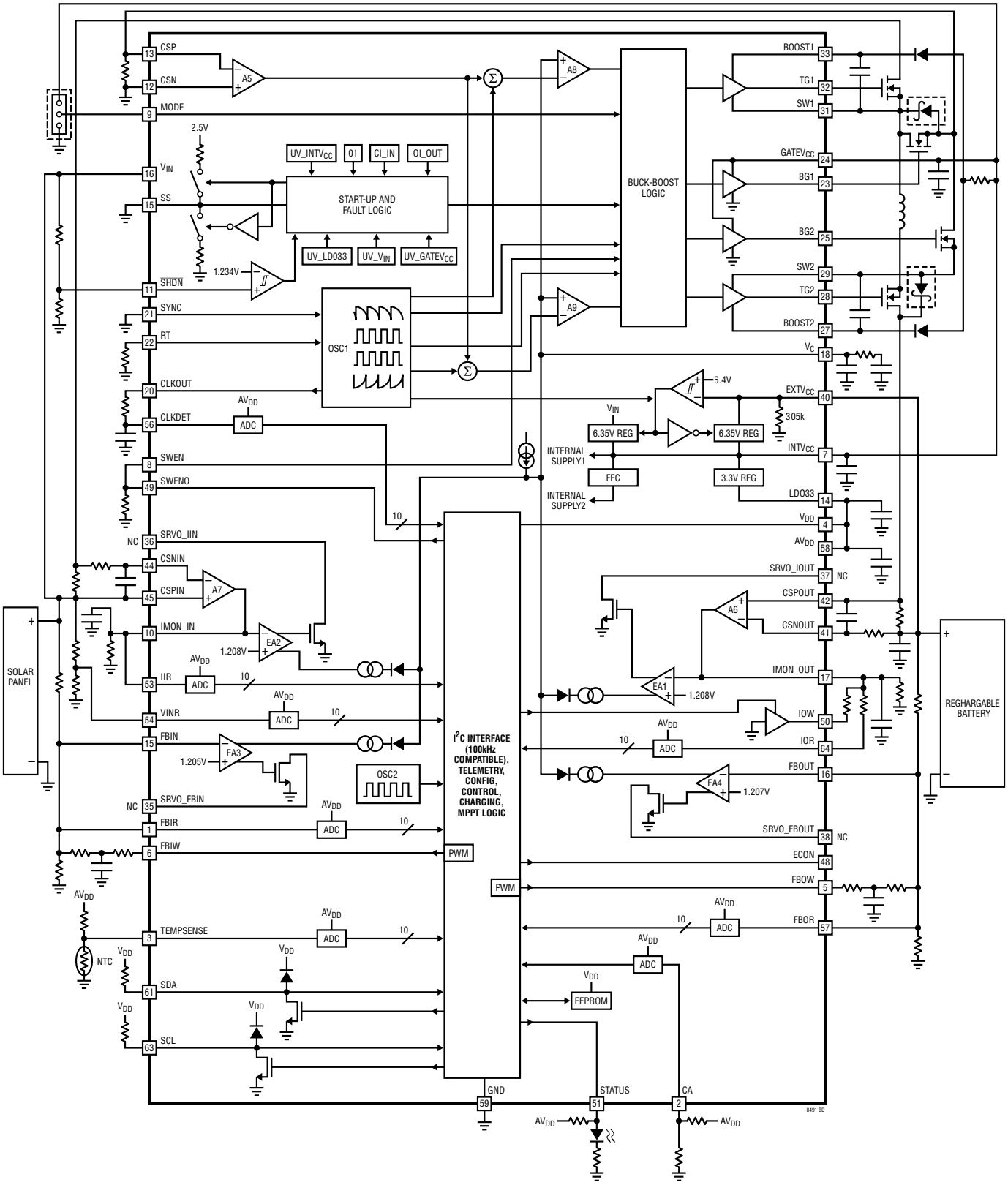


Figure 1. Block Diagram

OPERATION

OVERVIEW

The LT8491 is a powerful and easy to use battery charging controller with automatic maximum power point tracking (MPPT), temperature compensation and an I²C interface for telemetry, status, control and configuration. The LT8491 is based on the LT8705 buck-boost controller with additional battery charging and MPPT control functions. Refer to the LT8705 data sheet for more detailed information about the switching regulator portions of the LT8491.

Several reference applications are included in this data sheet to simplify system design. Many battery-charging applications can be implemented using one of the reference applications with little or no modification required. Various charging parameters can be configured via the digital I²C interface and can be made permanent in the on-chip EEPROM. Since the battery charging and MPPT are controlled by the LT8491, no firmware development is required. Interfacing to the I²C pins is only required to configure and/or monitor the charger. For reference, factory default I²C configuration settings are listed in the I²C Register Map section.

The LT8491 includes four different forms of regulation: output current, input current, input voltage and output voltage (EA1 - EA4 respectively as shown in Figure 1). The commanded inductor current is limited by whichever form of regulation requires the lowest voltage on the V_C pin. When powered by a solar panel, the MPPT function uses input voltage regulation to locate and track the maximum power point of the solar panel. Input current regulation is used to limit the maximum current drawn from the input supply to safe levels. The output current regulation sets the maximum battery charging current, and the output voltage regulation is used to set the maximum battery charging voltage.

The LT8491 offers user configurable charge timers. If a timer has been set and subsequently expires, the LT8491 will halt charging and communicate this through the I²C interface and the STATUS pin. Options for automatic restart of the charging cycle are discussed later in the Configure Automatic Restart section.

The LT8491 also includes a TEMPSENSE pin, which can be connected to an NTC resistor divider network thermally coupled to the battery pack. The TEMPSENSE pin can facilitate several functions including temperature compensated charging, battery temperature telemetry, and charging disable when the battery is outside of safe temperature limits. Detection of the NTC resistor can also give an indication to the charger if the battery is connected or not.

The LT8491 also provides charging telemetry and status through the I²C interface and the STATUS pin. Refer to the Telemetry Registers and Status Registers sections for the I²C indicators. The behavior of the STATUS pin is described in the STATUS Indicator Pin section.

I²C SERIAL INTERFACE

The LT8491 includes a slave I²C compatible interface facilitating digital control of the charger settings and digital readouts of telemetry and status. The following subsections explain how to read and write data to the LT8491. The I²C Register Map and I²C Register Descriptions sections provide detailed descriptions of all the I²C registers and their functions.

I²C: START and STOP Conditions

When the bus is idle, both SCL and SDA are high. A bus master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high, as shown in Figure 2. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

I²C: ACKnowledge

The acknowledge signal (ACK) is used in handshaking between the transmitter and receiver to indicate that the most recent byte of data was received. When the slave is the receiver, it pulls down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge, by leaving SDA high, then the master may abort the transmission by generating a STOP condition. When the master is receiving data

OPERATION

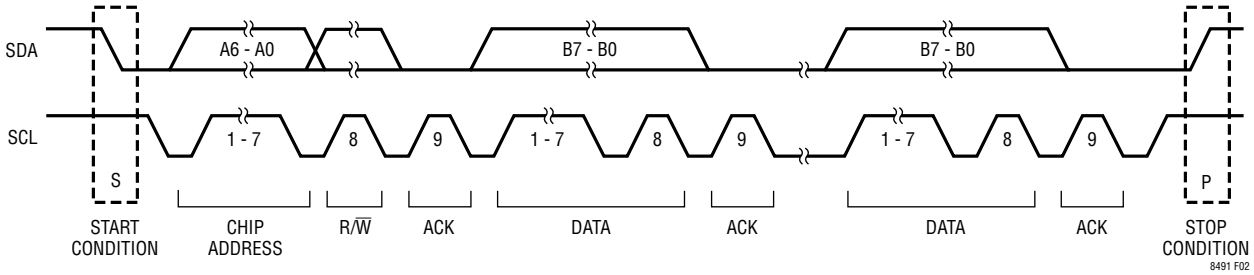


Figure 2. Data Transfer Over I²C Bus

from the slave, the master pulls down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master leaves the SDA line HIGH (NACK) and issues a STOP (P) condition to terminate the transmission.

I²C: Chip Addressing

The CA pin is used to select one of four 7-bit chip addresses (A6:A0). This address is sent by the master to identify which IC it is transferring data with. The CA pin can be tied to ground, AV_{DD} or connected to a resistor divider to select the desired chip address. See the HW Config: I²C Chip Address section for more detailed information.

I²C: Clock Stretching

The charger supports clock speeds up to 100kHz for the I²C interface. The master is required to support I²C clock stretching to properly communicate with this charger (slave).

I²C: Data Transfer Transactions

The LT8491 supports byte-writes, byte-reads, and word-reads using the transaction formats shown in Figure 3 to Figure 5 respectively. Figure 3 shows the required format for writing a byte of data to the LT8491. Again, the required chip address (A6:A0) depends on the CA pin.

A single byte of data is read from the LT8491 using the byte-read transaction shown in Figure 4. The register address selects the data byte that is returned. This transaction requires four I²C bytes to read one byte of chip data.

The word-read transaction, shown in Figure 5, should be used to read telemetry such as power, volts and amps that is stored in 16-bit formats. The word-read transaction ensures that both bytes of data are properly paired together and can be combined into a valid word. Due to the time latency between I²C transactions, combining bytes from two byte-read transactions may not result in valid 16-bit telemetry data.

Referring again to Figure 5, the register address selects the first byte of data (DATA0) that is returned. Data from the next higher byte address is returned in the second byte (DATA1). When reading Word or Long Word data, note that the least significant byte is at the lowest address location (little-endian). B0 of the register address should typically be set to 0 since all words in the LT8491 are aligned to even register addresses. This transaction requires five I²C bytes to read two bytes of chip data and must be repeated for each subsequent word of data that is read.

I²C: Powering the Interface

The I²C control logic and I/O are powered from the V_{DD} pin. V_{DD} is ultimately supplied from either V_{IN} or $EXTV_{CC}$ when the $\overline{SHDN}$ pin is high. This can be seen in the block diagram which shows that V_{IN} and $EXTV_{CC}$ supply the $INTV_{CC}$ regulator that, in turn, supplies the LDO33 regulator which is finally connected to V_{DD}. After $\overline{SHDN}$ and V_{DD} rise, I²C communication is enabled after a delay of 10ms (typical). Note that the LT8491 contains diodes from the SDA and SCL pins to the V_{DD} pin (see Figure 8). These diodes are normally reverse biased and have no effect on the I²C bus. However, when the LT8491 is unpowered, the V_{DD} pin voltage will drop and may pull down on the SDA and SCL pins, thus effecting communication on the bus.

OPERATION

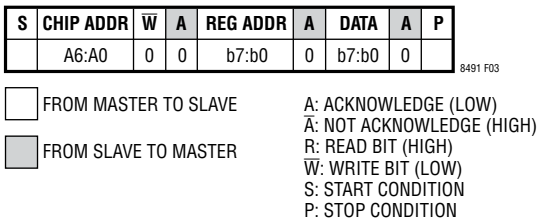


Figure 3. I²C Byte-Write Transaction

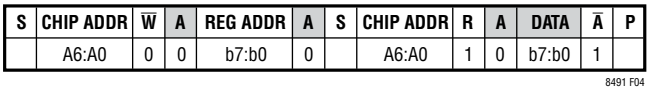


Figure 4. I²C Byte-Read Transaction

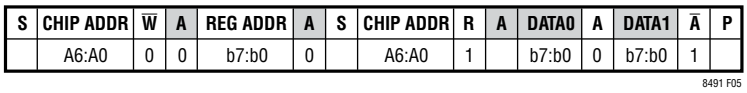


Figure 5. I²C Word-Read Transaction

I²C DATA

Data: Memory Regions

Data in the LT8491 is arranged into six regions as shown in Table 1.

Table 1. LT8491 I²C Addressable Memory Regions

REGION	TYPE	I²C REG ADDR RANGE	DESCRIPTION
Telemetry	Registers	0x00-0x11	Charging telemetry.
Status	Registers	0x12-0x1F	Charging and system status.
Control	Registers	0x20-0x27	Control charging on/off and EEPROM access.
Configuration	Registers	0x28-0x5B	Charger configuration settings.
Manufacturer	Registers	0x5C-0x61	Manufacturer Data.
Boot	EEPROM	0x88-0xBD	Non-volatile storage of start-up configuration.

Telemetry Region: These read-only registers indicate telemetry such as temperature, voltage, current, power and efficiency. These word-sized values must be read using the I²C word-read transaction to avoid retrieving mismatched bytes (see I²C: Data Transfer Transactions). See the Telemetry Operation and Telemetry Registers sections for further telemetry information.

Status Region: These read-only registers indicate status such as charging state, solar panel state, faults, timers and others. Detailed status register descriptions are provided in the Status Registers section.

Control Region: These read-write registers are used to start and stop the charger, write to the EEPROM, reset the chip and other related functions. The contents of these registers revert to their default values, as listed in the I²C Register Map, after power is cycled or the CTRL_RESTART_CHIP register is written to 0x99. Detailed control register descriptions are provided in the I²C Register Descriptions section.

Configuration Region: These read-write registers determine the charger settings such as timer limits, restart options, V_{BAT} stage voltages, and many others. After power-up or reset, the configuration registers are automatically loaded with data from the EEPROM (see the Startup Sequence section). Factory default EEPROM values are provided in the I²C Register Map. Detailed configuration register descriptions are provided in the I²C Register Descriptions section.

Manufacturer Region: These read-only registers indicate manufacturer data that is determined at the factory.

OPERATION

Boot Region: The boot data is stored in non-volatile EEPROM and is copied into the configuration registers during startup or after the CTRL_RESTART_CHIP register is written to 0x99, as described in the Startup Sequence section.

Each EEPROM location in the boot region corresponds to a register in the configuration region. As such, the boot region data is arranged in the exact same order and format as in the configuration region but is read from an I^2C address 0x60 higher than the corresponding configuration register address. Reading of the boot data is described in the EEPROM: Reading section.

Writing directly to the EEPROM is prohibited. Instead, data can be copied from the configuration registers into the EEPROM by writing to appropriate control registers. Further information about writing the EEPROM is in the EEPROM: Writing section.

Data: Bytes, Words and Long Words

LT8491 data is stored in three sizes: bytes, words (2 bytes) and long words (4 bytes). Tables are provided throughout this data sheet indicating the sizes for each piece of data. Since the I^2C bus addresses one byte at a time, word and long word data is spread across multiple I^2C register address locations.

Words and long words are stored in an arrangement commonly referred to as little endian. The least significant byte (LSB) is stored at the lower I^2C register address location. The next most significant byte (MSB) is stored at the next higher I^2C register address and so on.

As an example, suppose the TELE_IOUT register is indicating output current of 5.274 Amps (see Telemetry Registers). This 16-bit register, starting at I^2C address 0x08 will contain the value 0x149A. The two bytes comprising TELE_IOUT are stored as shown:

Table 2. Example of TELE_IOUT Word Storage

I^2C REG ADDRESS	BYTE VALUE
0x08	0x9A
0x09	0x14

Reading TELE_IOUT with the word-read transaction from register address 0x08 returns two bytes, DATA0 (0x9A) and then DATA1 (0x14) indicating 5.274 Amps.

The temperature compensation coefficients, in the configuration region, are the only data stored as long words. For example, suppose CFG_TC1 has the value 1.54e-3 stored as the 32-bit floating point value 0xBAC9D9D3. This data is stored as follows in Table 3:

Table 3. Example of CFG_TC1 Long Word Storage

I^2C REG ADDRESS	BYTE VALUE
0x56	0xD3
0x57	0xD9
0x58	0xC9
0x59	0xBA

Reading the entire long word requires four byte-read transactions, or two word-read transactions. Writing the entire long word requires four byte-write transactions at addresses 0x56 through 0x59.

Data: Min/Max Register Values

Some configuration registers have minimum and maximum acceptable values (i.e. CFG_VS3_25C). The value limits for each register (if any) are listed in the I^2C Register Descriptions section. If a configuration register is written to a value outside of the min/max limits, the LT8491 will automatically modify the register contents to the factory default register value.

Data: Access Permissions

I^2C read and/or write access to various regions is conditional. Table 4 and Table 5 illustrate the conditions required to access the various regions. When writing to a register, while write access permission is denied, the data is ignored and not written to the addressed location. When reading from a location while read access permission is denied, the returned data is all zeros.

As shown in Table 4 and Table 5, most address locations can be read unconditionally after startup is complete. However, the boot region is also unreadable while EEPROM writing is ongoing and will return 0x00 during that time.

OPERATION

Table 4. Register Access Permissions (Except Control Region)

MEMORY REGION	REGISTER NAME	I²C REG ADDRESS RANGE	READ ACCESS	WRITE ACCESS
Telemetry	All	0x00-0x11	Always[1]	Never
Status	All	0x12-0x1F	Always[1]	Never
Configuration	All	0x28-0x5B	Always[1]	Only when CHRG_LOGIC_ON=0[3] and CTRL_EE_WRT_EN≠0xCC and SYSTEM_BUSY=b00[3].
Manufacturer	All	0x5D-0x61	Always[1]	Never
Boot	All	0x88-0xBD	Always[1, 2]	Never See EEPROM: Writing section.

1. Except when chip is powered down or the I²C interface has not been activated yet during the startup sequence.
2. Except when EEPROM write operation is occurring. This is indicated by a read of 10b from STAT_SYSTEM→SYSTEM_BUSY, or a read of 1 from CTRL_WRT_TO_BOOT→RDY_BUSY.
3. CHRG_LOGIC_ON is a read-only bit in the STAT_CHARGER register. It is cleared shortly after CTRL_CHRG_EN is written 0x00. SYSTEM_BUSY are read-only bits in the STAT_SYSTEM register.

Table 5. Control Region Access Permissions

REGISTER NAME	I²C REG ADDR	READ ACCESS	WRITE REQUIRES…			
			CHRG_LOGIC_ON[3] = 0	CTRL_EE_WRT_EN ≠ 0xCC	CTRL_EE_WRT_EN = 0xCC	SYSTEM_BUSY[3] = 00b
CTRL_WRT_TO_BOOT	0x20	Always[1]	✓		✓	✓
CTRL_EE_WRT_EN	0x21		✓			✓
CTRL_HALT_STARTUP	0x22					
CTRL_CHRG_EN	0x23		✓[4]	✓		✓
CTRL_RESTART_CHIP	0x24		✓			✓
CTRL_RESET_FLAG	0x25					✓
CTRL_UPDATE_TELEM	0x26		✓	✓		✓
Reserved	0x27		Writes to this reserved register always ignored.			

4. Only required when writing 1 to CHRG_EN bit.

All I²C byte-write registers have conditions under which the data is accepted. These conditions prevent changes to the charger configuration while the charging is ongoing and to help prevent inadvertent changes to the configuration and/or EEPROM.

STARTUP SEQUENCE

Figure 6 illustrates the startup sequence for the LT8491. Not all details are shown. The sequence is initiated when the V_{DD} pin rises above 2.7V (typical). If the device is already powered on and CTRL_CHRG_EN=0, the startup sequence can be re-initiated by writing CTRL_RESTART_CHIP to 0x99.

At the beginning of the startup sequence the I²C interface is disabled and the default values for the telemetry, status and control registers are set as indicated in the I²C Register Map section.

Next, a CRC check of the EEPROM boot region and factory settings is performed. If the boot region fails the CRC check, the LT8491 recalculates the CRC indefinitely until the CRC check passes, or the process is interrupted by writing CTRL_HALT_STARTUP to 0x5A. If startup is halted then the configuration registers revert to their factory default values, as listed in the I²C Register Map, before completing startup. If the factory settings fail the CRC check, the LT8491 recalculates the CRC indefinitely

OPERATION

until the CRC check passes. More information about the CRC checking is discussed in the CRC Operation section.

When the boot CRC and the factory CRC check passes, the STAT_SYSTEM→BOOT_SUCCESS bit is set to 1. Subsequently, CTRL_CHRG_EN is preset with the value read from BOOT_MISC in the EEPROM. This determines if the charging starts automatically, at the end of the sequence, or not.

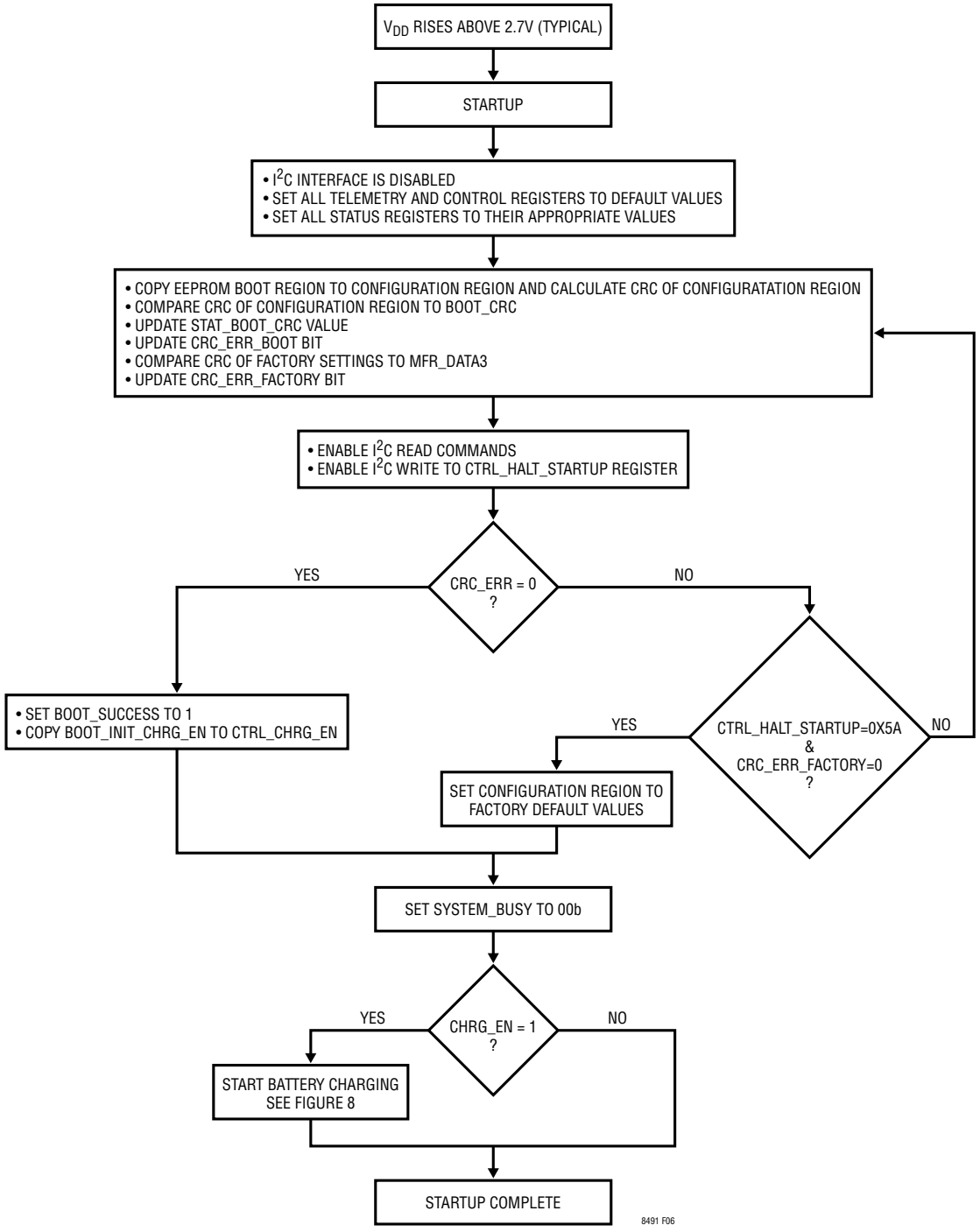


Figure 6. Startup Sequence

OPERATION

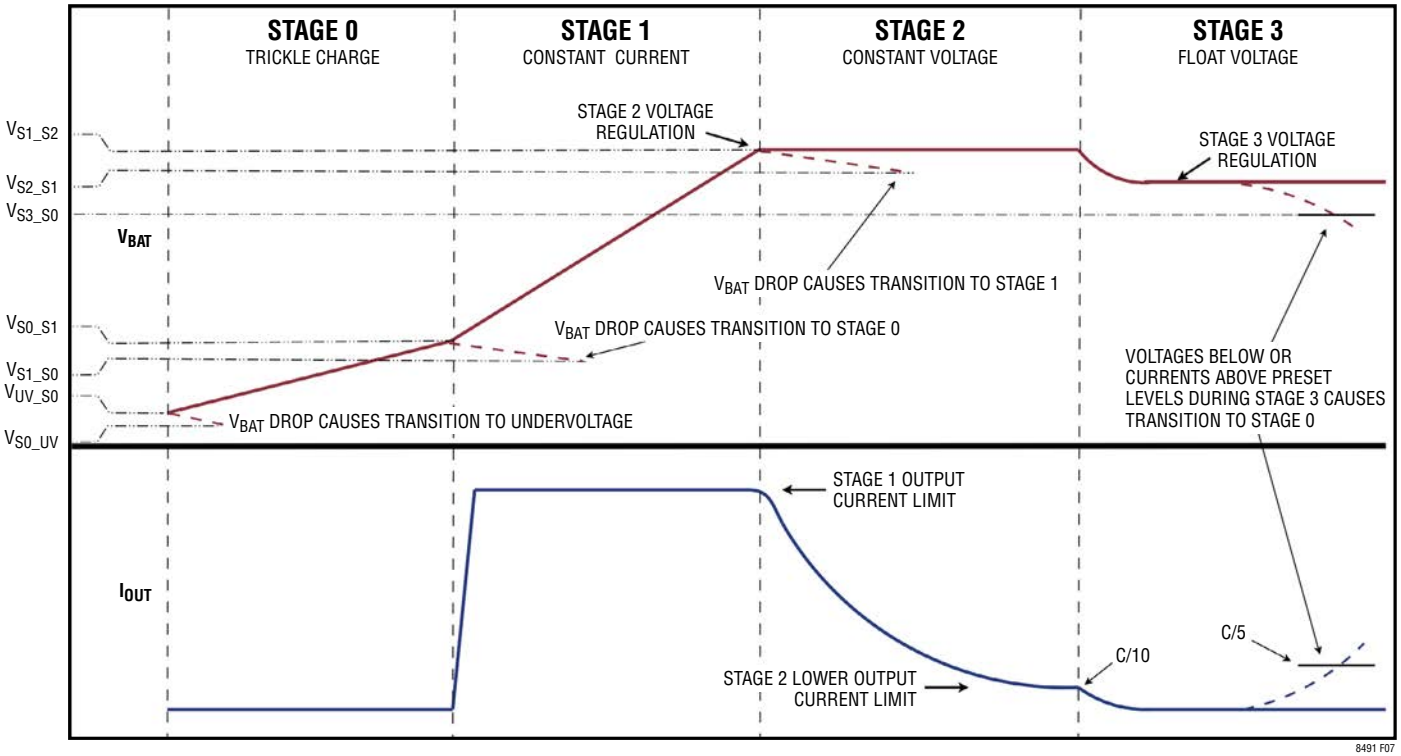


Figure 7. Typical Battery Charging Cycle

BATTERY CHARGING ALGORITHM

The LT8491 implements a CCCV charging algorithm. The idealized charging profile is shown in Figure 7 and assumes constant temperature and adequate input power. As battery temperature and illumination conditions on the panel change, the actual current and voltage seen by the battery will vary accordingly.

Figure 8 illustrates a flow chart for the charging algorithm. Many options are available to configure the algorithm as needed. Options include…

- Stage 3 is enabled or not
- Stop charging when I_{OUT} < C/10 or not
- Timer expiration indicates a fault or not
- Various automatic restart options

Footnotes at the bottom of Figure 8 indicate configurable aspects of the algorithm and the related thresholds.

Stage 0: Trickle Charging

In Stage 0 the LT8491 charges the battery with a reduced constant current that is hardware configurable (see HW Config: Output Current Sense and Limit section). This stage typically occurs for battery voltages between 35% to 70% of the Stage 2 battery voltage limit (V_{S2}). However, the Stage 0 battery thresholds are I^2C configurable as discussed in the Configure V_{BAT} for Stages 0, 1 and 3 section. Stage 0 charging is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 000b and the CHRG_LOGIC_ON bit is 1.

Stage 1: Full Constant Current

At higher battery voltage, the LT8491 enters Stage 1 and charges the battery with full constant current (see HW Config: Output Current Sense and Limit section). Stage 1 typically occurs for battery voltages between 70% to 98% of the Stage 2 battery voltage limit. The threshold for entering Stage 1 is I^2C configurable as discussed in the

OPERATION

Configure V_{BAT} for Stages 0, 1 and 3 section. Stage 1 is often referred to as bulk charging in the battery charging community. However, this stage will continue to be called Stage 1 for the remainder of this document. Stage 1 charging is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 001b and the CHRG_LOGIC_ON bit is 1.

Stage 2: Constant Voltage

In Stage 2, the LT8491 charges the battery to a constant voltage (V_{S2}). This constant voltage stage is indicated for battery voltages above 98% (typical) of the Stage 2 voltage. Stage 2 is often referred to as float charging for lithium-ion batteries and absorption charging for lead-acid batteries. To avoid confusion, this stage is referred to as Stage 2 for the remainder of this document. Stage 2 charging is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 010b and the CHRG_LOGIC_ON bit is 1.

Charging in Stage 2 typically continues until the output current (I_{OUT}) falls below C/10. Options are available to configure how the charger proceeds from Stage 2. These options include:

- Terminate charging when I_{OUT} < C/10
- Terminate when the Stage 2 timer expires
- Proceed to Stage 3 when I_{OUT} < C/10
- Continue charging in Stage 2 indefinitely

Footnotes in Figure 8 indicate the respective I^2C configuration registers for these options.

Stage 3: (Optional) Reduced Constant Voltage

Stage 3 is optionally enabled in the CFG_CHRG_MISC register. In Stage 3 the LT8491 charges the battery with a reduced constant voltage. Stage 3 is often referred to as float charging for lead-acid batteries. It will continue to be called Stage 3 for the remainder of this document. Stage 3 charging is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 011b and the CHRG_LOGIC_ON bit is 1.

Done Charging

When done charging, the power stage is disabled, and charging is complete. This is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 100b and the CHRG_LOGIC_ON bit is 1. Telemetry acquisition generally continues although some telemetry, related to the battery side of the charger, may be limited as discussed in the Telemetry: Acquisition section. In addition, although some telemetry continues to be acquired, no charging faults will be reported. Restarting the charging, when done charging, can be done in four ways:

- The charging can be restarted by toggling the control charger enable bit low to high. See the CTRL_CHRG_EN register description.
- The charger can be configured to restart automatically under various conditions. See the Configure Automatic Restart section.
- The charger can be reset by cycling the power.
- Issuing a restart chip command while CTRL_CHRG_EN is cleared, will also restart the charger if CFG_INIT_CHRG_EN is set. See the CTRL_RESTART_CHIP register description.

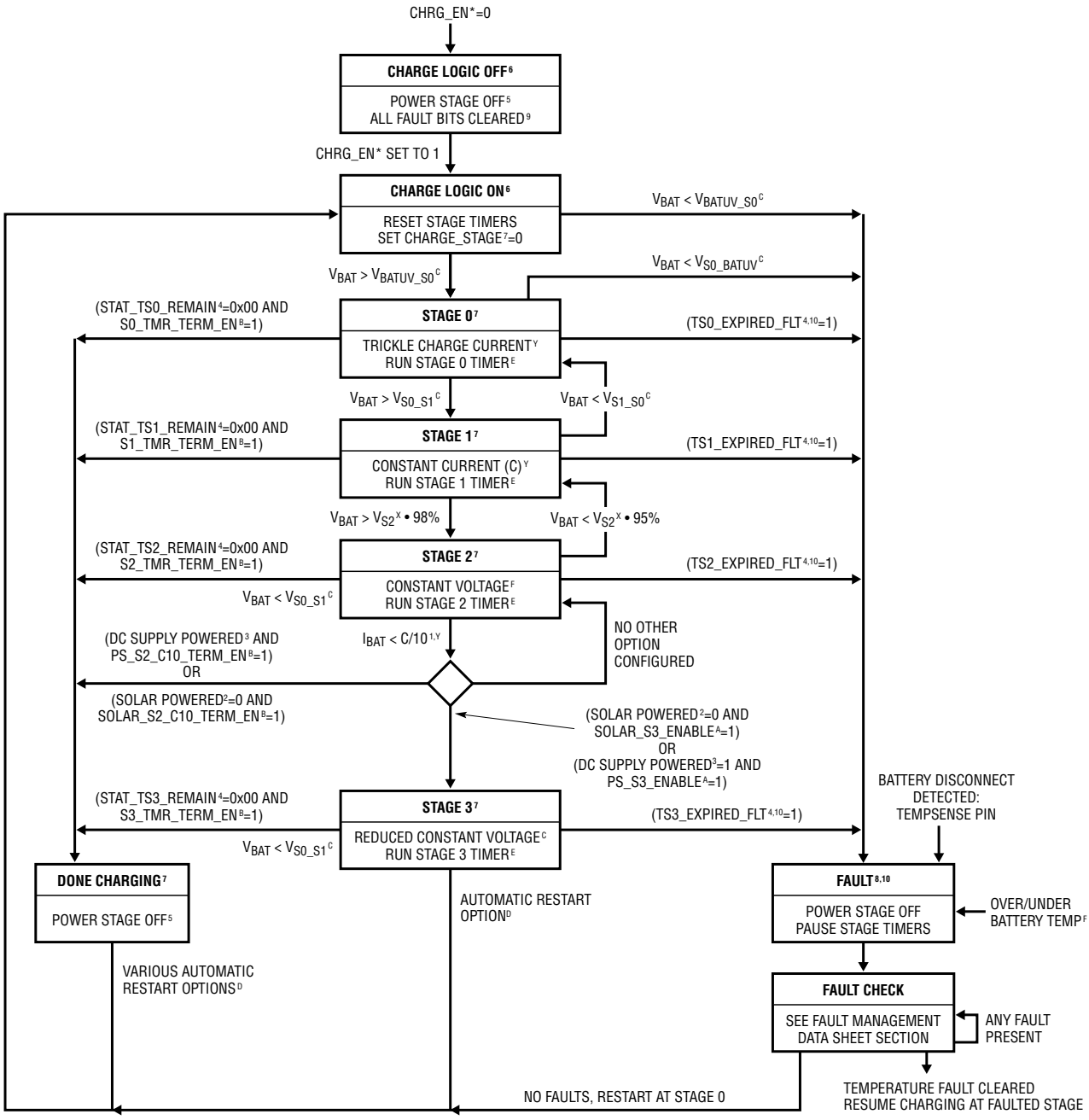
Charging Faults

The LT8491 periodically monitors for the following fault conditions, on a priority basis, while the charging logic is on (STAT_CHARGER→CHRG_LOGIC_ON=1) and the charger isn't in an input UVLO condition (STAT_SUPPLY→VIN_UVLO=0):

- V_{BAT} too low for charging
- Battery temperature too low for charging
- Battery temperature too high for charging
- Battery disconnected
- Stage timer expired and configured to be a fault, indicating that charging took too much time

These faults are reported in the STAT_CHRG_FAULTS register. Detailed information about each fault bit and its' source is provided in the register's data sheet section.

OPERATION



I²C CONFIGURATION

A: SEE CONFIGURE MISC.
B: SEE CONFIGURE TERMINATION
C: SEE CONFIGURE V_{BAT} FOR STAGES 0, 1, AND 3
D: SEE CONFIGURE AUTOMATIC RESTART
E: SEE CONFIGURE STAGE TIMEOUT LIMITS
F: SEE CONFIGURE TEMPERATURE FAULT LIMITS

I²C CONTROL

*: I²C CONTROL BIT SETTING

HARDWARE CONFIGURABLE

X: SEE HW CONFIG: V_{BAT} IN STAGE 2 (V_{S2})
Y: (C) AND THE TRICKLE CURRENT ARE HW CONFIGURABLE: SEE HW CONFIG: OUTPUT CURRENT SENSE AND LIMIT

INDICATED IN I²C STATUS REGISTERS

1: GT_C10=0 STAT_CHARGER
2: PS_OR_SOLAR=0 IN STAT_SUPPLY
3: PS_OR_SOLAR=1 IN STAT_SUPPLY
4: TIMERS DON'T OPERATE WHEN SOLAR POWERED
5: SWEN0=0 IN STAT_SYSTEM
6: CHARG_LOGIC_ON BIT IN STAT_CHARGER
7: CHARG_STAGE BITS IN STAT_CHARGER
8: CHARG_FLT=1 IN STAT_CHARGER
9: STAT_CHRG_FAULTS REGISTER
10: STAT_TSx_REMAIN REGISTERS

NOTE: IF V_{BAT} FALLS BELOW THE V_{S1_S0} THRESHOLD WHILE IN STAGE 2 OR STAGE 3, THE CHARGING ALGORITHM WILL RESET.

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Figure 8. LT8491 Charging Algorithm

OPERATION

Any active fault causes the charging to stop, the stage timers to pause their countdown, and the status to be reported as follows:

- STAT_CHARGER→CHRG_FAULT=1, indicating the presence of a fault.
- STAT_CHARGER→CHRG_STAGE holds its last value.
- STAT_CHRG_FAULTS indicates the source of the fault.
- STAT_SUPPLY→SOLAR_STATE=000b.
- STATUS pin indication. See Table 25.

After a fault is detected, the LT8491 typically continues to monitor for the presence of faults and, when no faults are present, the charging resumes or restarts. However, this behavior depends on the CFG_RSTRT_IN_FLT register settings discussed in the Configure Automatic Restart section and below. Telemetry acquisition generally continues during a fault although some telemetry, related to the battery side of the charger, may be limited as discussed in the Telemetry: Acquisition section.

Faults are monitored on a priority basis as follows:

- *Battery Disconnect Fault:* (BAT_DISCON_FLT=1) The presence of a battery disconnect fault, as measured at the TEMPSENSE pin, inhibits checking for all faults except this one. As such, the low V_{BAT} and V_{BAT} temperature faults are cleared. If CFG_RSTRT_IN_FLT→NO_RSTRT_ON_DISCON_FLT=1 then the detection of this fault stops the LT8491 from checking the status of all faults and the charging won't restart until it's reset or cycled off-then-on via the CHRG_EN control bit.
- *TBAT Battery Temperature Fault:* (LOW_TBAT_FLT or HIGH_TBAT_FLT=1) During a T_{BAT} fault the LOW_VBAT_FLT bit is not updated. If CFG_RSTRT_IN_FLT→NO_RESUME_ON_TBAT_FLT=1 then the charging won't resume until the charger is reset or cycled off-then-on via the CHRG_EN control bit.
- *Stage Timer Expired Fault:* (TSx_EXPIRED_FLT=1) During a stage timer fault, if CFG_RSTRT_IN_FLT→NO_RSTRT_ON_VOLTS=0 and there is no battery disconnect or T_{BAT} fault, the LT8491 measures V_{BAT} every 5 seconds to check if an automatic restart can be initiated. The TELE_VBAT register and the LOW_VBAT_FLT bit are updated with each new V_{BAT} measurement.

  During a stage timer fault, if CFG_RSTRT_IN_FLT→NO_RSTRT_ON_VOLTS=1, then the charging will not restart until the charger (1) is reset or (2) is cycled off-then-on via the CHRG_EN control bit, or (3) automatically restarts due to the CFG_RSTRT_IN_FLT→RSTRT_ON_TMR_FLT_HRS settings. In addition, the LOW_VBAT_FLT bit is not updated until the charging restarts.
- *V_{BAT} Low Fault:* (LOW_VBAT_FLT=1) When LOW_VBAT_FLT is the only fault present, V_{BAT} is measured once per second to check for higher voltage to restart the charger. However, if CFG_RSTRT_IN_FLT→ NO_RSTRT_ON_BATLOW_FLT=1 then the charging and V_{BAT} measurements stop until the charger is reset or cycled off-then-on via the CHRG_EN control bit.

MAXIMUM POWER POINT TRACKING

When powered by a solar panel, the LT8491 employs a proprietary Perturb and Observe algorithm for identifying the maximum power point. This algorithm provides accurate MPPT for slow to moderate changes in panel illumination. The panel is also fully scanned periodically to avoid settling on a false maximum power point for long periods of time, in the case of non-uniform panel illumination. The frequency of performing full panel scans can be configured in the CFG_SCAN_RATE and CFG_SCAN_RATE_LP registers.

TELEMETRY OPERATION

The LT8491 generates digital telemetry including battery temperature, input and output current, input and output voltage, power and efficiency. The latest measurement results are stored in the read-only telemetry registers summarized in the I^2C Register Map and in Table 9. These word-sized values must be read using the I^2C word-read transaction to avoid retrieving mismatched bytes (see I^2C: Data Transfer Transactions)

OPERATION

Telemetry: Configuration Settings

All of the telemetry measurements, except for TELE_TBAT and TELE_VINR, first require that valid PCB resistor values are written to the appropriate configuration registers as discussed in the Configure the Telemetry section. These registers are not configured at the factory.

Telemetry: Acquisition

Updated telemetry measurements occur at various rates, depending on the operating conditions of the LT8491. Refer to Table 6 which summarizes when telemetry is acquired.

The LT8491 periodically updates the telemetry measurements while the charging logic is enabled. The STAT_CHARGER→TELEM_ACTIVE bit indicates that the telemetry registers are being periodically updated, and all possible telemetry has been updated at least once, since CTRL_CHRG_EN→CHRG_EN was most recently set from 0 to 1.

When the charging logic is disabled, telemetry stops updating and most of the telemetry registers retain their last reported values. While the charging logic is disabled, writing 0xAA to the CTRL_UPDATE_TELEM register will force some measurement updates to occur.

While the charging logic is enabled, but a fault is present, or the done charging stage has been reached (see Battery Charging Algorithm), the LT8491 has limited ability to measure telemetry. This is because the output feedback divider is (optionally) disconnected and the output current sense amplifier is disabled to reduce discharge current from the battery. As such, telemetry acquisition in these stages is limited as shown in Table 6.

CRC OPERATION

The LT8491 performs CRC calculations during startup and when writing the EEPROM. The CRCs validate the integrity of the user configuration information and prevent self-starting with invalid data. For reference, Table 7 provides a summary of the I^2C registers that are related to CRC operations.

During startup, the LT8491 calculates the CRC for the boot region and the factory settings. It compares the calculated results to the expected values found in the respective EEPROM locations. The calculated and expected values must match before the startup sequence can continue. See the Startup Sequence section for more information. The BOOT_CRC and the MFR_DATA3 value are preset at the factory. The BOOT_CRC automatically updates to the correct value whenever the EEPROM is modified. See the EEPROM: Writing section for further details.

The BOOT_CRC is calculated from the 52 bytes of data located in addresses 0x28-0x5B (configuration registers) or the corresponding 52 bytes located in the EEPROM. The CRC-16-ANSI polynomial ($x^{16} + x^{15} + x^2 + 1$) is used for the calculations.

Table 6. Telemetry Acquisition

<table>
<tr><th rowspan="2">TELEMETRY REGISTER</th><th colspan="3">CHARGER ENABLED (STAT_CHARGER→TELEM_ACTIVE = 1)</th><th rowspan="2">CHARGER DISABLED (STAT_CHARGER→TELEM_ACTIVE = 0)</th></tr>
<tr><th>ALL OTHER STAGES</th><th>DONE CHARGING STAGE</th><th>FAULT</th></tr>
<tr><td>TELE_VBAT</td><td rowspan="8">Periodic telemetry updates occur for these nine registers.</td><td colspan="2">Telemetry update occurs every second except during a battery disconnect fault.</td><td rowspan="6">These six registers hold their last values. Telemetry values are only updated when CTRL_UPDATE_TELEM is written to 0xAA.</td></tr>
<tr><td>TELE_VIN</td><td colspan="2" rowspan="5">Periodic telemetry updates occur for these five registers.</td></tr>
<tr><td>TELE_VINR</td></tr>
<tr><td>TELE_IIN</td></tr>
<tr><td>TELE_PIN</td></tr>
<tr><td>TELE_TBAT</td></tr>
<tr><td>TELE_IOUT</td><td colspan="2" rowspan="3">No updates occur for these three registers. Reads return last measured value.</td><td rowspan="3">Reads return last measured value. Telemetry values update to initial value when CTRL_UPDATE_TELEM is written to 0xAA</td></tr>
<tr><td>TELE_POUT</td></tr>
<tr><td>TELE_EFF</td></tr>
</table>

OPERATION

Table 7. Summary of CRC-Related Registers

MEMORY REGION	REGISTER NAME	I²C REG ADDRESS	DESCRIPTION OF CRC OPERATION	REF PAGE
Status	STAT_SYSTEM	0x13	Indicates startup CRC calculation errors and startup CRC calculation status.	35
	STAT_BOOT_CRC	0x1C	Result of most recent CRC, calculated by the LT8491, from the boot region.	38
	STAT_CFG_CRC	0x1E	Result of most recent CRC, calculated by the LT8491, from the configuration region.	38
Control	CTRL_WRT_TO_BOOT	0x20	Initiates writing to EEPROM and re-calculation of the STAT_BOOT_CRC and STAT_CFG_CRC values.	39
	CTRL_HALT_STARTUP	0x22	Halts startup CRC calculations and checking if CRC checks are failing.	40
Boot	BOOT_CRC	0xBC	Expected CRC result for boot region.	-

EEPROM OPERATION

The on-chip non-volatile EEPROM stores data when the power is removed. During startup, this data is copied from the EEPROM boot region into the configuration registers as discussed in the Startup Sequence section. For reference, Table 8 provides a list of the LT8491 I²C registers that are related to EEPROM operation.

EEPROM: Startup

The initial configuration of the LT8491 is copied from the EEPROM during startup or chip reset. See the Startup Sequence section for more information.

EEPROM: Reading

The EEPROM boot region is read from I²C register addresses 0x88 - 0xBD. See the I²C Register Map for data descriptions. Note that attempts to read the EEPROM during an EEPROM write operation will return zeros.

EEPROM: Writing

Writing directly to the EEPROM is not supported through the I²C interface. Instead, the LT8491 can be instructed to either (1) copy the configuration registers to the EEPROM boot region or (2) restore the boot region to the factory default values. To prevent inadvertent writing of the EEPROM, or unintended charger operation, the EEPROM can only be modified when all of the following conditions are met:

- STAT_CHARGER→CHRG_LOGIC_ON=0 indicating that the charging logic is turned off.
- STAT_SYSTEM→SYSTEM_BUSY=00b indicating that the system is not busy with other operations.
- CTRL_EE_WRT_EN=0xCC to enable EEPROM write capability.

When the conditions are met, an EEPROM write operation is initiated by writing an appropriate byte to the CTRL_WRT_TO_BOOT register. After the register is written, the EEPROM write operation will commence.

Table 8. Summary of EEPROM-Related Registers

MEMORY REGION	REGISTER NAME	I²C REG ADDRESS	DESCRIPTION OF EEPROM-RELATED FUNCTION	REF PAGE
Status	STAT_SYSTEM	0x13	Indicates if the system is busy performing a write to the EEPROM. Indicates if a CRC error was detected in the EEPROM boot region.	35
	STAT_BOOT_CRC	0x1C	Result of most recent boot region CRC calculated by the LT8491.	38
Control	CTRL_WRT_TO_BOOT	0x20	Initiates writing to EEPROM and recalculation the boot region CRC.	39
	CTRL_EE_WRT_EN	0x21	Must be written 0xCC to allow writes to the EEPROM.	
Configuration	All registers in this region.	0x28-0x5B	Data in EEPROM is copied into these configuration region registers during startup. Contents of these registers can be copied back to the EEPROM boot region.	16
Boot	All registers in this region.	0x88-0xBD	I²C reads from this address range returns the boot EEPROM contents.	17

OPERATION

Copy the Configuration Registers to the EEPROM: The configuration register contents are copied to the boot region of the EEPROM by writing 0x30 to the CTRL_WRT_TO_BOOT register. This copy command performs the following operations:

- The status of this operation is indicated within the CTRL_WRT_TO_BOOT register where BUSY_RDY=1, WRITE_FAIL=0 and WRITE_SUCCESS=0. Also, STAT_SYSTEM→SYSTEM_BUSY=10b and STAT_SYSTEM→CRC_ERROR_BOOT=0.
- The configuration register data, located in I^2C addresses 0x28 through 0x5B, is copied to the boot region.
- A CRC of the configuration register data is calculated and written to STAT_CFG_CRC and BOOT_CRC.
- The boot region is read and verified against the configuration region. Any mismatch results in the CTRL_WRT_TO_BOOT→WRITE_FAIL bit being set.
- The CRC of the boot region is calculated and written to the STAT_BOOT_CRC register.
- If STAT_CFG_CRC or the new STAT_BOOT_CRC value don't match BOOT_CRC then a CRC error is indicated by STAT_SYSTEM→CRC_ERR_BOOT=1 and CTRL_WRT_TO_BOOT→WRITE_FAIL=1.
- Otherwise, a successful write operation is indicated by CTRL_WRT_TO_BOOT→WRITE_SUCCESS=1.
- Finally, CTRL_WRT_TO_BOOT→BUSY_RDY is cleared and STAT_SYSTEM→SYSTEM_BUSY is cleared to 00b.
- Approximately 200ms is required to proceed through all of these steps.

Restore Factory Defaults: The boot data can be restored to the factory defaults by writing 0x57 to the CTRL_WRT_TO_BOOT register. The default values are listed in the I^2C Register Map section. This restore command perform the following operations:

- The status of this operation is indicated within the CTRL_WRT_TO_BOOT register by setting BUSY_RDY=1, WRITE_FAIL=0 and WRITE_SUCCESS=0. Also, STAT_SYSTEM→SYSTEM_BUSY=10b and STAT_SYSTEM→CRC_ERROR_BOOT=0.
- The factory default values, including BOOT_CRC, are written to the boot region.
- The CRC of the boot region is calculated and the STAT_BOOT_CRC status register is updated with the calculated value.
- If the new STAT_BOOT_CRC value does not match BOOT_CRC then a CRC error is indicated by STAT_SYSTEM→CRC_ERR_BOOT=1 and CTRL_WRT_TO_BOOT→WRITE_FAIL=1.
- Otherwise, a successful write operation is indicated by CTRL_WRT_TO_BOOT→WRITE_SUCCESS=1.
- Finally, CTRL_WRT_TO_BOOT→BUSY_RDY is cleared and STAT_SYSTEM→SYSTEM_BUSY is cleared to 00b.
- Approximately 200ms is required to proceed through all these steps.

Note that this operation doesn't modify any data in the configuration registers. Refer to the CTRL_RESTART_CHIP register to restart the chip and automatically copy the factory setting into the configuration registers.

I²C REGISTER MAP

Summary Table

MEMORY REGION	REGISTER NAME	I²C REG ADDR	SIZE	REF PG.	BRIEF REG. DESCRIPTION	DEFAULT VALUE	DESCRIPTION OF DEFAULT VALUE
Telemetry	TELE_TBAT	0x00	Word	30	Battery temperature	0x7FFF	Indicates that the value has not been measured yet.
	TELE_POUT	0x02	Word		Output power	0x0000	Charger not on yet.
	TELE_PIN	0x04	Word		Input power	0x0000	Charger not on yet.
	TELE_EFF	0x06	Word		Charger efficiency	0x0000	Charger not on yet.
	TELE_IOUT	0x08	Word		Output current	0x0000	Charger not on yet.
	TELE_IIN	0x0A	Word		Input current	0x0000	Charger not on yet.
	TELE_VBAT	0x0C	Word		Battery voltage	0x0000	Indicates that the value has not been calculated yet.
	TELE_VIN	0x0E	Word		Input voltage measured from the FBIN pin.	0x0000	Indicates that the value has not been calculated yet.
	TELE_VINR	0x10	Word		Input voltage measured from the VINR pin.	0xFFFF	Indicates that the value has not been calculated yet.
Status	STAT_CHARGER	0x12	Byte	34	Charger status	0x00	Charging off.
	STAT_SYSTEM	0x13	Byte		System status	-	Indicates present system status.
	STAT_SUPPLY	0x14	Byte		Input supply status	-	Indicates present supply status.
	STAT_TS0_REMAIN	0x15	Byte		Stage 0 limit timer	0xFF	No Stage 0 time limit.
	STAT_TS1_REMAIN	0x16	Byte		Stage 1 limit timer	0xFF	No Stage 1 time limit.
	STAT_TS2_REMAIN	0x17	Byte		Stage 2 limit timer	0xFF	No Stage 2 time limit.
	STAT_TS3_REMAIN	0x18	Byte		Stage 3 limit timer	0xFF	No Stage 3 time limit.
	STAT_CHRG_FAULTS	0x19	Byte		Charging fault sources	0x00	No faults.
	STAT_VERSION	0x1A	Byte		LT8491 version code	0x00	-
	Reserved	0x1B	Byte		Reserved	-	Reserved
	STAT_BOOT_CRC	0x1C	Word		Calculated boot region CRC	-	Depends on boot region contents.
	STAT_CFG_CRC	0x1E	Word		Calculated configuration CRC	-	Depends on boot region contents.
Control	CTRL_WRT_TO_BOOT	0x20	Byte	39	Write to EEPROM	0x00	EEPROM writing not initiated.
	CTRL_EE_WRT_EN	0x21	Byte		Enable EEPROM writes	0x00	EEPROM writes not enabled.
	CTRL_HALT_STARTUP	0x22	Byte	40	Halt startup CRC checks	0x00	Always returns 0x00 on reads.
	CTRL_CHRG_EN	0x23	Byte		Enable/disable charger	-	See Startup Sequence section.
	CTRL_RESTART_CHIP	0x24	Byte		Restart the LT8491	0x00	Always returns 0x00 on reads.
	CTRL_RESET_FLAG	0x25	Byte		Reset flag	0x01	Indicates that LT8491 has been reset.
	CTRL_UPDATE_TELEM	0x26	Byte		Measure and update telemetry when charging logic is off	0x00	Telemetry update not initiated.
	Reserved	0x27	Byte		Reserved	-	Reserved

I²C REGISTER MAP

MEMORY REGION	REGISTER NAME	I²C REG ADDR	SIZE	REF PG.	BRIEF REG. DESCRIPTION	DEFAULT VALUE	DESCRIPTION OF DEFAULT VALUE
Configuration	CFG_RSENSE1	0x28	Word	42	PCB resistor value	Copied from EEPROM during startup. See Boot registers in this table for the factory settings.	
	CFG_RIMON_OUT	0x2A	Word		PCB resistor value		
	CFG_RSENSE2	0x2C	Word		PCB resistor value		
	CFG_RDACO	0x2E	Word		PCB resistor value		
	CFG_RFBOUT1	0x30	Word		PCB resistor value		
	CFG_RFBOUT2	0x32	Word		PCB resistor value		
	CFG_RDACI	0x34	Word		PCB resistor value		
	CFG_RFBIN2	0x36	Word		PCB resistor value		
	CFG_RFBIN1	0x38	Word		PCB resistor value		
	CFG_INIT_CHRG_EN	0x3A	Byte	45	Auto start charging after IC startup		
	CFG_VS3_25C	0x3B	Byte	46	Stage 3 V_{BAT} at 25°C		
	CFG_UV_S0	0x3C	Byte		Min. Stage 0 V_{BAT} voltage		
	CFG_S0_UV	0x3D	Byte		Low VBAT voltage		
	CFG_S0_S1	0x3E	Byte		Max. Stage 0 V_{BAT} voltage		
	CFG_S1_S0	0x3F	Byte		Min. Stage 1 V_{BAT} voltage		
	CFG_TBAT_MIN	0x40	Byte	50	Min. battery temperature		
	CFG_TBAT_MAX	0x41	Byte		Max. battery temperature		
	CFG_TMR_S0	0x42	Byte	51	Stage 0 time limit		
	CFG_TMR_S1	0x43	Byte		Stage 1 time limit		
	CFG_TMR_S2	0x44	Byte		Stage 2 time limit		
	CFG_TMR_S3	0x45	Byte		Stage 3 time limit		
	CFG_RSTRT_IN_FLT	0x46	Byte	52	Auto-restart when fault		
	CFG_RSTRT_IN_DONEA	0x47	Byte		Auto-restart threshold voltage when done charging		
	CFG_RSTRT_IN_DONEB	0x48	Byte		Auto-restart delay time when done charging		
	CFG_RSTRT_IN_S3	0x49	Byte		Auto-restart when in Stage 3		
	CFG_TERMINATE	0x4A	Byte	55	Charging termination options		
	CFG_SCAN_RATE_LP	0x4B	Byte	56	Full panel scan rate in LP		
	CFG_SCAN_RATE	0x4C	Byte		Full panel scan rate		
	CFG_CHRG_MISC	0x4D	Byte		Miscellaneous charger settings		
	CFG_TC3	0x4E	Long Word	58	Temperature coefficient		
	CFG_TC2	0x52			Temperature coefficient		
	CFG_TC1	0x56			Temperature coefficient		
	CFG_USER_CODE	0x5A	Word	59	Write user input data		
Manufacturer	MFR_DATA1	0x5C	Word	60	Manufacturer Data	-	Calculated at production.
	MFR_DATA2	0x5E	Word		Manufacturer Data	-	Calculated at production.
	MFR_DATA3	0x60	Word		Manufacturer Data	-	Calculated at production.

I²C REGISTER MAP

MEMORY REGION	REGISTER NAME	I²C REG ADDR	SIZE	REF PG.	BRIEF REG. DESCRIPTION	DEFAULT VALUE	DESCRIPTION OF DEFAULT VALUE
Boot (EEPROM)	BOOT_RSENSE1	0x88	Word	42	PCB resistor value	0x0000	Must be configured by user.
	BOOT_RIMON_OUT	0x8A	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RSENSE2	0x8C	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RDACO	0x8E	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RFBOUT1	0x90	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RFBOUT2	0x92	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RDACI	0x94	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RFBIN2	0x96	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_RFBIN1	0x98	Word		PCB resistor value	0x0000	Must be configured by user.
	BOOT_INIT_CHRG_EN	0x9A	Byte	45	Auto start charging after IC startup	0x00	Don't start charging automatically after startup.
	BOOT_VS3_25C	0x9B	Byte	46	Stage 3 V_{BAT} at 25°C	0x6B	V_{S3} = 95.7% of V_{S2}.
	BOOT_UV_S0	0x9C	Byte		Min. Stage 0 V_{BAT} voltage	0x46	$V_{(UV_S0)}$ = 35% of V_{S2}.
	BOOT_S0_UV	0x9D	Byte		Low V_{BAT} voltage	0x3E	$V_{(S0_UV)}$ = 31% of V_{S2}.
	BOOT_S0_S1	0x9E	Byte		Max. Stage 0 V_{BAT} voltage	0x8C	$V_{(S0_S1)}$ = 70% of V_{S2}.
	BOOT_S1_S0	0x9F	Byte		Min. Stage 1 V_{BAT} voltage	0x84	$V_{(S1_S0)}$ = 66% of V_{S2}.
	BOOT_TBAT_MIN	0xA0	Byte	50	Min. battery temperature	0x00	Under temperature fault limit = 0°C.
	BOOT_TBAT_MAX	0xA1	Byte		Max. battery temperature	0x32	Over temperature fault limit = 50°C.
	BOOT_TMR_S0	0xA2	Byte	51	Stage 0 time limit	0x00	Infinite time limit.
	BOOT_TMR_S1	0xA3	Byte		Stage 1 time limit	0x00	Infinite time limit.
	BOOT_TMR_S2	0xA4	Byte		Stage 2 time limit	0x00	Infinite time limit.
	BOOT_TMR_S3	0xA5	Byte		Stage 3 time limit	0x00	Infinite time limit.
	BOOT_RSTRT_IN_FLT	0xA6	Byte	52	Auto-restart when fault	0x20	RSTRT_ON_TMR_FLT_HRS = 1hour. NO_RSTRT_ON_VOLTS = 0. NO_RSTRT_ON_DISCON_FLT = 0. NO_RSTRT_ON_BATLOW_FLT = 0. NO_RSTRT_ON_TBAT_FLT = 0.
	BOOT_RSTRT_IN_DONEA	0xA7	Byte		Auto-restart threshold voltage when done charging	0x00	Don't restart charging automatically in Charge State Done.
	BOOT_RSTRT_IN_DONEB	0xA8	Byte		Auto-restart delay time when done charging	0x04	RSTRT_IN_DONE_HRS = 2 hours.
	BOOT_RSTRT_IN_S3	0xA9	Byte		Auto-restart when in Stage 3	0x01	RSTRT_S3_C5_VS3 = 1.
	BOOT_TERMINATE	0xAA	Byte	55	Charging termination options	0x08	S3_TMR_TERM_EN = 1.
	BOOT_SCAN_RATE_LP	0xAB	Byte	56	Full panel scan rate in LP	0x1F	Full panel scan every 8.5 minutes.
	BOOT_SCAN_RATE	0xAC	Byte		Full panel scan rate	0x0B	Full panel scan every 3 minutes.
	BOOT_CHRG_MISC	0xAD	Byte		Miscellaneous charger settings	0x08	Use V_{S3} in Stage 2 disabled. LP Mode enabled. Stage 3 disabled. Temperature Compensation disabled.
	BOOT_TC3	0xAE	Long Word	58	Temperature coefficient	0xB41F-FCCF	Coefficient = –1.49e-7.
	BOOT_TC2	0xB2			Temperature coefficient	0x3760-D090	Coefficient = 1.34e-5.
	BOOT_TC1	0xB6			Temperature coefficient	0xBAC9-D9D3	Coefficient = –1.54e-3.
	BOOT_USER_CODE	0xBA	Word	59	User input data	0x0000	-
	BOOT_CRC	0xBC	Word	60	Expected CRC result for boot region	-	Expected CRC result for boot region. Default value is factory CRC. This value will change if the user writes EEPROM with new values.

I²C REGISTER MAP

Note: I²C register addresses 0x62 through 0x87 and 0xBE through 0xFF are reserved locations. Byte read, or Word read of these locations return manufacturer reserved values. If the user writes these locations with new values they will not be stored.

I²C REGISTER DESCRIPTIONS

TELEMETRY REGISTERS

The telemetry registers, summarized in Table 9 and in the I²C Register Map, are read-only and indicate the latest telemetry measured by the LT8491. These word-sized values must be read using the I²C word-read transaction to avoid retrieving mismatched bytes (see I²C: Data Transfer Transactions). Refer to the Telemetry Operation section, earlier in the data sheet, for additional information.

Table 9. Summary of Telemetry Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	DESCRIPTION	REF PAGE
TELE_TBAT	WORD	0x00	Battery temperature measured at the TEMPSENSE pin.	30
TELE_POUT	WORD	0x02	Power delivered out of the charger.	31
TELE_PIN	WORD	0x04	Power draw from V_{IN} supply.	31
TELE_EFF	WORD	0x06	Charger efficiency.	31
TELE_IOUT	WORD	0x08	Output current to V_{BAT}.	32
TELE_IIN	WORD	0x0A	Input current from V_{IN}.	32
TELE_VBAT	WORD	0x0C	V_{BAT} voltage.	32
TELE_VIN	WORD	0x0E	V_{IN} voltage measured at the FBIR pin.	33
TELE_VINR	WORD	0x10	V_{IN} voltage measured at the VINR pin.	33

TELE_TBAT

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x00	[15:0]	°C • 10	Unsigned Integer	40°C = 0x0190 –15°C = 0xFF6A	Indicates the temperature measured at the TEMPSENSE pin or if the battery disconnect has been detected.

This register contains the most recently measured battery temperature in °C times 10 in a two's complement, signed integer format. The value can be converted to °C by casting it to a floating-point and dividing the result by 10. The temperature is measured on the TEMPSENSE pin via the external thermistor divider network. TELE_TBAT will report temperatures between approximately –45°C to 65°C, but with slightly reduced accuracy outside of the –40°C to 60°C range. The reset value of TELE_TBAT is 0x7FFF indicating that the temperature measurement has not been performed yet. A value of 0x7777 indicates that the TEMPSENSE pin voltage is high enough to indicate that the battery has been disconnected.

Related Data Sheet Sections: Telemetry Operation, HW Config: Battery Temperature and Disconnect Sensing

I²C REGISTER DESCRIPTIONS

TELE_POUT

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x02	[15:0]	Watts • 100	Unsigned Integer	210.6W = 0x5244 5.3W = 0x0212	Calculated power delivered out of the charger.

This register contains the most recently measured power delivered out of the charger. The value is in Watts multiplied by 100 in an unsigned integer format. TELE_POUT can be converted to Watts by casting it to a floating-point value and dividing the result by 100. TELE_POUT is the product of the most recently calculated TELE_IOUT and TELE_VBAT values.

Calculation of TELE_POUT requires that non-zero values are in the following telemetry configuration registers: CFG_RSENSE2, CFG_RIMON_OUT, CFG_RDACO, CFG_RFBOUT1, CFG_RFBOUT2. The contents of these registers must match the hardware values on the PCB to achieve the correct TELE_POUT values. Reading 0xFFFF from TELE_POUT indicates that one or more of the required configuration registers was set to 0x0000.

Related Data Sheet Section: Telemetry Operation

TELE_PIN

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x04	[15:0]	Watts • 100	Unsigned Integer	210.6W = 0x5244 5.3W = 0x0212	Calculated power drawn from the charger's supply.

This register contains the most recently measured power drawn from the charger's supply. The value is in Watts multiplied by 100 in an unsigned integer format. TELE_PIN can be converted to Watts by casting it to a floating-point value and dividing the result by 100. TELE_PIN is the product of the most recently calculated TELE_IIN and either TELE_VINR or TELE_VIN. TELE_VINR is used when powered by a solar panel. TELE_VIN is used when the VINR pin is pulled low to activate the DC supply charging mode.

Calculation of TELE_PIN requires that non-zero values are in the following telemetry configuration registers: CFG_RSENSE1 and, when powered by a DC supply, CFG_RDACI, CFG_RFBIN1, CFG_RFBIN2. The contents of these registers must match the hardware values on the PCB to achieve the correct TELE_PIN values. Reading 0xFFFF from TELE_PIN indicates that one or more of the required configuration registers was set to 0x0000.

Related Data Sheet Sections: Telemetry Operation, HW Config: DC Supply Powered Charging

TELE_EFF

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x06	[15:0]	%Efficiency • 100	Unsigned Integer	96.21% = 0x2595 84.75% = 0x211B	Calculated charger power efficiency.

This register contains the most recently measured power conversion efficiency. The value is in % multiplied by 100 in an unsigned integer format. TELE_EFF can be converted to % by casting it to a floating-point value and dividing the result by 100. TELE_EFF is the ratio of the most recently measured TELE_POUT and TELE_PIN.

Calculation of TELE_EFF requires that TELE_POUT and TELE_PIN are properly configured. See the data sheet description for those registers for further information. Reading 0xFFFF from TELE_EFF indicates that one or more of the required configuration registers was set to 0x0000. Note: The maximum calculated efficiency value is 99.99%.

Related Data Sheet Sections: Telemetry Operation, HW Config: DC Supply Powered Charging

I²C REGISTER DESCRIPTIONS

TELE_IOUT

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x08	[15:0]	Milliamps	Unsigned Integer	5.274A = 0x149A 0.039A = 0x0027	Output current to V_{BAT}.

This register contains the most recently measured current flowing out of the charger through the R_{SENSE2} resistor. The value is in milliamps in an unsigned integer format. TELE_IOUT can be converted to Amps by casting it to a floating-point value and dividing the result by 1000. To determine TELE_IOUT, the LT8491 measures the voltage at the IOR pin which is proportional to the output current as discussed in the HW Config: Output Current Sense and Limit section.

Calculation of TELE_IOUT requires that non-zero values are in the CFG_RIMON_OUT and CFG_RSENSE2 registers. The contents of these registers must match the hardware values on the PCB to achieve the correct TELE_IOUT values. Reading 0xFFFF from TELE_IOUT indicates that one or more of the required configuration registers was set to 0x0000.

Related Data Sheet Sections: Telemetry Operation, HW Config: Output Current Sense and Limit

TELE_IIN

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x0A	[15:0]	Milliamps	Unsigned Integer	5.274A = 0x149A 0.039A = 0x0027	Input current from V_{IN}.

This register contains the most recently measured current flowing into the charger through the R_{SENSE1} resistor. The value is in milliamps in an unsigned integer format. TELE_IIN can be converted to Amps by casting it to a floating-point value and dividing the result by 1000. To determine TELE_IIN, the LT8491 measures the voltage at the IIR pin which is proportional to the input current as discussed in the HW Config: Input Current Sense and Limit section.

Calculation of TELE_IIN requires that a non-zero value is in the CFG_RSENSE1 register. The contents of this register must match the hardware value on the PCB to achieve the correct TELE_IIN value. Reading 0xFFFF from TELE_IIN indicates that CFG_RSENSE1 was set to 0x0000.

Related Data Sheet Sections: Telemetry Operation, HW Config: Input Current Sense and Limit

TELE_VBAT

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x0C	[15:0]	Volts • 100	Unsigned Integer	27.42V = 0x0AB6	Charger V_{BAT} output voltage.

This register contains the most recently measured V_{BAT} voltage as measured at the FBOR pin. The value is in Volts multiplied by 100 in an unsigned integer format. TELE_VBAT can be converted to volts by casting it to a floating-point value and dividing the result by 100.

Proper reporting of TELE_VBAT requires that non-zero values are in the following telemetry configuration registers: CFG_RDACO, CFG_RFBOUT1, CFG_RFBOUT2. The contents of these registers must match the hardware values on the PCB to achieve the correct TELE_VBAT values. The reset default value of TELE_VBAT is 0x0000 indicating that the voltage has not yet been measured. Reading 0xFFFF from TELE_VBAT indicates one or more of the required configuration registers was set to 0x0000.

Related Data Sheet Sections: Telemetry Operation, HW Config: V_{BAT} in Stage 2 (V_{S2})

I²C REGISTER DESCRIPTIONS

TELE_VIN

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x0E	[15:0]	Volts • 100	Unsigned Integer	27.42V = 0x0AB6	V_{IN} voltage measured from the FBIR pin.

This register contains the most recently measured V_{IN} voltage as measured at the FBIR pin. The value is in Volts multiplied by 100 in an unsigned integer format. TELE_VIN can be converted to volts by casting it to a floating-point value and dividing the result by 100.

Proper reporting of TELE_VIN requires that non-zero values are in the following telemetry configuration registers: CFG_RDACI, CFG_RFBIN1, CFG_RFBIN2. The contents of these registers must match the hardware values on the PCB to achieve the correct TELE_VIN values. When solar supply operation is detected, TELE_VIN will indicate 0x0000. In this case, read V_{IN} voltage from TELE_VINR instead. The reset default value of TELE_VIN is 0x0000 indicating that the voltage has not yet been measured. Reading 0xFFFF from TELE_VIN indicates one or more of the required configuration registers was set to 0x0000.

Related Data Sheet Sections: Telemetry Operation, HW Config: Input Voltage Sensing and Modulation

TELE_VINR

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x10	[15:0]	Volts • 100	Unsigned Integer	27.42V = 0x0AB6	V_{IN} voltage measured from the VINR pin.

This register contains the most recently measured V_{IN} voltage as measured at the VINR pin. The value is in Volts multi-plied by 100 in an unsigned integer format. TELE_VINR can be converted to volts by casting it to a floating-point value and dividing the result by 100. During low power and V_{IN} pulsing, TELE_VINR reports the valley voltage. TELE_VINR will not accurately represent the V_{IN} voltage when the VINR pin is being pulled low for DC power supply operation (see HW Config: DC Supply Powered Charging). When DC power supply operation is detected TELE_VINR will indicate 0x0000. In this case, read V_{IN} voltage from TELE_VIN instead. The reset default value of TELE_VINR is 0xFFFF indicating that the voltage has not yet been measured.

Related Data Sheet Sections: Telemetry Operation, HW Config: Solar Panel Powered Charging, HW Config: DC Supply Powered Charging

I²C REGISTER DESCRIPTIONS

STATUS REGISTERS

The following read-only registers, shown in Table 10, indicate status information about the charger. Detailed information about each register and its respective data follows this table.

Table 10. Summary of Status Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	DESCRIPTION	REF PAGE
STAT_CHARGER	BYTE	0x12	Charging status including Stage #, fault and others.	34
STAT_SYSTEM	BYTE	0x13	System status including startup information, CRC results and system busy status.	35
STAT_SUPPLY	BYTE	0x14	Solar panel operating state, DC supply indicator and others.	36
STAT_TS0_REMAIN	BYTE	0x15	Time remaining on Stage 0 limit timer.	36
STAT_TS1_REMAIN	BYTE	0x16	Time remaining on Stage 1 limit timer.	
STAT_TS2_REMAIN	BYTE	0x17	Time remaining on Stage 2 limit timer.	
STAT_TS3_REMAIN	BYTE	0x18	Time remaining on Stage 3 limit timer.	
STAT_CHRG_FAULTS	BYTE	0x19	Indicates the source(s) of charging faults.	37
STAT_VERSION	BYTE	0x1A	LT8491 version code.	38
STAT_BOOT_CRC	WORD	0x1C	Indicates the latest CRC calculation result performed on the EEPROM boot region.	38
STAT_CFG_CRC	WORD	0x1E	Indicates the latest CRC calculation result performed on the configuration region.	38

STAT_CHARGER

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x12	CHRG_FAULT	[7]	1 indicates that one or more of the bits in the STAT_CHRG_FAULTS register is 1. 0 indicates that all the STAT_CHRG_FAULTS bits are presently 0.
	TELEM_ACTIVE	[6]	1 indicates that the telemetry registers are being periodically updated with the latest measurements and all possible telemetry measurements have been made at least once since CHRG_EN has toggled from 0 to 1. 0 indicates that none of the telemetry registers are being periodically updated. This bit becomes 1 shortly after setting CHRG_EN=1 (approximately 80ms delay) or immediately after initiating an update telemetry operation by writing the CTRL_UPDATE_TELEM register. This bit becomes 0 immediately after setting CHRG_EN=0 or when the telemetry update operation completes. See the Telemetry Registers section for further information. *Related Data Sheet Sections:* Startup Sequence, Telemetry Operation
	CHRG_STAGE	[5:3]	These bits reflect the present charging stage and are valid when CHRG_LOGIC_ON=1 (below). During a charging fault (CHRG_FAULT=1 above) they hold their last value. CHRG_STAGE is reset to 000b when the charging logic is turned off (CHRG_LOGIC_ON=0), when the part is reset, or when the charging automatically restarts at Stage 0. 000b = Stage 0 001b = Stage 1 010b = Stage 2 011b = Stage 3 100b = Done Charging

I²C REGISTER DESCRIPTIONS

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x12	CHARGING	[2]	1 indicates that battery charging is ongoing in one of the 4 charging stages (Stage 0 to 3). 0 indicates that the charging is not active, and the power stage has been turned off. 0 (not charging) is indicated due to any of the following conditions: • The charging logic is disabled as indicated by CHRG_LOGIC_ON=0 • The charging has been stopped due to a fault condition as indicated by CHRG_FAULT=1 • The charging has reached the done charging stage CHRG_STAGE=100b • The charging logic was recently enabled by setting CHRG_EN=1, but the logic hasn't started Stage 0 charging yet
	GT_C10	[1]	0 indicates that the charging current telemetry (TELE_IOUT) is less than C/10. 1 indicates that the charging current telemetry (TELE_IOUT) is greater than C/10.
	CHRG_LOGIC_ON	[0]	1 indicates that the charging logic is enabled and some I²C byte-write transactions will be ignored. Refer to Data: Access Permissions for further information about I²C write permissions. This bit is set to 1 immediately after the CHRG_EN bit, in the CTRL_CHRG_EN register, is set to 1. This bit clears to 0 typically 6ms to 90ms after the CHRG_EN bit is cleared to 0.

STAT_SYSTEM

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x13	Reserved	[7:6]	Reserved
	BOOT_SUCCESS	[5]	Indicates that startup was successful and configuration data was copied from the EEPROM boot region with a passing CRC check. More details are available in the Startup Sequence section.
	CRC_ERR_FACTORY	[4]	1 indicates that a CRC check of the factory settings failed. 0 indicates a successful CRC check of the settings. More details are available in the Startup Sequence section.
	CRC_ERR_BOOT	[3]	1 indicates that a CRC check of the boot EEPROM region failed. 0 indicates a successful CRC check of the boot EEPROM. More details are available in the Startup Sequence and EEPROM: Writing sections.
	SWENO	[2]	Indicates the present state of the SWENO pin. This pin state may toggle on/off while the charger is enabled as part of its normal operation.
	SYSTEM_BUSY	[1:0]	Indicates the status of the internal logic control system. Non-zero values indicate that the system is busy and may have limited ability to handle I²C byte-write commands, as discussed in the Data: Access Permissions section. • 00b = Not busy with other tasks • 01b = Busy with startup and related CRC checking • 10b = Busy with a long operation (EEPROM write or CTRL_UPDATE_TELEM command)

I²C REGISTER DESCRIPTIONS

STAT_SUPPLY

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x14	Reserved	[7:5]	Reserved
	VIN_UVLO	[4]	When powered by a panel: 1 indicates that the input voltage is below 10 Volts if Low Power Mode is enabled, otherwise input voltage is below 5.7 Volts. 0 indicates that the Input Panel Voltage is above 10 Volts if Low Power Mode is enabled, otherwise input panel voltage is above 5.7 Volts. *Related Data Sheet Sections:* Configure Misc. section
	PS_OR_SOLAR	[3]	1 Indicates that the LT8491 is being supplied by a DC power supply as detected by a low voltage on the VINR pin. MPPT and related functions are disabled. 0 Indicates that the LT8491 is being supplied by a solar panel. *Related Data Sheet Sections:* HW Config: DC Supply Powered Charging, Optional: DC Supply Detection Circuit, TELE_VINR
	SOLAR_STATE	[2:0]	Indicates the operating state of the solar panel: • 101b = Battery Limited: The battery may not presently be capable of drawing the maximum power available from the solar panel, therefore the panel may not be operating at the maximum power point. • 100b = Full Panel Scan: In this state, a full scan of the solar panel is being performed to make sure that the global maximum power point is being tracked. • 011b = Perturb and Observe: The solar panel is tracking a maximum power point. • 010b = LP Mode and V_{IN} Pulsing: The available panel current is too low for constant charging. Instead the low power operating mode is active, resulting in pulsing of the panel voltage as discussed in the Optional: Low Power Mode section. • 001b = LP Mode and V_{IN} too low: The available panel current is too low for constant charging and the panel voltage is too low to extract charging energy from. See Optional: Low Power Mode section. • 000b = None of the Above This is indicated if none of the above conditions exist. Examples may include: the input is not a solar panel; the panel voltage and/or current is not adequate for any of the above operations; a fault has occurred, and no charging is occurring; charger is in done charging state; other conditions may be possible.

STAT_TSx_REMAIN

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x15	STAT_TS0_REMAIN	[7:0]	Time remaining before respective stage timer expires. More details below.
0x16	STAT_TS1_REMAIN	[7:0]	
0x17	STAT_TS2_REMAIN	[7:0]	
0x18	STAT_TS3_REMAIN	[7:0]	

These four registers indicate the time remaining in the respective stage timers (Stages 0 to 3). Configuration of the starting values is discussed in the Configure Stage Timeout Limits section. If configured for a finite time limit and powered by a DC power supply, the respective timer will count down while charging in the respective stage. When a timer counts down to 0x00 the charging stops. The CFG_TERMINATE→Sx_TMR_TERM_EN bits determine if an expired timer indicates a fault or not.

I²C REGISTER DESCRIPTIONS

The time remaining is approximately 4.47 minutes multiplied by the register value. For example, 0x0D represents 58 minutes remaining. The countdown for each timer pauses when not charging (STAT_CHARGER→CHARGING=0) or a temperature fault occurs. The countdown for a timer also pauses when charging proceeds to the next stage. If either a battery disconnect fault or a low V_{BAT} fault is detected, all countdown timer values are reset. These registers indicate the values of the corresponding CFG_TMR_Sx registers when powered up in solar panel mode (STAT_SUPPLY→PS_OR_SOLAR=0).

Related Data Sheet Sections: Configure Stage Timeout Limits, Battery Charging Algorithm, Configure Charge Termination

STAT_CHRG_FAULTS

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x19	TS3_EXPIRED_FLT	[7]	1 indicates that a charging stage timeout fault has occurred. These fault bits are cleared to 0: • When the charging restarts automatically • When the charging is disabled by setting CHRG_EN=0. The bits may remain set until STAT_CHARGER→CHRG_LOGIC_ON indicates 0 • During the startup sequence Otherwise, one of these fault bits is set when: • The charging logic is on (STAT_CHARGER→CHRG_LOGIC_ON=1) *and* • The respective STAT_TSx_REMAIN register has counted down to 0x00 *and* • The timer's expiration is configured to be a fault (the respective Sx_TMR_TERM_EN bit, in the CFG_TERMINATE register, is set to 0) *Related Data Sheet Sections:* Charging Faults, Configure Stage Timeout Limits, Configure Automatic Restart, Status Registers, Startup Sequence
	TS2_EXPIRED_FLT	[6]	
	TS1_EXPIRED_FLT	[5]	
	TS0_EXPIRED_FLT	[4]	
	BAT_DISCON_FLT	[3]	1 indicates that the battery has been disconnected, as measured at the TEMPSENSE pin. This fault bit is cleared to 0: • When the charging is disabled by setting CHRG_EN=0. The bit may remain set until STAT_CHARGER→CHRG_LOGIC_ON indicates 0 • During the startup sequence Otherwise, the LT8491 periodically measures the TEMPSENSE pin to check for battery temperature and connection faults as discussed in the Charging Faults section. *Related Data Sheet Sections:* Charging Faults, HW Config: Battery Temperature and Disconnect Sensing, Configure Temperature Fault Limits, TELE_TBAT, Startup Sequence
	HIGH_TBAT_FLT	[2]	1 in either bit indicates that the battery temperature, as measured from the TEMPSENSE pin, is outside of the allowed battery temperature range. These fault bits are cleared to 0: • When the charging is disabled by setting CHRG_EN=0. The bit may remain set until STAT_CHARGER→CHRG_LOGIC_ON indicates 0 • During the startup sequence • During a battery disconnect fault (BAT_DISCON_FLT=1) Otherwise, the LT8491 periodically measures the TEMPSENSE pin to check for battery temperature and connection faults as discussed in the Charging Faults section. *Related Data Sheet Sections:* Charging Faults, HW Config: Battery Temperature and Disconnect Sensing, Configure Temperature Fault Limits, TELE_TBAT, Startup Sequence
	LOW_TBAT_FLT	[1]	

I²C REGISTER DESCRIPTIONS

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x19	LOW_VBAT_FLT	[0]	1 indicates that the low battery voltage fault has been detected. The V_{BAT} thresholds for this fault (V_{S0_UV} and V_{UV_S0}) are configured in the CFG_UV_S0 and CFG_S0_UV registers. This fault bit is cleared to 0: • When the charging is disabled by setting CHRG_EN=0. The bit may remain set until STAT_CHARGER→CHRG_LOGIC_ON indicates 0 • During the startup sequence • During a battery disconnect fault (BAT_DISCON_FLT=1) • During a low or high battery temperature fault • If the $V_{BAT} > V_{UV_S0}$ threshold is reached for a pre-determined amount of time *Related Data Sheet Sections:* Charging Faults, TELE_VBAT, Startup Sequence

STAT_VERSION

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x1A	-	[7:0]	LT8491 version information. See I²C Register Map for factory default value.

STAT_BOOT_CRC

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x1C	-	[15:0]	Contains the most recent CRC of the boot region calculated by the LT8491. See CRC Operation for more information.

STAT_CFG_CRC

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x1E	-	[15:0]	Contains the most recent CRC of the configuration region calculated by the LT8491. See CRC Operation for more information.

I²C REGISTER DESCRIPTIONS

CONTROL THE EEPROM

The following registers are used to initiate and monitor EEPROM write operations. Write access permissions are detailed in the Data: Access Permissions section.

CTRL_WRT_TO_BOOT

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x20	Reserved	[7:3]	Reserved
	WRITE_FAIL	[2]	Read of this bit returns a 1 if the most recent attempt to write the EEPROM boot region failed.
	WRITE_SUCCESS	[1]	Read of this bit returns a 1 if the most recent attempt to write the EEPROM boot region succeeded.
	BUSY_RDY	[0]	Read of this bit returns a 1 if a write to the EEPROM boot region is in progress.

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x20	-	[7:0]	Write to 0x30 to copy the configuration registers to the boot region of the EEPROM. Write to 0x57 to restore the boot region to the factory default settings.

This register is used to initiate a write to the EEPROM boot region. It can also be read to monitor status of the write operation. Writing one of two unique byte patterns initiates the desired write operation as listed above. Reading of this register indicates the status of the write operation, also shown above. Writes to this register are only accepted if CTRL_EE_WRT_EN=0xCC and STAT_SYSTEM→SYSTEM_BUSY=00b. Reads are permitted any time that the I²C interface is operational.

Related Data Sheet Sections: EEPROM: Writing, Data: Access Permissions

CTRL_EE_WRT_EN

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x21	CTRL_EE_WRT_EN	[7:0]	This register must be set to 0xCC to allow the on-chip EEPROM to be written. Any other value prohibits the EEPROM from being modified. Setting this register to 0xCC also prohibits writes to the configuration registers.

This register must be written to 0xCC before any on-chip EEPROM data can be modified. Any other value prohibits writes to the EEPROM. Note that this register can only be written when STAT_SYSTEM→SYSTEM_BUSY=00b and STAT_CHARGER→CHRG_LOGIC_ON=0. Setting this register to 0xCC also prohibits writes to the configuration registers within addresses 0x28-0x5B until this register is written to a value other than 0xCC.

Related Data Sheet Sections: EEPROM: Writing, Data: Access Permissions

I²C REGISTER DESCRIPTIONS

CONTROL OTHER FUNCTIONS

The following registers, shown in Table 11, can be written to control various functions of the LT8491. Write access permissions are detailed in the Data: Access Permissions section. Detailed information about each register and its respective function follow this table.

Table 11. Summary of Other Control Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	DESCRIPTION	REF PAGE
CTRL_HALT_STARTUP	BYTE	0x22	Halt failing startup CRC checking.	40
CTRL_CHRG_EN	BYTE	0x23	Enable/disable battery charging.	40
CTRL_RESTART_CHIP	BYTE	0x24	Restart the LT8491.	41
CTRL_RESET_FLAG	BYTE	0x25	Flag that is set upon reset of the LT8491.	41
CTRL_UPDATE_TELEM	BYTE	0x26	Write this register to measure and update telemetry registers when the charging logic is off.	41

CTRL_HALT_STARTUP

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x22	-	[7:0]	Write 0x5A to halt startup when the CRC checking is failing. The STAT_SYSTEM→SYSTEM_BUSY bits will indicate 00b when the halt sequence is complete. See Startup Sequence section for more information. Returns 0's on reads.

Related Data Sheet Sections: Startup Sequence, Data: Access Permissions

CTRL_CHRG_EN

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x23	Reserved	[7:1]	Reserved
	CHRG_EN	[0]	Discussed below.

CHRG_EN is the master on/off control bit for the charger. The battery charging, and telemetry starts after CHRG_EN is set high and is stopped when CHRG_EN is set low. More details are as follows.

After setting CHRG_EN=1:

- The charging control logic is immediately enabled as indicated by STAT_CHARGER→CHRG_LOGIC_ON=1.
- I²C write access is immediately restricted as discussed in the Data: Access Permissions section.
- The battery charging, stage timers, and fault checking starts as shown at the top of Figure 8.
- Telemetry acquisition commences as discussed in the Telemetry: Acquisition section.

After setting CHRG_EN=0:

- The power stage of the battery charger is immediately turned off as indicated by STAT_SYSTEM→SWENO=0.
- Telemetry measurements stop as discussed in the Telemetry: Acquisition section.
- The charger status register STAT_CHARGER normally clears to 0x00. If a fault was present and not cleared before CHRG_EN=0 then its value will be 0x80.

I²C REGISTER DESCRIPTIONS

- The supply status register STAT_SUPPLY→SOLAR_STATE bits [2:0] clear to 000b.
- The fault register STAT_CHRG_FAULTS holds its last value reported before CHRG_EN=0.
- The ECON pin is driven low (see Optional: $EXTV_{CC}$ Disconnect section).
- Some registers cannot be written until the CHRG_LOGIC_ON bit clears in the STAT_CHARGER register. Be sure to poll the CHRG_LOGIC_ON bit before attempting subsequent register writes.

After changing the CHRG_EN setting, some operations listed above may not happen immediately unless otherwise indicated. As discussed in the Startup Sequence section, the BOOT_INIT_CHRG_EN value is automatically copied from the EEPROM into this CTRL_CHRG_EN register near the end of the startup sequence. This provides a way to start the charging automatically after startup by storing 0x01 in the BOOT_INIT_CHRG_EN.

Related Data Sheet Sections: Data: Access Permissions

CTRL_RESTART_CHIP

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x24	-	[7:0]	Write 0x99 to restart the LT8491. See Startup Sequence section for more information. Returns 0's on reads.

To issue a restart chip command, the CTRL_CHRG_EN register must be cleared. The part will restart after 0x99 is written to the CTRL_RESTART_CHIP register. Upon restarting, the CTRL_CHRG_EN→CHRG_EN bit is set to the value read from the BOOT_INIT_CHRG_EN EEPROM location.

Related Data Sheet Sections: Startup Sequence, Data: Access Permissions

CTRL_RESET_FLAG

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x25	Reserved	[7:1]	Reserved
	RESET_FLAG	[0]	This bit is set to 1 during startup. It can be cleared by the user after startup completes. Subsequent reading of this bit will indicate if the IC has reset (power cycle) or restarted (write 0x99 to CTRL_RESTART_CHIP to restart the chip) since the last time the bit was cleared.

Related Data Sheet Sections: Startup Sequence, Data: Access Permissions

CTRL_UPDATE_TELEM

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x26	Reserved	[7:1]	Reserved
	BUSY_RDY	[0]	Read of this bit returns a 1 while the telemetry update is in progress.

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x26	-	[7:0]	Write to 0xAA to update telemetry.

I²C REGISTER DESCRIPTIONS

Writing 0xAA to this register initiates a telemetry update. It can be written when the charging logic is off and telemetry is not otherwise being acquired (see Telemetry: Acquisition). Reading back the BUSY_RDY bit indicates the status of the update which typically requires approximately 20ms to complete. Writes to this register are only accepted if STAT_CHARGER→CHRG_LOGIC_ON=0, CTRL_EE_WRT_EN≠0xCC and STAT_SYSTEM→SYSTEM_BUSY=00b. Reads are permitted any time that the I²C interface is operational.

This telemetry update operation causes the LT8491 to measure telemetry and update the following registers: TELE_TBAT, TELE_PIN, TELE_IIN, TELE_VBAT, TELE_VIN, TELE_VINR. The remaining telemetry registers are not updated because the charger is off. Note that if the TEMPSENSE pin measurement detects a disconnected battery condition, TELE_TBAT will become 0x7777 indicating the disconnect condition. Also note that in order to minimize battery discharge, the V_{BAT} feedback divider is optionally disconnected when the charging is off (see the Optional: Output Feedback Resistor Disconnect section). Updating the telemetry, by writing to CTRL_UPDATE_TELEM, temporarily reconnects the feedback divider to measure the battery voltage.

Related Data Sheet Sections: Telemetry: Acquisition, HW Config: Battery Temperature and Disconnect Sensing, Optional: Output Feedback Resistor Disconnect, Data: Access Permissions

CONFIGURE THE TELEMETRY

The registers in Table 12 must contain valid data before the LT8491 can properly calculate telemetry for volts, amps, power and efficiency. The contents of these registers don't affect any aspect of the charger's operation, including MPPT scanning, V_{S2}, V_{S3}, temperature calculation etc. The contents of these registers are only used by the LT8491 to calculate the read-only telemetry values found between I²C addresses 0x02 and 0x0E and to set/clear the STAT_CHARGER→GT_C10 bit.

Table 12. Summary of Telemetry Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_RSENSE1	WORD	0x28	0x88	Indicate the R_{SENSE1} resistor value.	42
CFG_RIMON_OUT	WORD	0x2A	0x8A	Indicate the R_{IMON_OUT} resistor value.	43
CFG_RSENSE2	WORD	0x2C	0x8C	Indicate the R_{SENSE2} resistor value.	43
CFG_RDACO	WORD	0x2E	0x8E	Indicate the total value of R_{DACO1} + R_{DACO2}.	43
CFG_RFBOUT1	WORD	0x30	0x90	Indicate the R_{FBOUT1} resistor value.	44
CFG_RFBOUT2	WORD	0x32	0x92	Indicate the R_{FBOUT2} resistor value.	44
CFG_RDACI	WORD	0x34	0x94	Indicate the total value of R_{DACI1} + R_{DACI2}.	44
CFG_RFBIN2	WORD	0x36	0x96	Indicate the R_{FBIN2} resistor value.	45
CFG_RFBIN1	WORD	0x38	0x98	Indicate the R_{FBIN1} resistor value.	45

CFG_RSENSE1

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x28	[15:0]	mΩ • 100	Unsigned Integer	4.7mΩ = 0x01D6 10mΩ = 0x03E8	R_{SENSE1} resistor value. Required to calculate telemetry for TELE_PIN, TELE_EFF, TELE_IIN.

The LT8491 uses this register value to calculate telemetry for the TELE_PIN, TELE_EFF and TELE_IIN registers. CFG_RSENSE1 is not used for any other purpose and does not affect charging in any way. Write this register to indicate the value of the R_{SENSE1} input current sense resistor. The value written to this register should be R_{SENSE1}, in milliohms,

I²C REGISTER DESCRIPTIONS

multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: Input Current Sense and Limit for information about R_{SENSE1}

CFG_RIMON_OUT

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x2A	[15:0]	kΩ • 100	Unsigned Integer	95.3kΩ = 0x253A 24.3kΩ = 0x097E	R_{IMON_OUT} resistor value. Required for calculate telemetry for TELE_IOUT, TELE_POUT, TELE_EFF.

The LT8491 uses this register value to calculate telemetry for the TELE_IOUT, TELE_POUT, and TELE_EFF registers. CFG_RIMON_OUT is not used for any other purpose and does not affect charging in any way. Write this register to indicate the value of the R_{IMON_OUT} output current monitoring resistor. The value written to this register should be R_{IMON_OUT}, in kΩ multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: Output Current Sense and Limit for information about R_{IMON_OUT}

CFG_RSENSE2

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x2C	[15:0]	mΩ • 100	Unsigned Integer	4.7mΩ = 0x01D6 10mΩ = 0x03E8	R_{SENSE2} resistor value. Required to calculate telemetry for TELE_POUT, TELE_EFF, TELE_IOUT.

The LT8491 uses this register value to calculate telemetry for the TELE_POUT, TELE_EFF and TELE_IOUT registers. CFG_RSENSE2 is not used for any other purpose and does not affect charging in any way. Write this register to indicate the value of the R_{SENSE2} output current sense resistor. The value written to this register should be R_{SENSE2}, in milliohms, multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: Output Current Sense and Limit for information about R_{SENSE2}

CFG_RDACO

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x2E	[15:0]	kΩ • 100	Unsigned Integer	95.3kΩ = 0x253A 24.3kΩ = 0x097E	Value of R_{DACO1} + R_{DACO2}. Required to calculate telemetry for TELE_VBAT, TELE_POUT, TELE_EFF.

The LT8491 uses this register value to calculate telemetry for the TELE_VBAT, TELE_POUT, and TELE_EFF registers. CFG_RDACO is not used for any other purpose and does not affect charging in any way. Write this register to indicate the total value of R_{DACO1} + R_{DACO2} in the output feedback divider network. The value written to this register should be the total value of R_{DACO1} + R_{DACO2}, in kΩ multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: V_{BAT} in Stage 2 (V_{S2}) for information about the R_{DACO} resistors

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CFG_RFBOUT1

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x30	[15:0]	kΩ • 10	Unsigned Integer	442kΩ = 0x1144 274kΩ = 0x0AB4	Value of R_{FBOUT1}. Required to calculate telemetry for TELE_VBAT, TELE_POUT, TELE_EFF.

The LT8491 uses this register value to calculate telemetry for the TELE_VBAT, TELE_POUT, and TELE_EFF registers. CFG_RFBOUT1 is not used for any other purpose and does not affect charging in any way. Write this register to indicate the value of R_{FBOUT1} in the output feedback divider network. The value written to this register should be R_{FBOUT1}, in kΩ multiplied by 10 in an unsigned integer format. See the examples above. The default value is all 0's indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: V_{BAT} in Stage 2 (V_{S2}) for information about R_{FBOUT1}

CFG_RFBOUT2

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x32	[15:0]	kΩ • 100	Unsigned Integer	10kΩ = 0x03E8 20kΩ = 0x07D0	Value of R_{FBOUT2}. Required to calculate telemetry for TELE_VBAT, TELE_POUT, TELE_EFF.

The LT8491 uses this register value to calculate telemetry for the TELE_VBAT, TELE_POUT, and TELE_EFF registers. CFG_RFBOUT2 is not used for any other purpose and does not affect charging in any way. Write this register to indicate the value of R_{FBOUT2} in the output feedback divider network. The value written to this register should be R_{FBOUT2}, in kΩ multiplied by 100 in an unsigned integer format. See the examples above. The default value is all 0's indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: V_{BAT} in Stage 2 (V_{S2}) for information about R_{FBOUT2}

CFG_RDACI

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x34	[15:0]	kΩ • 100	Unsigned Integer	95.3kΩ = 0x253A 24.3kΩ = 0x097E	Value of R_{DACI1} + R_{DACI2}. Required to calculate telemetry for TELE_VIN. Also required for TELE_PIN and TELE_EFF telemetry when powered by a DC power supply.

The LT8491 uses this register value to calculate telemetry for the TELE_VIN register. It is also used to calculate telemetry for TELE_PIN and TELE_EFF when powered by a DC power supply. CFG_RDACI is not used for any other purpose and does not affect charging in any way. Write this register to indicate the total value of R_{DACI1} + R_{DACI2} in the input feedback divider network. The value written to this register should be the total value of R_{DACI1} + R_{DACI2}, in kΩ multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Sections: HW Config: Input Voltage Sensing and Modulation, HW Config: DC Supply Powered Charging

I²C REGISTER DESCRIPTIONS

CFG_RFBIN2

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x36	[15:0]	kΩ • 100	Unsigned Integer	10kΩ = 0x03E8 20kΩ = 0x07D0	Value of R_{FBIN2}. Required to calculate telemetry for TELE_VIN. Also required for TELE_PIN and TELE_EFF telemetry when powered by a DC power supply.

The LT8491 uses this register value to calculate telemetry for the TELE_VIN register. It is also used to calculate telemetry for TELE_PIN and TELE_EFF when powered by a DC power supply. CFG_RFBIN2 is not used for any other purpose and does not affect charging in any way. Write this register to indicate value of R_{FBIN2} in the input feedback divider network. The value written to this register should be R_{FBIN2}, in kΩ multiplied by 100 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: Input Voltage Sensing and Modulation for information about R_{FBIN2}

CFG_RFBIN1

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x38	[15:0]	kΩ • 10	Unsigned Integer	442kΩ = 0x1144 274kΩ = 0x0AB4	Value of R_{FBIN1}. Required to calculate telemetry for TELE_VIN, TELE_PIN, TELE_EFF.

The LT8491 uses this register value to calculate telemetry for the TELE_VIN register. It is also used to calculate telemetry for TELE_PIN and TELE_EFF when powered by a DC power supply. This register value is not used for any other purpose and does not affect charging in any way. Write this register to indicate value of R_{FBIN1} in the input feedback divider network. The value written to this register should be R_{FBIN1}, in k multiplied by 10 in an unsigned integer format. See the examples above. The default value is 0x0000 indicating that this value has not been configured.

Related Data Sheet Section: See HW Config: Input Voltage Sensing and Modulation for information about R_{FBIN1}

CONFIGURE INITIAL CHARGER ENABLE

Table 13. Summary of Register to Configure Initial Charger Enable

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_INIT_CHRG_EN	BYTE	0x3A	0x9A	Configures automatic start of charger.	45

CFG_INIT_CHRG_EN

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x3A	Reserved	[7:1]	Reserved
	INIT_CHRG_EN	[0]	Value of this bit is copied to CTRL_CHRG_EN during the startup sequence if CRC error checking passes.

This register value is used to automatically start the charger only if CRC error checking passes during the startup sequence. A user value of 0x01 automatically starts the charger, or a user value of 0x00 means the charger does not start automatically.

Related Data Sheet Sections: Startup Sequence

I²C REGISTER DESCRIPTIONS

CONFIGURE V_{BAT} FOR STAGES 0, 1 AND 3

The following registers configure the battery voltages for some of the charging stage transitions. These are set as a percentage of V_{S2} which is initially configured with external resistors as discussed in the HW Config: V_{BAT} in Stage 2 (V_{S2}) section.

Note: The following registers have minimum and maximum values. The LT8491 boundary checking occurs when CTRL_CHRG_EN transitions from 0 to 1. If a value written to any of these registers violates the defined maximum value, the default register value will be used instead.

Table 14. Summary of Stage 0, 1 and 3 V_{BAT} Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_VS3_25C	BYTE	0x3B	0x9B	V_{S3} at 25°C and when temperature compensation is disabled.	46
CFG_UV_S0	BYTE	0x3C	0x9C	Threshold for V_{BAT} entering Stage 0 from low V_{BAT} fault.	47
CFG_S0_UV	BYTE	0x3D	0x9D	Threshold for V_{BAT} entering low V_{BAT} fault from Stage 0.	47
CFG_S0_S1	BYTE	0x3E	0x9E	Threshold for V_{BAT} entering Stage 1 from Stage 0.	48
CFG_S1_S0	BYTE	0x3F	0x9F	Threshold for V_{BAT} entering Stage 0 from Stage 1.	49

CFG_VS3_25C

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	MIN VALUE	MAX VALUE	DESCRIPTION
0x3B	[7:0]	1000 • (% of V_{S2}) – 850	Unsigned Integer	87.2% = 0x16 95.0% = 0x64	85% = 0x00	99% = 0x8C	Setting for V_{S3} (25°C). V_{S3} (25°C) is the Stage 3 battery voltage at 25°C which is a percentage of the Stage 2 battery voltage (V_{S2}) at 25°C. It has a resolution of 0.1% per bit.

This register sets V_{S3} which is the Stage 3 battery charging voltage. This setting is used when T_{BAT} = 25°C and when temperature compensation is disabled. V_{S3} can be configured to change with battery temperature as discussed in the Configure Temperature Compensation section.

CFG_VS3_25C is an 8-bit unsigned integer, representing a percentage of V_{S2} (25°C) between 85% to 99%, and is calculated as follows:

$$CFG_VS3_25C = 1000 \bullet \left[\frac{V_{S3}(25°C)}{V_{S2}(25°C)} \bullet 100\% \right] - 850$$

V_{S2} (25°C) is set by external resistors as discussed in the HW Config: V_{BAT} in Stage 2 (V_{S2}) section.

Example: Presume that V_{S2} (25°C) is set to 14.2V, via external resistors, and we wish to configure V_{S3} (25°C) = 13.59V. CFG_VS3_25C should be set as follows:

$$CFG_VS3_25C = 1000 \bullet \left[\frac{13.59V}{14.2V} \bullet 100\% \right] - 850$$
$$= 1000 \bullet 95.7\% - 850$$
$$= 107 \text{ (decimal)}$$
$$= 0x6B \text{ (hexadecimal)}$$

I²C REGISTER DESCRIPTIONS

Related Data Sheet Sections: Battery Charging Algorithm, HW Config: V_{BAT} in Stage 2 (V_{S2}), Configure Temp. Compensation, CFG_CHRG_MISC

CFG_UV_S0

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	MIN VALUE	MAX VALUE	DESCRIPTION
0x3C	[7:0]	200 • (% of V_{S2})	Unsigned Integer	30% = 0x3C 55.5% = 0x6F	0% = 0x00	90% = 0xB4	Configure V_{UV_S0} voltage as percentage of V_{S2}. Resolution of 0.5% per bit.

This register sets V_{UV_S0}, the minimum V_{BAT} voltage required to exit the low V_{BAT} fault condition and enter Stage 0 charging. This effectively sets the minimum battery voltage required to start charging. V_{UV_S0} is a percentage of the Stage 2 voltage V_{S2}. Therefore, if Stage 2 temperature compensation is enabled, via the CFG_CHRG_MISC→TC_ENABLE bit, V_{UV_S0} will vary with temperature in proportion to V_{S2}. Setting CFG_UV_S0 = 0x00 effectively disables the minimum V_{BAT} voltage checking to enter Stage 0. Consider setting CFG_UV_S0 = 0x00, for example when charging a lithium-ion battery that uses battery undervoltage protection circuitry.

CFG_UV_S0 is an 8-bit unsigned integer, representing a percentage of V_{S2} between 0% to 90% and is calculated as follows:

$$CFG_UV_S0 = 200 \bullet \left[\frac{V_{UV_S0}}{V_{S2}} \bullet 100\% \right]$$

Example: Presume that V_{S2} is set to 14.2V and we wish to set V_{UV_S0} = 7.81V. Set CFG_UV_S0 as follows:

$$CFG_UV_S0 = 200 \bullet \left[\frac{7.81V}{14.2V} \bullet 100\% \right]$$
$$= 200 \bullet [55\%]$$
$$= 110 \text{ (decimal)}$$
$$= 0x6E \text{ (hexadecimal)}$$

Therefore, writing CFG_UV_S0 to 0x6E configures V_{UV_S0} to be 55% of V_{S2}. Be sure to set CFG_UV_S0 to a higher V_{S2} percentage than CFG_S0_UV to achieve threshold hysteresis and avoid oscillating between stages. A 4%, or more, difference is recommended. Also, be sure to set CFG_UV_S0 lower than CFG_S1_S0 to avoid stage selection oscillations. A 4%, or more, difference is also recommended.

Related Data Sheet Sections: Charging Faults, Battery Charging Algorithm, HW Config: V_{BAT} in Stage 2 (V_{S2}), Configure Temp. Compensation

CFG_S0_UV

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	MIN VALUE	MAX VALUE	DESCRIPTION
0x3D	[7:0]	200 • (% of V_{S2})	Unsigned Integer	30% = 0x3C 55.5% = 0x6F	0% = 0x00	90% = 0xB4	Configure V_{S0_UV} voltage as percentage of V_{S2}. Resolution of 0.5% per bit.

I²C REGISTER DESCRIPTIONS

This register is used to set V_{S0_UV}, the falling V_{BAT} threshold to exit Stage 0 charging and enter the low V_{BAT} fault condition. V_{S0_UV} is a percentage of the Stage 2 voltage V_{S2}. Therefore, if Stage 2 temperature compensation is enabled, via the CFG_CHRG_MISC→TC_ENABLE bit, V_{S0_UV} will vary with temperature in proportion to V_{S2}.

CFG_S0_UV is an 8-bit unsigned integer, representing a percentage of V_{S2} between 0% to 90% and is calculated as follows:

$$CFG_S0_UV = 200 \bullet \left[\frac{V_{S0_UV}}{V_{S2}} \bullet 100\% \right]$$

Example: Presume that V_{S2} is set to 14.2V and we wish to configure V_{S0_UV} = 7.1V. Set CFG_S0_UV as follows:

$$CFG_S0_UV = 200 \bullet \left[\frac{7.1V}{14.2V} \bullet 100\% \right]$$
$$= 200 \bullet [50\%]$$
$$= 100 \text{ (decimal)}$$
$$= 0x64 \text{ (hexadecimal)}$$

Therefore, writing CFG_S0_UV to 0x64 configures V_{S0_UV} to be 50% of V_{S2}. Be sure to set CFG_S0_UV to a lower V_{S2} percentage than CFG_UV_S0 to achieve threshold hysteresis and avoid oscillating between stages. A 4%, or more, difference is recommended

Note: CFG_UV_S0 and CFG_S0_UV allow the charger to start even if there is a battery protection circuit in between the V_{BAT} terminal and the battery. Setting both registers to 0x00 ensures that the charger can start and will not enter fault, even if the initial V_{BAT} voltage is 0.

Related Data Sheet Sections: Charging Faults, Battery Charging Algorithm, HW Config: V_{BAT} in Stage 2 (V_{S2}), Configure Temp. Compensation

CFG_S0_S1

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	MIN VALUE	MAX VALUE	DESCRIPTION
0x3E	[7:0]	200 • (% of V_{S2})	Unsigned Integer	70% = 0x8C 55.5% = 0x6F	0% = 0x00	90% = 0xB4	Configure V_{S0_S1} voltage as percentage of V_{S2}. Precision of 0.5% per bit.

This register is used to set V_{S0_S1}, the rising V_{BAT} threshold to exit Stage 0 trickle charging and enter Stage 1 constant-current charging. V_{S0_S1} is a percentage of the Stage 2 voltage V_{S2}. Therefore, if Stage 2 temperature compensation is enabled, via the CFG_CHRG_MISC→TC_ENABLE bit, V_{S0_S1} will vary with temperature in proportion to V_{S2}.

CFG_S0_S1 is an 8-bit unsigned integer, representing a percentage of V_{S2} between 0% - 90% and is calculated as follows:

$$CFG_S0_S1 = 200 \bullet \left[\frac{V_{S0_S1}}{V_{S2}} \bullet 100\% \right]$$

I²C REGISTER DESCRIPTIONS

Example: Presume that V_{S2} is set to 14.2V and we wish to configure V_{S0_S1} = 9.94V. Set CFG_S0_S1 as follows:

$$CFG_S0_S1 = 200 \bullet \left[\frac{9.94V}{14.2V} \bullet 100\% \right]$$
$$= 200 \bullet [70\%]$$
$$= 140 \text{ (decimal)}$$
$$= 0x8C \text{ (hexadecimal)}$$

Therefore, writing CFG_S0_S1 to 0x8C configures V_{S0_S1} to be 70% of V_{S2}. Be sure to set CFG_S0_S1 to a higher V_{S2} percentage than CFG_S1_S0 to achieve threshold hysteresis and avoid stage selection oscillations. A 4%, or more, difference is recommended.

Related Data Sheet Sections: Battery Charging Algorithm, HW Config: V_{BAT} in Stage 2 (V_{S2}), Configure Temp. Compensation

CFG_S1_S0

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	MIN VALUE	MAX VALUE	DESCRIPTION
0x3F	[7:0]	200 • (% of VS2)	Unsigned Integer	66% = 0x84 55.5% = 0x6F	0% = 0x00	90% = 0xB4	Configure V_{S1_S0} threshold as percentage of V_{S2}. Resolution of 0.5% per bit.

This register is used to set V_{S1_S0}, the falling V_{BAT} threshold to exit Stage 1 charging and return to Stage 0 trickle charging. V_{S1_S0} is a percentage of the Stage 2 voltage V_{S2}. Therefore, if Stage 2 temperature compensation is enabled, via the CFG_CHRG_MISC→TC_ENABLE bit, V_{S1_S0} will vary with temperature in proportion to V_{S2}.

CFG_S1_S0 is an 8-bit unsigned integer, representing a percentage of V_{S2} between 0% to 90% and is calculated as follows:

$$CFG_S1_S0 = 200 \bullet \left[\frac{V_{S1_S0}}{V_{S2}} \bullet 100\% \right]$$

Example: Presume that V_{S2} is set to 14.2V and we wish to configure V_{S1_S0} = 9.39V. Set CFG_S1_S0 as follows:

$$CFG_S1_S0 = 200 \bullet \left[\frac{9.39V}{14.2V} \bullet 100\% \right]$$
$$= 200 \bullet [66\%]$$
$$= 132 \text{ (decimal)}$$
$$= 0x84 \text{ (hexadecimal)}$$

Therefore, writing CFG_S1_S0 to 0x84 configures V_{S1_S0} to be 66% of V_{S2}. Make sure to set CFG_S1_S0 to a lower V_{S2} percentage than CFG_S0_S1 to achieve threshold hysteresis and avoid stage selection oscillations. A 4%, or more, difference is recommended. Also, be sure to set CFG_S1_S0 to higher V_{S2} percentage than CFG_UV_S0 threshold to avoid stage selection oscillations. A 4%, or more, difference is also recommended.

Note: If V_{BAT} falls below the V_{S1_S0} threshold while in Stage 2 or Stage 3, the charging algorithm will reset.

Related Data Sheet Sections: Battery Charging Algorithm, HW Config: V_{BAT} in Stage 2 (V_{S2}), Configure Temp. Compensation

I²C REGISTER DESCRIPTIONS

CONFIGURE TEMPERATURE FAULT LIMITS

The following two registers set the battery temperature operating range by setting the upper and lower temperature fault limits. The register values are stored in °C as two's complement, signed integers.

Table 15. Summary of Battery Temperature Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_TBAT_MIN	BYTE	0x40	0xA0	Configures battery low temperature fault limit threshold.	50
CFG_TBAT_MAX	BYTE	0x41	0xA1	Configures battery high temperature fault limit threshold.	50

CFG_TBAT_MIN

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x40	[7:0]	°C	Signed Integer	0°C = 0x00 –20°C = 0xEC	Configures battery low temperature fault limit.

This register sets the battery low temperature limit. If the temperature measured at the TEMPSENSE pin is equal to or less than the limit set, a low temperature fault will occur (STAT_CHRG_FAULTS→LOW_TBAT_FAULT=1). To clear a low temperature fault, the temperature must rise approximately 5°C above the battery low temperature limit (5°C of hysteresis). If the fault properly clears, it will be indicated by STAT_CHRG_FAULTS→LOW_TBAT_FAULT=0. For normal operation, CFG_TBAT_MIN must be lower than CFG_TBAT_MAX.

Temperature measurement accuracy at the TEMPSENSE pin is decreased for temperatures below –40°C. If colder battery charging is desired then consider setting CFG_TBAT_MIN to –128 (signed integer) to disable the minimum temperature fault limit.

Related Data Sheet Section: Charging Faults, HW Config: Battery Temperature and Disconnect Sensing, TELE_TBAT, Configure Automatic Restart

CFG_TBAT_MAX

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x41	[7:0]	°C	Signed Integer	0°C = 0x00 35°C = 0x23	Configures battery high temperature fault limit.

This register sets the battery high temperature limit. If the temperature measured at the TEMPSENSE pin is equal to or greater than the limit set, a high temperature fault will occur (STAT_CHRG_FAULTS→HIGH_TBAT_FAULT=1). To clear a high temperature fault, the temperature must fall approximately 5°C below the battery high temperature limit (5°C of hysteresis). If the fault properly clears, it will be indicated by STAT_CHRG_FAULTS→HIGH_TBAT_FAULT=0. For normal operation, CFG_TBAT_MAX must be higher than CFG_TBAT_MIN.

Temperature measurement accuracy at the TEMPSENSE pin is decreased for temperatures above 60°C. If hotter battery charging is desired then consider setting CFG_TBAT_MAX to 127(signed integer) to disable the maximum temperature fault limit.

Related Data Sheet Section: Charging Faults, HW Config: Battery Temperature and Disconnect Sensing, TELE_TBAT, Configure Automatic Restart

I²C REGISTER DESCRIPTIONS

CONFIGURE STAGE TIMEOUT LIMITS

In power supply mode the user can set finite charging time limits for each stage separately by properly configuring the following register values. Charging time limits are not recommended for use when a load is present on the battery due to the unpredictable amount of time required to achieve full charge. If stage timers are not required, then writing 0x00 to the appropriate registers disables them, allowing the charging to run indefinitely in lieu of any fault conditions.

Charging time limits are disabled when solar powered. In this case, any finite time limit setting of these registers is interpreted as an infinite time limit.

Table 16. Summary of Stage 0 to 3 Timer Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_TMR_S0	BYTE	0x42	0xA2	Configures Stage 0 charging time limit for power supply mode.	51
CFG_TMR_S1	BYTE	0x43	0xA3	Configures Stage 1 charging time limit for power supply mode.	51
CFG_TMR_S2	BYTE	0x44	0xA4	Configures Stage 2 charging time limit for power supply mode.	51
CFG_TMR_S3	BYTE	0x45	0xA5	Configures Stage 3 charging time limit for power supply mode.	51

CFG_TMR_S0

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x42	[7:0]	Minutes	Unsigned Integer	22 Min = 0x05 63 Min = 0x0E	Configures Stage 0 charging time limit. 4.47 minutes per bit. Value of 0x00 disables timer.

CFG_TMR_S1

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x43	[7:0]	Minutes	Unsigned Integer	179 Min = 0x28 10 Hrs. = 0x86	Configures Stage 1 charging time limit. 4.47 minutes per bit. Value of 0x00 disables timer.

CFG_TMR_S2

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x44	[7:0]	Minutes	Unsigned Integer	22 Min = 0x05 63 Min = 0x0E	Configures Stage 2 charging time limit. 4.47 minutes per bit. Value of 0x00 disables timer.

CFG_TMR_S3

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x45	[7:0]	Minutes	Unsigned Integer	179 Min = 0x28 10 Hrs. = 0x86	Configures Stage 3 charging time limit. 4.47 minutes per bit. Value of 0x00 disables timer.

Related Data Sheet Section: STAT_TSx_REMAIN, Battery Charging Algorithm, Configure Automatic Restart.

I²C REGISTER DESCRIPTIONS

CONFIGURE AUTOMATIC RESTART

The following registers in Table 17 configure some of the conditions under which the charging will automatically restart or resume after stopping. The LT8491 employs many features and checks that may cause the charger to stop until more favorable operating conditions return. Upon automatic restart, all timers are reset except when resuming from a battery temperature fault.

Table 17. Summary of Automatic Restart Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_RSTRT_IN_FLT	BYTE	0x46	0xA6	Configures the fault condition automatic charger restart settings.	52
CFG_RSTRT_IN_DONEA	BYTE	0x47	0xA7	Configures the done charging automatic charger restart settings.	54
CFG_RSTRT_IN_DONEB	BYTE	0x48	0xA8	Configures the done charging automatic charger restart settings.	55
CFG_RSTRT_IN_S3	BYTE	0x49	0xA9	Configures the automatic charger restart settings when in Stage 3.	55

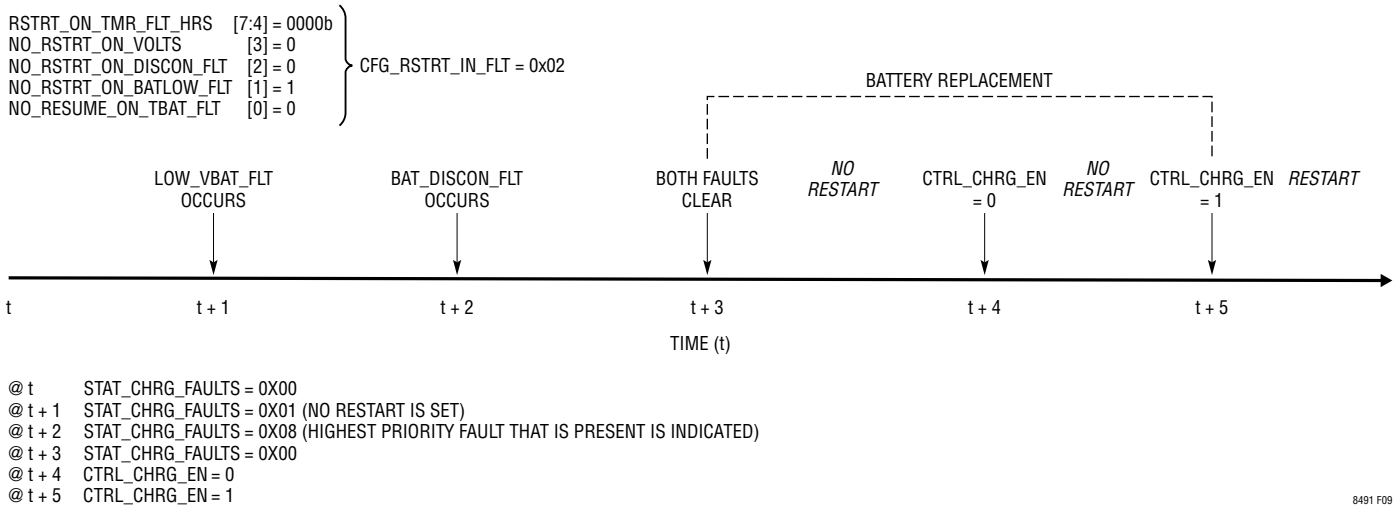
CFG_RSTRT_IN_FLT

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x46	RSTRT_ON_TMR_FLT_HRS	[7:4]	After a timer fault occurs (TSx_EXPIRED_FLT=1) the charger will wait for the time specified here and then restart charging in Stage 0. This restart delay can be set from 0.5 to 7.5 hours in ½ hour steps. Setting these bits to all-zeros disables this automatic restart function. The detection of a fault that also has its respective NO_RSTRT or NO_RESUME configuration set (see bits below) takes priority over this restart setting and prevents the automatic restart from subsequently occurring. Example: 0100b = 2-hour restart delay.
	NO_RSTRT_ON_VOLTS	[3]	If 0 then restart the charging automatically when any of the following occur: • Stage 2 timer fault occurred (TS2_EXPIRED_FLT=1) and $V_{BAT} \le V_{S1_S0}$ • Stage 1 timer fault occurred (TS1_EXPIRED_FLT=1) and (V_{BAT} rises 5% or V_{BAT} rises to 98% of V_{S2}) • Stage 0 timer fault occurred (TS0_EXPIRED_FLT=1) and $V_{BAT} \ge V_{S0_S1}$ If 1 then don't automatically restart due to any of these conditions.
	NO_RSTRT_ON_DISCON_FLT	[2]	If 1 and a battery disconnect fault is detected, then stop charging and don't allow charging to automatically restart. Restarting the charger, after a battery disconnect fault will require that the charging logic is cycled off-then-on via the CTRL_CHRG_EN register.
	NO_RSTRT_ON_BATLOW_FLT	[1]	If 1 and a low V_{BAT} fault is detected, then stop charging and don't allow charging to automatically restart. Restarting the charger, after a low V_{BAT} fault will require that the charging logic is cycled off-then-on via the CTRL_CHRG_EN register.
	NO_RESUME_ON_TBAT_FLT	[0]	If 1 and a battery temperature fault is detected, then stop charging and don't allow charging to automatically resume. Charging can only restart after a battery temperature fault, by cycling the charging control logic off-then-on via the CTRL_CHRG_EN register.

I²C REGISTER DESCRIPTIONS

A specific use case for the CFG_RSTRT_IN_FLT register is when a dead battery needs to be replaced. The user may want the charger to remain off until the battery is exchanged. A voltage measurement might be required prior to starting the charger. Once the battery is verified, CTRL_CHRG_EN can be used to start the charging logic. Figure 9 shows a sample setup for the CFG_RSTRT_IN_FLT register. The scenario displays what happens when the LT8491 is configured to not restart when a low battery fault is detected. In time, the LT8491 first detects a LOW_VBAT_FLT, followed by a BAT_DISCON_FLT due to the dead battery being disconnected from the charger. The fault indication is priority based but the restart condition behaves unconditionally from the prioritized fault indication.

Related Data Sheet Sections: Charging Faults, Battery Charging Algorithm, CFG_TERMINATE, Configure Stage Timeout Limits



@ t STAT_CHRG_FAULTS = 0X00
@ t + 1 STAT_CHRG_FAULTS = 0X01 (NO RESTART IS SET)
@ t + 2 STAT_CHRG_FAULTS = 0X08 (HIGHEST PRIORITY FAULT THAT IS PRESENT IS INDICATED)
@ t + 3 STAT_CHRG_FAULTS = 0X00
@ t + 4 CTRL_CHRG_EN = 0
@ t + 5 CTRL_CHRG_EN = 1

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Figure 9. No Restart Condition Example

I²C REGISTER DESCRIPTIONS

CFG_RSTRT_IN_DONEA

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x47	RSTRT_IN_DONE_ON_VOLTS	[7]	Setting this bit causes the battery charging to automatically restart, if in the done charging stage, when the V_{BAT} voltage is detected to be below the voltage configured in the RSTRT_IN_DONE_SET_VOLTS bits. See Figure 8.
	RSTRT_IN_DONE_SET_VOLTS	[6:0]	Configure V_{DONE_RSTRT} voltage as percentage of V_{S2}. Maximum value is 99% or 0x8C, with a resolution of 1% per bit.

The RSTRT_IN_DONE_SET_VOLTS bits set V_{DONE_RSTRT}, the falling V_{BAT} voltage that causes an automatic charging restart when in the done charging stage. The done charging stage is indicated in the STAT_CHARGER register when the CHRG_STAGE bits are 100b and the CHRG_LOGIC_ON bit is 1. V_{DONE_RSTRT} is a percentage of the Stage 2 voltage V_{S2}. Therefore, if Stage 2 temperature compensation is enabled, via the CFG_CHRG_MISC→TC_ENABLE bit, V_{DONE_RSTRT} will vary with temperature in proportion to V_{S2}.

RSTRT_IN_DONE_SET_VOLTS is a 7-bit unsigned integer, representing a percentage of V_{S2} between 0% to 99% and is calculated as follows:

$$RSTRT_IN_DONE_SET_VOLTS = 100 \bullet \left[\frac{V_{DONE_RSTRT}}{V_{S2}} \bullet 100\% \right]$$

Example: Presume that V_{S2} is set to 14.2V and we wish to configure V_{DONE_RSTRT} = 12.07V. Set RSTRT_IN_DONE_SET_VOLTS as follows:

$$RSTRT_IN_DONE_SET_VOLTS = 100 \bullet \left[\frac{12.07V}{14.2V} \bullet 100\% \right]$$
$$= 100 \bullet [85\%]$$
$$= 85 \text{ (decimal)}$$
$$= 0x55 \text{ (hexadecimal)}$$

Therefore, writing RSTRT_IN_DONE_SET_VOLTS to 0x55 configures V_{DONE_RSTRT} to be 85% of V_{S2}. Be sure to always set RSTRT_IN_DONE_SET_VOLTS lower than V_{S3} over all T_{BAT} conditions if Stage 3 charging is configured. Also, to avoid STAT_CHRG_FAULTS→LOW_VBAT_FLT from being triggered, it's recommended to set RSTRT_IN_DONE_SET_VOLTS higher than the CFG_S0_UV threshold over all T_{BAT} conditions. A 4%, or more, difference is recommended.

Related Data Sheet Sections: Battery Charging Algorithm, Done Charging

I²C REGISTER DESCRIPTIONS

CFG_RSTRT_IN_DONEB

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x48	Reserved	[7:6]	Reserved
	RSTRT_IN_DONE_HRS	[5:0]	By setting these bits to a non-zero value, the charger will wait for a delay time after reaching the done charging stage (see Figure 8), then automatically restart the charging in Stage 0. These bits set the delay in ½ hour steps between 0.5 to 31.5 hours. Setting these bits to all-zeros disables this automatic restart function. Example: 000100b = 2-hour automatic restart delay.

CFG_RSTRT_IN_S3

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x49	Reserved	[7:1]	Reserved
	RSTRT_S3_C5_VS3	[0]	Setting this bit causes the charging to restart when in Stage 3 and (1) I_{OUT} exceeds C/5 or (2) V_{BAT} falls below 96% of the V_{S3} voltage threshold set in register CFG_VS3_25C.

Related Data Sheet Section: Battery Charging Algorithm, Configure Automatic Restart, Configure V_{BAT} for Stages 0, 1 and 3

CONFIGURE CHARGE TERMINATION

CFG_TERMINATE

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x4A	Reserved	[7:6]	Reserved
	PS_S2_C10_TERM_EN	[5]	*DC Power Supply Powered, Stage 2, C/10 Termination Enable:* Setting this bit to 1 causes the charging to terminate when the I_{OUT} current falls below C/10 in Stage 2 while powered by a DC power supply. Upon termination, the charging will stop, and the charger will proceed to the Done Charging state as described in the Battery Charging Algorithm section. If the CFG_CHRG_MISC→PS_S3_ENABLE bit is also set, then the charging will instead proceed to Stage 3 rather than terminating.
	SOLAR_S2_C10_TERM_EN	[4]	*Solar Powered, Stage 2, C/10 Termination Enable:* Setting this bit to 1 causes the charger to terminate charging when the I_{OUT} current falls below C/10 in Stage 2 while powered by a solar panel. Upon termination, the charging will stop, and the charger will proceed to the Done Charging state as described in the Battery Charging Algorithm Section. Refer to the HW Config: Solar Panel Powered Charging section for additional information about C/10 termination when powered by a solar panel. If the CFG_CHRG_MISC→SOLAR_S3_ENABLE bit is set, then the charging will instead proceed to Stage 3 rather than terminating.
0x4A	S3_TMR_TERM_EN	[3]	*Stage Timer Termination Enable:* Setting the respective bit to 1 causes the charging to terminate, without activating a fault flag, when the respective stage timer expires while charging in that stage. Upon termination, the charging will stop, and the charger will proceed to the Done Charging state as described in the Battery Charging Algorithm Section. A 0 setting causes the expiration of the timer to be treated as a fault condition. Note that timers and timer termination are automatically deactivated when powered by a solar panel.
	S2_TMR_TERM_EN	[2]	
	S1_TMR_TERM_EN	[1]	
	S0_TMR_TERM_EN	[0]	

Related Data Sheet Sections: Battery Charging Algorithm, HW Config: Solar Panel Powered Charging, HW Config: DC Supply Powered Charging, Configure Stage Timeout Limits

I²C REGISTER DESCRIPTIONS

CONFIGURE MISC.

Table 18. Summary of Miscellaneous Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_SCAN_RATE_LP	BYTE	0x4B	0xAB	Configures timed full panel scan frequency in solar low power mode.	56
CFG_SCAN_RATE	BYTE	0x4C	0xAC	Configures timed full panel scan frequency when solar powered.	56
CFG_CHRG_MISC	BYTE	0x4D	0xAD	Configure Use V_{S3} in Stage 2, Low Power Mode, Stage 3 and Temperature Compensation.	57

CFG_SCAN_RATE_LP

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x4B	[7:0]	Seconds	Unsigned Integer	183 sec = 0x0B 20 min = 0x48	Configures timed full panel scan period in solar low power mode. 16.66 seconds per bit.

This register sets the timed full panel scan period in solar low power mode. For example, a value of 0x0B causes a full panel scan to be performed every 183 seconds. If not solar powered, this register setting is ignored, and no full scans are performed. Note that performing full panel scans at short intervals can disrupt the charger output power and efficiency.

A value of 0x00 disables full panel scans in low power mode. The charger will still perform a full panel scan during startup and between certain stage transitions as part of the proprietary algorithm for identifying the maximum power point.

Related Data Sheet Section: HW Config: Solar Panel Powered Charging, Maximum Power Point Tracking, Optional: Low Power Mode

CFG_SCAN_RATE

I²C REG ADDRESS	BIT(S)	UNITS	FORMAT	EXAMPLES	DESCRIPTION
0x4C	[7:0]	Seconds	Unsigned Integer	183 sec = 0x0B 20 min = 0x48	Configures timed full panel scan period when solar powered. 16.66 seconds per bit.

This register sets the timed full panel scan period. For example, a value of 0x48 causes a full panel scan to be performed every 20 minutes. If not solar powered, this register setting is ignored, and no full scans are performed. Note that performing full panel scans at short intervals can disrupt the charger output power and efficiency.

A value of 0x00 disables most full panel scans. The charger will still perform a full panel scan during startup and between certain stage transitions as part of the proprietary algorithm for identifying the maximum power point.

Related Data Sheet Section: HW Config: Solar Panel Powered Charging, Maximum Power Point Tracking, Optional: Low Power Mode

I²C REGISTER DESCRIPTIONS

CFG_CHRG_MISC

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x4D	Reserved	[7:5]	Reserved
	USE_VS3_IN_STAGE2	[4]	Reduces the Stage 2 battery charging voltage to the value set in CFG_VS3_25C. See below for details.
	LPMODE_EN	[3]	Setting this bit enables low power mode as discussed in the Optional: Low Power Mode section.
	PS_S3_ENABLE	[2]	When powered by a DC power supply, 1 permits the use of Stage 3 charging and 0 disables the use of Stage 3. See HW Config: Solar Panel Powered Charging and Battery Charging Algorithm for more information.
	SOLAR_S3_ENABLE	[1]	When powered by a solar panel, 1 permits the use of Stage 3 charging and 0 disables the use of Stage 3. See HW Config: DC Supply Powered Charging and Battery Charging Algorithm for more information.
	TC_ENABLE	[0]	Set to 1 to enable temperature compensation of V_{S2} and V_{S3}. See Configure Temperature Compensation section.

BIT[4] – USE_VS3_IN_STAGE2: Setting this bit allows for reduced voltage battery charging in Stage 2. It can be used, for example, for in-situ lead-acid battery charging when the battery load current exceeds C/10 (see the In-Situ Battery Charging section). In this case the charger is unable to proceed to Stage 3 because the charger output current does not drop below C/10 and maintaining V_{S2} voltage on the battery may be undesirable.

Setting USE_VS3_IN_STAGE2 effects the charger as follows:

- In Stage 2 the battery will charge to a maximum voltage of V_{S3} instead of V_{S2}. V_{S3} is configured in the following registers: CFG_VS3_25C, CFG_TC3, CFG_TC2, CFG_TC1 and the TC_ENABLE bit (listed above).
- The V_{BAT} stage voltage thresholds V_{UV_S0}, V_{S0_UV}, V_{S0_S1}, V_{S1_S0} remain unaffected by this bit setting (see Battery Charging Algorithm and Configure V_{BAT} for Stages 0, 1 and 3).
- The transition from Stage 1 to Stage 2 will occur when V_{BAT} rises to 98% of V_{S3} instead of 98% of V_{S2}.
- The transition from Stage 2 to Stage 1 will occur when V_{BAT} falls to 95% of V_{S3} instead of 95% of V_{S2}.

See Figure 7 and Figure 8 for additional detail.

When setting this bit, it is also recommended to:

- Disable Stage 3 charging by setting PS_S3_ENABLE and SOLAR_S3_ENABLE to 0 in the CFG_CHRG_MISC register. Stage 3 charging can be re-enabled when USE_VS3_IN_STAGE2 is cleared.
- Consider disabling the C/10 charger termination in Stage 2 by clearing the PS_S2_C10_TERM_EN and SOLAR_S2_C10_TERM_EN bits in the CFG_TERMINATE register.

I²C REGISTER DESCRIPTIONS

CONFIGURE TEMPERATURE COMPENSATION

Table 19. Summary of Temperature Compensation Configuration Registers

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_CHRG_MISC	BYTE	0x4D	0xAD	Contains bit to enable temperature compensation.	57
CFG_TC3	LONG-WORD	0x4E	0xAE	3rd order coefficient for Stage 2 and 3 temperature compensation.	59
CFG_TC2	LONG-WORD	0x52	0xB2	2nd order coefficient for Stage 2 and 3 temperature compensation.	
CFG_TC1	LONG-WORD	0x56	0xB6	1st order coefficient for Stage 2 and 3 temperature compensation.	

Some battery chemistries charge best when the charging voltages are adjusted with battery temperature (T_{BAT}). Lead-acid batteries experience a significant change in their ideal charging voltage as temperature changes. The LT8491 can automatically adjust the V_{S2} and V_{S3} voltages when a temperature sensing thermistor is coupled to the battery. The temperature compensation is enabled in the CFG_CHRG_MISC register. See the HW Config: Battery Temperature and Disconnect Sensing section for more information about the thermistor connection.

When Stage 2 temperature compensation is enabled (CFG_CHRG_MISC→TC_ENABLE bit=1), the PWM duty cycle of the FBOW pin is automatically adjusted with temperature. This adjusts V_{S2} as T_{BAT} changes. This also changes all the V_{BAT} stage voltages listed in the Configure V_{BAT} for Stages 0, 1 and 3 section, since they are all percentages of V_{S2}.

V_{S2} is automatically adjusted with temperature as follows:

$$V_{S2}(T_{BAT}) = V_{S2}(25°C) \bullet TFACTOR(T_{BAT})$$

$$V_{S3}(T_{BAT}) = V_{S3}(25°C) \bullet TFACTOR(T_{BAT})$$

Where:

$V_{S2}(25°C)$ = Stage 2 V_{BAT} at 25°C (see HW Config: V_{BAT} in Stage 2 (V_{S2}) section)

$V_{S3}(25°C)$ = Stage 3 V_{BAT} at 25°C (see Configure V_{BAT} for Stages 0, 1, and 3)

$TFACTOR(T_{BAT}) = (1 + \Delta T \bullet TC1 + \Delta T^2 \bullet TC2 + \Delta T^3 \bullet TC3)$

$\Delta T = (T_{BAT}$ in °C) – 25°C

Using the default TCx coefficients, listed in the I²C Register Map, V_{S2} and V_{S3} adjust with T_{BAT} as shown:

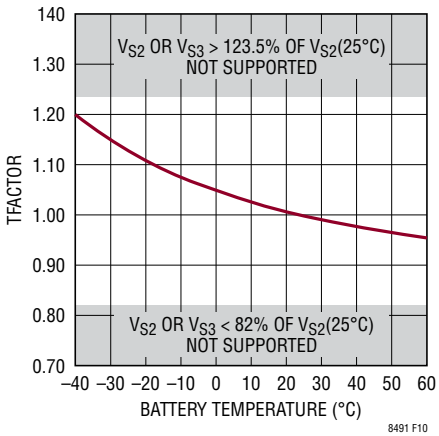

Figure 10. Default Battery Voltage Temperature Compensation in Stage 2

I²C REGISTER DESCRIPTIONS

The curve in Figure 10 can be modified via the CFG_TCx registers if needed. Note that hardware limitations restrict $V_{S2}(T_{BAT})$ and $V_{S3}(T_{BAT})$ to the range of approximately 82% to 123.5% of $V_{S2}(25°C)$.

For proper charger operation, V_{S3} must always be set lower than V_{S2}.

CFG_TC3, CFG_TC2, CFG_TC1

I²C REG ADDRESS	REGISTER NAME	BIT(S)	FORMAT	EXAMPLES	DESCRIPTION
0x4E	CFG_TC3	[31:0]	Single Precision Float	–1.49e-7 = 0xB41FFCCF	The TC3 temperature coefficient.
0x52	CFG_TC2	[31:0]		1.34e-5 = 0x3760D090	The TC2 temperature coefficient.
0x56	CFG_TC1	[31:0]		–1.54e-3 = 0xBAC9D9D3	The TC1 temperature coefficient.

These registers set the battery voltage temperature compensation for Stage 2 and Stage 3. These values are only used when charging in Stage 2 or 3 and when CFG_CHRG_MISC→TC_ENABLE=1. Equations describing the use of these values are described in the prior section.

CONFIGURE USER CODE

Table 20. User Code Register

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	I²C BOOT READ ADDRESS	DESCRIPTION	REF PAGE
CFG_USER_CODE	WORD	0x5A	0xBA	2 bytes of user information.	59

CFG_USER_CODE

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x5A	USER_INPUT_DATA	[15:0]	2 bytes for user information.

These two bytes can be used to store any desired data from the user such as revision, lot, assembly, or other information. This data is not used for any function by the LT8491.

I²C REGISTER DESCRIPTIONS

MANUFACTURER DATA

Table 21. Manufacturer CRC

REGISTER NAME	SIZE	I²C REGISTER ADDRESS	DESCRIPTION	REF PAGE
MFR_DATA1	WORD	0x5C	Manufacturer data.	60
MFR_DATA2	WORD	0x5E	Manufacturer data.	60
MFR_DATA3	WORD	0X60	Manufacturer data.	60

MFR_DATA1

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x5C	-	[15:0]	Manufacturer data.

MFR_DATA2

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x5E	-	[15:0]	Manufacturer data.

MFR_DATA3

I²C REGISTER ADDRESS	BIT NAME	BIT(S)	DESCRIPTION
0x60	-	[15:0]	Manufacturer data.

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HARDWARE CONFIGURATION

HW Config: Input Voltage Sensing and Modulation

The passive component network shown in Figure 11 is required to modulate the solar panel voltage. It is also used to measure the V_{IN} voltage when powered by a DC power supply. This network is required whether the supply is a solar panel or a DC voltage source.

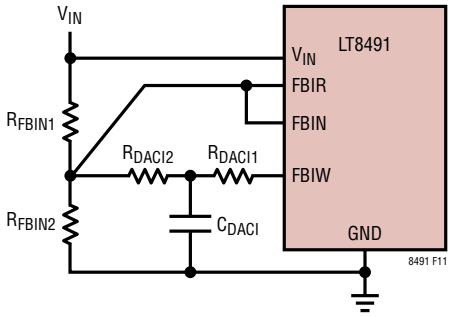

Figure 11. Input Feedback Resistor Network

Choosing the component values requires knowing the maximum panel open-circuit voltage (V_{OCMAX}) as well as the maximum DC input supply voltage (V_{DCMAX}) desired (see the HW Config: DC Supply Powered Charging section). V_{OCMAX} typically occurs at cold temperatures and should be specified in the panel manufacturer's data sheet. Use the following equations to determine the proper component values:

$$R_{FBIN1} = 100k \bullet \left[\frac{1+\left(\frac{4.470V}{V_{MAX}-6V}\right)}{1+\left(\frac{5.593}{V_{MAX}-6V}\right)} \right] \Omega$$

$$R_{DACI2} = 2.75 \bullet \left(\frac{R_{FBIN1}}{V_{MAX}-6V} \right) \Omega$$

$$R_{FBIN2} = \frac{1}{\left(\frac{1}{100k - R_{FBIN1}}\right) - \left(\frac{1}{R_{DACI2}}\right)} \Omega$$

$$R_{DACI1} = 0.2 \bullet R_{DACI2} \Omega$$

$$C_{DACI} = \frac{1}{1000 \bullet R_{DACI1}} F$$

where V_{MAX} is the greater of V_{OCMAX} and V_{DCMAX} with some additional margin. The resistors should have a 1% tolerance or better.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to match the calculated results. Otherwise, use standard resistor values and check the final component selections with the following equations.

$$V_{X2} = 1.205 \bullet \left[\frac{R_{FBIN1}}{R_{DACI1}+R_{DACI2}} + \left(\frac{R_{FBIN1}}{R_{FBIN2}} \right) + 1 \right]$$

V_{X2} indicates the actual V_{MAX} resulting from the use of the selected resistors. Make sure this result is greater than or equal to the desired V_{MAX} for the application.

$$V_{X1} = V_{X2} - 3.3 \bullet \left(\frac{R_{FBIN1}}{R_{DAC1}+R_{DAC2}} \right)$$

V_{X1} should be as close to 6V as possible. Iterations may be required to determine the best standard resistor values.

Table 22 shows good sets of standard value components for maximum input voltages (V_{MAX}) of 20V, 40V, 60V and 80V. Iterative calculations were required to select these values that achieve the best overall results.

Table 22. Input Feedback Network vs V_{MAX}

V_{MAX} (V)	R_{FBIN1} (kΩ)	R_{FBIN2} (kΩ)	R_{DACI1} (kΩ)	R_{DACI2} (kΩ)	C_{DACI} (nF)
20	95.3	8.45	3.4	19.1	270
40	107	4.87	1.69	8.66	560
60	105	3.24	1.05	5.36	1000
80	133	3.09	1.05	4.87	1000

As discussed later in HW Config: DC Supply Powered Charging, arbitrarily setting V_{MAX} to 80V may not result in the best operation of the LT8491 for all conditions, particularly at low input voltages. Be sure to consider the required voltage range for each application.

HW Config: VINR Pin Connections

The VINR pin is used for two functions. First, while the LT8491 is powered by a solar panel, the VINR pin is

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measured to determine the absolute panel voltage and check for under voltage conditions. As such, VINR must be connected to the resistor divider network shown in Figure 12. These resistors should have a 1% tolerance or better.

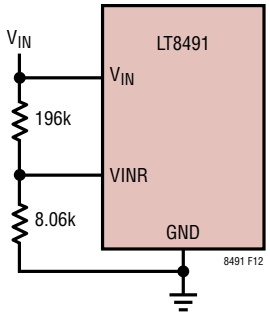

Figure 12. VINR Resistor Divider Circuit

Second, the LT8491 enters power supply mode when VINR is pulled low (<174mV typical). Power supply mode disables unnecessary solar panel functions and allows the LT8491 to operate properly from a DC voltage source. The activation of power supply mode is indicated in the STAT_SUPPLY and TELE_VINR registers.

If the charger is only going to be powered by a DC voltage source, then the VINR pin can be grounded. If the charger will only be powered by a solar panel, then connect VINR as shown in Figure 12. If both supply methods may be used, then see the Optional: DC Supply Detection Circuit section for a method to pull down the VINR pin when a DC supply is detected.

HW Config: Solar Panel Powered Charging

There are a few special items to consider when the charger is powered by a solar panel as discussed in these subsections below.

VINR Connection: The VINR pin must be connected as shown in Figure 12 when being powered by a solar panel.

Timers Disabled: When powered by a solar panel, the charging timers are disabled. Timer termination and timer faults are also disabled regardless of their configuration settings. See data sheet sections: Configure Stage Timeout Limits and Configure Charge Termination.

Timers are disabled when solar powered due to the inability to guarantee full charging current during the entire charging cycle when panel illumination conditions change. In addition, the timers can reset if all power to the charger is lost due to insufficient lighting. This makes the use of timers potentially unreliable in solar powered applications.

C/10 Detection: When powered by a solar panel, charging current may drop below C/10 either because (1) the battery is approaching full charge or (2) insufficient panel power is available. The LT8491 can determine which condition has caused the current to drop. When configured for a C/10 termination or stage transition (see CFG_TERMINATE and CFG_CHRG_MISC registers) the transition will only occur if C/10 is due to the battery approaching full charge. Otherwise the C/10 or charging termination transition will not occur. See Figure 8 for more information about available C/10 state transitions.

Minimum Panel Voltage: A minimum panel voltage of 6V is required to operate the charger. However higher panel voltages are required in various other cases.

1. LOW POWER MODE ENABLED: Low power mode allows additional power to be recovered from the solar panel under very weak lighting conditions. When low power mode is enabled (CFG_CHRG_MISC→LPMODE_EN=1), the panel voltage must initially exceed 10V (typical – as measured through the VINR pin) before the charger will attempt to charge the battery. Read the Optional: Low Power Mode section for more details.
2. LOW POWER MODE DISABLED: If low power mode is disabled (CFG_CHRG_MISC→LPMODE_EN=0) the charger will attempt to charge the battery if the panel is above 6V. However, if sufficient panel current is not detected, the LT8491 will temporarily stop charging. The charger will check for sufficient panel current at 30 second intervals (typical) or will check sooner if the LT8491 detects a significant rise in panel voltage or a significant fall in battery voltage.
3. LOW INPUT VOLTAGE EFFECTS: Figure 13 shows the minimum input voltage, below which the maximum charging current may be reduced. This limit is a function of the input V_{MAX} as discussed previously in the

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HW Config: Input Voltage Sensing and Modulation section. Maximum charging current can reduce as FBIN gets closer to its regulation voltage of 1.205V (typical). This is not normally a significant issue unless 1) the charger is powered by a low voltage DC power supply or 2) a low voltage panel is used with a charger that is configured for a much higher voltage panel. The farther that V_{IN} is below the Normal Configuration line in Figure 13 the more the current can reduce.

When using a solar panel supply, choose a panel having a maximum open-circuit voltage (V_{OCMAX}) close to V_{MAX} (discussed in the HW Config: Input Voltage Sensing and Modulation section). The maximum power point voltage is typically well above the voltage thresholds in Figure 13 and current limiting is rarely an issue. Avoid using solar panels that operate dramatically below V_{MAX}, particularly if the maximum power point voltage is typically below the Normal Configuration line in Figure 13.

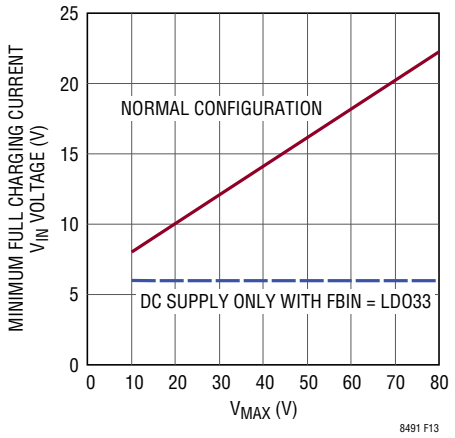

Figure 13. Minimum Full Charging Current V_{IN} Voltage

Input Current Limiting: Review the solar section of the HW Config: Input Current Sense and Limit section.

HW Config: DC Supply Powered Charging

There are a few special items to consider when the charger is powered by a DC power supply as discussed in these subsections below.

Selecting Power Supply Mode: Power supply mode must be enabled when supplying the LT8491 by a DC voltage source. This is done by pulling the VINR pin low, or to ground, as discussed in the HW Config: VINR Pin Connections section. The Optional: DC Supply Detection Section describes a method to pull VINR low automatically when a DC supply is present.

Minimum Input Voltage Requirement: When in power supply mode, the LT8491 will operate from an input as low as 6V. However, charging current capability can become limited at low input voltages depending on the V_{MAX} voltage used when determining the input voltage sensing network resistor values (see previous HW Config: Input Voltage Sensing and Modulation section). Figure 13 shows the minimum input supply voltage required, below which, charging current can drop below the maximum output current limit. If the LT8491 will only be powered by a DC supply, the minimum input voltage shown in Figure 13 can be reduced to 6V by (1) disconnecting FBIN from FBIR and (2) connecting the FBIN pin directly to LDO33.

Input Current Limiting: Input current limiting should be considered when using DC power supplies. This is discussed later in the HW Config: Input Current Sense and Limit section.

HW Config: V_{BAT} in Stage 2 (V_{S2})

The Stage 2 battery voltage (V_{S2}) is the maximum battery charging voltage. The voltage limits for Stages 0, 1 and 3 are configured as percentages of V_{S2} as discussed in the Configure V_{BAT} for Stages 0,1 and 3 section. If temperature compensated charging is enabled, then V_{S2} will change with temperature as discussed in the Configure Temperature Compensation section. As such, the settings for the other stages will also change with temperature in proportion to V_{S2}.

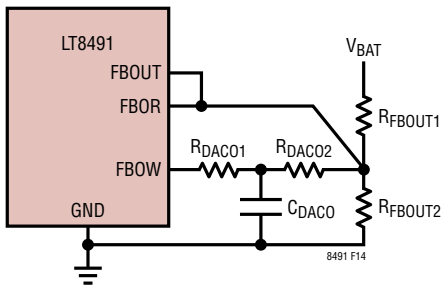

Figure 14. Output Feedback Resistor Network

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Setting the Stage 2 Battery Voltage (V_{S2}): The resistor network shown in Figure 14 is used to set the Stage 2 battery voltage and to measure V_{BAT} via the FBOR pin (see TELE_VBAT register). Battery manufacturers typically call for a higher Stage 2 voltage limit than the nominal battery voltage. For example, a 12V lead-acid battery used in automotive applications commonly has a Stage 2 charging voltage limit of 14.2V. If temperature compensated charging is used (see the Configure Temperature Compensation section) then use the 25˚C value of V_{S2} in the equations below.

R_{FBOUT2} is often selected to be between 4.99kΩ and 49.9kΩ. Choosing higher values for R_{FBOUT2} reduces the amount of current draw from the battery through the feedback network.

$$R_{FBOUT1} = R_{FBOUT2} \bullet \left[V_{S2} \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$R_{DACO2} = \frac{R_{FBOUT1} \bullet R_{FBOUT2} \bullet 0.833}{\left(R_{FBOUT2} \bullet V_{S2} \bullet \frac{1.241}{1.211} \right) - R_{FBOUT2} - R_{FBOUT1}} \Omega$$

$$R_{DACO1} = 0.2 \bullet R_{DACO2} \Omega$$

$$C_{DACO} = \frac{1}{500 \bullet R_{DACO1}} F$$

For greater charging voltage accuracy, it is recommended that 0.1% tolerance resistors are used for the output feedback resistor network.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to match the calculated results. Otherwise, use standard resistor values and check the final results with the following equations:

$$V_{X3} = \left(\frac{R_{FBOUT1}}{R_{DACO1} + R_{DACO2}} \right) \bullet (X - 1.89)$$

where

$$X = 1.211 \bullet \left[1 + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT2}} \right) + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT1}} \right) \right]$$

V_{X3} indicates the actual 25°C V_{S2} voltage using the selected resistors.

$$N1 = \frac{X - 1.89}{X - 3.3}$$

N1 should be as close as possible to 1.22.

$$N2 = 1 - \frac{1.89}{X}$$

N2 should be as close as possible to 0.806. Iterations may be required to determine best standard resistor values.

Table 23 shows good sets of standard value components for charging nominal battery voltages of 12V, 24V, 36V, 48V and 60V. Iterative calculations were performed to select these values that achieve the best overall results.

Table 23. Standard Value Output Feedback Network vs Output Regulation Voltage

BATTERY VOLTAGE	TARGET V_{S2} (V)	R_{FBOUT1} (kΩ)	R_{FBOUT2} (kΩ)	R_{DACO1} (kΩ)	R_{DACO2} (kΩ)	C_{DACO} (nF)
12	14.2	274	23.2	26.1	124	82
24	28.4	487	20	28	107	68
36	42.6	787	21	22.6	121	100
48	56.8	1000	20	22.6	115	100
60	71.0	866	13.7	13.3	80.6	150

HW Config: Input Current Sense and Limit

This section discusses the LT8491's input current sensing and limiting circuit and how to properly configure it.

Solar Panel Supply Considerations: Solar panels are inherently current limited and may not be able to provide maximum power at the lowest input voltages. The LT8491 uses its MPPT algorithm to scan the panel voltage as low as 6V to find the maximum power point. Make sure that the charger's input current limit is set higher than the maximum panel current capability, plus at least 20% to 30% margin, in order to achieve the maximum charging capability of the system.

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In addition, note that the LT8491 uses the same circuit (shown in Figure 15) to measure the input current as to limit it. The input current is measured by an A/D conversion of the IIR pin which is connected to IMON_IN and is proportional to input current. The digitized input current measurement is used to locate the maximum power point of the solar panel. Setting a higher input current limit reduces the resolution of the digitized reading of the input current. Avoid setting the input current limit significantly higher than necessary, as this may affect the accuracy of the maximum power point calculations.

DC Power Supply Considerations: When charging a battery at the maximum charging current limit, and thus power, a low voltage input supply must provide more current than a high voltage input supply. This can be seen by equating output power to input power, less some efficiency loss.

$$V_{IN} \bullet I_{IN} \bullet \eta = V_{BAT} \bullet I_{BAT}$$

or

$$I_{IN(MAX)} = \frac{V_{BAT} \bullet I_{BAT(MAX)}}{V_{IN(MIN)} \bullet \eta}$$

Where the efficiency factor η is typically between 0.95 and 0.99.

When powered by a DC voltage supply, appropriate input current limiting is recommended for supplies that might (1) become overloaded as the supply ramps up or down through 6V or (2) provide more input current than the charger components can tolerate.

Configuring the Input Current Sense and Limit: The input current is sensed through R_{SENSE1} as shown in Figure 15. The current through R_{SENSE1} is converted to a voltage on the IMON_IN pin according to the following equation:

$$V_{IMON_IN} = \left[\left(\frac{I_{IN} \bullet R_{SENSE1}}{1000} + 7\mu A\right) \bullet R_{IMON_IN}\right] V$$

The LT8491 performs an A/D conversion of the IIR pin voltage to report input current telemetry in the TELE_IIN register. IMON_IN voltages exceeding 1.208V (typical) are detected by EA2 and cause the V_C voltage to reduce, thus limiting the input current. R_{IMON_IN} should be 21kΩ ±1% or better. Using this information, the appropriate value for R_{SENSE1} can be calculated using the following equation:

$$R_{SENSE1} = \frac{1000 \bullet \left(\frac{1.208V}{21k\Omega} - 7nA\right)}{I_{IN(MAX)}} = \frac{0.0505}{I_{IN(MAX)}} \Omega$$

where $I_{IN(MAX)}$ is the desired maximum input current limit in Amps. R_{SENSE1} values greater than 25mΩ are not recommended.

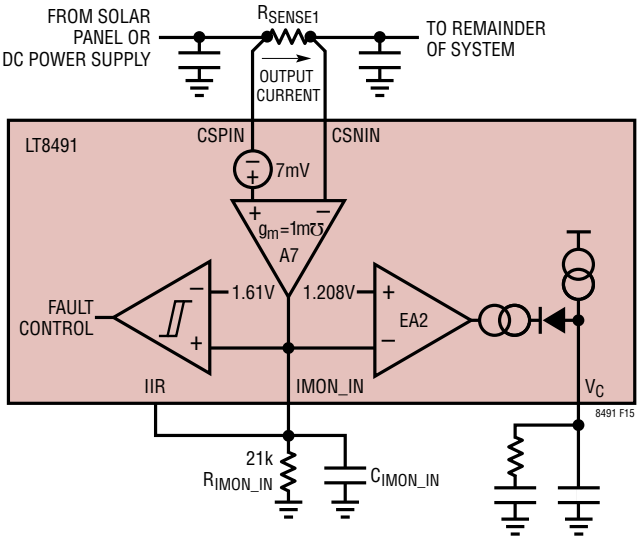

Figure 15. Input Current Regulation Loop

C_{IMON_IN} reduces IMON_IN ripple and stabilizes the input current limit control loop. Reducing C_{IMON_IN} improves stability and minimizes inductor current overshoot. However, this is at the expense of increased IMON_IN ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_IN must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_IN} capacitor of 4.7nF to 22nF is suitable for most applications.

HW Config: Output Current Sense and Limit

The maximum battery charging current, commonly referred to as C, is configured with the output current sensing and limiting circuit. The output current is sensed through R_{SENSE2} and converted to a proportional current flowing out of the IMON_OUT pin (see Figure 16). An A/D measurement of the IOR pin voltage is used to determine

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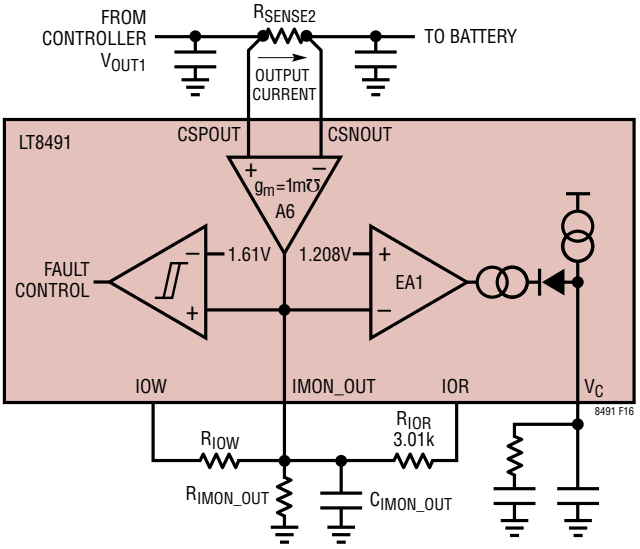

Figure 16. Output Current Regulation Loop

the output current telemetry reported in the TELE_IOUT register. The IOR voltage measurement is also used to determine C/10 for charging state changes and termination as illustrated in Figure 8.

IMON_OUT voltages above 1.208V (typical) cause V_C to reduce due to EA1, and thus limit the output current. The IOW pin is either driven to ground or floated depending on charging conditions. This allows the current limit for Stage 0 ($I_{OUT(MAXS0)}$) to be set independently of the remaining stages ($I_{OUT(MAX)}$) with proper selection of R_{IOW} and R_{IMON_OUT}. Use the following equations to configure the current limits:

$$R_{SENSE2} = \frac{0.0497}{I_{OUT(MAX)}}\Omega$$

$$R_{IMON_OUT} = \frac{1208}{I_{OUT(MAXS0)} \bullet R_{SENSE2}}\Omega$$

$$R_{IOW} = \frac{24.3k \bullet R_{IMON_OUT}}{R_{IMON_OUT} - 24.3k}\Omega$$

$$R_{IOR} = 3.01k$$

$$C_{IMON_OUT} = \text{ read below}$$

where $I_{OUT(MAX)}$ is the maximum charging current (C) in Amps, $I_{OUT(MAXS0)}$ is the maximum trickle charging current in Stage 0 and $I_{OUT(MAXS0)}$ is no greater than $I_{OUT(MAX)}$. For cases where $I_{OUT(MAX)} = I_{OUT(MAXS0)}$ it is OK to exclude R_{IOW} from the PCB and float the IOW pin. $I_{OUT(MAXS0)}$ must be at least 20% of $I_{OUT(MAX)}$.

C_{IMON_OUT} reduces IMON_OUT ripple and stabilizes the constant charging current control loop. Reducing C_{IMON_OUT} improves stability and minimizes inductor current overshoot that can occur if a discharged battery is quickly disconnected then reconnected to the charger. However, this is at the expense of increased IMON_OUT ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_OUT must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_OUT} capacitor in the range of 4.7nF to 22nF is suitable for most applications.

HW Config: Current Sense Filtering

The C_{SX} and R_{SX} current sense filter components shown in Figure 17 can improve the accuracy of the input and output current measurements at low average current levels. Amplifiers A6 and A7 (Figure 15 and Figure 16) can only amplify positive R_{SENSE} voltages. Although the average R_{SENSE} voltage is always positive, the voltage ripple at low average current levels may contain negative components that are averaged out by the filter. Recommended values for R_{S1}, R_{S2} and C_{S1}, C_{S2} are 22Ω and 470nF.

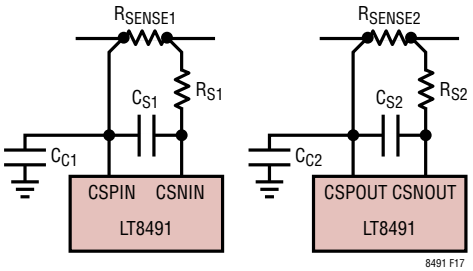

Figure 17. Recommended Current Sense Filter

C_{C1} and C_{C2} may be required, depending on board layout, to reduce common mode noise that may reach the LT8491 pins. 100nF ceramic capacitors, with the appropriate voltage ratings, work well in most cases. Be sure to place all the filter components (C_{SX}, R_{SX}, C_{CX}) close to the LT8491 for best performance.

Finally, note that a small voltage drop (typically ~0.25mV per 10Ω) will occur across R_{S1} and R_{S2} due to the input

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bias currents of the C_{SNOUT} and C_{SNIN} pins. This represents a ~0.5% reduction in the maximum current limit which typically occurs with ~50mV across R_{SENSE}. The C/10 threshold (typically when 5mV is measured across C_{SPOUT} and C_{SNOUT}) would also reduce to C/10.5 due to the 0.25mV drop across R_{S2}. The voltage drop across R_{S1} and R_{S2} will show up in the telemetry as a small error.

HW Config: Battery Temperature and Disconnect Sensing

The LT8491 can measure the battery temperature using an NTC (negative temperature coefficient) thermistor thermally coupled to the battery pack. Connect a 10kΩ, β = 3380 NTC thermistor from the TEMPSENSE pin to ground and an 18.2k (1% tolerance or better) resistor from AV_{DD} to TEMPSENSE, as shown in Figure 18. If battery temperature monitoring is not required, then use a 10k resistor in place of the thermistor. This will indicate to the LT8491 that the battery is always at 25°C.

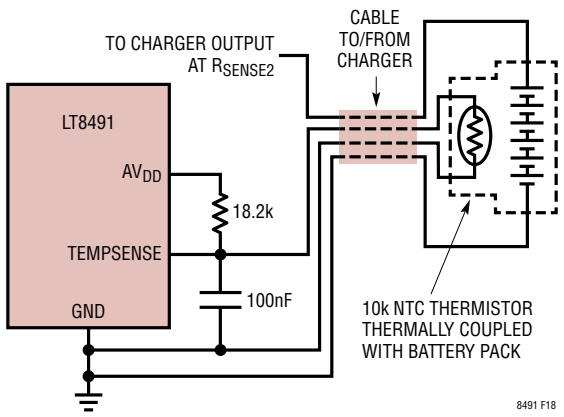

Figure 18. Battery Temperature and Disconnect Sensing Circuit

Using the thermally coupled thermistor, the LT8491 can accurately measure battery temperatures from –40°C to 60°C which can be read from the TELE_TBAT register. TELE_TBAT will report temperatures between ~ –45°C to 65°C, but with reduced accuracy outside of the –40°C to 60°C range.

The LT8491 can use the battery temperature information to compensate the battery charging voltages as discussed in the Configure Temperature Compensation section. High and low temperature fault limits can also be configured as discussed in the Configure Temperature Fault Limits section.

The LT8491 detects if the battery has been disconnected from the charger by monitoring the TEMPSENSE pin voltage. When the connection to the battery is severed, the connection to the thermistor is also severed and the TEMPSENSE voltage rises to AV_{DD} through the 18.2k resistor. A TEMPSENSE voltage greater than 96% of AV_{DD} (typical) indicates that the thermistor has been disconnected and activates a fault condition. See the Charging Faults section for details.

HW Config: $\overline{SHDN}$ Pin Connections

The LT8491 requires more than 1.234V (typical) on the $\overline{SHDN}$ pin to start up. A minimum of 5V on V_{IN} is also required for proper start-up operation; therefore, a resistor divider from V_{IN} to the $\overline{SHDN}$ pin is used to set this threshold. Connect the $\overline{SHDN}$ pin as shown in Figure 19 (1% resistor tolerance or better required).

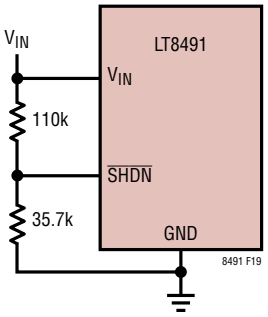

Figure 19. $\overline{SHDN}$ Pin Resistor Divider

HW Config: MODE Pin – Current Conduction Mode

The LT8491 has two modes of switching behavior controlled by the state of the MODE pin. Tying MODE to a voltage above 2.3V (i.e., V_{DD} or $INTV_{CC}$) configures the part for discontinuous conduction mode (DCM) which allows only positive current flow to the battery. More information about this mode of operation can be found in the LT8705 data sheet.

Tying the MODE pin below 0.4V (i.e. ground) changes the switching behavior as follows:

1. *Automatic CCM/DCM Mode Switching:* Very large inductor current ripple can lead the LT8491 to operate with high peak inductor currents while still in DCM. In this case, the M4 switch (highlighted in Figure 20) can

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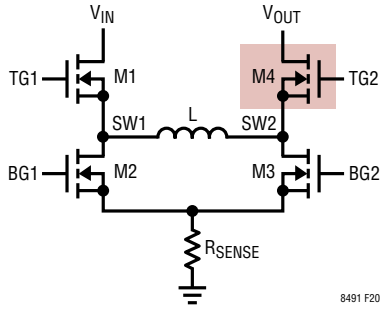

Figure 20. Simplified Diagram of Power Switches

become hot due to the battery charging current flowing through the body diode of this device.

Connecting the MODE pin low can reduce the M4 heating by activating the hybrid conduction mode (HCM). In this mode the average charging current is monitored at the IMON_OUT pin. The LT8491 operates in conventional DCM while the battery charging current, and thus IMON_OUT, is low (below 122mV typically). As the output charging current increases, IMON_OUT will eventually rise above ~195mV signaling the LT8491 to enter CCM operation that will turn on M4 and reduce heating. While the average charging current will always be positive, this mode does allow some negative current flow within each switching cycle. Use DCM operation (MODE tied high) if this behavior is not desired.

2. *Automatic $EXTV_{CC}$ Regulator Disconnect:* As discussed in more detail in the LT8705 data sheet, the $INTV_{CC}$ pin is regulated to 6.35V from one of two possible input pins, V_{IN} or $EXTV_{CC}$. The $EXTV_{CC}$ pin is often connected to the battery to minimize power loss and heating in the LT8491. However, $EXTV_{CC}$ should be disconnected from the battery when charging current is low to avoid discharging the battery.

   When MODE is below 0.4V, the $INTV_{CC}$ regulator is forced to use V_{IN} instead of $EXTV_{CC}$ for its input supply when charging current becomes low, thus minimizing possible battery discharge. Charging current is monitored on the IMON_OUT pin. When IMON_OUT falls below 122mV (typical) the $INTV_{CC}$ regulator uses V_{IN} as the input supply. When IMON_OUT rises above ~195mV $INTV_{CC}$ will regulate from $EXTV_{CC}$ if $EXTV_{CC}$ is also above 6.4V (typical). This same functionality can be achieved when MODE is tied high by using the external circuit discussed in the Optional: $EXTV_{CC}$ Disconnect section.

   Finally, a 305k (typical) resistor is connected from $EXTV_{CC}$ to ground inside the LT8491. This resistor draws draw current from the battery unless $EXTV_{CC}$ is disconnected. See the Optional: $EXTV_{CC}$ Disconnect section for a way to automatically disconnect $EXTV_{CC}$ when charging current becomes low or charging stops.

HW Config: Driving an LED with the STATUS Pin

The STATUS pin on the LT8491 can be used to drive an LED indicator. This section describes how to properly drive a STATUS LED. The STATUS Indicator Pin section describes the STATUS pin operation.

Figure 21 shows the simplest configuration for driving the LED from this pin. The STATUS pin can drive up to 2.5mA into an LED. Choose R_{DSA} to limit the LED current to 2.5mA or less when STATUS is driven close to 3.3V. Choose R_{DSB} to conduct a current equivalent to the LED current when STATUS is driven close to ground and R_{DSB} has ~3.3V across the terminals. D_S, in Figure 21, conducts ~2.5mA when STATUS is driven high. R_{DSB} conducts ~2.5mA when the STATUS is driven low.

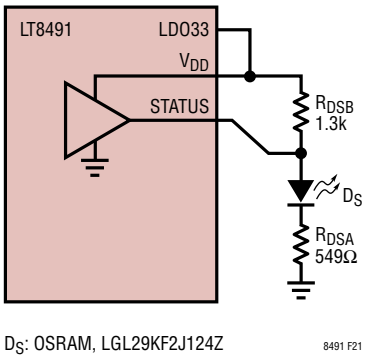

Figure 21. 2.5mA STATUS LED Indicator

For driving a higher current LED, the circuit in Figure 22 can be used. The LED current for D_S is provided by V_{IN} in this case. Do not draw current for D_S from $INTV_{CC}$ since this increases power dissipation in the LT8491. Transistor Q1 must have a collector-emitter breakdown greater than V_{IN}. MMBT5550L has a breakdown voltage of 140V and is suitable for most applications.

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To properly set the resistors shown in Figure 22, use the following equation:

$$R_E \cong \frac{2.6}{I_D}\Omega$$

where I_D is the desired bias current through the LED.

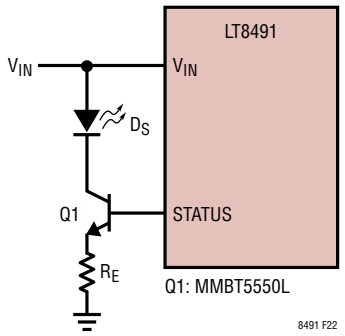

Figure 22. Higher Current Drive for STATUS LED

HW Config: I²C Chip Address Pin

The CA pin on the LT8491 is a resistor programmable ADC input used to select one of four possible I²C chip addresses for the LT8491.

Figure 23 shows a sample configuration for a desired I²C Address of 0x19 (7-bit).

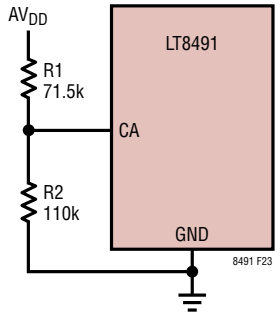

Figure 23. Chip Address Select Circuit

Use the recommended resistor values stated in Table 24. The given resistor value combinations select the proper function and yield low current consumption.

Table 24. I²C Address Resistor Values

I²C ADDRESS	R1	R2
0x10	100k (Pull-Up)	–
0x19	71.5k	110k
0x20	187k	107k
0x29	–	100k (Pull-Down)

IN-SITU BATTERY CHARGING

The LT8491 can be used to charge a battery while the battery is powering a load. The load should be directly connected to the battery terminals as shown in Figure 24. The variable nature of some loads can make charging times unpredictable. Due to this unpredictability, it is recommended that charging time limits be disabled (see Configure Stage Timeout Limits section).

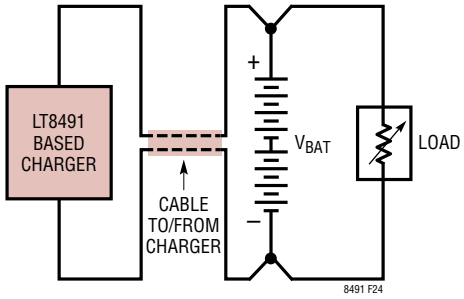

Figure 24. Load Connection to Battery in LT8491 Application

Because a load connected to the battery may draw more power than provided by the charger, the battery may discharge while the LT8491 is charging the battery. If this case occurs and the battery voltage falls below the V_{S0_UV} threshold (31% default) of the Stage 2 voltage limit, the undervoltage fault will become active and the charger will halt until the battery voltage rises above the V_{UV_S0} threshold (35% default) of the Stage 2 voltage limit. Note that these thresholds are configurable. See Configure V_{BAT} for Stages 0, 1, and 3. Consider disabling the load current if the battery depletes below an unacceptably low voltage.

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The arrow in Figure 24 shows the proper disconnect point if removing the battery from the charger in an in-situ battery charging application. This disconnect point removes the load and the battery from the charger and is specified because the LT8491 is not designed to provide power directly to a load without the presence of a battery.

HOT-PLUGGING CONSIDERATIONS

When connecting a battery to an LT8491 charger, there can be significant inrush current due to charge equalization between the partially charged battery stack and the charger output capacitors. To a lesser extent, a similar effect can occur when connecting an illuminated panel or powered DC supply to the input. The magnitude of the inrush current depends on (1) the battery, panel or supply voltage, (2) ESR of the input or output capacitors, (3) initial voltage of the capacitors, and (4) cable impedance. Excessive inrush current can lead to sparking that can compromise connector integrity and/or voltage overshoot that can cause electrical overstress on LT8491 pins.

Excessive inrush current can be mitigated by first connecting the battery or supply to the charger through a resistive path, followed quickly by a short-circuit. This can be accomplished using staggered length pins in a multi-pin connector. This can also be accomplished using the optional circuit shown in Figure 34 by first connecting the (+) and (–) battery remote sense connections, which allow the charger output capacitors to charge through resistors R2 and R3. Alternatively, consider the use of a Hot Swap Controller such as the LT1641, LT4256, etc. to make a current limited connection.

STATUS INDICATOR PIN

The LT8491 reports charger status through the STATUS pin. To get visual user feedback this pin can be used to drive a LED. Table 25 describes the LED behavior of this pin in relationship to the charger status.

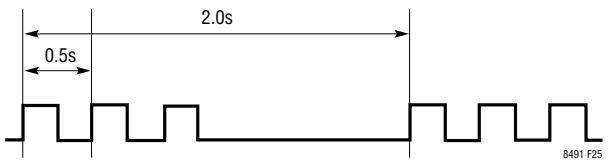

Figure 25. Example Waveform for STATUS Pin in STAGE 3

While the LT8491 is operating, the STATUS pin toggles on a 2 Sec (typical) interval as shown in Figure 25. The three pulses shown in Figure 25 represent the charger operation in Stage 3. The STATUS pin will pull up to turn the LED on and drive to ground to turn the LED off.

Table 25. Status LED Indicator

CHARGER STATUS	STATUS LED PULSES/2.0s, APPROXIMATE ON-TIME PER PULSE	FOR MORE INFORMATION SEE SECTION
Stage 0	1, 10ms	Battery Charging Algorithm
Stage 1	1, 250ms	Battery Charging Algorithm
Stage 2 and (Stage 3 Enabled or Timer Limits Enabled or I_{OUT} Rising Above C/5)	2, 250ms	Battery Charging Algorithm, Configure Stage Timeout Limits, and Configure Misc.
Stage 2 and (Stage 3 Disabled and Timer Limits Disabled and I_{OUT} Falling Below C/10)	ON	Battery Charging Algorithm, Configure Stage Timeout Limits, and Configure Misc.
Stage 3	3, 250ms	Battery Charging Algorithm
Done Charging	ON	Configure Charge Termination
CTRL_CHRG_EN = 0	OFF	Control Other Functions
Battery Disconnect Fault	OFF	HW Config: Battery Temperature and Disconnect Sensing
Invalid Battery Temperature Fault	OFF	HW Config: Battery Temperature and Disconnect Sensing
Timer Expiration Fault	OFF	Configure Stage Timeout Limits
Battery Undervoltage Fault	OFF	Configure V_{BAT} for Stages 0, 1 and 3

LITHIUM-ION BATTERY CHARGING

The LT8491 is well suited to charge lithium-ion batteries. Table 26 shows a sample configuration that puts the LT8491 into a typical setup for lithium-ion battery charging.

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Table 26. Lithium-Ion Battery Register Settings

REGISTER NAME	I²C REG ADDR	VALUE
CFG_TBAT_MIN	0x40	0x00 → (0°C)
CFG_TBAT_MAX	0x41	0x32 → (50°C)
CFG_TMR_S0	0x42	0x00
CFG_TMR_S1	0x43	0x00
CFG_TMR_S2	0x44	0x00
CFG_TMR_S3	0x45	0x00
CFG_CHRG_MISC [2:0]	0x4D	000b

Figure 26 shows a typical lithium-ion charging cycle in this configuration. If no timer termination has been selected (CFG_TERMINATE→S2_TIMER_TERM_EN=0), the LT8491 will charge the lithium-ion battery stack to the desired Stage 2 voltage limit, maintaining that limit indefinitely. Consider setting C/10 termination bits as discussed in Configure Charge Termination section. When the charging current is < C/10, the STATUS pin will go high as described in Table 25.

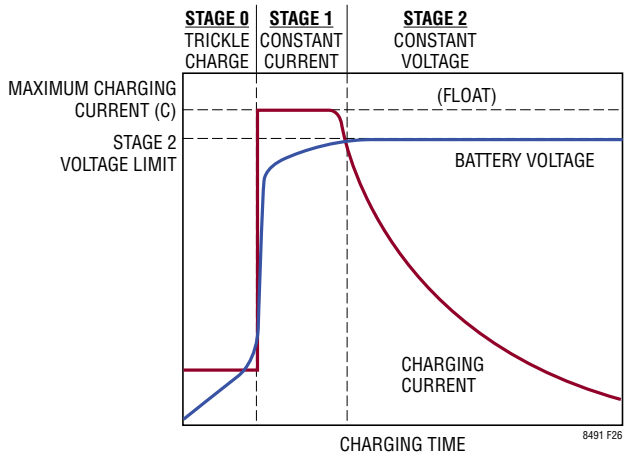

Figure 26. Lithium-Ion Battery Charging Cycle

NOTE: When solar charging a lithium-ion battery without time limits it is recommended that the Stage 2 voltage limit NOT exceed 95% of the lithium-ion maximum cell voltage. Since this configuration can charge indefinitely, following this guideline keeps the lifetime of the batteries from degrading quickly. Also, if battery protection circuitry is used, consider setting V_{UV_S0} and V_{S0_UV} to 0. See Configure V_{BAT} for Stages 0, 1, and 3 section.

LEAD-ACID BATTERY CHARGING

The LT8491 can be used to charge lead-acid batteries. Table 27 shows a sample configuration that puts the LT8491 into a typical setup for lead-acid battery charging.

Table 27. Lead-Acid Battery Register Settings

REGISTER NAME	I²C REG ADDR	VALUE
CFG_VS3_25C	0x3B	0x7A → (97.2%)
CFG_TBAT_MIN	0x40	0xEC → (–20°C)
CFG_TBAT_MAX	0x41	0x32 → (50°C)
CFG_TMR_S0	0x42	0x00
CFG_TMR_S1	0x43	0x00
CFG_TMR_S2	0x44	0x00
CFG_TMR_S3	0x45	0x00
CFG_RSTRT_IN_S3 [0]	0x49	1b
CFG_CHRG_MISC [2:0]	0x4D	111b

The above example does have temperature compensation enabled, a standard setting for lead-acid batteries. See Configure Temperature Compensation section for more information.

Consider setting the USE_VS3_IN_STAGE2 bit to 1 for in-situ lead acid battery charging. See CFG_CHRG_MISC register definition for an in-depth explanation.

If time limits have been disabled, the LT8491 will charge the lead-acid battery stack to the desired Stage 3 voltage limit and restart the charging cycle if 1) the battery voltage falls below 96% of the Stage 3 voltage limit (V_{S3}) or 2) the charging current rises above C/5. Figure 27 shows a typical lead-acid charging cycle.

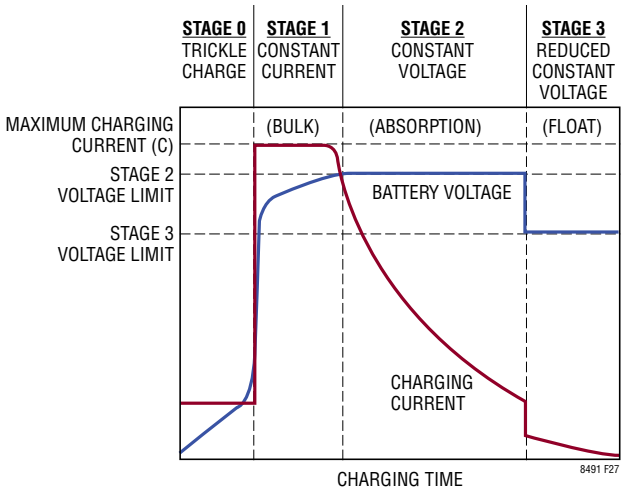

Figure 27. Lead-Acid Battery Charging Cycle

APPLICATIONS INFORMATION

OPTIONAL FEATURES

Optional: Low Power Mode

When current from the solar panel is not high enough to reliably measure the maximum power point, the LT8491 will automatically begin operating in low power mode. Low power mode is automatically disabled when operating from a DC supply in power supply mode. The low power mode feature is enabled by default register setting CFG_CHRG_MISC→LP_MODE_EN=1 and allows the LT8491 to charge a battery under very low light conditions that would otherwise cause the LT8491 to stop charging. Low power mode can be disabled by setting CFG_CHRG_MISC→LP_MODE_EN=0. See Configure Misc. section for more information.

In low power mode, the LT8491 momentarily stops charging, allowing the panel voltage to rise. When the panel has sufficiently charged the input capacitor, the LT8491 transfers energy from the input capacitor to the battery while drawing down the panel voltage. This behavior repeats rapidly, delivering charge to the battery as shown in the Panel Voltage in Low Power Mode plot in the Typical Performance Characteristics section.

Minimum Input Capacitance for Low Power Mode: A minimum amount of energy must be transferred from the input capacitor to the battery during each charge transfer cycle. Otherwise the battery may be drained instead of being charged. Figure 28 shows the minimum input capacitance required when the charger is operating near the 10V minimum input voltage. As the panel voltage rises, due to increased illumination, more energy is stored in the input capacitor and a corresponding increase of energy is delivered to the battery. Carefully check the solar panel voltage for good stability and minimal ripple when operating with low input capacitance.

Minimum Input Voltage: With low power mode enabled, the panel voltage must initially exceed 10V (typical – as measured through the VINR pin) before the charger will attempt to charge the battery. If the panel voltage is below 10V, the charger may temporarily wait for more voltage before transferring the input charge to the battery.

Exiting Low Power Mode: The charger will automatically exit low power mode and resume normal charging after adequate input power is detected. The charger typically requires the input current to exceed 2.5% to 3% of the maximum input current limit to make a valid power point reading and exit low power mode. The panel voltage may be adjusted as low as 6V when searching for the maximum power point.

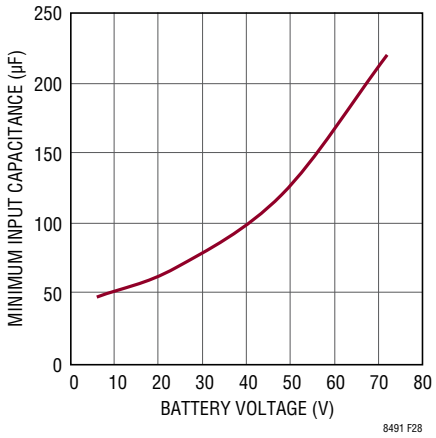

Figure 28. Minimum Input Capacitance Required for Low Power Mode

Optional: Output Feedback Resistor Disconnect

To measure and regulate the battery voltage, the LT8491 uses the resistor feedback network discussed in the HW Config: V_{BAT} in Stage 2 (V_{S2}) section. Unless these resistors are disconnected from the battery, they will draw current from the battery even when it is not charging as shown in Figure 29. This may be undesirable when using small capacity batteries.

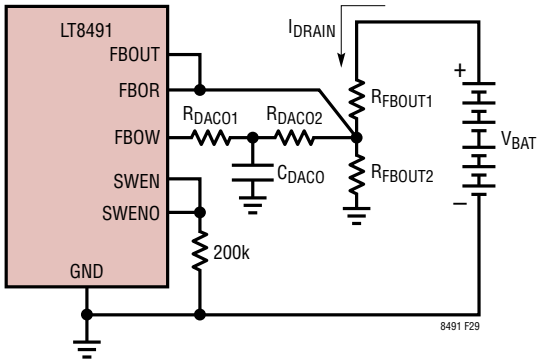

Figure 29. Battery Discharge when Not Charging

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If desired, the resistors can be automatically disconnected from the battery when charging stops by using one of the circuits shown in Figure 30 and Figure 31. The circuits are controlled by the SWENO signal from the LT8491 and connect the resistor feedback network when charging is taking place. When charging stops, the network is disconnected and current draw from the battery becomes negligible.

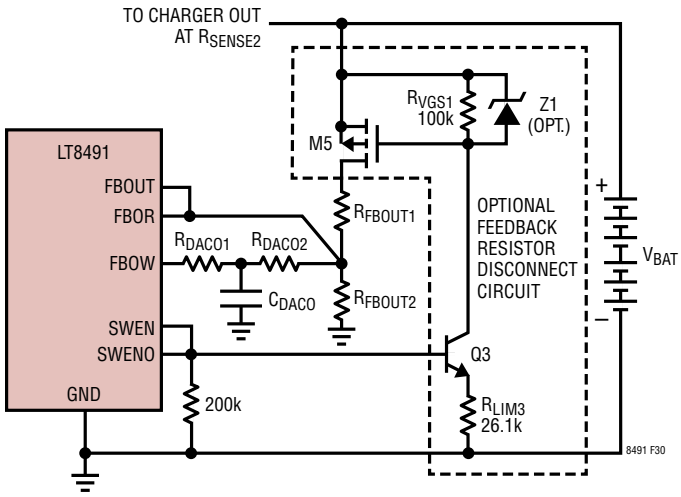

Figure 30. Optional Feedback Resistor Disconnect Circuit #1

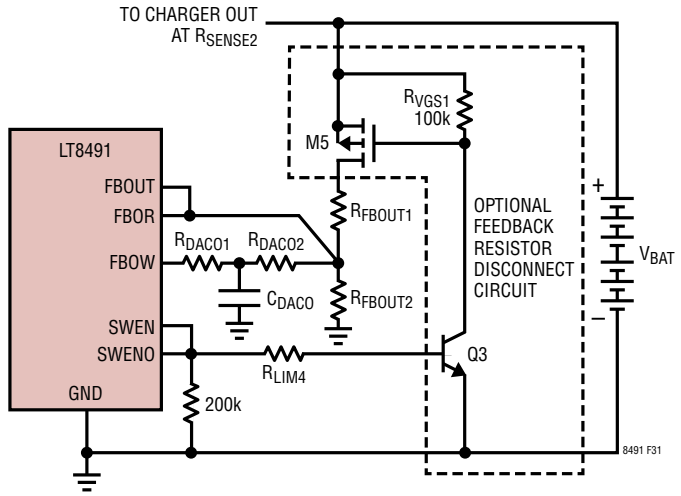

Figure 31. Optional Feedback Resistor Disconnect Circuit #2

Selecting M5: This PMOS must have a drain to source breakdown voltage greater than the maximum V_{BAT}. The ZVP3310F is rated for 100V making it suitable for most applications.

Selecting Q3: This NPN must have a collector to emitter breakdown voltage greater than the maximum V_{BAT}. The MMBT5550L is also suitable for most applications due to its 140V breakdown rating.

Selecting R_{LIM3}: Using $V_{GS(ON)}$ and setting R_{VGS1} to 100k

$$R_{LIM3} = \left(\frac{R_{VGS1}}{V_{GS(ON)}} \right) \bullet 2.6V\ \Omega$$

where $V_{GS(ON)}$ is the desired gate to source voltage needed to turn on M5. If M5 is not properly selected, the on resistance may be large enough to cause a significant voltage drop across the drain-source terminals of this device. Check this voltage drop to determine if the application can tolerate this error.

Selecting Z1: Due to the transients that may occur during hot-plugging of a battery, this Zener diode is recommended to protect device M5 from excessive gate to source voltage. If using device Z1, the reverse breakdown voltage should be selected such that $V_{GS(ON)} < V_{Z1(BREAKDOWN)} < V_{GSMAX}$ where V_{GSMAX} is the maximum rated gate to source voltage specified by the device manufacturer. The BZT52C13 has a reverse breakdown voltage of 13V making it suitable for the RLIM3 value shown in Figure 30.

Alternate Circuit: For lower battery voltages (< 20V), Q3 in Figure 30 may saturate. To avoid this, consider connecting the emitter of Q3 directly to ground by removing R_{LIM3} and adding resistor R_{LIM4} to the base of Q3 as shown in Figure 31. Employing the optional feedback resistor disconnect at arbitrarily low battery voltages will be limited by the required gate to source voltage of M5.

Use the following equation to properly set R_{LIM4}:

$$R_{LIM4} = 91 \bullet \frac{R_{VGS1}}{V_{BAT}}$$

Optional: $EXTV_{CC}$ Disconnect

It is often desirable to connect $EXTV_{CC}$ to the battery to reduce power loss (increase efficiency) and heating in the LT8491. However, the LT8491 draws current into the $EXTV_{CC}$ pin that can drain the battery when charging currents are low or when charging stops. Tying the MODE pin

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low, as discussed in the HW Config: MODE Pin – Current Conduction Mode section, eliminates most of the current draw from $EXTV_{CC}$ when the charging current becomes low. However, there is a 305kΩ (typical) path from $EXTV_{CC}$ to ground through the LT8491 at all times. If desired, this current path can be disconnected through the optional circuit shown in Figure 32.

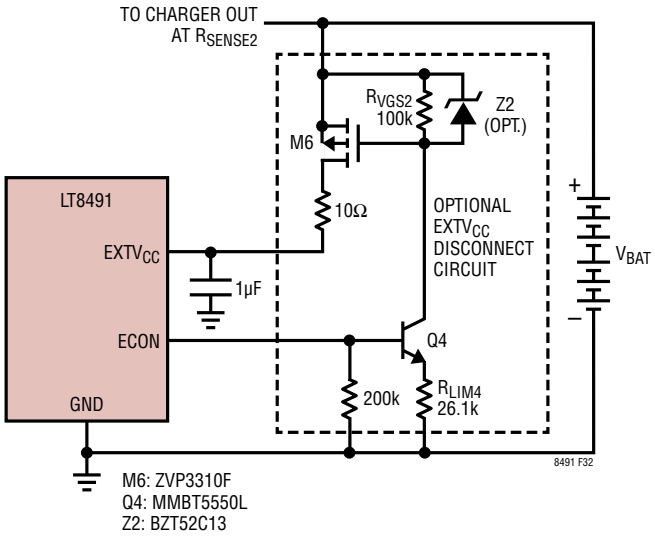

Figure 32. Optional $EXTV_{CC}$ Disconnect Circuit

The LT8491, via the ECON signal, disconnects $EXTV_{CC}$ from the battery when charging current becomes low. Charging current is monitored by measuring the IMON_OUT pin voltage with the IOR pin's A/D input. When IMON_OUT falls below 122mV (typical) the ECON signal goes low and $EXTV_{CC}$ is disconnected from the LT8491. When IMON_OUT rises above 195mV (typical) the ECON signal goes high and $EXTV_{CC}$ is reconnected to the LT8491.

Follow the same recommendations and equations from the previous section for choosing components for the optional $EXTV_{CC}$ disconnect circuit.

Optional: Remote Battery Voltage Sensing

The LT8491 senses the battery voltage continually during charging. The apparent battery voltage is sensed from ground of the LT8491 to the top of R_{FBOUT1}. During charging, resistance in the battery cables (R_{CABLE}^+/R_{CABLE}^- in Figure 33) causes the apparent voltage to be higher than the actual battery voltage by 2 • V_{IR}.

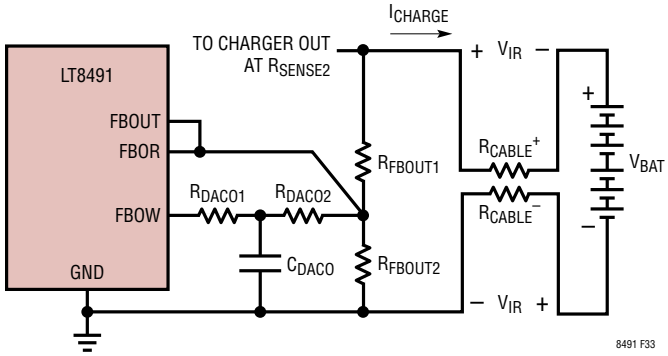

Figure 33. IR Drop Present in Battery Connection

The effects of this cable drop are most significant when charging low voltage batteries at high currents. As an example, a 4-foot battery cable using 14 AWG wire can have a voltage drop exceeding 0.5V at 15A of current. Note however that the voltage drop, along with the charging current, reduces automatically as the battery approaches full charge.

The most significant effects from the V_{IR} voltage drops are as follows:

1. When approaching full charge in Stage 2, the V_{IR} error causes the charger to reduce the charging current earlier than otherwise necessary. This increases the total charging time.
2. Terminating at C/10 in Stage 2 will occur at a reduced battery voltage equal to C/10 • (R_{CABLE}^+ + R_{CABLE}^-) which is 10% of the voltage drop at full charging current.
3. The STATUS pin will indicate a transition from Stage 1 to Stage 2 earlier than would otherwise occur without the cable drop.
4. The V_{BAT} telemetry measurement will have some error since the measurement is taken at the FBOR pin of the LT8491.

Again, these effects become less significant at higher battery voltages because the charging current is typically lower, and the cable drop becomes a smaller percentage of the total battery voltage. Using thicker and/or shorter battery cables is the simplest method for reducing these effects. Otherwise the remote battery sensing circuit in Figure 34 can correct for these effects.

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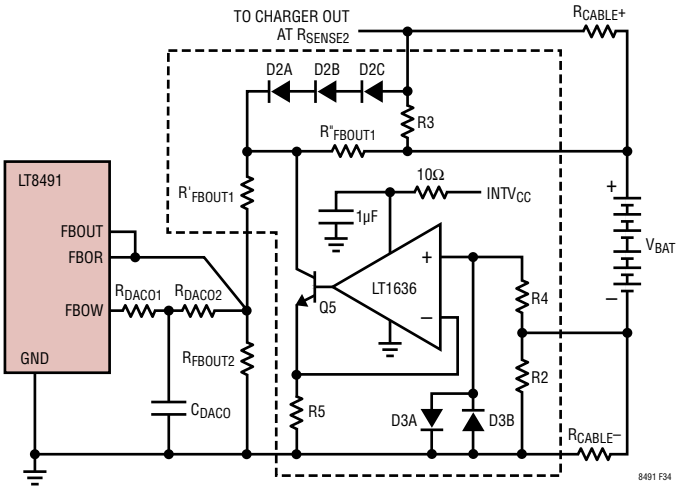

Figure 34. Remove (+) and (–) Cable V_{IR} Measurement Errors

The R_{CABLE}^+ measurement error is eliminated by including an additional (+) terminal sensing cable. The negative cable error is eliminated by subtracting the R_{CABLE}^- drop from the voltage measured at the positive battery terminal using a (–) terminal sensing cable, the LT1636, Q5 and R5. R'_{FBOUT}, R''_{FBOUT} and R5 are determined as follows:

$$R''_{FBOUT1} = \frac{0.5 \bullet R_{FBOUT1}}{V_{S2} - 1.211}\Omega$$

$$R'_{FBOUT1} = \left(R_{FBOUT1} - R''_{FBOUT1}\right)\Omega$$

$$R5 = R''_{FBOUT1}\Omega$$

where V_{S2} is the room temperature Stage 2 voltage limit and the solution for R_{FBOUT1} was discussed previously in the HW Config: V_{BAT} in Stage 2 (V_{S2}) section. Solutions for determining R_{DACO1}, R_{DACO2}, R_{FBOUT2} and C_{DACO} are also discussed in the HW Config: V_{BAT} in Stage 2 (V_{S2}) section.

Due to its low current draw (<1mA) Q5 can be a small signal device with a collector-emitter breakdown voltage at least as high as the battery voltage. The MMBT3904 is a good BJT rated to 40V. Alternatively, the MMBT5550L is rated for 140V.

R3 is for safety in case the (+) battery sensing cable becomes disconnected. R3 prevents overcharging the battery in such an event by creating an alternate path to pull up the R''_{FBOUT1} battery voltage sensing resistor. The R3 resistance should be less than 1% of R_{FBOUT1}. Selecting R3 as a 100Ω resistor is often a good choice. During normal operation, the voltage across R3 is about the same as across R_{CABLE}^+. However, R3 may experience voltage up to $V_{S2} – V_{BAT}$ across its terminals if R_{CABLE}^+ becomes disconnected. R3 should be selected with an appropriate power rating, often at least 1 Watt.

D2A - D2C protect the charger if the positive charging cable (R_{CABLE}^+) becomes disconnected while the others remain intact. Without the diodes, the output of the charger may overvoltage and become damaged. BAV99 diodes are a good choice and are available in a dual-diode package to minimize board space. Note that the diodes limit the maximum R_{CABLE}^+ error to 0.3 to 0.5V. If a greater voltage drop is typical in the positive cable, then place more diodes in series. In Figure 35, D2D protects the M5 device by limiting the gate to source voltage when making the remote sense connection.

D3A, D3B and R4 protect the input of the LT1636 from possible voltage extremes at the (–) battery terminal sensing connection. The dual-diode BAV99 is also suitable in this case. 4.99k is a good value for R4.

R2 maintains a negative voltage reference in case R_{CABLE}^- becomes disconnected. Selecting R2 as a 100Ω resistor is often a good choice. During normal operation, the voltage across R2 is about the same as across R_{CABLE}^-. However, R2 may experience voltage in excess of $V_{S2} – V_{BAT}$ across its terminals if R_{CABLE}^- becomes disconnected. R2 should be selected with an appropriate power rating, often at least 1 Watt due to the case where the (+) and (–) wires of the remote sense circuit are first connected to the battery to address hot-plugging issues (see the Hot-Plugging Considerations section for more detail).

Figure 35 shows how to combine the remote sensing circuit (Figure 34) and the feedback resistor disconnect (Figure 30) for applications that require the most accurate battery voltage sensing and negligible battery drain when charging completes. The R_{VGS1} resistor can no longer connect to the source of M5 (as in Figure 30) since the R_{VGS1} current would also flow through R''_{FBOUT1} causing an error in the measured battery voltage. Figure 34 shows that R_{VGS1} has been reconnected to the (+) battery sensing terminal.

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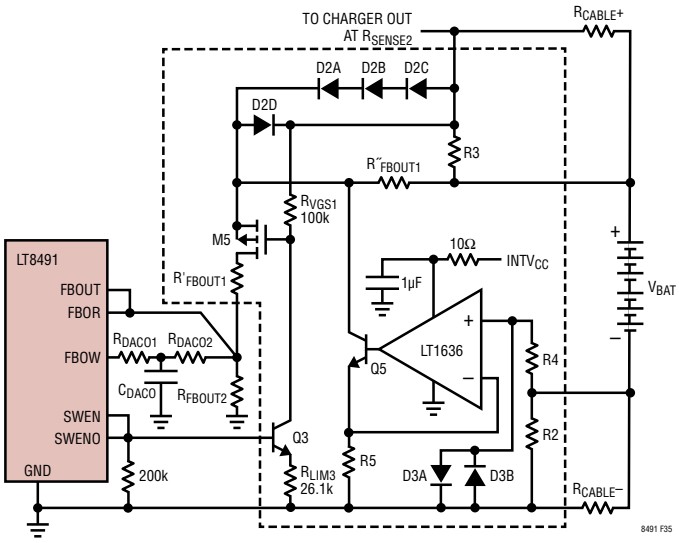


Figure 35. How to Combine Figure 30 and Figure 34

Optional: DC Supply Detection Circuit

A dual input application can be configured where the charger can be supplied by either a solar panel or a DC supply. When powered by a DC supply, the VINR pin must be pulled low to activate Power Supply Mode. In addition, blocking diodes should be incorporated to prevent the supplies from backfeeding into each other. The circuit shown in Figure 36 shows a way to incorporate those features.

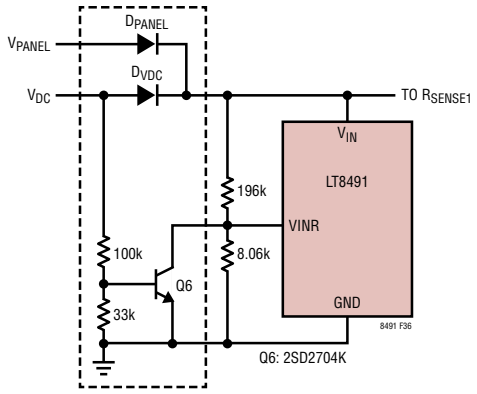


Figure 36. Optional DC Supply Detection Circuit

As shown in Figure 36, when the DC supply is connected the Q6 NPN pulls VINR below 174mV (typical) to activate the Power Supply Mode of the LT8491. Be sure to choose an NPN that can pull VINR below the Power Supply Mode threshold before fully saturating. Alternatively, Q6 can be replaced with an NMOS device with proper care taken to avoid overvoltage of the NMOS gate.

Depending on the current limit settings, diodes D_{PANEL} and D_{VDC} can incur significant current and heat. Consider the use of Schottky diodes or an appropriate ideal diode such as the LTC4358, LTC4412, LTC4352, etc. to minimize heating.

BOARD LAYOUT CONSIDERATIONS

For all power components and board routing associated with the LT8705 portion of the LT8491, please refer to the LT8705 documentation in which a Circuit Board Layout Checklist and drawing is provided.

DESIGN EXAMPLE

In this design example, the LT8491 is paired with a 175W/5.4A Panel (V_{MAX} = 53V) and a 12V flooded lead-acid battery. The desired maximum battery charging current (C) is 10A with a trickle charge current of 2.5A (C/4). Charger settings are as follows: –20°C to 50°C valid battery temperature range, temperature compensated charging limits, no time limits and Stage 3 is enabled with V_{S3}/V_{S2} = 97.2%. In this example resistors are rounded to the nearest standard value. If better accuracy is required, then multiple resistors in series may be required.

- With R_{FBOUT2} set at 20k and a desired Stage 2 voltage limit of 14.2V, the top output feedback resistor, R_{FBOUT1}, is calculated according to the following equation:

$$R_{FBOUT1} = R_{FBOUT2} \bullet \left[V_{S2} \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$= 20k \bullet \left[14.2 \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$= 234{,}684\Omega$$

Choose R_{FBOUT1} = 237k which is the closest standard value resistor.

APPLICATIONS INFORMATION

- Following the calculation of R_{FBOUT1}, solve for R_{DACO1}, R_{DACO2} and C_{DACO} according to the following formulas:

$$R_{DACO2} = \frac{0.833 \bullet R_{FBOUT1} \bullet R_{FBOUT2}}{\left(R_{FBOUT2} \bullet V_{S2} \bullet \frac{1.241}{1.211}\right) - R_{FBOUT2} - R_{FBOUT1}} \Omega$$

$$= \frac{0.833 \bullet 234,684 \bullet 20k}{\left(20k \bullet 14.2 \bullet \frac{1.241}{1.211}\right) - 20k - 234,684} \Omega$$

$$= 107,556\Omega$$

Choose R_{DACO2} = 107k which is the closest standard value resistor.

$$R_{DACO1} = 0.2 \bullet R_{DACO2}\Omega$$
$$= 0.2 \bullet 107,556\Omega$$
$$= 21,511\Omega$$

Choose R_{DACO1} = 21.5k which is the closest standard value resistor.

$$C_{DACO} = \frac{1}{500 \bullet R_{DACO1}} F$$
$$= \frac{1}{500 \bullet 21,511} F$$
$$= 93nF$$

- Using the standard value resistors calculated above, the V_{X3}, N1 and N2 checking equations yield the following:

  V_{X3} = 14.31V

  N1 = 1.22

  N2 = 0.804

- To find a resistor combination that yields V_{X3} closer to the desired 14.2V, R_{FBOUT2} is increased to the next higher standard value and the above calculations are repeated.

- Iterations of the previous step are performed that include adjustments to R_{FBOUT1}, R_{DAC01} and R_{DAC02} until the following standard value feedback resistors were chosen:

  R_{FBOUT1} = 274k

  R_{FBOUT2} = 23.2k

  R_{DACO1} = 26.1k

  R_{DACO2} = 124k

  C_{DACO} = 0.082µF

  where:

  V_{X3} = 14.27V

  N1 = 1.22

  N2 = 0.805

- With the output feedback network determined, use V_{MAX} and solve for the input resistor feedback network according to the following formulas:

$$R_{FBIN1} = 100k \bullet \left[\frac{1 + \left(\frac{4.47V}{V_{MAX} - 6V}\right)}{1 + \left(\frac{5.593V}{V_{MAX} - 6V}\right)}\right] \Omega$$

$$= 100k \bullet \left[\frac{1 + \left(\frac{4.47V}{53V - 6V}\right)}{1 + \left(\frac{5.593V}{53V - 6V}\right)}\right] \Omega$$

$$= 97,865\Omega$$

The closest standard value for R_{FBIN1} is 97.6k.

$$R_{DACI2} = 2.75 \bullet \left(\frac{R_{FBIN1}}{V_{MAX} - 6V}\right) \Omega$$

$$= 2.75 \bullet \left(\frac{97,865}{53V - 6V}\right) \Omega$$

$$= 5726\Omega$$

APPLICATIONS INFORMATION

Choose R_{DACI2} = 5.76k which is the closest standard value.

$$R_{FBIN2} = \frac{1}{\left(\frac{1}{100k - R_{FBIN1}}\right) - \left(\frac{1}{R_{DACI2}}\right)}\Omega$$

$$= \frac{1}{\left(\frac{1}{100k - 97,865}\right) - \left(\frac{1}{5726}\right)}\Omega$$

$$= 3404\Omega$$

Choose R_{FBIN2} = 3.4k which is the closest standard value.

$$R_{DACI1} = 0.2 \bullet R_{DACI2}\ \Omega$$

$$= 0.2 \bullet 5726\Omega$$

$$= 1145\Omega$$

Choose R_{DAC1} = 1.1k which is the closest standard value.

$$C_{DACI} = \frac{1}{1000 \bullet R_{DACI1}}F$$

$$= \frac{1}{1000 \bullet 1,145}F$$

$$= 873nF$$

- Like the output feedback resistors, the final input feedback resistors were chosen to be standard values using an iterative process. The V_{X1} and V_{X2} equations in the HW Config: Input Voltage Sensing and Modulation network section were used to validate the selections:

  R_{FBIN1} = 93.1kΩ

  R_{FBIN2} = 3.24kΩ

  R_{DACI1} = 1.05kΩ

  R_{DACI2} = 5.49kΩ

  C_{DACI} = 1µF

  where:

  V_{X1} = 6V

  V_{X2} = 53V

- The 10A maximum charge current limit and 2.5A trickle charge current limit are set by choosing R_{SENSE2}, R_{IMON_OUT} and R_{IOW} using the following formulas:

$$R_{SENSE2} = \frac{0.0497}{I_{OUT(MAX)}}\Omega = \frac{0.0497}{10} \cong 5m\Omega$$

$$R_{IMON_OUT} = \frac{1208}{I_{OUT(MAXS0)} \bullet R_{SENSE2}}\Omega$$

$$= \frac{1208}{2.5 \bullet 5m}\Omega$$

$$= 96.64k\Omega$$

  where the nearest standard value is 97.6kΩ

$$R_{IOW} = \frac{24.3k \bullet R_{IMON_OUT}}{R_{IMON_OUT} - 24.3k}\Omega$$

$$= \frac{24.3k \bullet 47.6k}{97.6k - 24.3k}\Omega$$

$$= 32,356\Omega$$

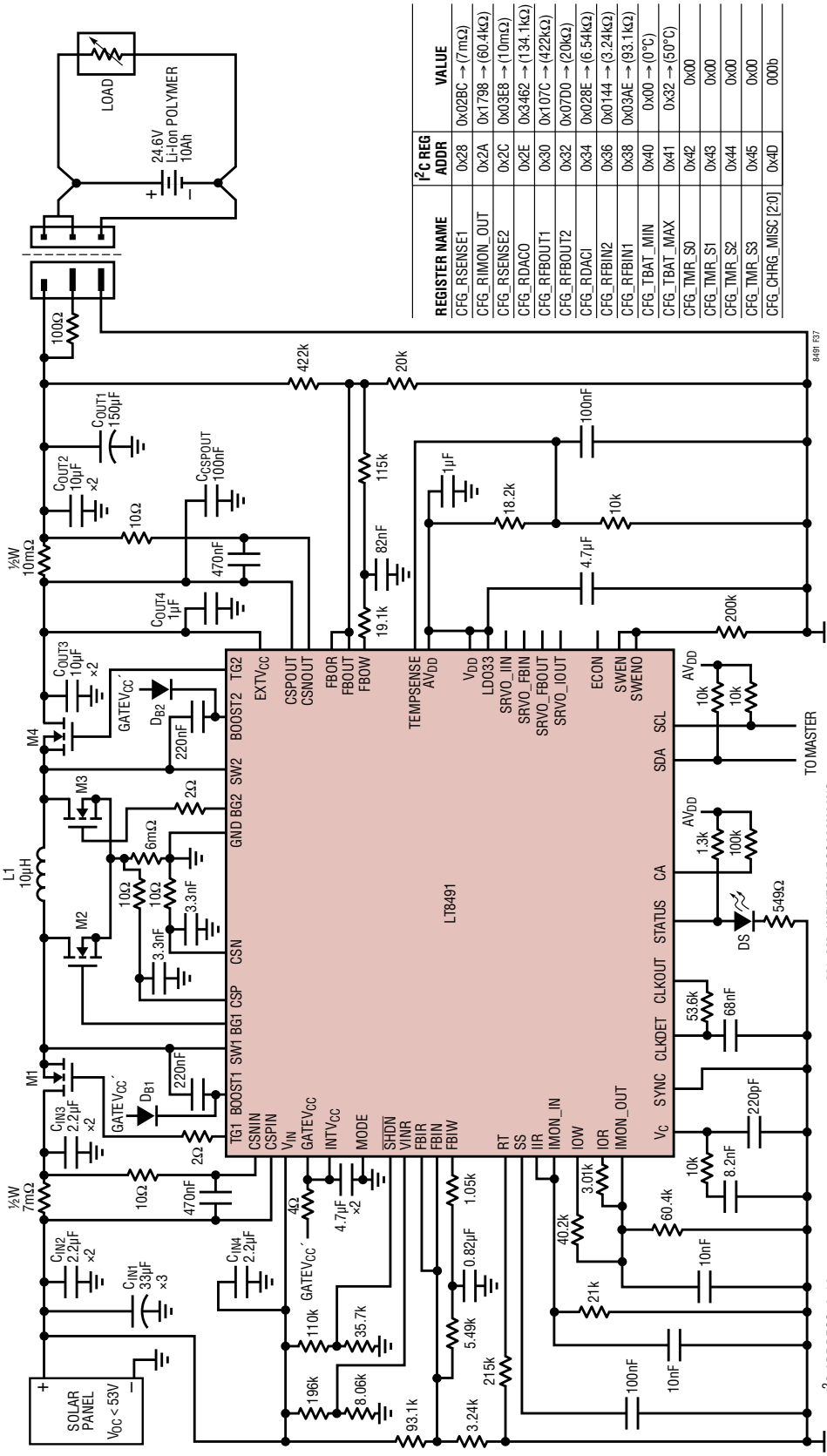
  where the nearest standard value is 32.4kΩ

- The input current limit is set by properly choosing R_{SENSE1}. In this example, the panel can deliver up to 5.4A. Choosing a margin of 30% yields...

$$R_{SENSE1} = \frac{0.0505}{I_{IN(MAX)}} = \frac{0.0505}{1.3 \bullet 5.4} = 7.2M\Omega$$

- For greater charging voltage accuracy, it is recommended that 0.1% tolerance resistors be used for the output feedback resistor network.
- Please reference the LT8705 data sheet for completing the remaining power portions of the LT8491.

TYPICAL APPLICATIONS

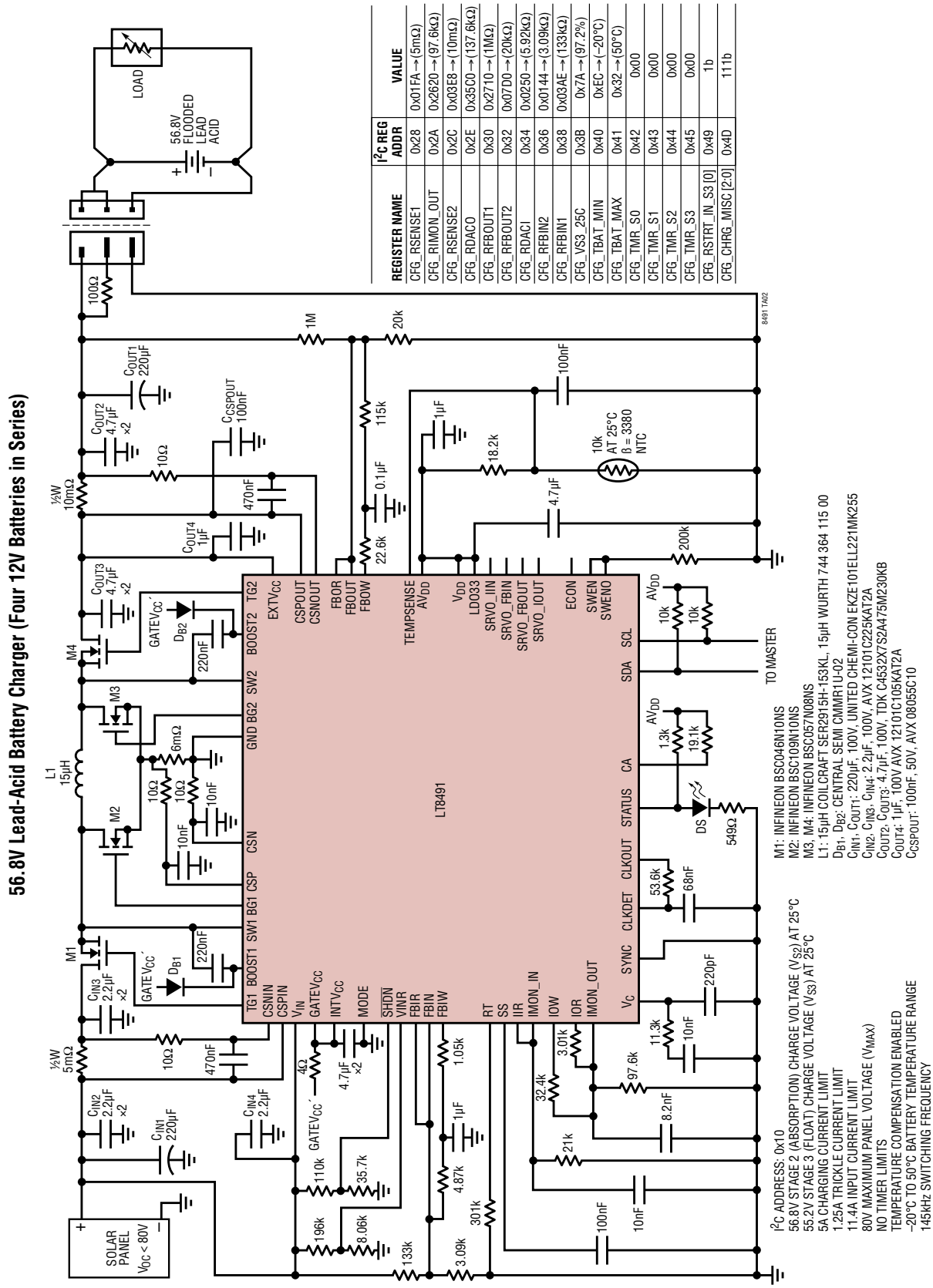


REGISTER NAME	I²C REG ADDR	VALUE
CFG_RSENSE1	0x28	0x02BC → (7mΩ)
CFG_RIMON_OUT	0x2A	0x1798 → (60.4kΩ)
CFG_RSENSE2	0x2C	0x03E8 → (10mΩ)
CFG_RDACO	0x2E	0x3462 → (134.1kΩ)
CFG_RFBOUT1	0x30	0x107C → (422kΩ)
CFG_RFBOUT2	0x32	0x07D0 → (20kΩ)
CFG_RDACI	0x34	0x028E → (6.54kΩ)
CFG_RFBIN2	0x36	0x0144 → (3.24kΩ)
CFG_RFBIN1	0x38	0x03AE → (93.1kΩ)
CFG_TBAT_MIN	0x40	0x00 → (0°C)
CFG_TBAT_MAX	0x41	0x32 → (50°C)
CFG_TMR_S0	0x42	0x00
CFG_TMR_S1	0x43	0x00
CFG_TMR_S2	0x44	0x00
CFG_TMR_S3	0x45	0x00
CFG_CHRG_MISC [2:0]	0x4D	000b

Figure 37. 24.6V Lithium-Ion Polymer Battery Charger

TYPICAL APPLICATIONS

56.8V Lead-Acid Battery Charger (Four 12V Batteries in Series)



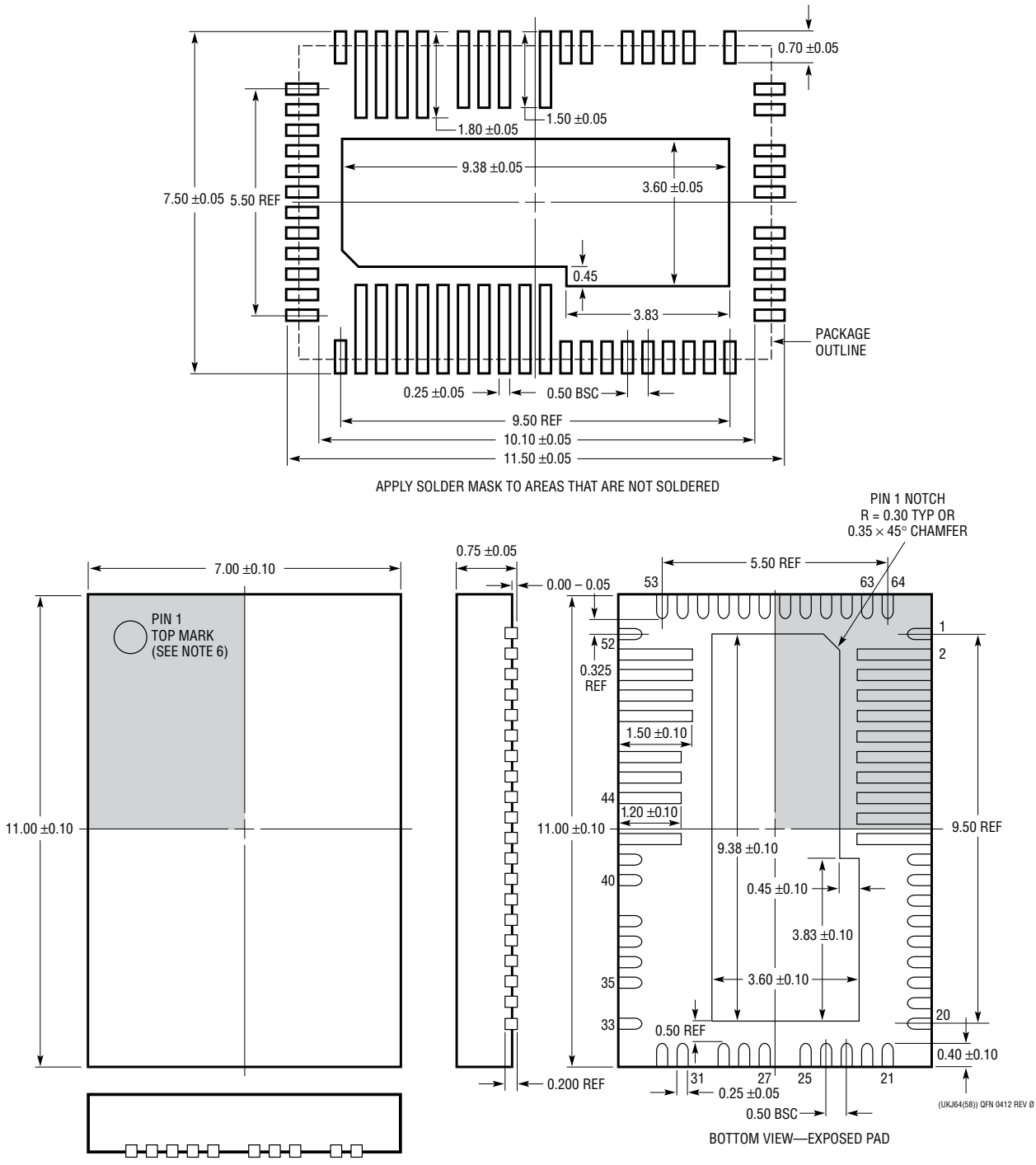
REGISTER NAME	I²C REG ADDR	VALUE
CFG_RSENSE1	0x28	0x01FA → (5mΩ)
CFG_RIMON_OUT	0x2A	0x2620 → (97.6kΩ)
CFG_RSENSE2	0x2C	0x03E8 → (10mΩ)
CFG_RDACO	0x2E	0x35C0 → (137.6kΩ)
CFG_RFBOUT1	0x30	0x2710 → (1MΩ)
CFG_RFBOUT2	0x32	0x07D0 → (20kΩ)
CFG_RDACI	0x34	0x0250 → (5.92kΩ)
CFG_RFBIN2	0x36	0x0144 → (3.09kΩ)
CFG_RFBIN1	0x38	0x03AE → (133kΩ)
CFG_VS3_25C	0x3B	0x7A → (97.2%)
CFG_TBAT_MIN	0x40	0xEC → (–20°C)
CFG_TBAT_MAX	0x41	0x32 → (50°C)
CFG_TMR_S0	0x42	0x00
CFG_TMR_S1	0x43	0x00
CFG_TMR_S2	0x44	0x00
CFG_TMR_S3	0x45	0x00
CFG_RSTRT_IN_S3 [0]	0x49	1b
CFG_CHRG_MISC [2:0]	0x4D	111b

I²C ADDRESS: 0x10
56.8V STAGE 2 (ABSORPTION) CHARGE VOLTAGE (V_{S2}) AT 25°C
55.2V STAGE 3 (FLOAT) CHARGE VOLTAGE (V_{S3}) AT 25°C
5A CHARGING CURRENT LIMIT
1.25A TRICKLE CURRENT LIMIT
11.4A INPUT CURRENT LIMIT
80V MAXIMUM PANEL VOLTAGE (V_{MAX})
NO TIMER LIMITS
TEMPERATURE COMPENSATION ENABLED
–20°C TO 50°C BATTERY TEMPERATURE RANGE
145kHz SWITCHING FREQUENCY
EXAMPLE SOLAR PANEL: SHARP NT-175UC1 175W,
SHARP NU-U235F3 235W

M1: INFINEON BSC046N10NS
M2: INFINEON BSC109N10NS
M3, M4: INFINEON BSC057N08NS
L1: 15µH COILCRAFT SER2915H-153KL, 15µH WURTH 744 364 115 00
D_{B1}, D_{B2}: CENTRAL SEMI CMMR1U-02
C_{IN1}, C_{OUT1}: 220µF, 100V, UNITED CHEMI-CON EKZE101ELL221MK255
C_{IN2}, C_{IN3}, C_{IN4}: 2.2µF, 100V, AVX 12101C225KAT2A
C_{OUT2}, C_{OUT3}: 4.7µF, 100V, TDK C4532X7S2A475M230KB
C_{OUT4}: 1µF, 100V AVX 12101C105KAT2A
C_{CSPOUT}: 100nF, 50V, AVX 08055C10

PACKAGE DESCRIPTION

UKJ Package
Variation: UKJ64(58)
64(58)-Lead Plastic QFN (7mm × 11mm)
(Reference LTC DWG # 05-08-1922 Rev Ø)



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2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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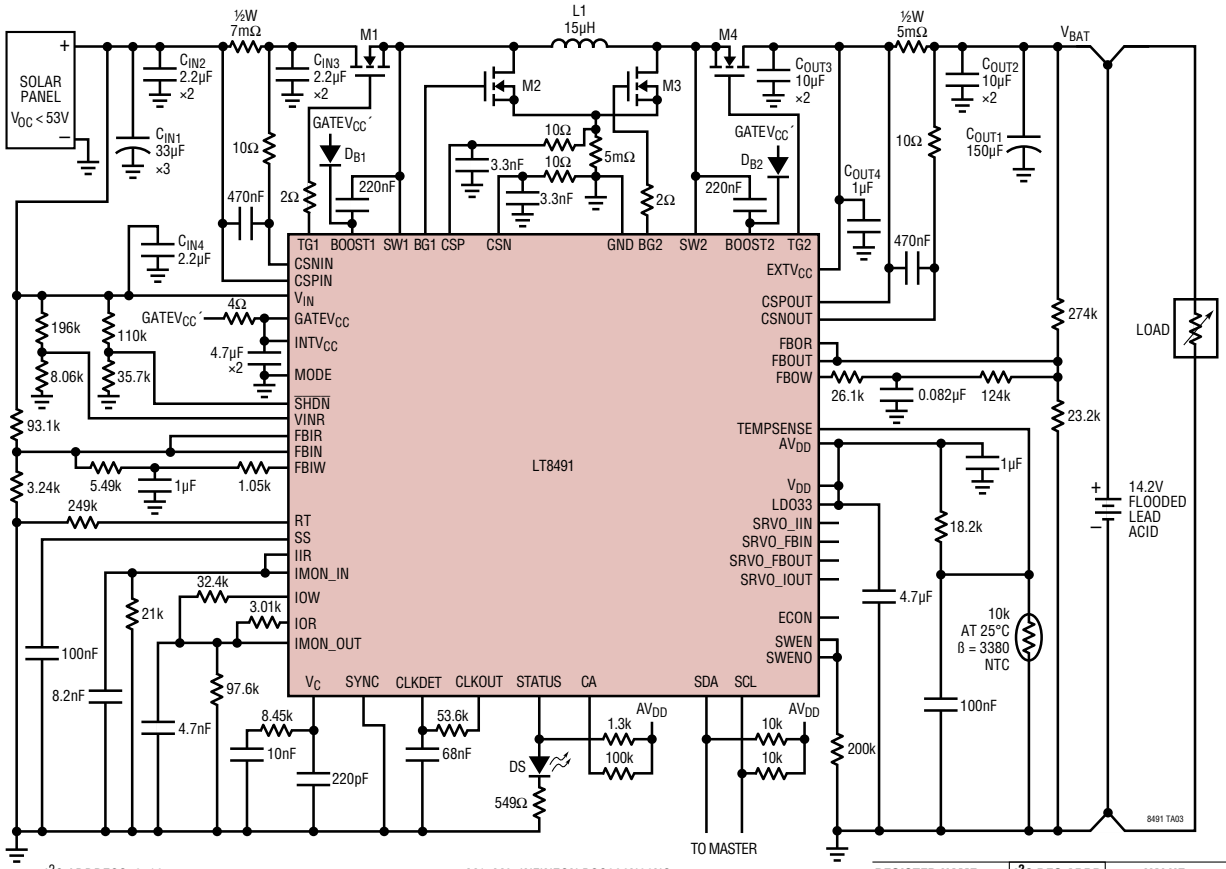
TYPICAL APPLICATION

14.2V Flooded Lead-Acid Battery Charger



I²C ADDRESS: 0x10
14.27V STAGE 2 (ABSORPTION) CHARGE VOLTAGE (V_{S2}) AT 25°C
13.87V STAGE 3 (FLOAT) CHARGE VOLTAGE (V_{S3}) AT 25°C
10A CHARGING CURRENT LIMIT
2.5A TRICKLE CURRENT LIMIT
7.2A INPUT CURRENT LIMIT
53V MAXIMUM PANEL VOLTAGE (V_{MAX})
NO TIMER LIMITS
TEMPERATURE COMPENSATION ENABLED
–20°C TO 50°C BATTERY TEMPERATURE RANGE
175kHz SWITCHING FREQUENCY
EXAMPLE SOLAR PANEL: SHARP NT-175UC1 175W

M1, M2: INFINEON BSC028N06NS
M3, M4: INFINEON BSC042N03LSG
L1: 15µH COILCRAFT SER2915H-153KL,
15µH WURTH 744 364 1500
D_{B1}, D_{B2}: CENTRAL SEMI CMMR1U-02
C_{IN1}: 33µF, 63V, SUNCON 63HVH33M
C_{IN2}, C_{IN3}, C_{IN4}: 2.2µF, 100V, AVX 12101C225KAT2A
C_{OUT1}: 150µF, 25V SUNCON 25HVH 150M
C_{OUT2}, C_{OUT3}: 10µF, 35V, MURATA GRM32ER7YA106KA2L
C_{OUT4}: 1µF, 25V AVX 12063C105KAT2A

REGISTER NAME	I²C REG ADDR	VALUE
CFG_RSENSE1	0x28	0x02BC→(7mΩ)
CFG_RIMON_OUT	0x2A	0x2620→(97.6kΩ)
CFG_RSENSE2	0x2C	0x01FA→(5mΩ)
CFG_RDACO	0x2E	0x3AA2→(150.1kΩ)
CFG_RFBOUT1	0x30	0x0AB4→(274kΩ)
CFG_RFBOUT2	0x32	0x0910→(23.2kΩ)
CFG_RDACI	0x34	0x028E→(6.54kΩ)
CFG_RFBIN2	0x36	0x0144→(3.24kΩ)
CFG_RFBIN1	0x38	0x03AE→(93.1kΩ)
CFG_VS3_25C	0x3B	0x7A→(97.2%)
CFG_TBAT_MIN	0x40	0xEC→(–20°C)
CFG_TBAT_MAX	0x41	0x32→(50°C)
CFG_TMR_S0	0x42	0x00
CFG_TMR_S1	0x43	0x00
CFG_TMR_S2	0x44	0x00
CFG_TMR_S3	0x45	0x00
CFG_RSTRT_IN_S3 [0]	0x49	1b
CFG_CHRG_MISC [2:0]	0x4D	111b

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8490	High Voltage, High Current Buck-Boost Battery Charger with MPPT	V_{IN} Range = 6V to 80V, V_{BAT} Range = 1.3V to 80V
LT3652/LT3652HV	Power Tracking 2A Battery Charger for Solar Power	V_{IN} Range = 4.95V to 32V (LT3652), 4.95V to 34V (HV), MPPC
LTC4000-1	High Voltage, High Current Controller for Battery Charger with MPPC	V_{IN} and V_{OUT} Range = 3V to 60V, MPPC
LTC4200	55V V_{IN}/V_{OUT} Buck-Boost Multi-Chemistry Battery Charging Controller	Li-Ion and Lead-Acid Algorithms, MPPC

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