THE DATASHEET OF

NCS20282FCTTAG

ON Semiconductor

Is Now

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Dual Operational Amplifier, 7 MHz Bandwidth with Shutdown

NCS20282

ON Semiconductor®

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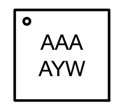
WLCSP9
CASE 567UW

WLCSP9
CASE 567YD

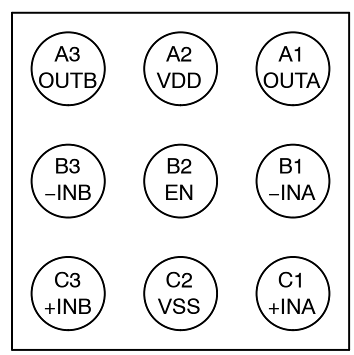
MARKING DIAGRAM



AAA = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

(Note: Microdot may be in either location)

PIN CONNECTIONS



Package Bottom View (Bump Up)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

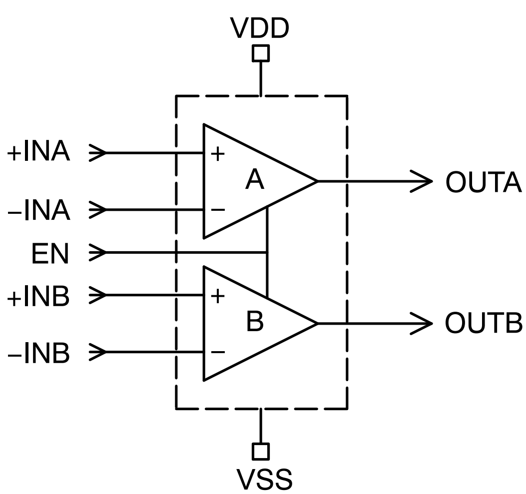
The NCS20282 high precision op amp features a wide bandwidth along with shutdown. These amplifiers provide low bias current useful for transimpedance applications. The wide bandwidth eases the design of active filters. The NCS20282 is specified for operation from −40°C to +125°C.

Features

- High Bandwidth: 7 MHz typical
- Low Bias Current: 50 pA typical
- Rail−to−Rail Input/Output
- Shutdown Current: 1 μA max
- Offset Voltage: 1.5 mV max
- Offset Drift: 10 μV/°C max
- Supply Voltage: 2.5 V to 5.5 V
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Transducer Applications
- Sensor Conditioning
- Medical Instrumentation
- Impedance Sensing



This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

Table 1. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage (VDD− VSS)	7	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	(V_{SS} – 0.5) to 7	V
Input Current (Note 1)	±5	mA
Output Pin Voltage, Disabled	7	V
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	–40 to +125	°C
Storage Temperature	–65 to +150	°C
Junction Temperature	+150	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	1000	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.
2. Short−circuit to ground.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017
   ESD Charged Device Model tested per JEDEC standard JS−002−2014
4. Latch−up Current tested per JEDEC standard: JESD78

Table 2. THERMAL INFORMATION

Parameter	Symbol	Cu Area mm^2	1.0 oz	2.0 oz	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	10	301	263	°C/W
		25	263	230	
		40	246	215	
		80	229	204	
		140	220	196	
		250	211	188	
		350	206	183	
		500	200	179	
		650	197	175	
		800	194	173	

NOTE: Four layer JSEC JESD51−7

Table 3. OPERATING CONDITIONS

Parameter	Symbol	Range	Units
Supply Voltage (V_{DD} – V_{SS})	V_S	2.5 to 5.5	V
Specified Operating Temperature Range	T_A	–40 to +125	°C
Input Common Mode Voltage Range	V_{CM}	V_{SS} to V_{DD}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS: V_S = 2.5 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ, V_{CM} = V_{OUT} = midsupply, Enable input connected to V_{DD}, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			300	1500	µV
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$			**2**	**10**	µV/°C
Input Bias Current (Note 5)	I_{IB}			50	**800**	pA
Input Offset Current	I_{OS}			10		pA
Input Common–Mode Voltage Range	V_{CM}			V_{SS} to V_{DD}		V
Common Mode Rejection Ratio	CMRR	V_{CM} = –0.1V to (V_{DD}+0.1V)	66	86		dB
Input Resistance	R_{IN}	Differential		10		GΩ
		Common Mode		10		
Input Capacitance	C_{IN}	Differential		2		pF
		Common Mode		5		
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	0.4 V ≤ V_{OUT} ≤ V_{DD} – 0.4 V	96	116		dB
Closed Loop Output Impedance	Z_{OUT_CL}	See Figure 23		See Figure 23		Ω
Output Voltage High, Referenced to V_{DD}	V_{OH}			V_{DD}–3	**V_{DD}–10**	mV
Output Voltage Low, Referenced to V_{SS}	V_{OL}			V_{SS}+6	**V_{SS}+10**	mV
Short Circuit Current (Note 5)	I_{SC}	Sinking Current		10	**15**	mA
		Sourcing Current		10	**15**	
Capacitive Load Drive (Note 5)	C_L			100	300	pF
DYNAMIC PERFORMANCE						
Gain Bandwidth Product (Note 5)	GBW	V_S = 3 V; R_L = 10 kΩ, C_L = 100 pF	5.4	7		MHz
Gain Margin	A_M	C_L = 100 pF		50		dB
Phase Margin	Ψ_M	C_L = 100 pF		55		°
Slew Rate	SR	A_V = +1		5		V/µs
Overload Recovery Time	t_{OR}	V_{IN} X A_V > V_S		1		µs
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f_{IN} = 10 kHz		20		nV/√Hz
Current Noise Density	i_N	f_{IN} = 1 Hz		300		fA/√Hz
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR		90	120		dB
Shutdown Enable Time (Notes 5, 6)	t_{ON}			30	50	µs
Shutdown Disable Time (Note 6)	t_{OFF}			30		µs
Shutdown Leakage – Input		V_{IN} = V_S+400 mV			**500**	nA
Shutdown Leakage – Output		V_{OUT} = V_S+1 V			**500**	
Enable Input Threshold Voltage	$V_{th(EN)}$	Operating	1.3			V
		Disabled			0.5	
Enable Input Leakage Current	I_{Enable}	Enable = + 5.0 V		1.1		µA
		Enable = V_{SS}		1.1		
Quiescent Current	I_Q	Per Channel No load – Quiescent		850	1300	µA
		Per Channel No load – Shutdown		0.3	1	

5. Guaranteed by design and/or characterization
6. Shutdown Disable Time (t_{OFF}) and Enable Time (t_{ON}) are defined as the time between the 50% point of the signal applied to the EN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

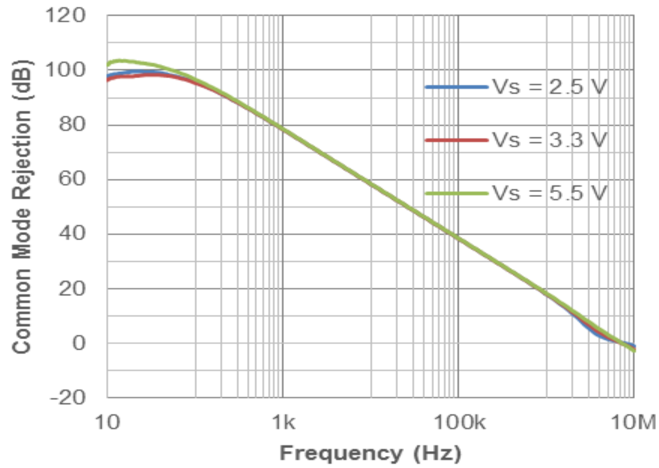


Figure 1. CMRR vs. Frequency

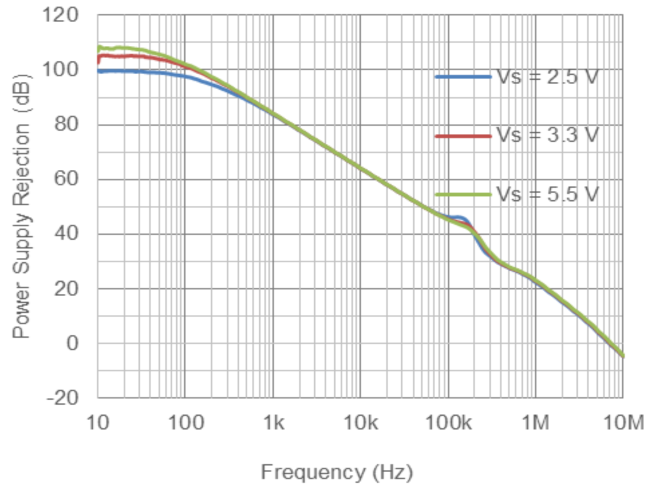


Figure 2. PSRR vs. Frequency

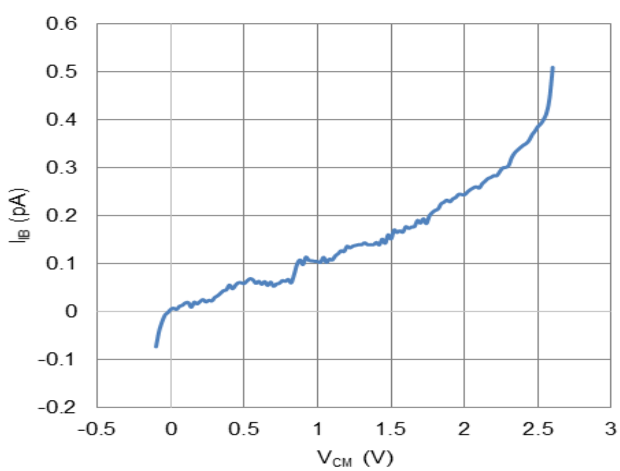


Figure 3. Input Bias Current vs. V_{CM} at V_S = 2.5 V

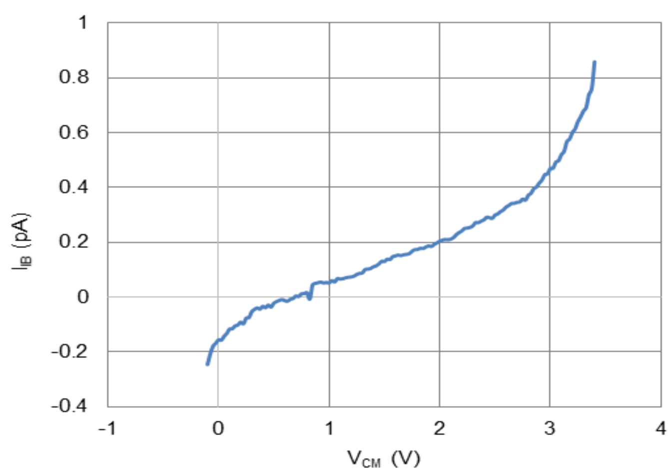


Figure 4. Input Bias Current vs. V_{CM} at V_S = 3.3 V

TYPICAL CHARACTERISTICS

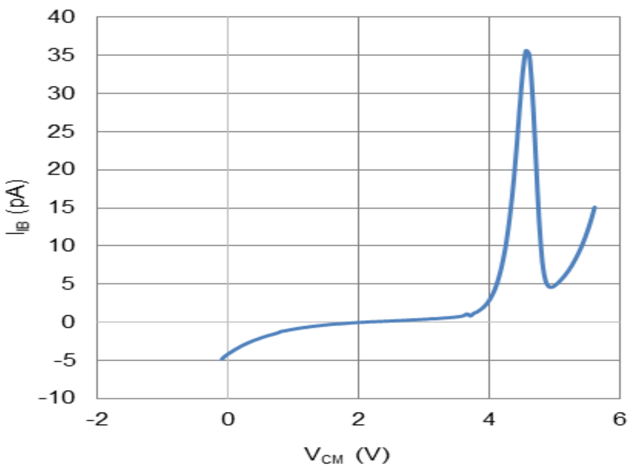


Figure 5. Input Bias Current vs. V_{CM} at V_S = 5.5 V

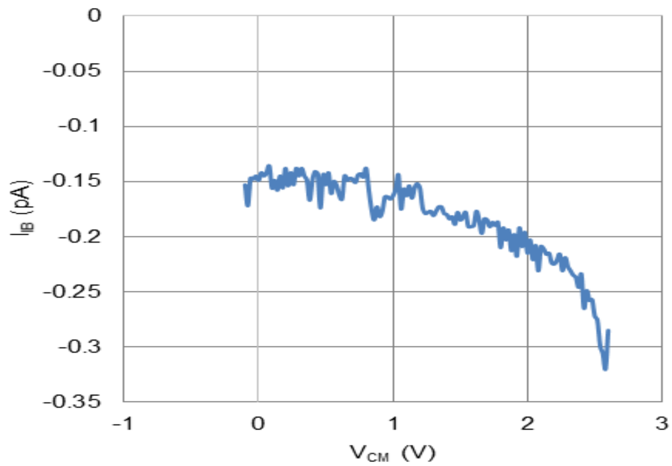


Figure 6. Input Offset Current vs. V_{CM} at V_S = 2.5 V

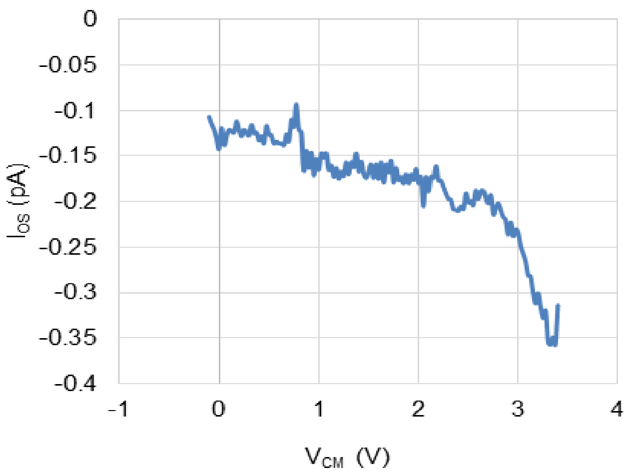


Figure 7. Input Offset Current vs. V_{CM} at V_S = 3.3 V

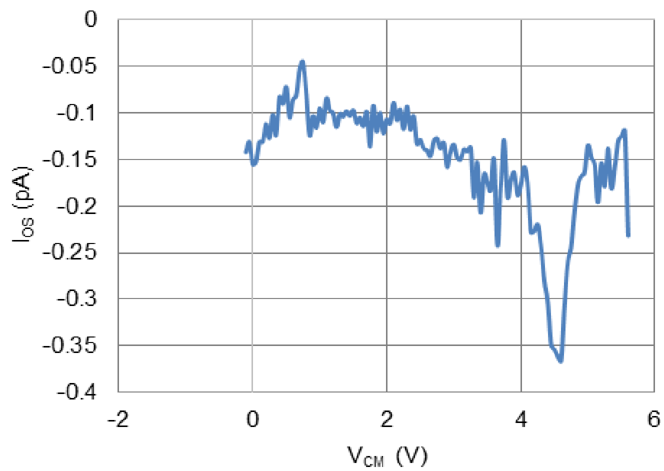


Figure 8. Input Offset Current vs. V_{CM} at V_S = 5.5 V

TYPICAL CHARACTERISTICS

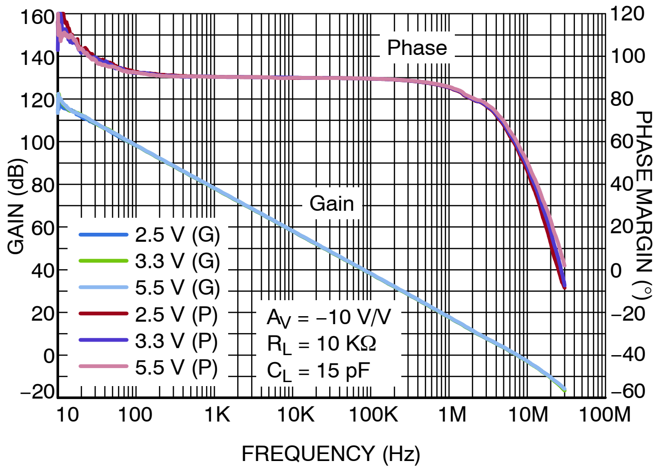


Figure 9. Open Loop Gain and Phase Margin vs. Frequency

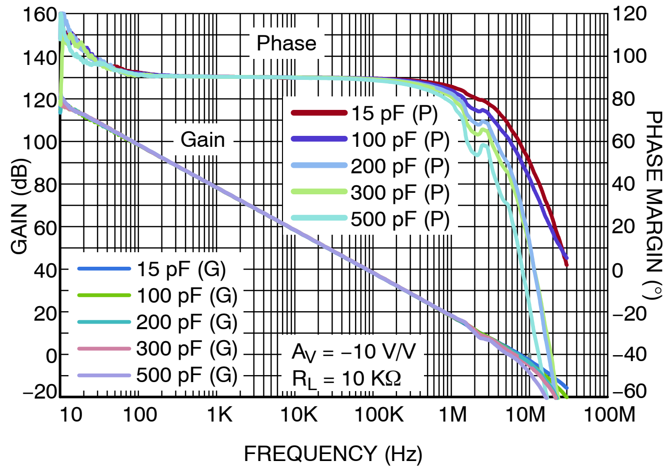


Figure 10. Open Loop Gain and Phase Margin vs. CL

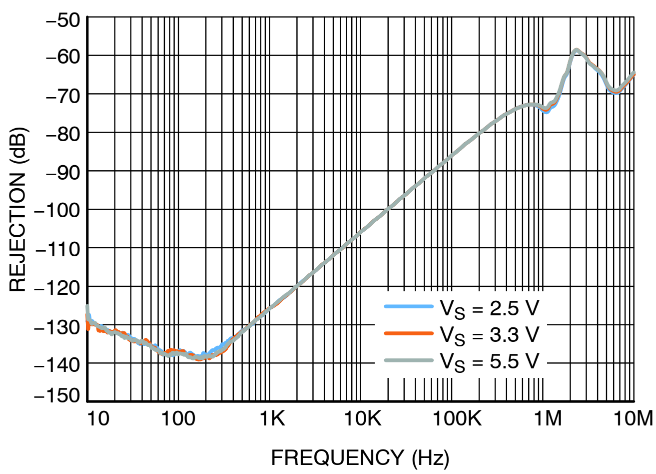


Figure 11. Channel Separation

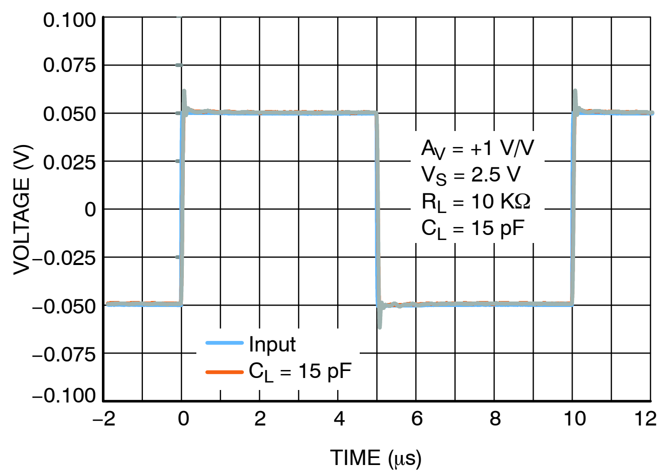


Figure 12. Non Inverting Small Signal Transient Response

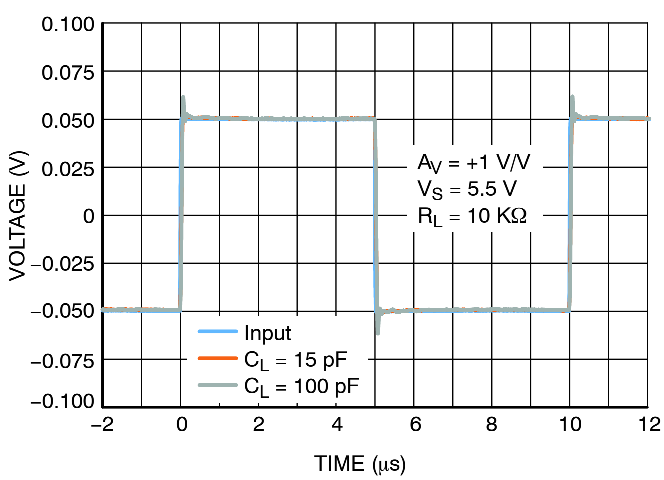


Figure 13. Non Inverting Small Signal Transient Response

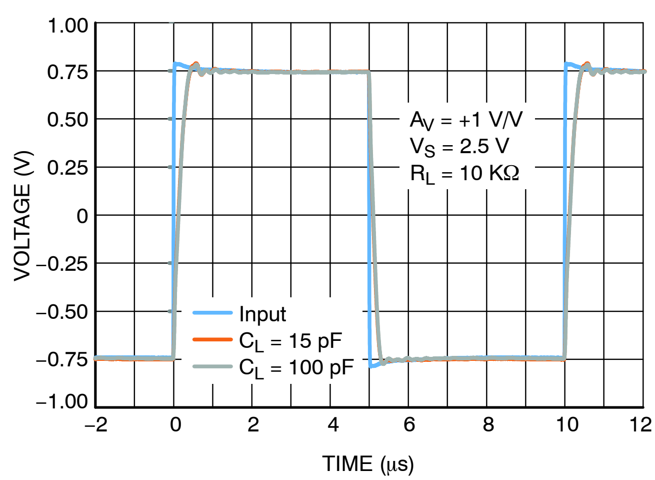


Figure 14. Non Inverting Large Signal Transient Response

TYPICAL CHARACTERISTICS

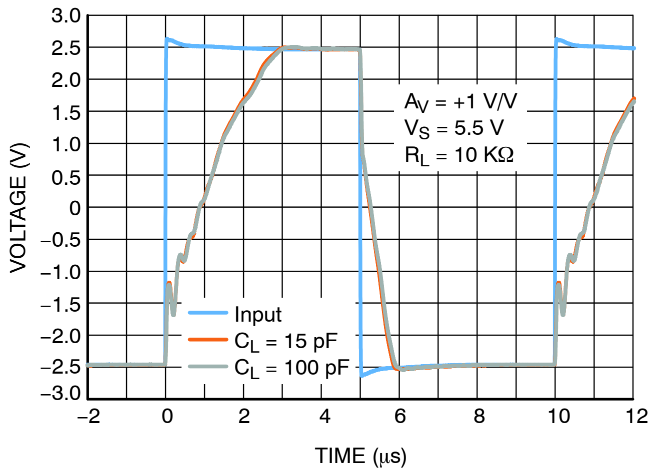


Figure 15. Non Inverting Large Signal Transient Response

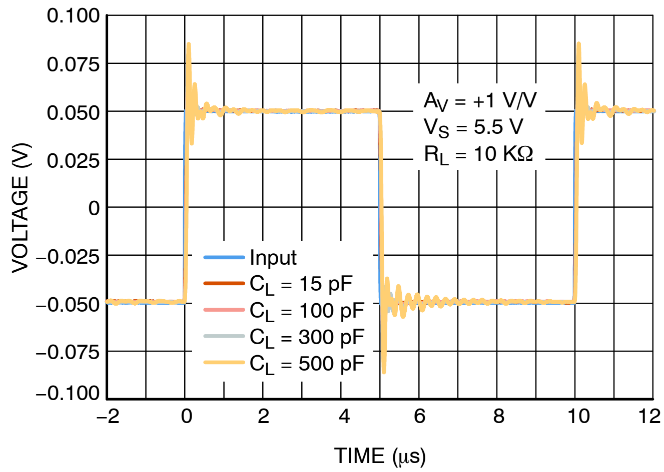


Figure 16. Non Inverting Large Signal Transient Response vs. C_{Load}

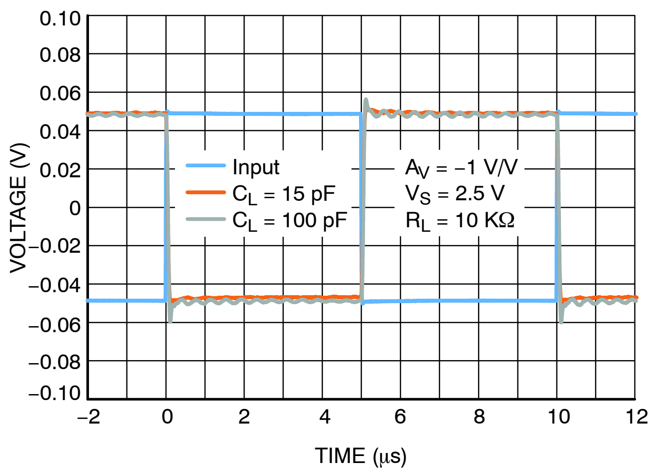


Figure 17. Inverting Small Signal Transient Response

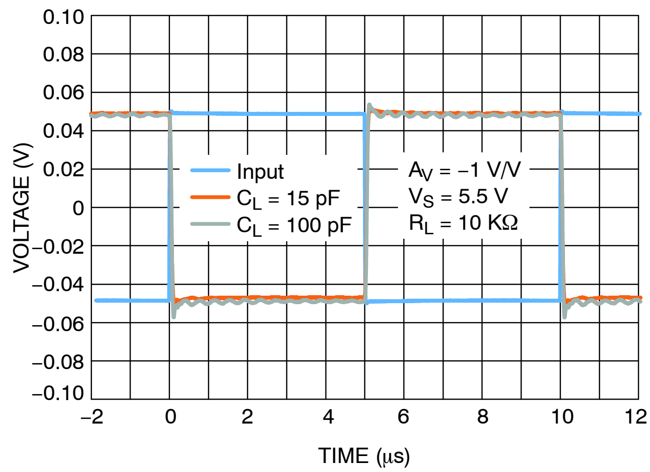


Figure 18. Inverting Small Signal Transient Response

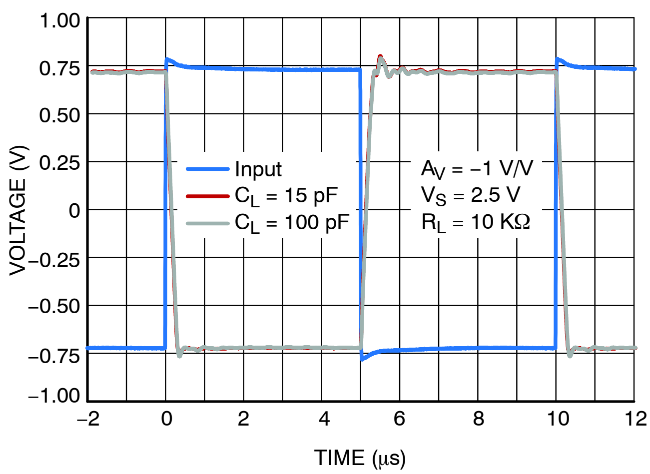


Figure 19. Inverting Large Signal Transient Response

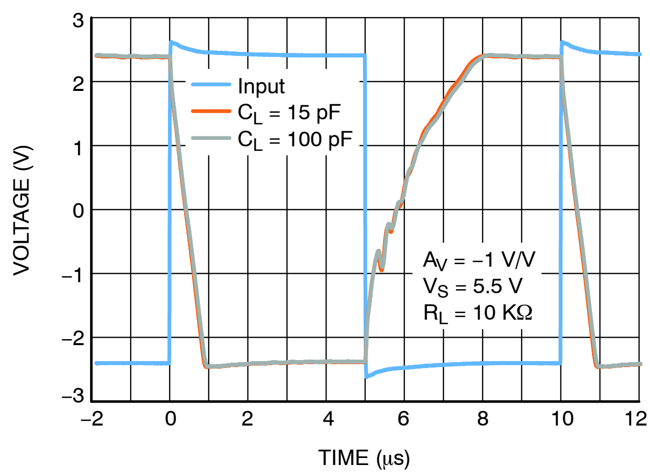


Figure 20. Inverting Large Signal Transient Response

TYPICAL CHARACTERISTICS

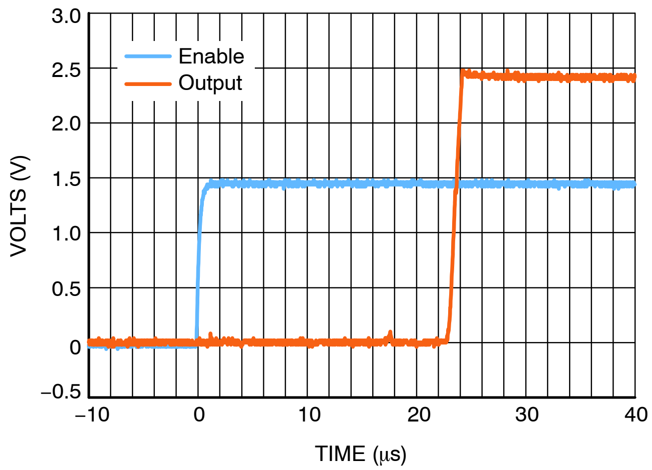


Figure 21. Enable Turn−On Time

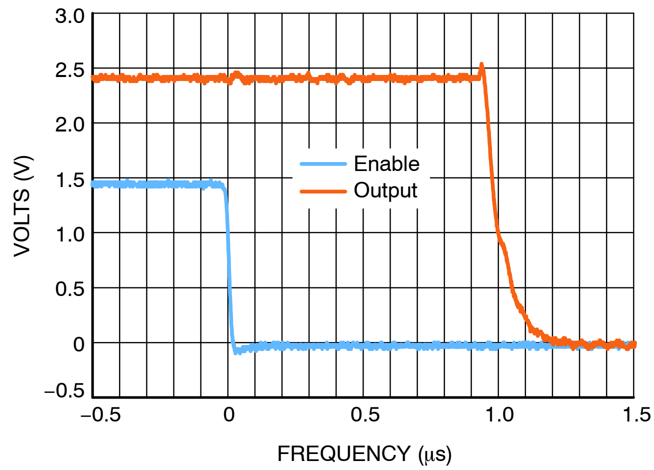


Figure 22. Disable Turn−Off Time

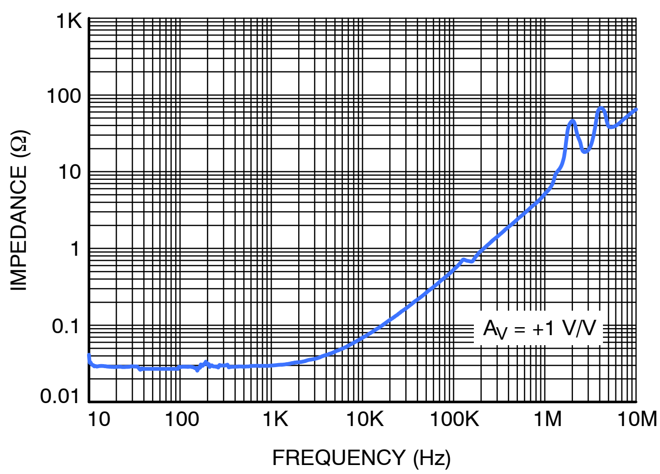


Figure 23. Closed Loop Output Impedance

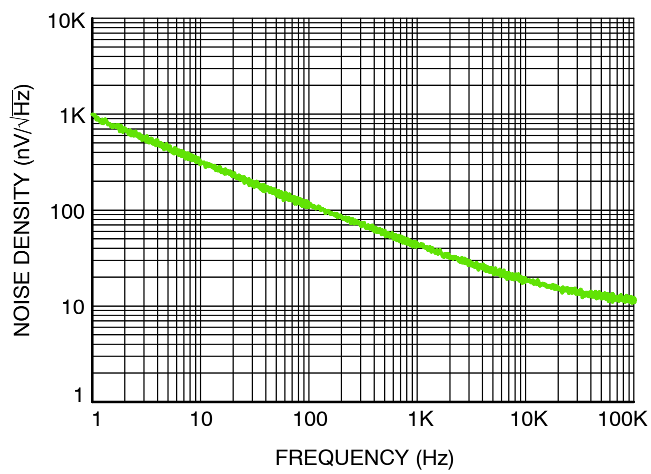


Figure 24. Voltage Noise Density vs. Frequency

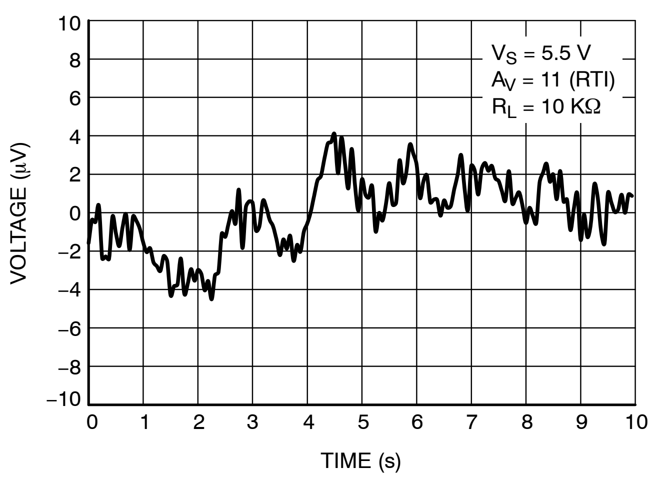


Figure 25. 0.1 Hz to 10 Hz Noise

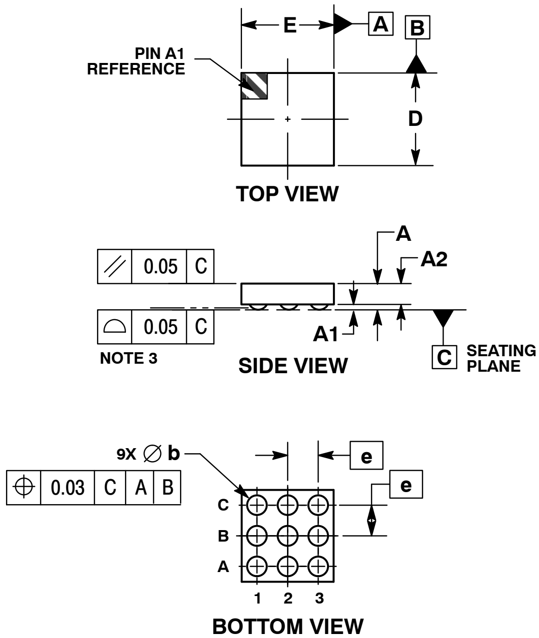
DEVICE ORDERING INFORMATION

Device	Marking	Bump Type	Case Outline	Package	Shipping†
NCS20282FCTTAG	AAA	Sn Plate	567UW	WLCSP−9 (Pb−Free)	5000 / Tape & Reel
NCS20282FCSTAG* (In Development)	AAA	SAC 405	567YD	WLCSP−9 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

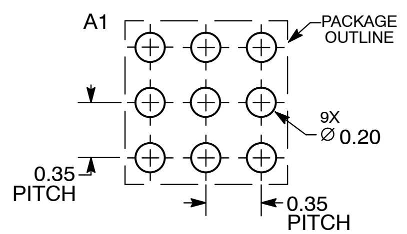
WLCSP9, 1.02x1.02x0.33
CASE 567UW
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	0.33
A1	0.04	0.06	0.08
A2		0.23 REF	
b	0.180	0.200	0.220
D	0.99	1.02	1.05
E	0.99	1.02	1.05
e		0.35 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

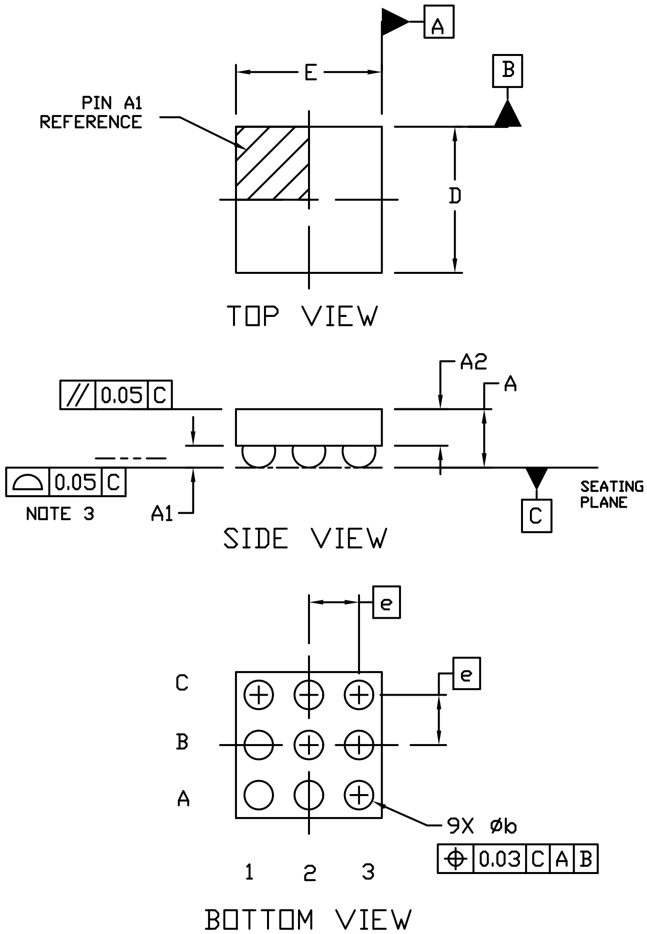


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

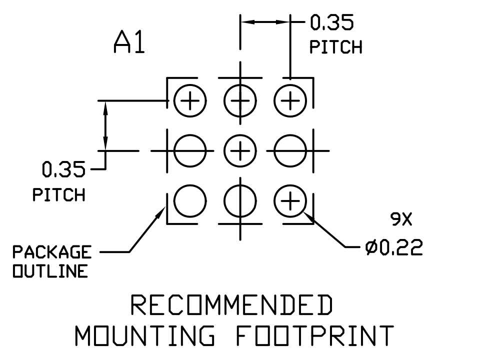
WLCSP9, 1.02x1.02x0.441
CASE 567YD
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS MIN.	NOM.	MAX.
A	---	---	0.441
A1	0.133	0.153	0.173
A2	0.255 REF		
b	0.183	0.203	0.223
D	0.99	1.02	1.05
E	0.99	1.02	1.05
e	0.35 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
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