THE DATASHEET OF

LTM8071EY#PBF

LTM8071

$60V_{IN}$, 5A Silent Switcher µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Low Noise Silent Switcher® Architecture**
- **CISPR22 Class B Compliant**
- **Wide Input Voltage Range: 3.6V to 60V**
- **Wide Output Voltage Range: 0.97V to 15V**
- **5A Continuous Output Current at 24_{IN}, $3.3V_{OUT}$, T_A = 85°C**
- **7.25A Peak Current at $12V_{IN}$, $3.3V_{OUT}$**
- **Parallelable for Increased Output Current**
- Selectable Switching Frequency: 200kHz to 2.2MHz
- Programmable Soft-Start
- 9mm × 11.25mm × 3.32mm RoHS Compliant BGA Package

APPLICATIONS

- Test and Measurement Equipment
- Aviation
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

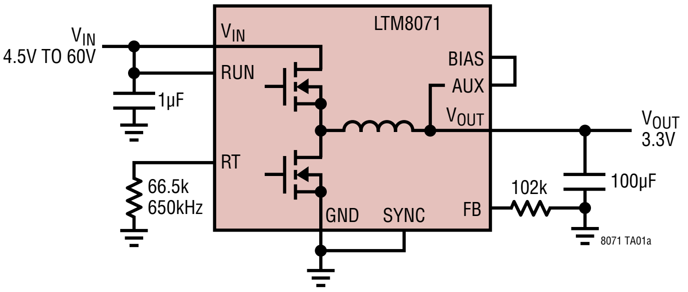
DESCRIPTION

The LTM®8071 is a $60V_{IN}$, 5A (continuous) step-down Silent Switcher µModule® (power module) regulator. The Silent Switcher architecture minimizes EMI while delivering high efficiency at frequencies up to 2.2MHz. Included in the package are the switching controller, power switches, inductor, and all support components. Operating over an input voltage range of 3.6V to 60V, the LTM8071 supports an output voltage range of 0.97V to 15V and a switching frequency range of 200kHz to 2.2MHz, each set by a single resistor. Only the input and output filter capacitors are needed to finish the design.

The LTM8071 is packaged in a compact over-molded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8071 is available with SnPb (BGA) or RoHS compliant terminal finish.

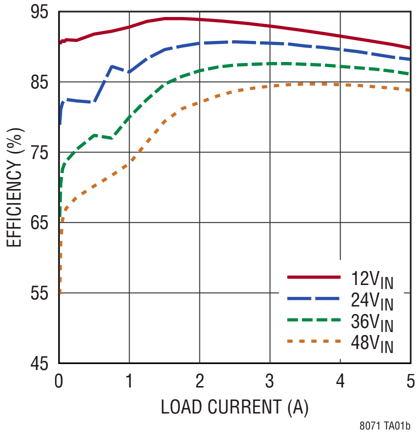
TYPICAL APPLICATION

$3.3V_{OUT}$ from $4.5V_{IN}$ to $60V_{IN}$ Step-Down Converter



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG, SHARE

Efficiency, V_{OUT} = 3.3V, BIAS = 3.3V

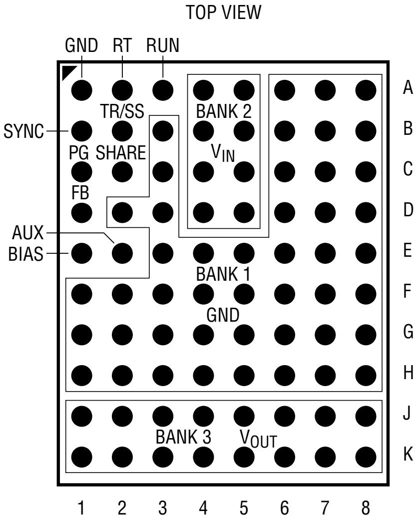


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 4)

V_{IN}, RUN Voltage	65V
PG Voltage	42V
AUX, V_{OUT}, BIAS Voltage	19V
FB, TR/SS Voltage	4V
SYNC Voltage	6V
Maximum Internal Temperature	125°C
Storage Temperature	–50°C to 125°C
Peak Reflow Solder Body Temperature	250°C

PIN CONFIGURATION



BGA PACKAGE
80-LEAD (11.25mm × 9mm × 3.32mm)

T_{JMAX} = 125°C, θ_{JA} = 18°C/W, $\theta_{JCbottom}$ = 3.4°C/W,
θ_{JCtop} = 8.4°C/W, θ_{JB} = 2.8°C/W, WEIGHT = 1.0g
θ VALUES DETERMINED PER JESD 51-9, 51-12

ORDER INFORMATION

PART NUMBER	TERMINAL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (NOTE 3, 4)
		DEVICE	FINISH CODE			
LTM8071EY#PBF	SAC305 (RoHS)	LTM8071	e1	BGA	3	–40°C to 125°C
LTM8071IY#PBF						
LTM8071IY	SnPb (63/37)		e0			

- Contact the factory for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, RUN = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN} Rising	●			3.6	V
Output DC Voltage	R_{FB} Open			0.97		V
	R_{FB} = 16.9kΩ			15		V
Peak Output DC Current	V_{OUT} = 3.3V, f_{SW} = 1MHz		7.25			A
Quiescent Current Into V_{IN}	RUN = 0V				3	µA
	BIAS = 0V, No Load, SYNC = 0V, Not Switching				300	µA
Quiescent Current Into BIAS	BIAS = 5V, RUN = 0V				1	µA
	BIAS = 5V, No Load, SYNC = 0V, Not Switching				275	µA
	BIAS = 5V, V_{OUT} = 3.3V, I_{OUT} = 3.5A, f_{SW} = 1MHz				25	mA
Line Regulation	5.5V < V_{IN} < 36V, I_{OUT} = 1A			0.5		%
Load Regulation	0.1A < I_{OUT} < 3.5A			0.5		%
Output Voltage Ripple	I_{OUT} = 3.5A			10		mV
Switching Frequency	R_T = 232kΩ			200		kHz
	R_T = 41.2kΩ			1		MHz
	R_T = 15.8kΩ			2.2		MHz
Voltage at FB		●	955	970	985	mV
Minimum BIAS Voltage	(Note 5)				3.2	V
RUN Threshold Voltage	Run Rising		0.9		1.06	V
Run Leakage Current					1	µA
TR/SS Current	TR/SS = 0V			2		µA
TR/SS Pull-Down	TR/SS = 0.1V			200		Ω
PG Threshold Voltage at FB (Upper)	FB Falling (Note 6)			1.05		V
PG Threshold Voltage at FB (Lower)	FB Rising (Note 6)			0.89		V
PG Leakage Current	PG = 42V				1	µA
PG Sink Current	PG = 0.1V			150		µA
SYNC Threshold Voltage	Synchronization		0.4		1.5	V
SYNC Voltage	To Enable Spread Spectrum		2.9		4.2	V
SYNC Current	SYNC = 0V				35	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise noted, the absolute minimum voltage is zero.

Note 3: The LTM8071E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8071I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 4: The LTM8071 contains overtemperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

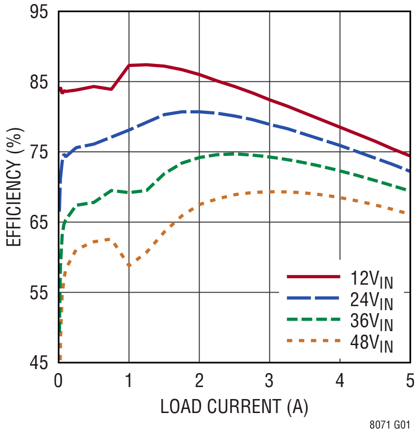
Note 5. Below this specified voltage, internal circuitry will draw power from V_{IN}.

Note 6. PG transitions from low to high.

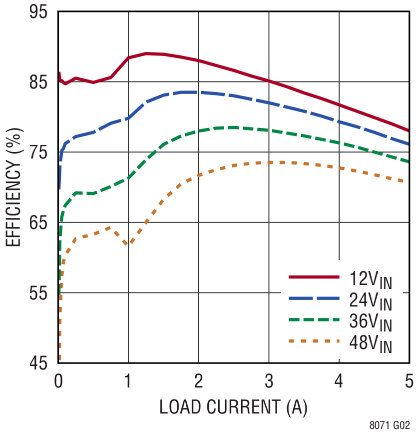
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

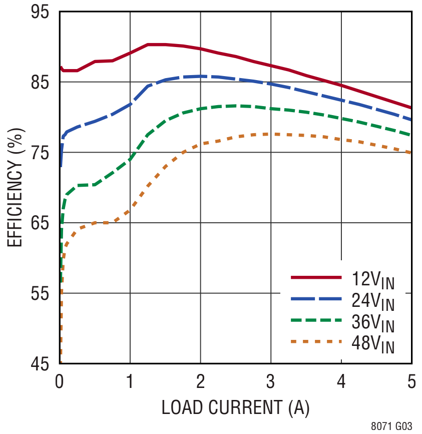
Efficiency vs Load Current
V_{OUT} = 0.97V, BIAS = 5V,
f_{SW} = 400kHz



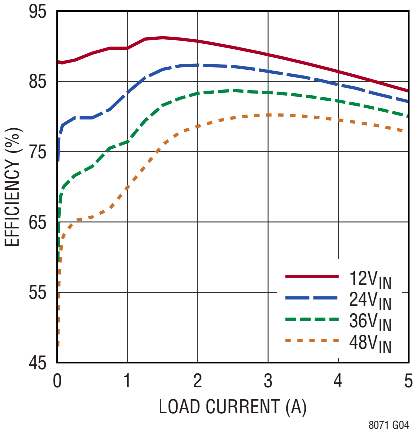
Efficiency vs Load Current
V_{OUT} = 1.2V, BIAS = 5V,
f_{SW} = 400kHz



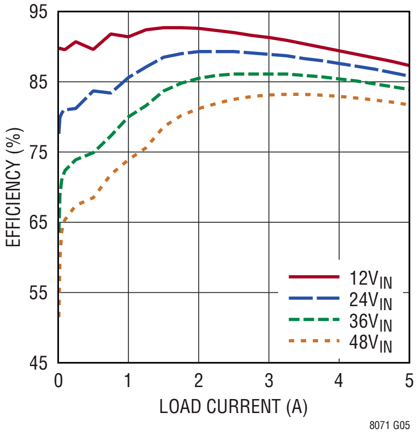
Efficiency vs Load Current
V_{OUT} = 1.5V, BIAS = 5V,
f_{SW} = 400kHz



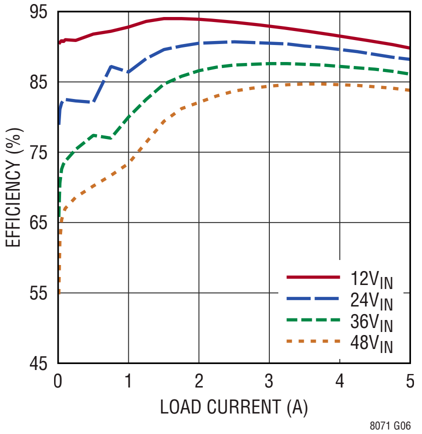
Efficiency vs Load Current
V_{OUT} = 1.8V, BIAS = 5V,
f_{SW} = 400kHz



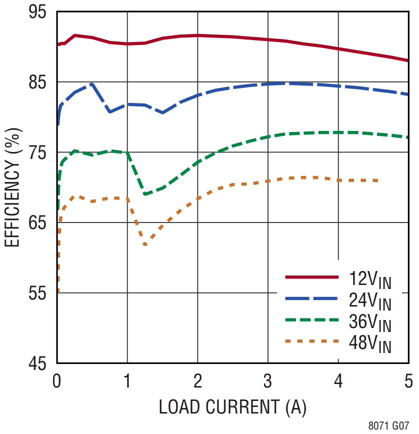
Efficiency vs Load Current
V_{OUT} = 2.5V, BIAS = 5V,
f_{SW} = 500kHz



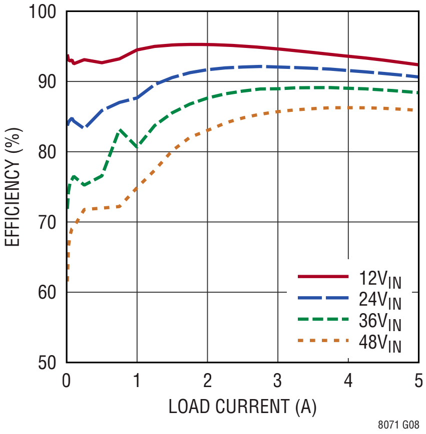
Efficiency vs Load Current
V_{OUT} = 3.3V, BIAS = 5V,
f_{SW} = 650kHz



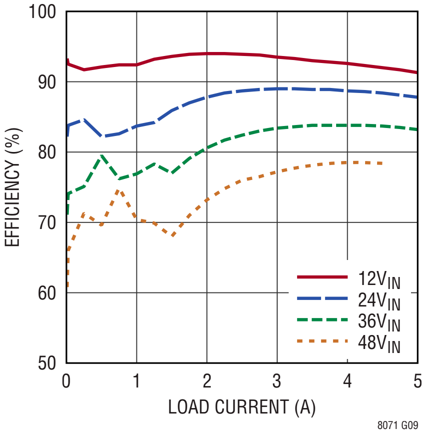
Efficiency vs Load Current
V_{OUT} = 3.3V, BIAS = 5V
f_{SW} = 2MHz



Efficiency vs Load Current
V_{OUT} = 5V, BIAS = 5V,
f_{SW} = 1MHz



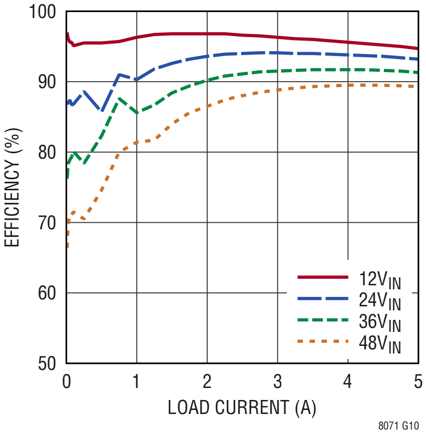
Efficiency vs Load Current
V_{OUT} = 5V, BIAS = 5V
f_{SW} = 2MHz



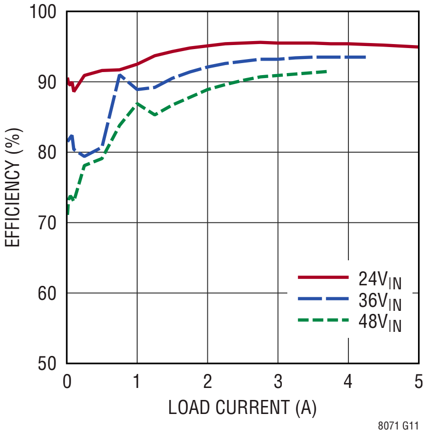
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

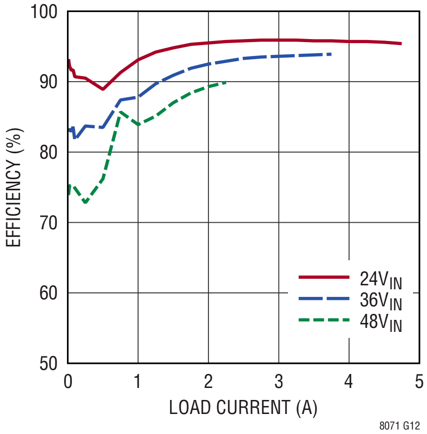
Efficiency vs Load Current
V_{OUT} = 8V, BIAS = 5V,
f_{SW} = 1.2MHz



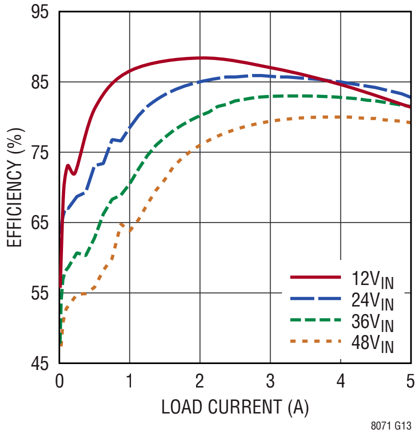
Efficiency vs Load Current
V_{OUT} = 12V, BIAS = 5V,
f_{SW} = 1.4MHz



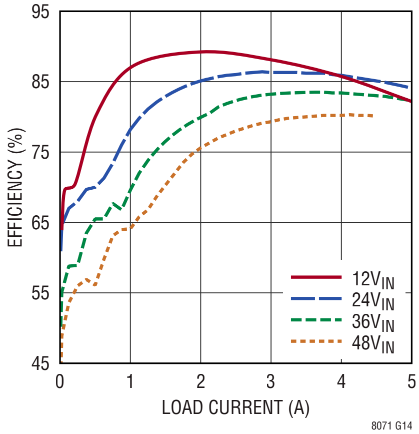
Efficiency vs Load Current
V_{OUT} = 15V, BIAS 5V,
f_{SW} = 1.8MHz



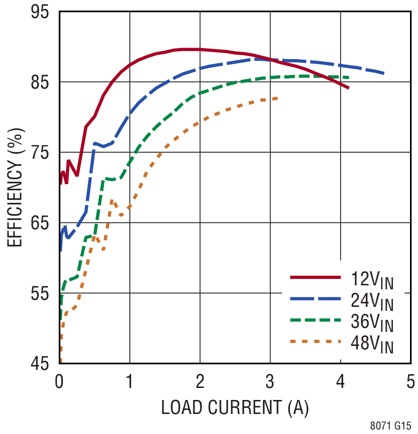
Efficiency vs Load Current
V_{OUT} = –3.3V, BIAS Tied to
LTM8071 GND, f_{SW} = 650kHz



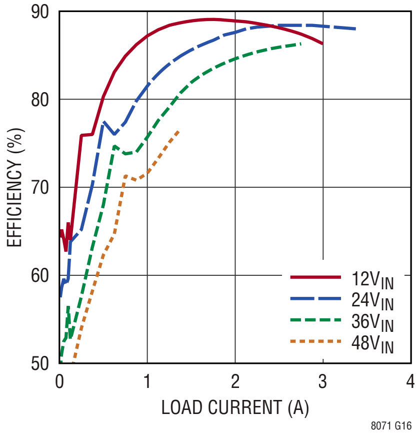
Efficiency vs Load Current
V_{OUT} = –5V, BIAS Tied to
LTM8071 GND, f_{SW} = 1MHz



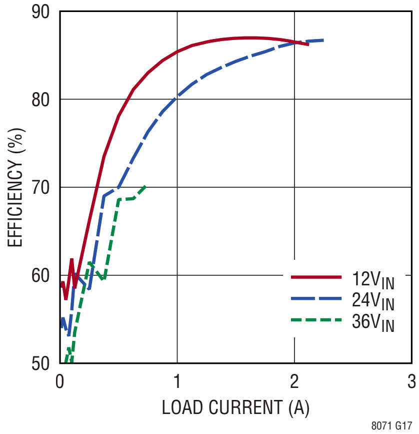
Efficiency vs Load Current
V_{OUT} = –8V, BIAS Tied to
LTM8071 GND, f_{SW} = 1.2MHz



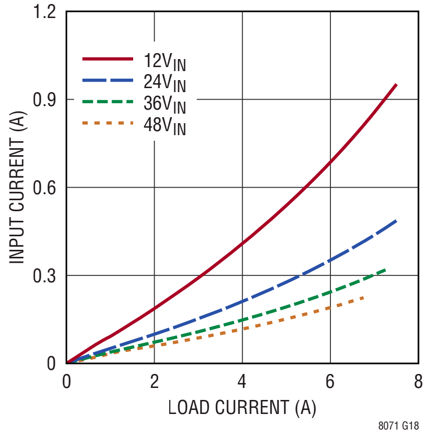
Efficiency vs Load Current
V_{OUT} = –12V, BIAS Tied to
LTM8071 GND, f_{SW} = 1.4MHz



Efficiency vs Load Current
V_{OUT} = –15V, BIAS Tied to
LTM8071 GND, f_{SW} = 1.8MHz



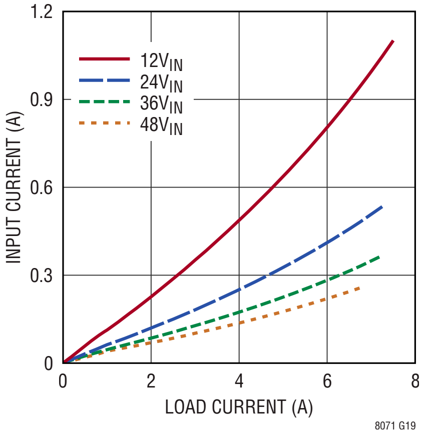
Input vs Load Current
V_{OUT} = 0.97V



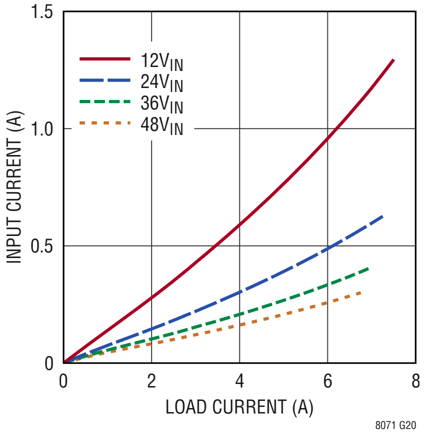
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, unless otherwise noted.

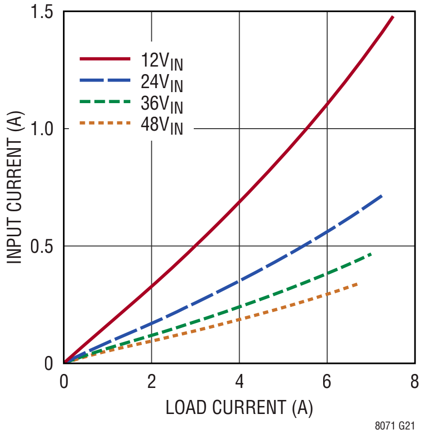
Input vs Load Current
$V_{OUT} = 1.2V$



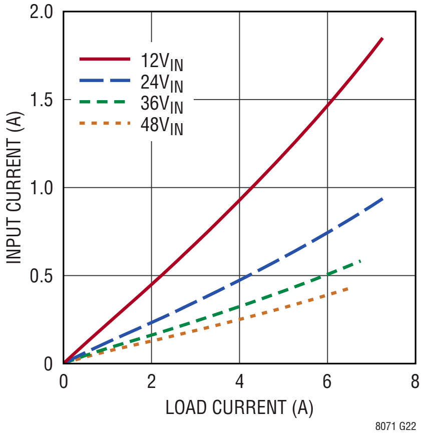
Input vs Load Current
$V_{OUT} = 1.5V$



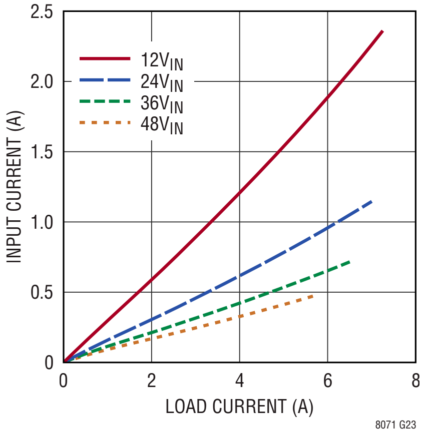
Input vs Load Current
$V_{OUT} = 1.8V$



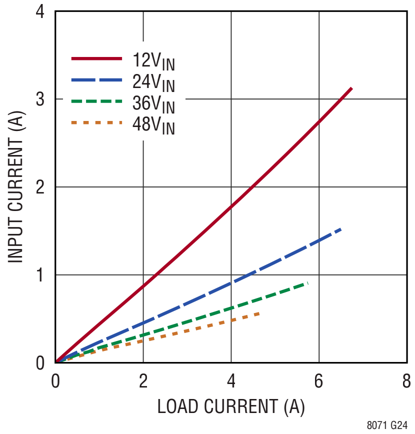
Input vs Load Current
$V_{OUT} = 2.5V$



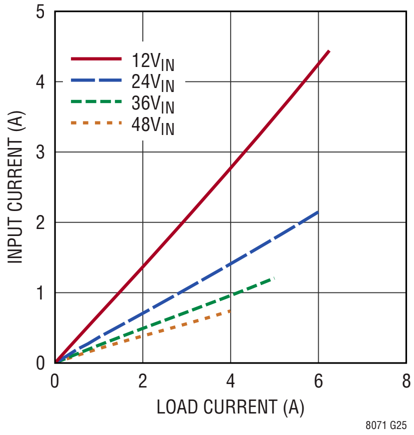
Input vs Load Current
$V_{OUT} = 3.3V$



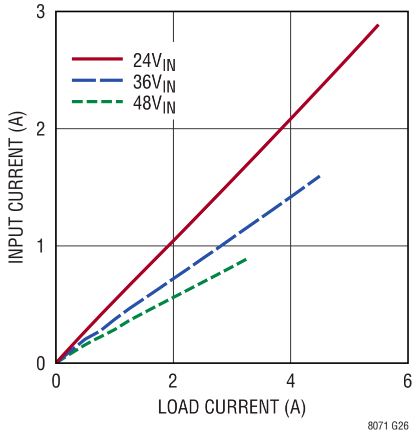
Input vs Load Current
$V_{OUT} = 5V$



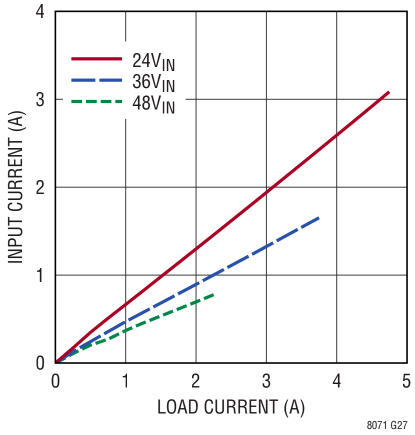
Input vs Load Current
$V_{OUT} = 8V$



Input vs Load Current
$V_{OUT} = 12V$



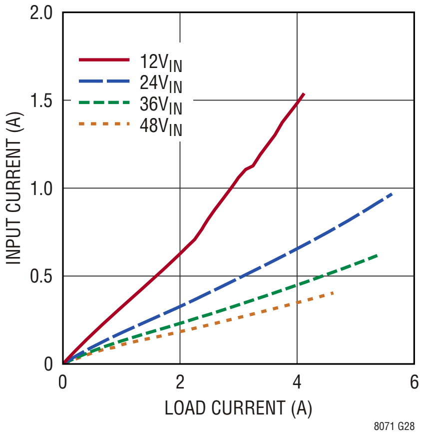
Input vs Load Current
$V_{OUT} = 15V$



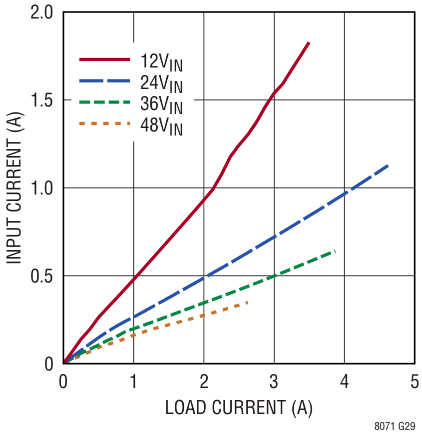
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

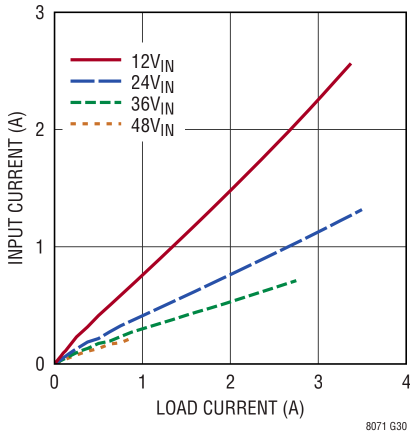
Input vs Load Current
V_{OUT} = –3.3V
BIAS Tied to LTM8071 GND



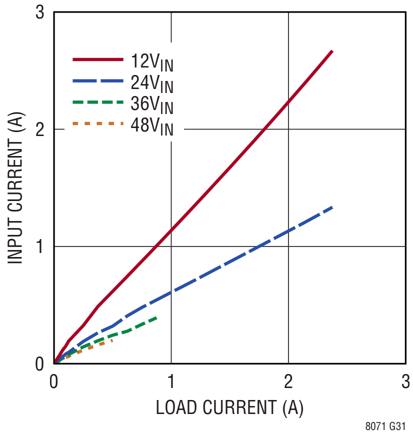
Input vs Load Current
V_{OUT} = –5V
BIAS Tied to LTM8071 GND



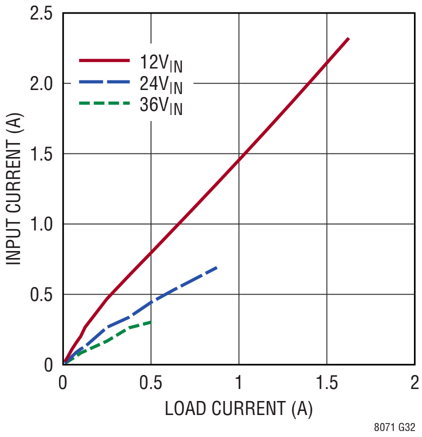
Input vs Load Current
V_{OUT} = –8V
BIAS Tied to LTM8071 GND



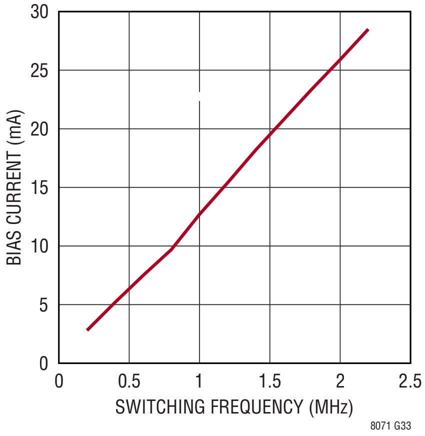
Input vs Load Current
V_{OUT} = –12V
BIAS Tied to LTM8071 GND



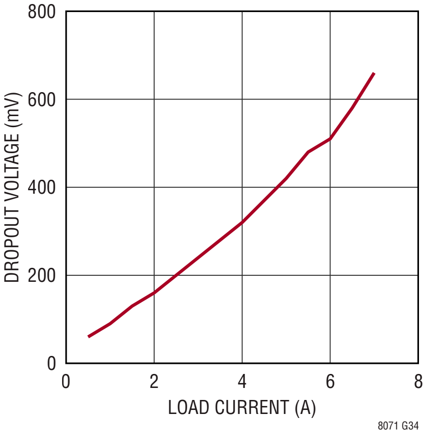
Input vs Load Current
V_{OUT} = –15V
BIAS Tied to LTM8071 GND



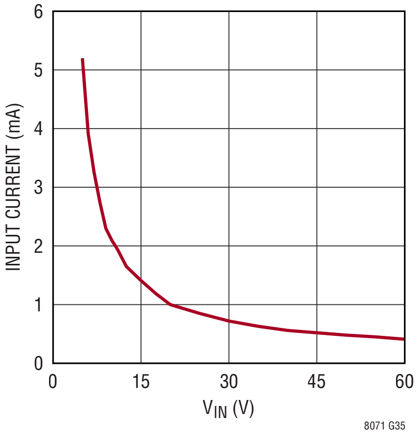
I_{BIAS} vs Switching Frequency
V_{BIAS} = 5V, V_{IN} = 24V, V_{OUT} = 5V



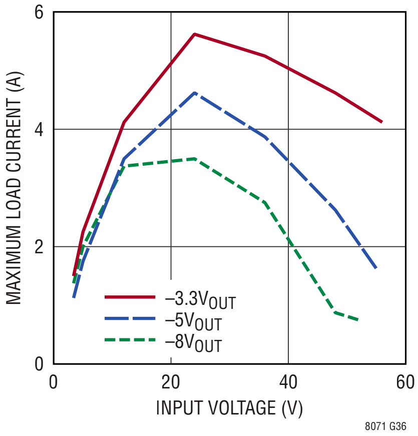
Dropout Voltage vs Load Current
V_{OUT} = 5V, BIAS = 5V



Input Current vs V_{IN}
V_{OUT} Short-Circuited



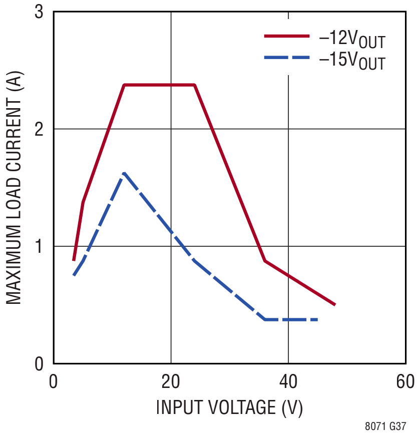
Maximum Load Current vs V_{IN}
BIAS Tied to LTM8071 GND



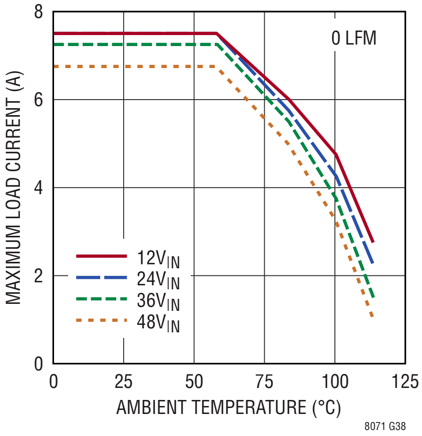
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

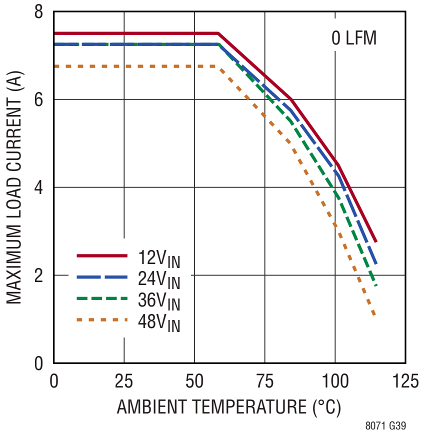
Maximum Load Current vs V_{IN} BIAS Tied to LTM8071 GND



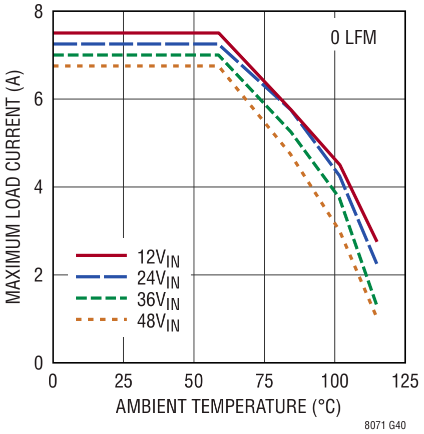
Derating, V_{OUT} = 0.97V, BIAS = 5V, DC2387A Demo Board



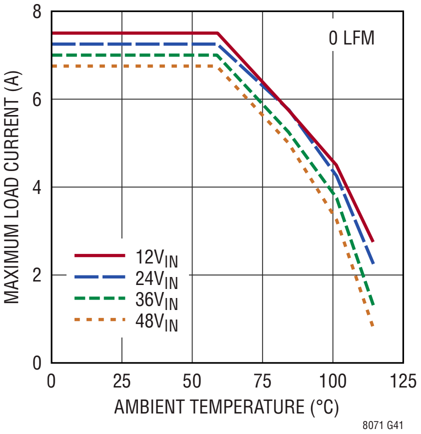
Derating, V_{OUT} = 1.2V, BIAS = 5V, DC2387A Demo Board



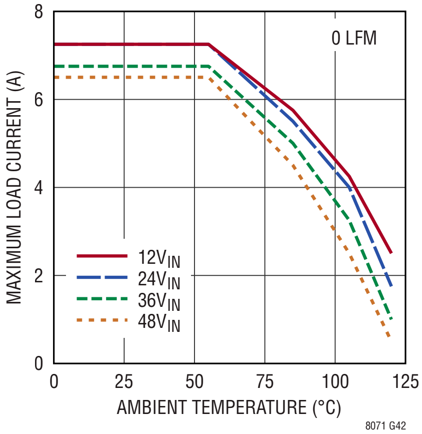
Derating, V_{OUT} = 1.5V, BIAS = 5V, DC2387A Demo Board



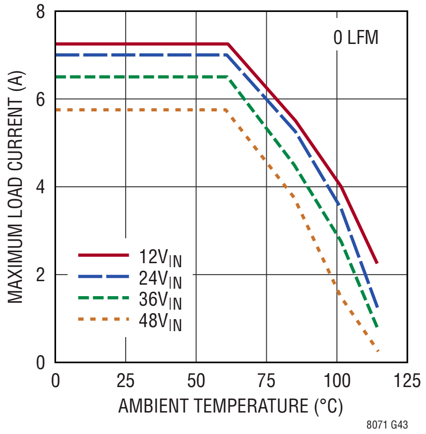
Derating, V_{OUT} = 1.8V, BIAS = 5V, DC2387A Demo Board



Derating, V_{OUT} = 2.5V, BIAS = 5V, DC2387A Demo Board



Derating, V_{OUT} = 3.3V, BIAS = 5V, DC2387A Demo Board



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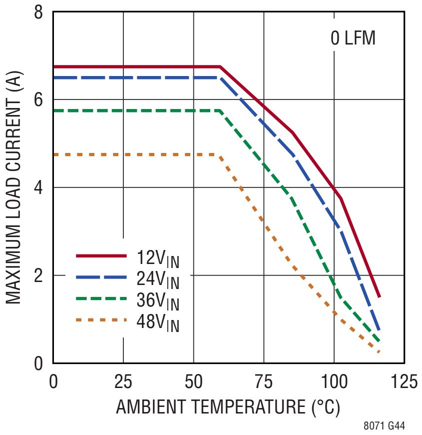
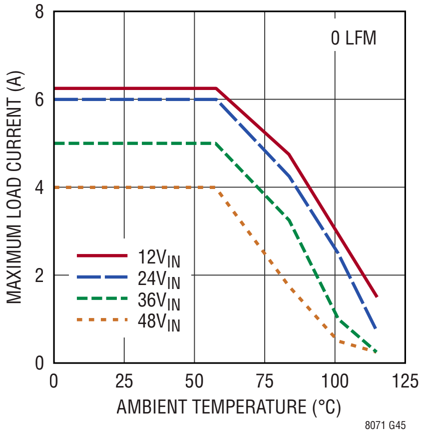
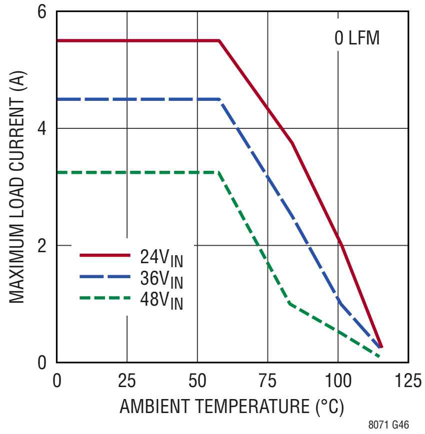


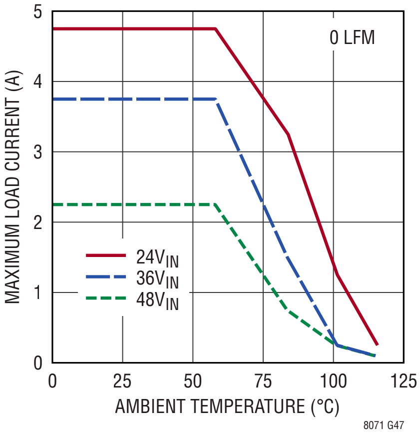
Derating, V_{OUT} = 8V, BIAS = 5V, DC2387A Demo Board

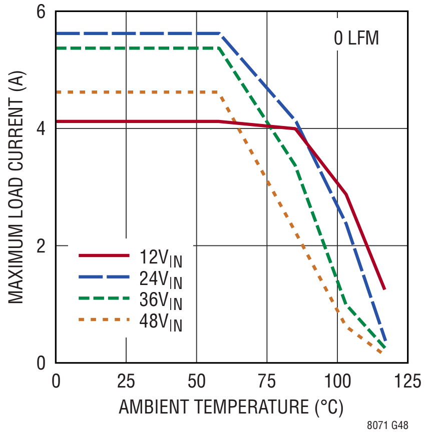


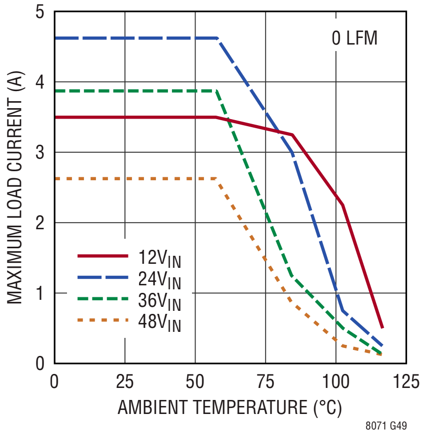
TYPICAL PERFORMANCE CHARACTERISTICS

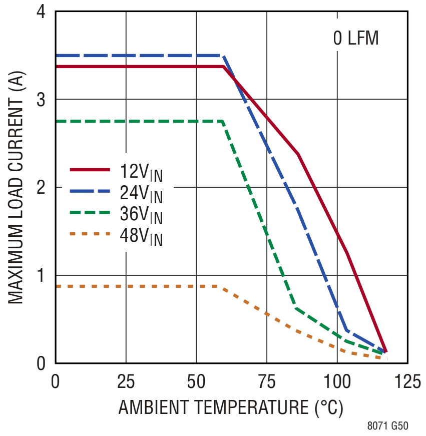
T_A = 25°C, unless otherwise noted.

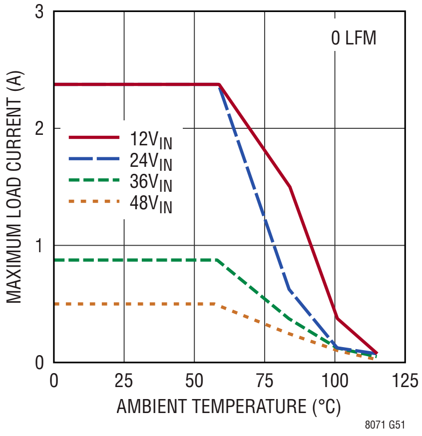

Derating, V_{OUT} = 12V, BIAS = 5V, DC2387A Demo Board


Derating, V_{OUT} = 15V, BIAS = 5V, DC2387A Demo Board


Derating, V_{OUT} = –3.3V, BIAS Tied to LTM8071 GND DC2387A Demo Board


Derating, V_{OUT} = –5V, BIAS Tied to LTM8071 GND DC2387A Demo Board

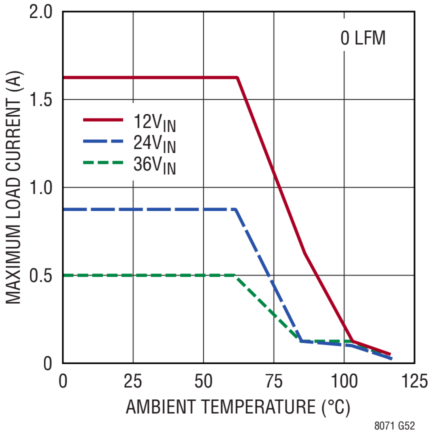

Derating, V_{OUT} = –8V, BIAS Tied to LTM8071 GND DC2387A Demo Board


Derating, V_{OUT} = –12V, BIAS Tied to LTM8071 GND DC2387A Demo Board

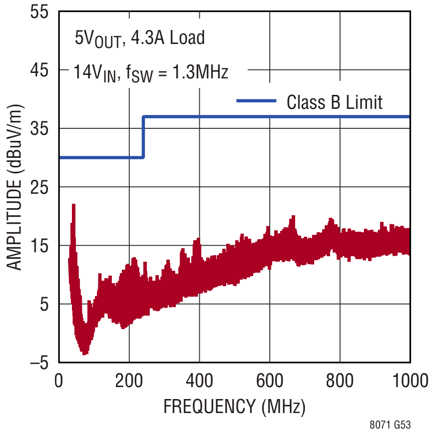
Rev. B

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

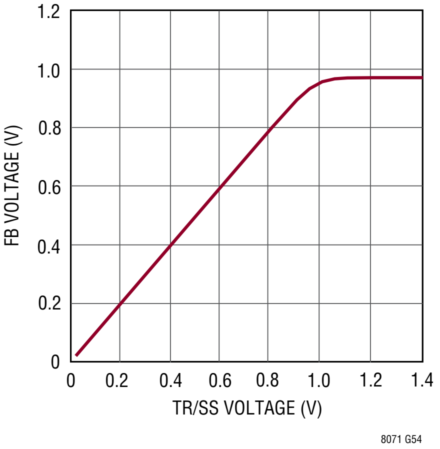
Derating, V_{OUT} = –15V, BIAS Tied to LTM8071 GND DC2387A Demo Board



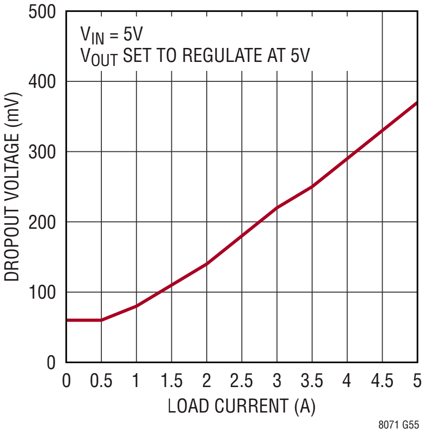
CISPR22 Class B Emissions DC2387A Demo Board, No EMI Filter (FB1 Short, C5, C6 Open)



Soft-Start Tracking



Dropout Voltage



PIN FUNCTIONS

GND (Bank 1, A1): Tie these GND pins to a local ground plane below the LTM8071 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8071 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 2): V_{IN} supplies current to the LTM8071's internal regulator and to the internal power switch. These pins must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

V_{OUT} (Bank 3): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

BIAS (Pin E1): The BIAS pin connects to the internal power bus. Connect to a power source greater than 3.2V. If V_{OUT} is greater than 3.2V, connect this pin to AUX. Decouple this pin with at least 1µF if the voltage source for BIAS is remote.

PG (Pin C1): The PG pin is the open-collector output of an internal comparator. PG remains low until the FB pin voltage is between 0.89V and 1.05V typical. The PG signal is valid when V_{IN} is above 3.6V. If V_{IN} is above 3.6V and RUN is low, PG will drive low. If this function is not used, leave this pin floating.

SHARE (Pin C2): Tie this to the SHARE pin of another LTM8071 to load share. Otherwise leave floating. Do not drive this pin.

RT (Pin A2): The RT pin is used to program the switching frequency of the LTM8071 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin. Do not drive this pin.

FB (Pin D1): The LTM8071 regulates its FB pin to 0.97V. Connect the adjust resistor from this pin to ground. The value of R_{FB} is given by the equation $R_{FB} = 241.5/(V_{OUT} – 0.97)$, where R_{FB} is in kΩ.

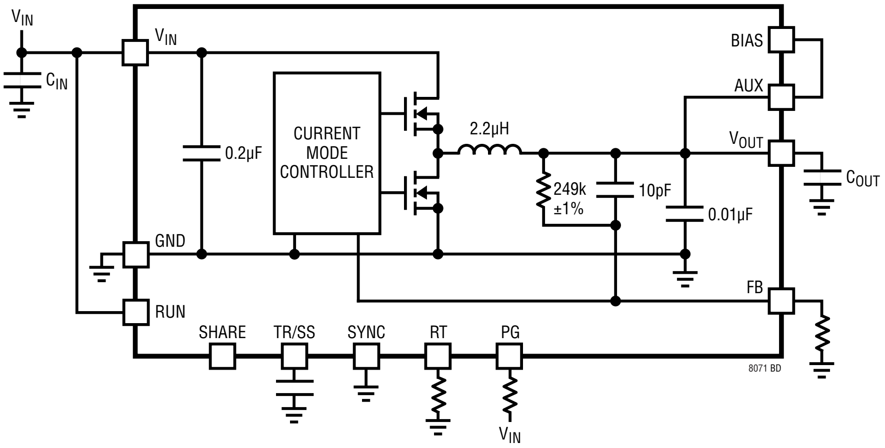
AUX (Pin E2): Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Also, some applications require a feed-forward capacitor; it can be connected from AUX to FB for convenient PCB routing. Although this pin is internally connected to V_{OUT}, it is not intended to deliver a high current, so do not draw current from this pin to the load.

SYNC (Pin B1): External clock synchronization input and operational mode. This pin programs four different operating modes: 1) Burst Mode®. Tie this pin to ground for Burst Mode operation at low output loads—this will result in low quiescent current. 2) Pulse-skipping mode. Float this pin for pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse-skipping mode occurs. 3) Spread spectrum mode. Tie this pin high (between 2.9V and 4.2V) for pulse-skipping mode with spread spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in pulse-skipping mode.

TR/SS (Pin B2): The TR/SS pin is used to provide a soft-start or tracking function. The internal 2µA pull-up current in combination with an external capacitor tied to this pin creates a voltage ramp. The output voltage tracks to this voltage. For tracking, tie a resistor divider to this pin from the tracked output. This pin is pulled to ground with an internal MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed. During start-up, if a relatively low capacitor is used on TR/SS, the output voltage may take longer to reach regulation than expected. If accurate start-up timing is required, please refer to the LTM8071 simulation model in LTspice for help selecting an appropriate soft-start capacitor.

RUN (Pin A3): Pull the RUN pin below 0.9V to shut down the LTM8071. Tie to 1.06V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin.

BLOCK DIAGRAM



OPERATION

The LTM8071 is a standalone nonisolated step-down switching DC/DC power supply that can deliver 7.25A at $3.3V_{OUT}$. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.97V to 15V. The input voltage range is 3.6V to 60V. Given that the LTM8071 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is given above.

The LTM8071 contains a current mode controller, power switching elements, power inductor and a modest amount of input and output capacitance. The LTM8071 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. This bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN pin is used to place the LTM8071 in shutdown, disconnecting the output and reducing the input current to a few µA.

If SYNC is less than about 0.4V, the LTM8071 automatically switches to enhanced efficiency Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current.

The oscillator reduces the LTM8071's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The TR/SS node acts as an auxiliary input to the error amplifier. The voltage at FB servos to the TR/SS voltage until TR/SS exceeds about 1.6V. Soft-start is implemented by generating a voltage ramp at the TR/SS pin using an external capacitor which is charged by an internal constant current. Alternatively, driving the TR/SS pin with a signal source or resistive network provides a tracking function. Do not drive the TR/SS pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8071 contains a power good comparator which trips when the FB pin is between 0.89V and 1.05V, typical. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when V_{IN} is above 3.6V. If V_{IN} is above 3.6V and RUN is low, PG will drive low.

The LTM8071 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB} and R_T values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8071 should be allowed to switch is given in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

MAX V_{IN}	V_{OUT}	R_{FB}	C_{IN}^2	C_{OUT}	BIAS	f_{SW}	R_T	MAX f_{SW}	MIN_{RT}
3.6V to 60V	0.97	Open	1µF 100V 1206 X7R	2x 100µF 4V 0805 X5R	3.2V to 19V	400kHz	110k	500kHz	88.7k
3.6V to 60V	1.2	1.05M	1µF 100V 1206 X7R	2x 100µF 4V 0805 X5R	3.2V to 19V	400kHz	110k	550kHz	80.6k
3.6V to 60V	1.5	442k	1µF 100V 1206 X7R	100µF 4V 0805 X5R	3.2V to 19V	400kHz	110k	700kHz	60.4k
3.6V to 60V	1.8	287k	1µF 100V 1206 X7R	100µF 4V 0805 X5R	3.2V to 19V	400kHz	110k	850kHz	47.5k
3.6V to 60V	2.5	154k	1µF 100V 1206 X7R	100µF 6.3V 1206 X5R	3.2V to 19V	500kHz	88.7k	1MHZ	41.2k
4.5V to 60V[1]	3.3	102k	1µF 100V 1206 X7R	100µF 6.3V 1206 X5R	3.2V to 19V	650kHz	66.5k	1.4MHz	28k
7V to 60V[1]	5	59k	1µF 100V 1206 X7R	100µF 6.3V 1206 X5R	3.2V to 19V	1MHz	41.2k	2.2MHz	15.8k
11V to 60V[1]	8	34k	1µF 100V 1210 X7R	3x 47µF 10V 1206 X5R	3.2V to 19V	1.2MHz	33.2k	2.2MHz	15.8k
16V to 60V[1]	12	21.5k	1µF 100V 1210 X7R	2x 47µF 16V 1210 X5R	3.2V to 19V	1.4MHz	28k	2.2MHz	15.8k
20V to 60V[1]	15	16.9k	1µF 100V 1210 X7R	2x 47µF 16V 1210 X5R	3.2V to 19V	1.8MHz	20.5k	2.2MHz	15.8k
3.6V to 56V	–3.3	102k	1µF 100V 1206 X7R	100µF 6.3V 1206 X5R	LTM8071 GND	650kHz	66.5k	1.4MHz	28k
3.6V to 55V	–5	59k	1µF 100V 1206 X7R	100µF 6.3V 1206 X5R	LTM8071 GND	1MHz	41.2k	2.2MHz	15.8k
3.6V to 52V	–8	34k	1µF 100V 1210 X7R	3x 47µF 10V 1206 X5R	LTM8071 GND	1.2MHz	33.2k	2.2MHz	15.8k
3.6V to 48V	–12	21.5k	1µF 100V 1210 X7R	2x 47µF 16V 1210 X5R	LTM8071 GND	1.4MHz	28k	2.2MHz	15.8k
3.6V to 45V	–15	16.9k	1µF 100V 1210 X7R	2x 47µF 16V 1210 X5R	LTM8071 GND	1.8MHz	20.5k	2.2MHz	15.8k

Note 1: The LTM8071 may be capable of operating lower input voltages but may skip off cycles.

Note 2: An input bulk capacitor is required.

APPLICATIONS INFORMATION

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8071's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8071 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8071. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8071 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8071 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	73.2
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	18.2
2.2	15.8

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8071 is flexible enough to accommodate a wide range of operating frequencies, the typical minimum OFF time of LTM8071 is 84nS, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8071 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

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BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIAS may be simply tied to AUX. If V_{OUT} is less than 3.2V, BIAS can be tied to V_{IN} or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8071 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency. In all cases, ensure that the maximum voltage at the BIAS pin is less than 19V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIAS pin may also be left open at the cost of a small degradation in efficiency.

If the LTM8071 is configured to provide a negative output, do not connect BIAS to V_{OUT} or AUX. Instead, tie to BIAS to the LTM8071 GND, which should be the negative output.

Maximum Load

The maximum practical continuous load that the LTM8071 can drive, while rated at 5A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8071 in the case of overload or short-circuit. The internal temperature of the LTM8071 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if the LTM8071 is configured to regulate at 1.2V, it may continuously deliver more than 7A from $12V_{IN}$ if the ambient temperature is controlled to less than 55°C; this is more than the 5A continuous rating. Please see the Derating, V_{OUT} = 1.2V curve in the Typical Performance Characteristics section. Similarly, if the output voltage is 15V and the ambient temperature is 100°C, the LTM8071 will deliver at most 0.25A from $48V_{IN}$, which is less than the 5A continuous rating.

Load Sharing

Two or more LTM8071s may be paralleled to produce higher currents. To do this, tie the V_{IN}, V_{OUT} and SHARE pins of all the paralleled LTM8071s together. To ensure that paralleled modules start up together, the TR/SS pins may be tied together, as well. If it is inconvenient to tie the TR/SS pins together, make sure that the same valued soft-start capacitors are used for each µModule regulator. An example of two LTM8071s configured for load sharing is given in the Typical Applications section.

For closer load sharing, synchronize the LTM8071s to an external clock source. When load sharing among n units and using a single R_{FB} resistor, the value of the resistor is:

$$R_{FB} = \frac{241.5}{n\left(V_{OUT} - 0.97\right)}$$

where R_{FB} is in kΩ.

Burst Mode Operation

If SYNC is less than about 0.4V, the LTM8071 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8071 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, V_{IN} and BIAS quiescent currents are greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8071 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Minimum Input Voltage

The LTM8071 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3.6V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3.6V may turn off the LTM8071.

Output Voltage Tracking and Soft-Start

The LTM8071 allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 2µA pulls up the TR/SS pin to about 2.4V. Putting an external capacitor on TR/SS enables soft starting the output to

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reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 1.6V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TR/SS pin. When TR/SS is above 1.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

During start-up, if a relatively low capacitor is used on TR/SS, the output voltage may take longer to reach regulation than expected. If accurate start-up timing is required, please refer to the LTM8071 simulation model in LTspice for help selecting an appropriate soft-start capacitor.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Prebiased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8071 regulates the output to the FB voltage determined by the TR/SS pin whenever TR/SS is less than 1.6V. If the LTM8071 output is higher than the target output voltage, the LTM8071 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8071.

Frequency Foldback

The LTM8071 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short-circuit or output overload condition. If the LTM8071 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNC pin, the SYNC pin is floated or held high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below about 0.4V (this can be ground or a logic low output). To synchronize the LTM8071 oscillator to an external frequency connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V.

The LTM8071 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LTM8071 may be synchronized over a 200kHz to 2.2MHz range. The R_T resistor should be chosen to set the LTM8071 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

For some applications it is desirable for the LTM8071 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. The first is that the clock stays awake at all times and all switching cycles are aligned to the clock. Second is that full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is floated.

The LTM8071 features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, apply between 2.9V and 4.2V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 3kHz. For example, when the LTM8071 is programmed to 1MHz, the frequency will

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vary from 1MHz to 1.2MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in pulse-skipping mode.

The LTM8071 does not operate in forced continuous mode regardless of SYNC signal.

Negative Output

The LTM8071 is capable of generating a negative output voltage by connecting its V_{OUT} to system GND and the LTM8071 GND to the negative voltage rail. An example of this is shown in the Typical Applications section. The most versatile way to generate a negative output is to use a dedicated regulator that was designed to generate a negative voltage, but using a buck regulator like the LTM8071 to generate a negative voltage is a simple and cost effective solution, as long as certain restrictions are kept in mind.

Figure 1a shows a typical negative output voltage application. Note that LTM8071 V_{OUT} is tied to system GND and input power is applied from V_{IN} to LTM8071 V_{OUT}. As a result, the LTM8071 is not behaving as a true buck regulator, and the maximum output current is depends upon the input voltage. In the example shown in the Typical Applications section, there is an attending graph that shows how much current the LTM8071 can deliver for given input voltages.

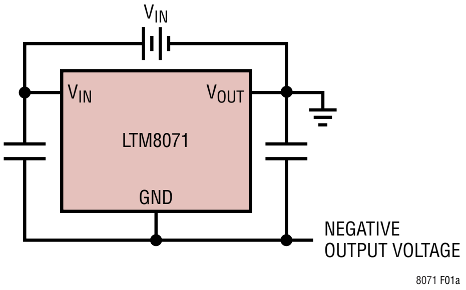


Figure 1a. The LTM8071 Can Be Used to Generate a Negative Voltage

Note that this configuration requires that any load current transient will directly impress the transient voltage onto the LTM8071 GND, as shown in Figure 1b, so fast load transients can disrupt the LTM8071's operation or even cause damage. Carefully evaluate whether the negative buck configuration is suitable for the application.

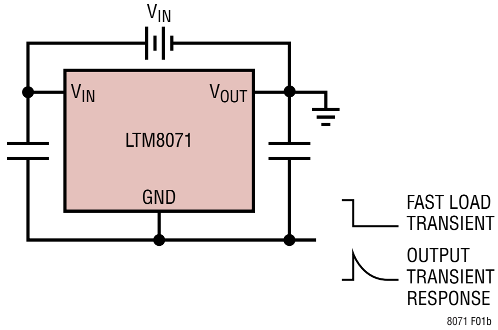


Figure 1b. Any Output Voltage Transient Appears on LTM8071 GND

The C_{IN} and C_{OUT} capacitors in Figure 1c form an AC divider at the negative output voltage node. If V_{IN} is hot-plugged or rises quickly, the resultant V_{OUT} will be a positive transient, which may be unhealthy for the application load. An antiparallel Schottky diode may be able to prevent this positive transient from damaging the load. The location of this Schottky diode is important. For example, in a system where the LTM8071 is far away from the load, placing the Schottky diode closest to the most sensitive load component may be the best design choice. Carefully evaluate whether the negative buck configuration is suitable for the application.

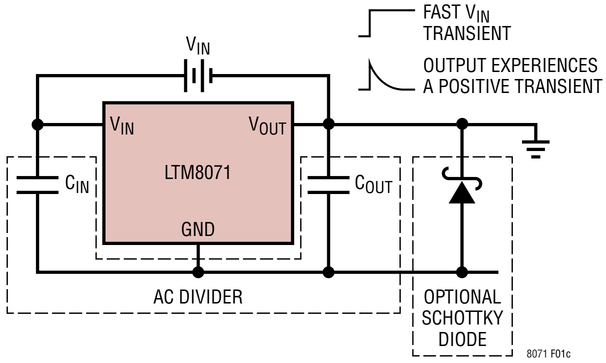


Figure 1c. A Schottky Diode Can Limit the Transient Caused by a Fast Rising V_{IN} to Safe Levels

If the LTM8071 is configured to provide a negative output, do not connect BIAS to V_{OUT} or AUX. Instead, tie BIAS to the LTM8071 GND, which should be the system's negative output.

APPLICATIONS INFORMATION

To safely operate the LTM8071 in this negative output configuration, the V_{IN} supply and negative output voltages must meet the following criteria:

$|V_{IN}| + |V_{OUT}| \le 60V$

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8071 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM8071's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8071's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM8071 can pull large currents from the output through the V_{IN} pin. Figure 2 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8071. The LTM8071 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

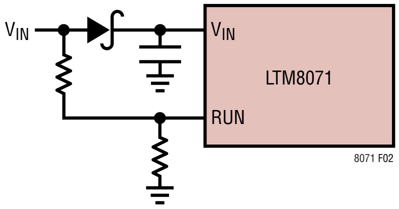


Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8071 Runs Only When the Input Is Present.

A few rules to keep in mind are:

1. Place R_{FB} and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8071.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8071.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8071.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8071.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8071 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

APPLICATIONS INFORMATION

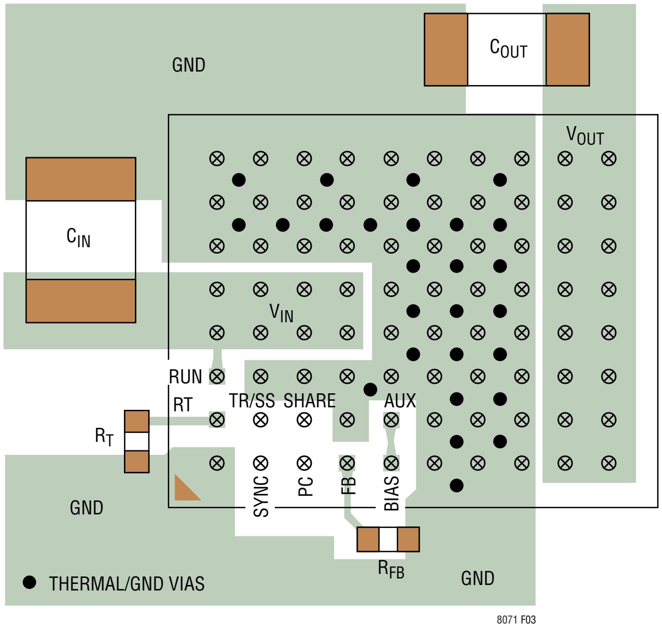


Figure 3. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8071. However, these capacitors can cause problems if the LTM8071 is plugged into a live supply (see Analog Devices' Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8071 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8071's rating and damaging the part. If the input supply is poorly controlled or the LTM8071 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8071 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8071 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (finite element analysis) to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still air although natural convection causes the air to move.

APPLICATIONS INFORMATION

This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is often just the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 4. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8071 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8071. The bulk of the heat flow out of the LTM8071 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

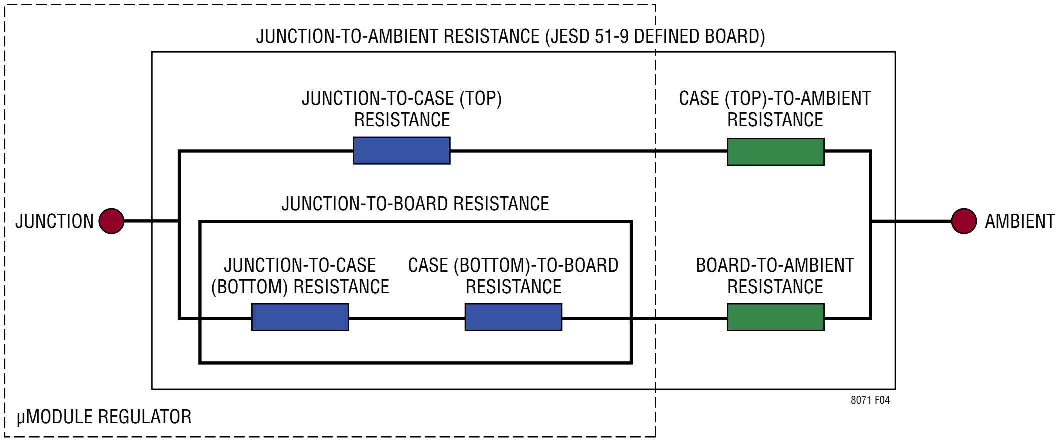
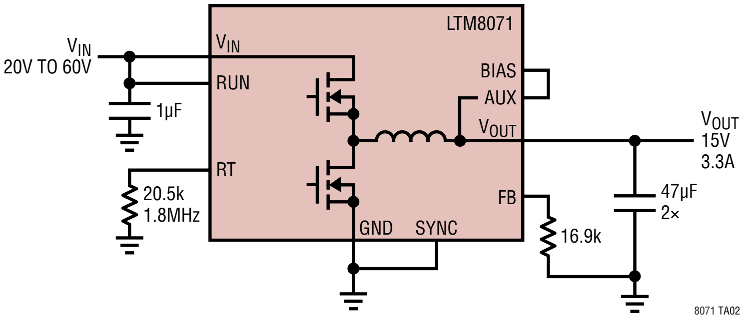


Figure 4. Graphical Representation of the Thermal Resistances Between the Device Junction and Ambient

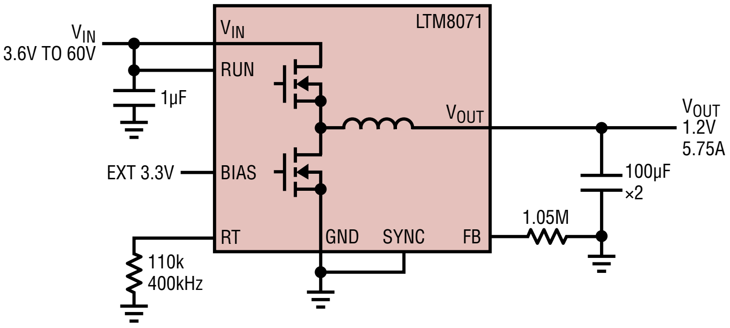
TYPICAL APPLICATIONS

15V_{OUT} from 20V_{IN} to 60V_{IN} Step-Down Converter. BIAS Is Tied to AUX



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG, SHARE

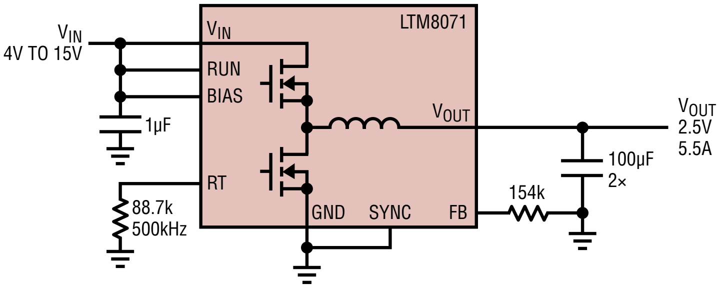
1.2V_{OUT} from 3.6V_{IN} to 60V_{IN} Step-Down Converter. BIAS Is Tied to an External 3.3V Source



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG, SHARE, AUX

8071 TA03

2.5V_{OUT} from 4V_{IN} to 15V_{IN} Step-Down Converter. BIAS Is Tied to V_{IN}

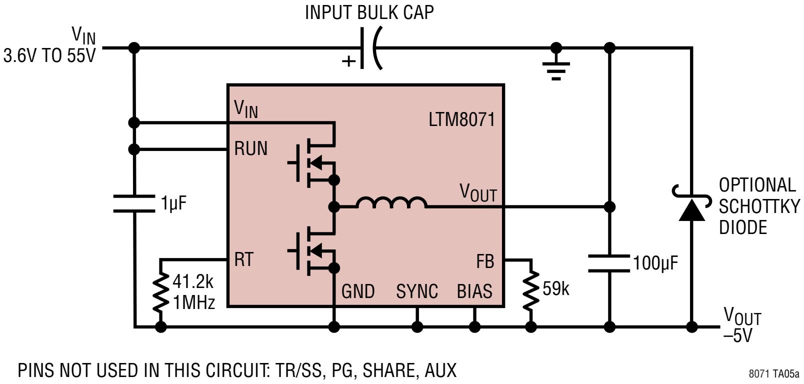


PINS NOT USED IN THIS CIRCUIT: TR/SS, PG, SHARE, AUX

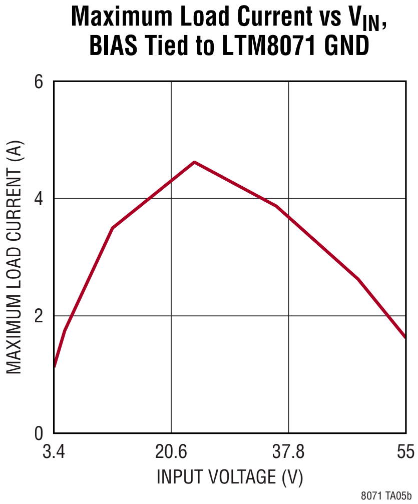
8071 TA04

TYPICAL APPLICATIONS

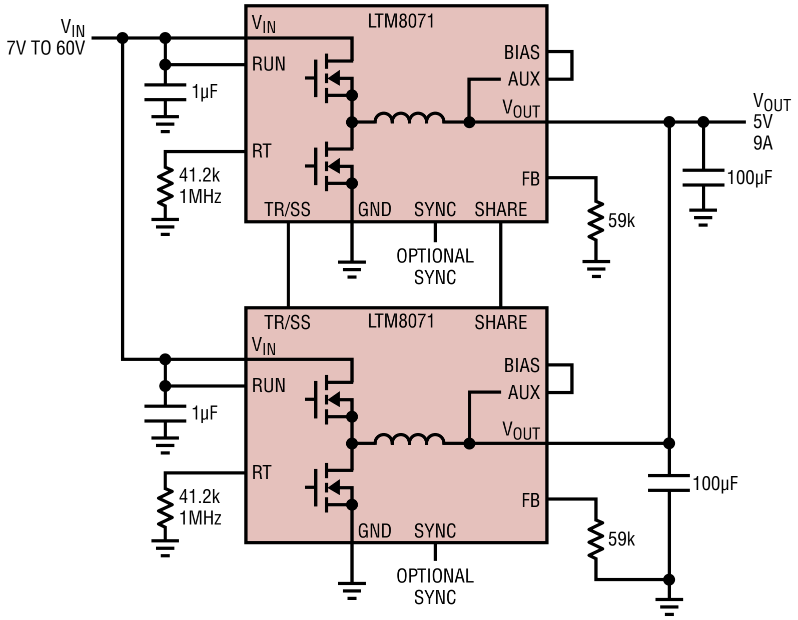
$-5V_{OUT}$ from $3.6V_{IN}$ to $55V_{IN}$ Positive to Negative Converter. BIAS Is Tied to LTM8071 GND



PINS NOT USED IN THIS CIRCUIT: TR/SS, PG, SHARE, AUX



Two LTM8071s Powered from the Same Input Source to Deliver Up to 9A



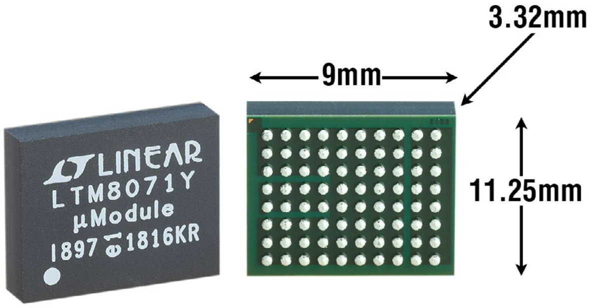
PIN NOT USED IN THIS CIRCUIT: PG

PACKAGE DESCRIPTION

Table 3. LTM8071 Pinout (Sorted by Pin Number)

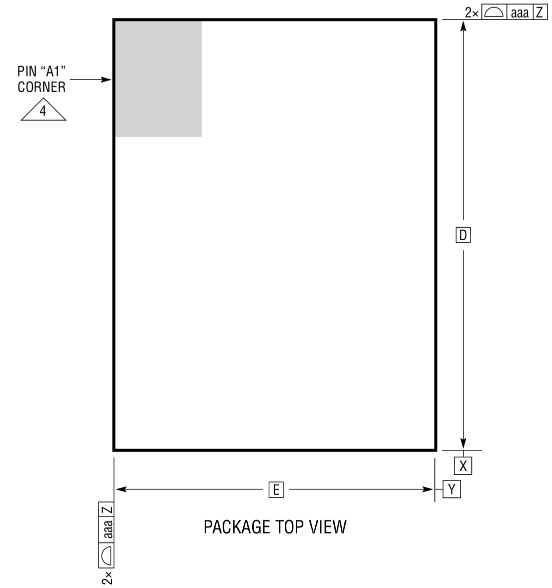
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GND	B1	SYNC	C1	PG	D1	FB	E1	BIAS
A2	RT	B2	TR/SS	C2	SHARE	D2	GND	E2	AUX
A3	RUN	B3	GND	C3	GND	D3	GND	E3	GND
A4	V_{IN}	B4	V_{IN}	C4	V_{IN}	D4	V_{IN}	E4	GND
A5	V_{IN}	B5	V_{IN}	C5	V_{IN}	D5	V_{IN}	E5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND
A8	GND	B8	GND	C8	GND	D8	GND	E8	GND
PIN	**NAME**	**PIN**	**NAME**	**PIN**	**NAME**	**PIN**	**NAME**	**PIN**	**NAME**
F1	GND	G1	GND	H1	GND	J1	V_{OUT}	K1	V_{OUT}
F2	GND	G2	GND	H2	GND	J2	V_{OUT}	K2	V_{OUT}
F3	GND	G3	GND	H3	GND	J3	V_{OUT}	K3	V_{OUT}
F4	GND	G4	GND	H4	GND	J4	V_{OUT}	K4	V_{OUT}
F5	GND	G5	GND	H5	GND	J5	V_{OUT}	K5	V_{OUT}
F6	GND	G6	GND	H6	GND	J6	V_{OUT}	K6	V_{OUT}
F7	GND	G7	GND	H7	GND	J7	V_{OUT}	K7	V_{OUT}
F8	GND	G8	GND	H8	GND	J8	V_{OUT}	K8	V_{OUT}

PACKAGE PHOTOS

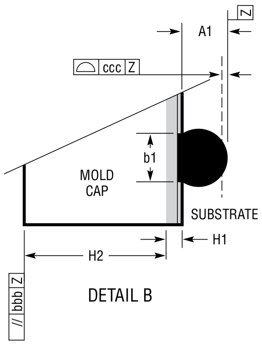


PACKAGE DESCRIPTION

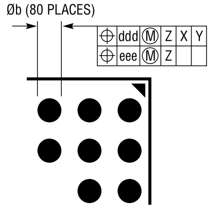
BGA Package
80-Lead (11.25mm × 9mm × 3.32mm)
(Reference LTC DWG # 05-08-1997 Rev B)



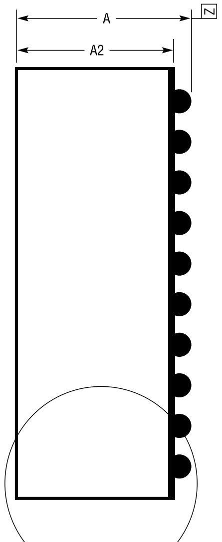
PACKAGE TOP VIEW



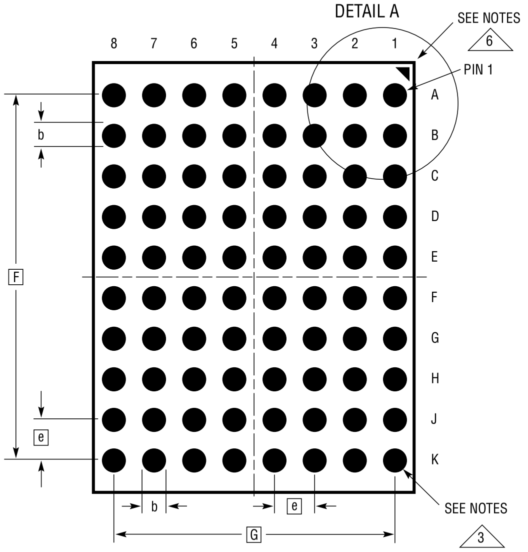
DETAIL B



DETAIL A



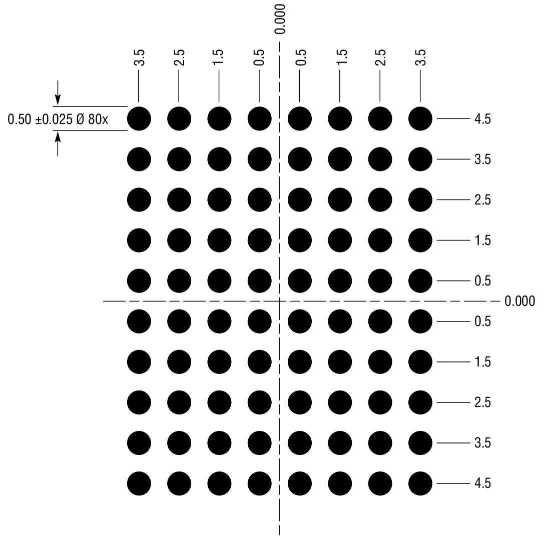
DETAIL B
PACKAGE SIDE VIEW



PACKAGE BOTTOM VIEW

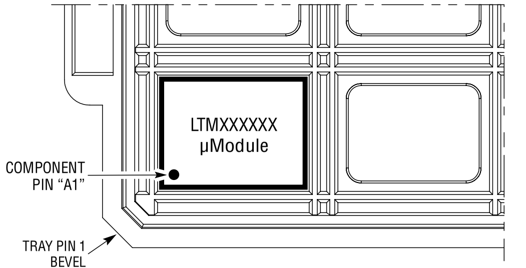
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	3.12	3.32	3.52	
A1	0.40	0.50	0.60	BALL HT
A2	2.72	2.82	2.92	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		11.25		
E		9.00		
e		1.00		
F		9.00		
G		7.00		
H1		0.32 REF		SUBSTRATE THK
H2		2.50 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	
TOTAL NUMBER OF BALLS: 80				



PACKAGE IN TRAY LOADING ORIENTATION

BGA 80 0418 REV B

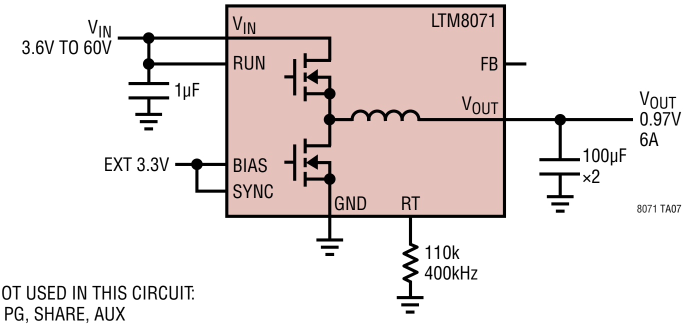
Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/21	Updated Typical Application values.	1
		Corrected Pin Configuration bottom notes, JESD (instead of JEDEC).	2
		Updated EC table R_{FB} = 16.9kΩ to match the rest of the DS.	3
		Updated Curves titles with switching frequency.	4
		Replaced $12V_{IN}$ curves on G13 and G14, added switching frequency on other curves.	5
		Added G54, Soft Start Tracking and G55, Dropout Voltage.	10
		Corrected Block Diagram internal V_{OUT} caps to 0.01µF (per BOM).	12
		Recommended values updated on Table 1.	13
		Corrected Application Information, added additional note $\|V_{IN}\| + \|V_{OUT}\| \le 60V$.	18
B	07/21	Feed Forward Capacitor in Block Diagram updated to 10pF.	12

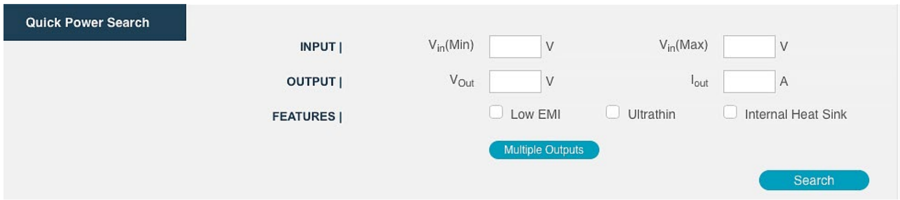
TYPICAL APPLICATION

0.97V_{OUT} from 3.6V_{IN} to 60V_{IN} Step-Down Converter with Spread Spectrum. BIAS Is Tied to an External 3.3V Source



PINS NOT USED IN THIS CIRCUIT:
TR/SS, PG, SHARE, AUX

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8050	58V, 2A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, 0.8V ≤ V_{OUT} ≤ 24V, 9mm × 15mm × 4.92mm BGA
LTM8073	60V, 3A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM8064	58V, ±6A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 36V, 11.9mm × 16mm × 4.92mm BGA
LTM4651	EN55022B Compliant, 58V_{IN}, 24W Inverting-Output µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, –26.5V ≤ V_{OUT} ≤ –0.5V, I_{OUT} ≤ 4A, 15mm × 9mm × 5.01mm BGA
LTM4653	EN55022B Compliant, 58V_{IN}, 4A, Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, –26.5V ≤ V_{OUT} ≤ –0.5V, I_{OUT} ≤ 4A, 15mm × 9mm × 5.01mm BGA
LTM8052	36V, ±5A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, 11.25mm × 15mm × 2.82mm LGA, 11.25mm × 15mm × 3.42mm BGA
LTM8053	40V, 3.5A Step-Down Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM4613	EN55022B Compliant, 36V, 8A Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, 15mm × 15mm × 4.32mm LGA, 15mm × 15mm × 4.92mm BGA