THE DATASHEET OF

LTM4609MPY

www.win-source.net 0086-755-83957316

36V_{IN}, 34V_{OUT} High Efficiency Buck-Boost DC/DC µModule Regulator

FEATURES

- **Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Wide V_{IN} Range: 4.5V to 36V**
- **Wide V_{OUT} Range: 0.8V to 34V**
- **I_{OUT}: 4A DC (10A DC in Buck Mode)**
- **Up to 98% Efficiency**
- **Current Mode Control**
- **Power Good Output Signal**
- **Phase-Lockable Fixed Frequency: 200kHz to 400kHz**
- **Ultrafast Transient Response**
- Current Foldback Protection
- Output Overvoltage Protection
- Small Surface Mount Footprint, Low Profile (15mm × 15mm × 2.82mm) LGA and (15mm × 15mm × 3.42mm) BGA Packages
- SnPb (BGA) or RoHS Compliant (LGA and BGA) Finish

APPLICATIONS

- Telecom, Servers and Networking Equipment
- Industrial and Automotive Equipment
- High Power Battery-Operated Devices

DESCRIPTION

The LTM®4609 is a high efficiency switching mode buck-boost power supply. Included in the package are the switching controller, power FETs and support components. Operating over an input voltage range of 4.5V to 36V, the LTM4609 supports an output voltage range of 0.8V to 34V, set by a resistor. This high efficiency design delivers up to 4A continuous current in boost mode (10A in buck mode). Only the inductor, sense resistor, bulk input and output capacitors are needed to finish the design.

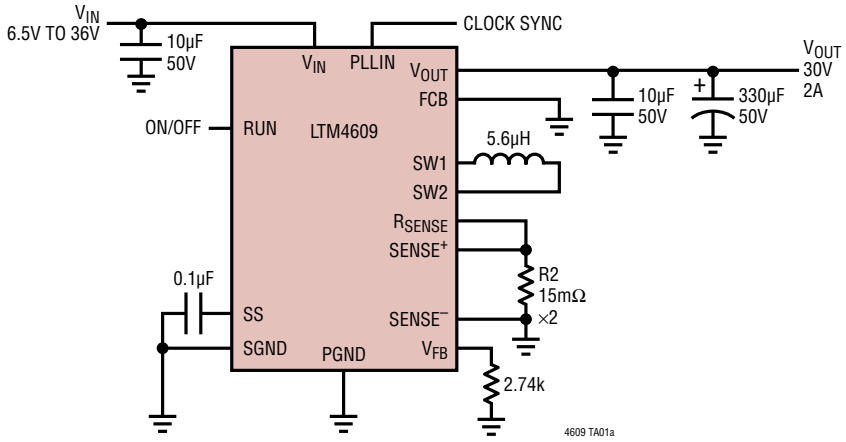
The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation. The high switching frequency and current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The LTM4609 can be frequency synchronized with an external clock to reduce undesirable frequency harmonics.

Fault protection features include overvoltage and foldback current protection. The DC/DC µModule® regulator is offered in small 15mm × 15mm × 2.82mm LGA and 15mm × 15mm × 3.42mm BGA packages. The LTM4609 is available with SnPb (BGA) or RoHS compliant terminal finish.

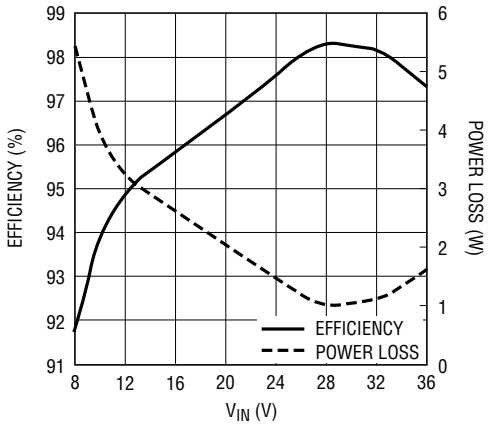
, LT, LTC, LTM, Linear Technology, the Linear logo, µModule, Burst Mode and PolyPhase are registered trademarks and No R_{SENSE} is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

30V/2A Buck-Boost DC/DC µModule Regulator with 6.5V to 36V Input



Efficiency and Power Loss vs Input Voltage

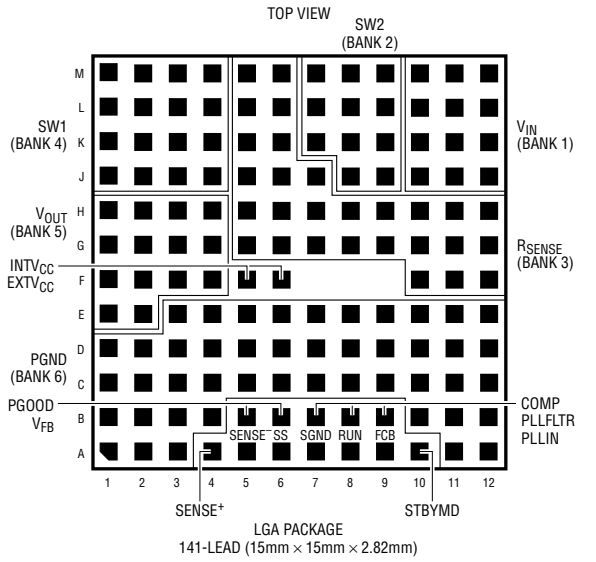


ABSOLUTE MAXIMUM RATINGS

(Note 1)

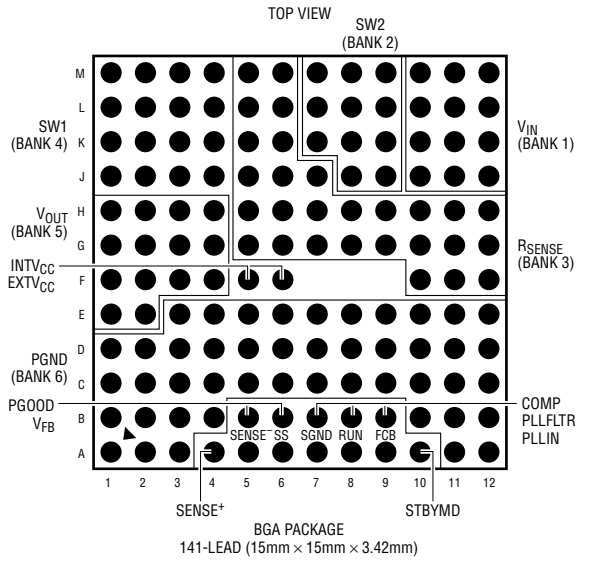
V_{IN} ..... –0.3V to 36V
V_{OUT} ..... 0.8V to 36V
$INTV_{CC}$, $EXTV_{CC}$, RUN, SS, PGOOD ..... –0.3V to 7V
SW1, SW2 (Note 7) ..... –5V to 36V
V_{FB} ..... –0.3V to 2.4V
COMP ..... –0.3V to 2V
FCB, STBYMD ..... –0.3V to $INTV_{CC}$
PLLIN ..... –0.3V to 5.5V
PLLFLTR ..... –0.3V to 2.7V
$INTV_{CC}$ ..... –40mA
Operating Temperature Range (Note 2)
E- and I-grades ..... –40°C to 85°C
MP-grade ..... –55°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Solder Temperature (Note 3) ..... 245°C

PIN CONFIGURATION (See Table 6 Pin Assignment)



LGA PACKAGE
141-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 11.4°C/W, θ_{JCtop} = 15°C/W, $\theta_{JCbottom}$ = 4°C/W, WEIGHT = 1.5g



BGA PACKAGE
141-LEAD (15mm × 15mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 11.4°C/W, θ_{JCtop} = 15°C/W, $\theta_{JCbottom}$ = 4°C/W, WEIGHT = 1.7g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4609EV#PBF	Au (RoHS)	LTM4609V	e4	LGA	3	–40°C to 85°C
LTM4609IV#PBF	Au (RoHS)	LTM4609V	e4	LGA	3	–40°C to 85°C
LTM4609MPV#PBF	Au (RoHS)	LTM4609V	e4	LGA	3	–55°C to 125°C
LTM4609EY#PBF	SAC305 (RoHS)	LTM4609Y	e1	BGA	3	–40°C to 85°C
LTM4609IY#PBF	SAC305 (RoHS)	LTM4609Y	e1	BGA	3	–40°C to 85°C
LTM4609IY	SnPb (63/37)	LTM4609Y	e0	BGA	3	–40°C to 85°C
LTM4609MPY #PBF	SAC305 (RoHS)	LTM4609Y	e1	BGA	3	–55°C to 125°C
LTM4609MPY	SnPb (63/37)	LTM4609Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Specifications							
$V_{IN(DC)}$	Input DC Voltage		●	4.5		36	V
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	V_{IN} Falling (–40°C to 85°C) V_{IN} Falling (–55°C to 125°C)	● ●		3.4 3.4	4 4.5	V V
$I_{Q(VIN)}$	Input Supply Bias Current Normal Standby Shutdown Supply Current	 V_{RUN} = 0V, V_{STBYMD} > 2V V_{RUN} = 0V, V_{STBYMD} = Open			 2.8 1.6 35	 60	 mA mA µA
Output Specifications							
I_{OUTDC}	Output Continuous Current Range (Note 3)	V_{IN} = 32V, V_{OUT} = 12V V_{IN} = 6V, V_{OUT} = 12V			10 4		A A
$\Delta V_{FB}/V_{FB(NOM)}$	Line Regulation Accuracy	V_{IN} = 4.5V to 36V, V_{COMP} = 1.2V (Note 4)			0.002	0.02	%/V
$\Delta V_{FB}/V_{FB(LOAD)}$	Load Regulation Accuracy	V_{COMP} = 1.2V to 0.7V V_{COMP} = 1.2V to 1.8V (Note 4)	● ●		0.15 –0.15	0.5 –0.5	% %
Switch Section (Note 5)							
M1 t_r	Turn-On Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			50		ns
M1 t_f	Turn-Off Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			40		ns
M3 t_r	Turn-On Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			25		ns
M3 t_f	Turn-Off Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			20		ns
M2, M4 t_r	Turn-On Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			20		ns
M2, M4 t_f	Turn-Off Time	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			20		ns
t_{1d}	M1 Off to M2 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			50		ns
t_{2d}	M2 Off to M1 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			50		ns
t_{3d}	M3 Off to M4 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			50		ns
t_{4d}	M4 Off to M3 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			50		ns
Mode Transition 1	M2 Off to M4 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			220		ns
Mode Transition 2	M4 Off to M2 On Delay	Drain to Source Voltage V_{DS} = 12V, Bias Current I_{SW} = 10mA			220		ns
M1 $R_{DS(ON)}$	Static Drain-to-Source On-Resistance	Bias Current I_{SW} = 3A			10		mΩ
M2 $R_{DS(ON)}$	Static Drain-to-Source On-Resistance	Bias Current I_{SW} = 3A			14	20	mΩ
M3 $R_{DS(ON)}$	Static Drain-to-Source On-Resistance	Bias Current I_{SW} = 3A			14	20	mΩ
M4 $R_{DS(ON)}$	Static Drain-to-Source On-Resistance	Bias Current I_{SW} = 3A			14	20	mΩ
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		260	300	330	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		170	200	220	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ = 2.4V		340	400	440	kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current	$f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			–15 15		µA µA
Control Section							
V_{FB}	Feedback Reference Voltage	V_{COMP} = 1.2V(–40°C to 85°C) V_{COMP} = 1.2V (–55°C to 125°C)	● ●	0.792 0.785	0.8 0.8	0.808 0.815	V V
V_{RUN}	RUN Pin ON/OFF Threshold			1	1.6	2.2	V
I_{SS}	Soft-Start Charging Current	V_{RUN} = 2.2V			–1.7	–1	µA
$V_{STBYMD(START)}$	Start-Up Threshold	V_{STBYMD} Rising		0.4	0.7		V
$V_{STBYMD(KA)}$	Keep-Active Power On Threshold	V_{STBYMD} Rising, V_{RUN} = 0V			1.25		V
V_{FCB}	Forced Continuous Threshold			0.76	0.8	0.84	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.85V		–0.3	–0.2	–0.1	µA
V_{BURST}	Burst Inhibit (Constant Frequency) Threshold	Measured at FCB Pin			5.3	5.5	V
$DF_{(BOOST, MAX)}$	Maximum Duty Factor	% Switch M4 On			99		%
$DF_{(BUCK, MAX)}$	Maximum Duty Factor	% Switch M1 On			99		%
$t_{ON(MIN, BUCK)}$	Minimum On-Time for Synchronous Switch in Buck Operation	Switch M1 (Note 6)			200	250	ns
RFBHI	Resistor Between V_{OUT} and V_{FB} Pins			99.5	100	100.5	kΩ
Internal V_{CC} Regulator							
$INTV_{CC}$	Internal V_{CC} Voltage	V_{IN} = 12V, V_{EXTVCC} = 5V V_{IN} = 7V, V_{EXTVCC} = 5V	● ●	5.7 5.56	6 6	6.3 6.35	V V
$\Delta V_{LDO}/V_{LDO}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 5V			0.3	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, V_{EXTVCC} Rising	●	5.4	5.6		V
$\Delta V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				300		mV
ΔV_{EXTVCC}	$EXTV_{CC}$ Switch Drop Voltage	I_{CC} = 20mA, V_{EXTVCC} = 6V			60	150	mV
Current Sensing Section							
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	Boost Mode Buck Mode	● ●	 –95	160 –130	190 –150	mV mV
$V_{SENSE(MIN, BUCK)}$	Minimum Current Sense Threshold	Discontinuous Mode			–6		mV
I_{SENSE}	Sense Pins Total Source Current	V_{SENSE}^- = V_{SENSE}^+ = 0V			–380		µA
PGOOD							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		5.5	7.5	10	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–5.5	–7.5	–10	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			2.5		%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 2mA			0.2	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4609 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4609E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4609I is guaranteed over the –40°C to 85°C operating temperature range. The LTM4609MP is guaranteed and tested over the –55°C to 125°C operating temperature range. For output current derating at high temperature, please refer to Thermal Considerations and Output Current Derating discussion.

Note 3: See output current derating curves for different V_{IN}, V_{OUT}, and T_A.

Note 4: The LTM4609 is tested in a feedback loop that servos V_{COMP} to a specified voltage and measures the resultant V_{FB}.

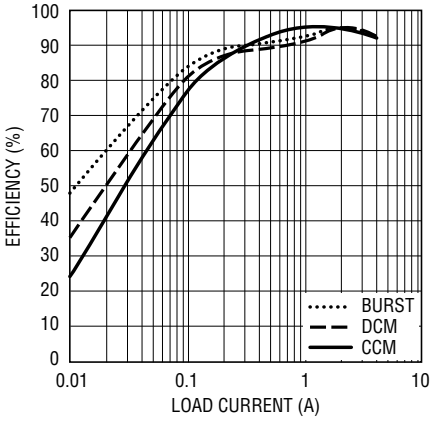
Note 5: Turn-on and turn-off time are measured using 10% and 90% levels. Transition delay time is measured using 50% levels.

Note 6: 100% test at wafer level only.

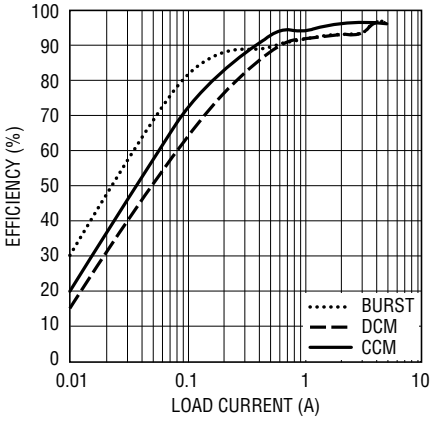
Note 7: Absolute Maximum Rating of –5V on SW1 and SW2 is under transient condition only.

TYPICAL PERFORMANCE CHARACTERISTICS (Refer to Figure 18)

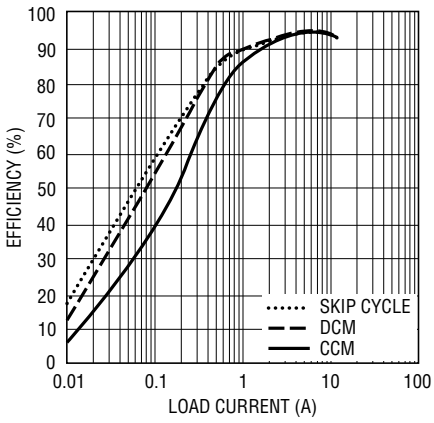
Efficiency vs Load Current 6V_{IN} to 12V_{OUT}



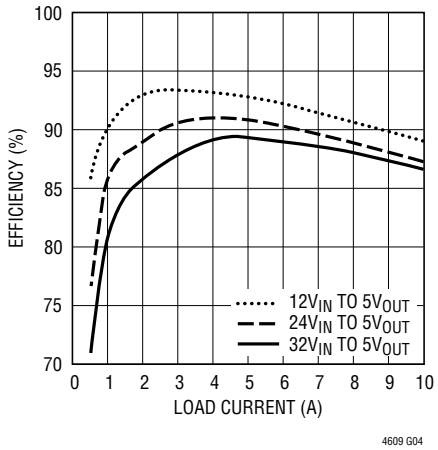
Efficiency vs Load Current 12V_{IN} to 12V_{OUT}



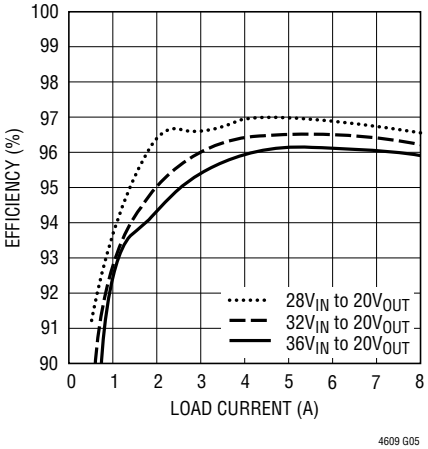
Efficiency vs Load Current 32V_{IN} to 12V_{OUT}



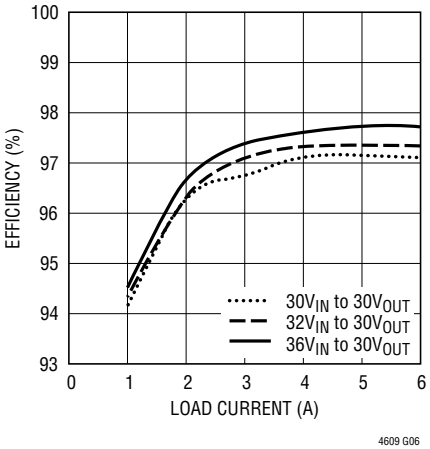
Efficiency vs Load Current 3.3µH Inductor



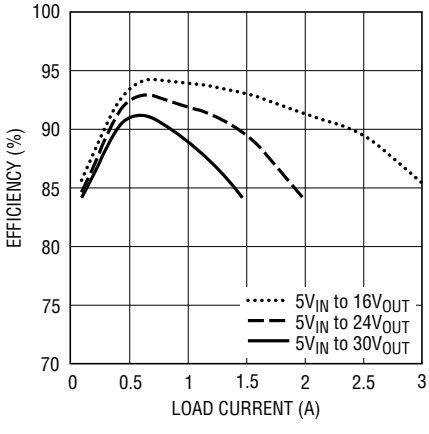
Efficiency vs Load Current 5.6µH Inductor



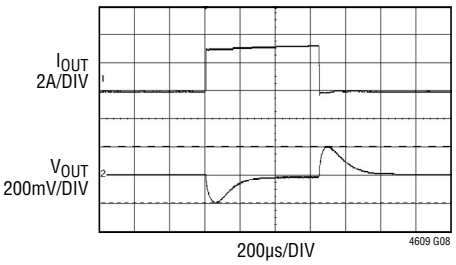
Efficiency vs Load Current 8µH Inductor



Efficiency vs Load Current 3.3µH Inductor

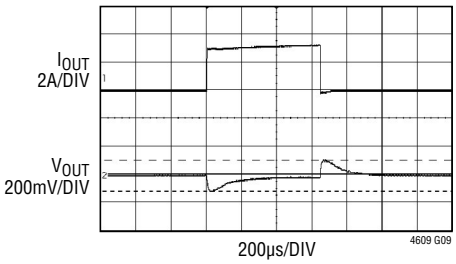


Transient Response from 6V_{IN} to 12V_{OUT}



LOAD STEP: 0A TO 3A AT CCM
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 15mΩ SENSING RESISTORS

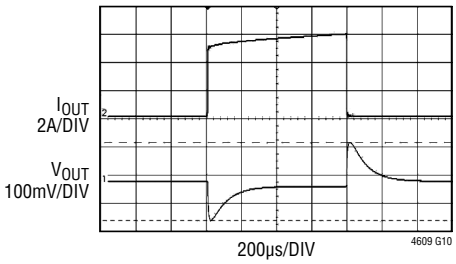
Transient Response from 12V_{IN} to 12V_{OUT}



LOAD STEP: 0A TO 3A AT CCM
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 15mΩ SENSING RESISTORS

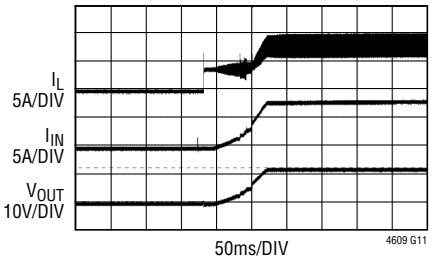
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response from $32V_{IN}$ to $12V_{OUT}$



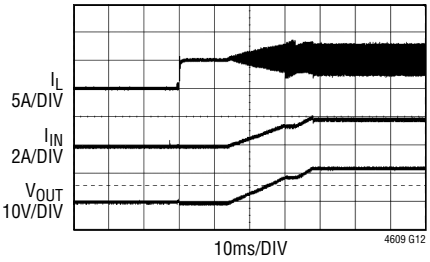
LOAD STEP: 0A TO 5A AT CCM
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 12mΩ SENSING RESISTORS

Start-Up with $6V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 4A



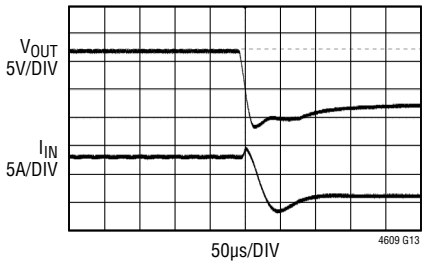
0.1µF SOFT-START CAP
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 12mΩ SENSING RESISTORS

Start-Up with $32V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 5A



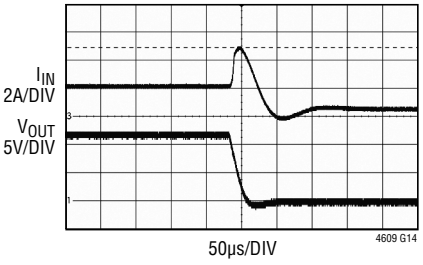
0.1µF SOFT-START CAP
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 12mΩ SENSING RESISTORS

Short Circuit with $6V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 4A



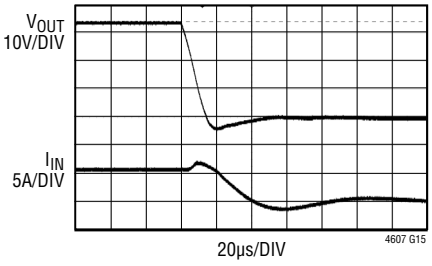
OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 12mΩ SENSING RESISTORS

Short Circuit with $32V_{IN}$ to $12V_{OUT}$ at I_{OUT} = 5A



OUTPUT CAPS: 4x 22µF CERAMIC CAPS AND
2x 180µF ELECTROLYTIC CAPS
2x 12mΩ SENSING RESISTORS

Short Circuit with $12V_{IN}$ to $34V_{OUT}$ at I_{OUT} = 2A



OUTPUT CAPS: 2x 10µF 50V CERAMIC CAPS AND
2x 47µF 50V ELECTROLYTIC CAPS
2x 15mΩ SENSING RESISTORS

PIN FUNCTIONS

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

V_{OUT} (Bank 5): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins.

PGND (Bank 6): Power Ground Pins for Both Input and Output Returns.

SW1, SW2 (Bank 4, Bank 2): Switch Nodes. The power inductor is connected between SW1 and SW2.

R_{SENSE} (Bank 3): Sensing Resistor Pin. The sensing resistor is connected from this pin to PGND.

$SENSE^+$ (Pin A4): Positive Input to the Current Sense and Reverse Current Detect Comparators.

$SENSE^-$ (Pin A5): Negative Input to the Current Sense and Reverse Current Detect Comparators.

$EXTV_{CC}$ (Pin F6): External V_{CC} Input. When $EXTV_{CC}$ exceeds 5.7V, an internal switch connects this pin to $INTV_{CC}$ and shuts down the internal regulator so that the controller and gate drive power is drawn from $EXTV_{CC}$. Do not exceed 7V at this pin and ensure that $EXTV_{CC} < V_{IN}$

$INTV_{CC}$ (Pin F5): Internal 6V Regulator Output. This pin is for additional decoupling of the 6V internal regulator. Do not source more than 40mA from $INTV_{CC}$.

PLLIN (Pin B9): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. The phase-locked loop will force the rising bottom gate signal of the controller to be synchronized with the rising edge of PLLIN signal.

PLLFLTR (Pin B8): The lowpass filter of the phase-locked loop is tied to this pin. This pin can also be used to set the frequency of the internal oscillator with an AC or DC voltage. See the Applications Information section for details.

SS (Pin A6): Soft-Start Pin. Soft-start reduces the input surge current from the power source by gradually increasing the controller's current limit.

STBYMD (Pin A10): LDO Control Pin. Determines whether the internal LDO remains active when the controller is shut down. See Operations section for details. If the STBYMD pin is pulled to ground, the SS pin is internally pulled to ground to disable start-up and thereby providing a single control pin for turning off the controller. An internal decoupling capacitor is tied to this pin.

V_{FB} (Pin B6): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 100k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See the Applications Information section.

FCB (Pin A9): Forced Continuous Control Input. The voltage applied to this pin sets the operating mode of the module. When the applied voltage is less than 0.8V, the forced continuous current mode is active in boost operation and the skip cycle mode is active in buck operation. When the pin is tied to $INTV_{CC}$, the constant frequency discontinuous current mode is active in buck or boost operation. See the Applications Information section.

SGND (Pin A7): Signal Ground Pin. This pin connects to PGND at output capacitor point.

COMP (Pin B7): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V.

PGOOD (Pin B5): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN (Pin A8): Run Control Pin. A voltage below 1.6V will turn off the module. There is a 100k resistor between the RUN pin and SGND in the module. Do not apply more than 6V to this pin. See the Applications Information section.

SIMPLIFIED BLOCK DIAGRAM

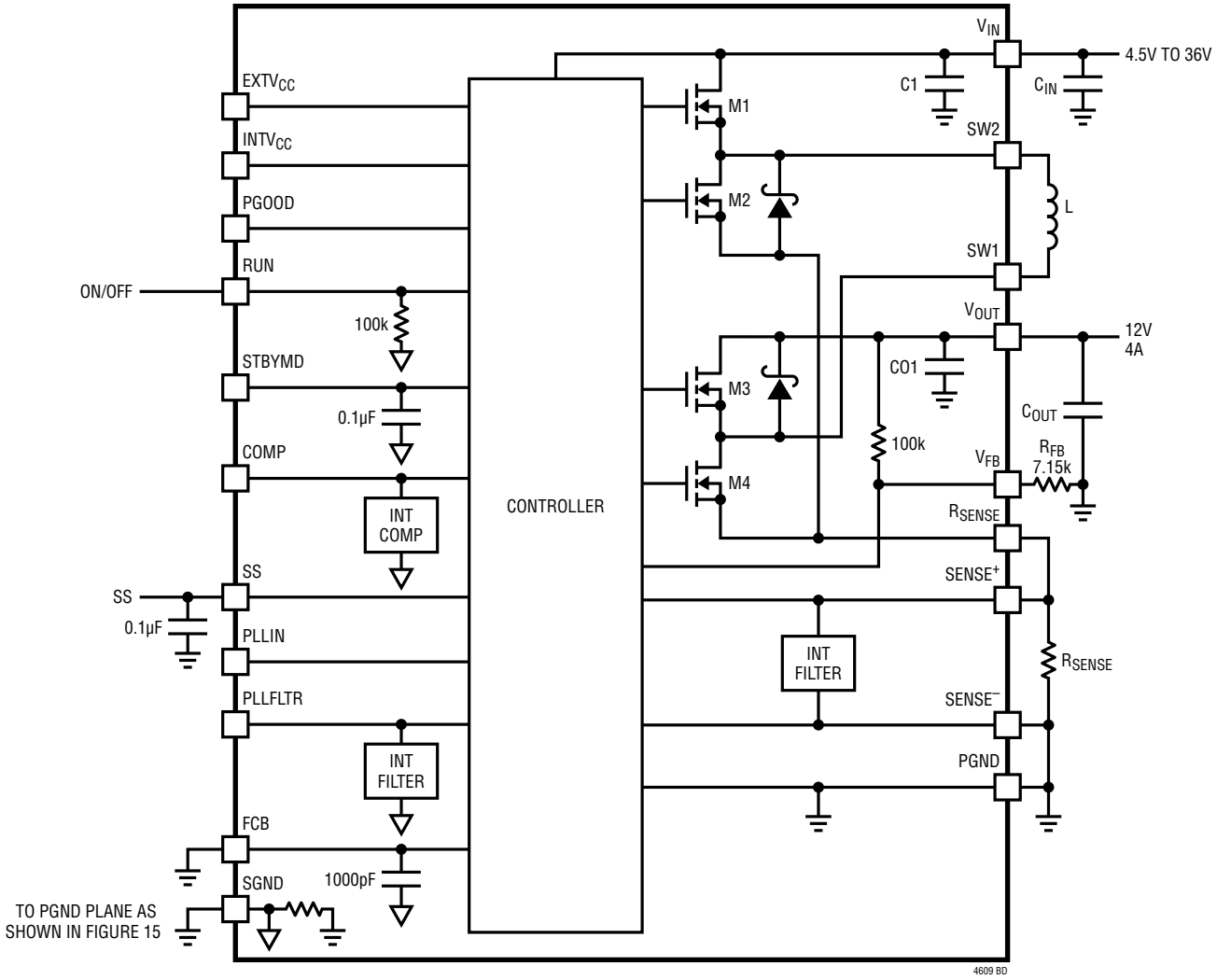


Figure 1. Simplified LTM4609 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 36V, V_{OUT} = 12V)	I_{OUT} = 4A	10			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 36V, V_{OUT} = 12V)	I_{OUT} = 4A	200	300		µF

OPERATION

Power Module Description

The LTM4609 is a non-isolated buck-boost DC/DC power supply. It can deliver a wide range output voltage from 0.8V to 34V over a wide input range from 4.5V to 36V, by only adding the sensing resistor, inductor and some external input and output capacitors. It provides precisely regulated output voltage programmable via one external resistor. The typical application schematic is shown in Figure 18.

The LTM4609 has an integrated current mode buck-boost controller, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. With current mode control and internal feedback loop compensation, the LTM4609 module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors. The operating frequency of the LTM4609 can be adjusted from 200kHz to 400kHz by setting the voltage on the PLLFLTR pin. Alternatively, its frequency can be synchronized by the input clock signal from the PLLIN pin. The typical switching frequency is 400kHz.

The Burst Mode® and skip-cycle mode operations can be enabled at light loads to improve efficiency, while the forced continuous mode and discontinuous mode operations are used for constant frequency applications. Foldback current limiting is activated in an overcurrent condition as V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits the ±7.5% window around the regulation point. Pulling the RUN pin below 1.6V forces the controller into its shutdown state.

If an external bias supply is applied on the $EXTV_{CC}$ pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher end of the input voltage range.

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The typical LTM4609 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 3 for specific external capacitor requirements for a particular application.

Output Voltage Programming

The PWM controller has an internal 0.8V reference voltage. As shown in the Block Diagram, a 100k internal feedback resistor connects V_{OUT} and V_{FB} pins together. Adding a resistor R_{FB} from the V_{FB} pin to the SGND pin programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{100k + R_{FB}}{R_{FB}}$$

Table 1. R_{FB} Resistor (0.5%) vs Output Voltage

V_{OUT}	0.8V	1.5V	2.5V	3.3V	5V	6V	8V	9V
R_{FB}	Open	115k	47.5k	32.4k	19.1k	15.4k	11k	9.76k
V_{OUT}	10V	12V	15V	16V	20V	24V	30V	34V
R_{FB}	8.66k	7.15k	5.62k	5.23k	4.12k	3.4k	2.74k	2.37k

Operation Frequency Selection

The LTM4609 uses current mode control architecture at constant switching frequency, which is determined by the internal oscillator's capacitor. This internal capacitor is charged by a fixed current plus an additional current that is proportional to the voltage applied to the PLLFLTR pin. The PLLFLTR pin can be grounded to lower the frequency to 200kHz or tied to 2.4V to yield approximately 400kHz. When PLLFLTR is left open, the PLLFLTR pin goes low, forcing the oscillator to its minimum frequency.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 2. As the operating frequency increases, the gate charge losses will be higher, thus the efficiency is lower. The maximum switching frequency is approximately 400kHz.

FREQUENCY SYNCHRONIZATION

The LTM4609 can also be synchronized to an external source via the PLLIN pin instead of adjusting the voltage on the PLLFLTR pin directly. The power module has a

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phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows turning on the internal top MOSFET for locking to the rising edge of the external clock. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop. The input pulse width of the clock has to be at least 400ns, and 2V in amplitude. The synchronized frequency ranges from 200kHz to 400kHz, corresponding to a DC voltage input from 0V to 2.4V at PLLFLTR. During the start-up of the regulator, the phase-locked loop function is disabled.

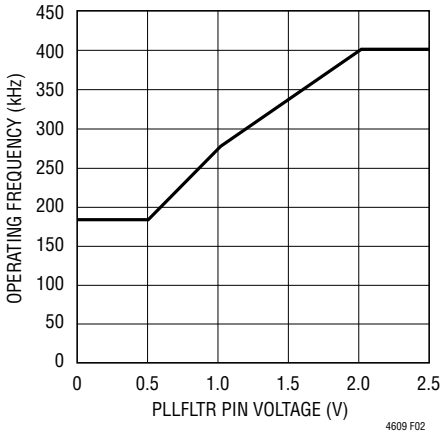

Figure 2. Frequency vs PLLFLTR Pin Voltage

Low Current Operation

To improve efficiency at low output current operation, LTM4609 provides three modes for both buck and boost operations by accepting a logic input on the FCB pin. Table 2 shows the different operation modes.

Table 2. Different Operating Modes (V_{INTVCC} = 6V)

FCB PIN	BUCK	BOOST
0V to 0.75V	Force Continuous Mode	Force Continuous Mode
0.85V to V_{INTVCC} – 1V	Skip-Cycle Mode	Burst Mode Operation
>5.3V	DCM with Constant Freq	DCM with Constant Freq

When the FCB pin voltage is lower than 0.8V, the controller behaves as a continuous, PWM current mode synchronous switching regulator. When the FCB pin voltage is below V_{INTVCC} – 1V, but greater than 0.85V, where V_{INTVCC} is 6V, the controller enters Burst Mode operation in boost operation or enters skip-cycle mode in buck operation. During boost operation, Burst Mode operation is activated if the load current is lower than the preset minimum output current level. The MOSFETs will turn on for several cycles, followed by a variable "sleep" interval depending upon the load current. During buck operation, skip-cycle mode sets a minimum positive inductor current level. In this mode, some cycles will be skipped when the output load current drops below 1% of the maximum designed load in order to maintain the output voltage.

When the FCB pin voltage is tied to the $INTV_{CC}$ pin, the controller enters constant frequency discontinuous current mode (DCM). For boost operation, if the output voltage is high enough, the controller can enter the continuous current buck mode for one cycle to discharge inductor current. In the following cycle, the controller will resume DCM boost operation. For buck operation, constant frequency discontinuous current mode is turned on if the preset minimum negative inductor current level is reached. At very light loads, this constant frequency operation is not as efficient as Burst Mode operation or skip-cycle, but does provide low noise, constant frequency operation.

Input Capacitors

In boost mode, since the input current is continuous, only minimum input capacitors are required. However, the input current is discontinuous in buck mode. So the selection of input capacitor C_{IN} is driven by the need of filtering the input square wave current.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η is the estimated efficiency of the power module. C_{IN} can be a switcher-rated electrolytic aluminum capacitor, OS-CON capacitor or high volume ceramic capacitors. Note the capacitor ripple current ratings are often based on temperature and hours of life.

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This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

Output Capacitors

In boost mode, the discontinuous current shifts from the input to the output, so the output capacitor C_{OUT} must be capable of reducing the output voltage ripple.

For boost and buck modes, the steady ripple due to charging and discharging the bulk capacitance is given by:

$$V_{RIPPLE,BOOST} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$V_{RIPPLE,BUCK} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{8 \bullet L \bullet C_{OUT} \bullet V_{IN(MAX)} \bullet f^2}$$

The steady ripple due to the voltage drop across the ESR (effective series resistance) is given by:

$$V_{ESR,BUCK} = \Delta I_{L(MAX)} \bullet ESR$$

$$V_{ESR,BOOST} = I_{L(MAX)} \bullet ESR$$

The LTM4609 is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough ESR to meet the output voltage ripple and transient requirements. C_{OUT} can be the low ESR tantalum capacitor, the low ESR polymer capacitor or the ceramic capacitor. Multiple capacitors can be placed in parallel to meet the ESR and RMS current handling requirements. The typical capacitance is 300µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot at a current transient.

Inductor Selection

The inductor is chiefly decided by the required ripple current and the operating frequency. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current. In the inductor design, the worst cases in continuous mode are considered as follows:

$$L_{BOOST} \geq \frac{V^2_{IN} \bullet \left(V_{OUT(MAX)} - V_{IN}\right)}{V^2_{OUT(MAX)} \bullet f \bullet I_{OUT(MAX)} \bullet Ripple\%}$$

$$L_{BUCK} \geq \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \bullet f \bullet I_{OUT(MAX)} \bullet Ripple\%}$$

where:

f is operating frequency, Hz

Ripple% is allowable inductor current ripple, %

$V_{OUT(MAX)}$ is maximum output voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

$I_{OUT(MAX)}$ is maximum output load current, A

The inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturation. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. Please refer to Table 3 for the recommended inductors for different cases.

R_{SENSE} Selection and Maximum Output Current

R_{SENSE} is chosen based on the required inductor current. Since the maximum inductor valley current at buck mode is much lower than the inductor peak current at boost mode, different sensing resistors are suggested to use in buck and boost modes.

The current comparator threshold sets the peak of the inductor current in boost mode and the maximum inductor valley current in buck mode. In boost mode, the allowed maximum average load current is:

$$I_{OUT(MAX,BOOST)} = \left(\frac{160mV}{R_{SENSE}} - \frac{\Delta I_L}{2}\right) \bullet \frac{V_{IN}}{V_{OUT}}$$

where ΔI_L is peak-to-peak inductor ripple current.

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In buck mode, the allowed maximum average load current is:

$$I_{OUT(MAX,BUCK)} = \frac{130mV}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

The maximum current sensing R_{SENSE} value for the boost mode is:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet 160mV \bullet V_{IN}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_L \bullet V_{IN}}$$

The maximum current sensing R_{SENSE} value for the buck mode is:

$$R_{SENSE(MAX,BUCK)} = \frac{2 \bullet 130mV}{2 \bullet I_{OUT(MAX,BUCK)} - \Delta I_L}$$

A 20% to 30% margin on the calculated sensing resistor is usually recommended. Please refer to Table 3 for the recommended sensing resistors for different applications.

Soft-Start

The SS pin provides a means to soft-start the regulator. A capacitor on this pin will program the ramp rate of the output voltage. A 1.7µA current source will charge up the external soft-start capacitor. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = \frac{2.4V \bullet C_{SS}}{1.7\mu A}$$

When the RUN pin falls below 1.6V, then the soft-start pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and force continuous mode are disabled during the soft-start process. Do not apply more than 6V to the SS pin.

Run Enable

The RUN pin is used to enable the power module. The pin can be driven with a logic input, not to exceed 6V.

The RUN pin can also be used as an undervoltage lockout (UVLO) function by connecting a resistor from the input supply to the RUN pin. The equation:

$$V\_UVLO = \frac{R1+R2}{R2} \bullet 1.6V$$

Power Good

The PGOOD pin is an open drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±7.5% window around the regulation point.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages. A spice model is available for other control loop optimization.

Fault Conditions: Current Limit and Overcurrent Foldback

LTM4609 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady state operation, but also in transient. Refer to Table 3.

To further limit current in the event of an overload condition, the LTM4609 provides foldback current limiting. If the output voltage falls by more than 70%, then the maximum output current is progressively lowered to about 30% of its full current limit value for boost mode and about 40% for buck mode.

Standby Mode (STBYMD)

The standby mode (STBYMD) pin provides several choices for start-up and standby operational modes. If the pin is pulled to ground, the SS pin is internally pulled to ground, preventing start-up and thereby providing a single control

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pin for turning off the controller. If the pin is left open or decoupled with a capacitor to ground, the SS pin is internally provided with a starting current, permitting external control for turning on the controller. If the pin is connected to a voltage greater than 1.25V, the internal regulator ($INTV_{CC}$) will be on even when the controller is shut down (RUN pin voltage <1.6V). In this mode, the onboard 6V output linear regulator can provide power to keep-alive functions such as a keyboard controller.

$INTV_{CC}$ and $EXTV_{CC}$

An internal P-channel low dropout regulator produces 6V at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the control chip and internal circuitry within the module.

The LTM4609 also provides the external supply voltage pin $EXTV_{CC}$. When the voltage applied to $EXTV_{CC}$ rises above 5.7V, the internal regulator is turned off and an internal switch connects the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal power. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 5.4V. This allows the MOSFET driver and control power to be derived from the output when ($5.7V < V_{OUT} < 7V$) and from the internal regulator when the output is out of regulation (start-up, short-circuit). If more current is required through the $EXTV_{CC}$ switch than is specified, an external Schottky diode can be interposed between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Ensure that $EXTV_{CC} \leq V_{IN}$.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 6V regulator at the cost of a small efficiency penalty.
2. $EXTV_{CC}$ connected directly to V_{OUT} ($5.7V < V_{OUT} < 7V$). This is the normal connection for a 6V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5.5V to 7V range, it may be used to power $EXTV_{CC}$ provided it is compatible with the MOSFET gate drive requirements.

Thermal Considerations and Output Current Derating

In different applications, LTM4609 operates in a variety of thermal environments. The maximum output current is limited by the environmental thermal condition. Sufficient cooling should be provided to ensure reliable operation. When the cooling is limited, proper output current derating is necessary, considering ambient temperature, airflow, input/output condition, and the need for increased reliability.

The power loss curves in Figures 5 and 6 can be used in coordination with the load current derating curves in Figures 7 to 14 for calculating an approximate θ_{JA} for the module. Column designation delineates between no heat sink, and a BGA heat sink. Each of the load current derating curves will lower the maximum load current as a function of the increased ambient temperature to keep the maximum junction temperature of the power module at 115°C allowing a safe margin for the maximum operating temperature below 125°C. Each of the derating curves and the power loss curve that corresponds to the correct output voltage can be used to solve for the approximate θ_{JA} of the condition.

DESIGN EXAMPLES

Buck Mode Operation

As a design example, use input voltage V_{IN} = 12V to 36V, V_{OUT} = 12V and f = 400kHz.

Set the PLLFLTR pin at 2.4V or more for 400kHz frequency and connect FCB to ground for continuous current mode operation. If a divider is used to set the frequency as shown in Figure 16, the bottom resistor R3 is recommended not to exceed 1kΩ.

To set the output voltage at 12V, the resistor R_{FB} from V_{FB} pin to ground should be chosen as:

$$R_{FB} = \frac{0.8V \bullet 100k}{V_{OUT} - 0.8V} \approx 7.15k$$

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To choose a proper inductor, we need to know the current ripple at different input voltages. The inductor should be chosen by considering the worst case in the practical operating region. If the maximum output power P is 120W at buck mode, we can get the current ripple ratio of the current ripple ΔI_L to the maximum inductor current I_L as follows:

$$\frac{\Delta I_L}{I_L} = \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}^2}{V_{IN} \bullet L \bullet f \bullet P}$$

Figure 3 shows the current ripple ratio at different input voltages based on the inductor values: 2.5µH, 3.3µH, 4.7µH and 6µH. If we need about 40% ripple current ratio at all inputs, the 4.7µH inductor can be selected.

At buck mode, sensing resistor selection is based on the maximum output current and the allowed maximum sensing threshold 130mV.

$$R_{SENSE} = \frac{2 \bullet 130mV}{2 \bullet (P / V_{OUT}) - \Delta I_L}$$

Consider the safety margin about 30%, we can choose the sensing resistor as 9mΩ.

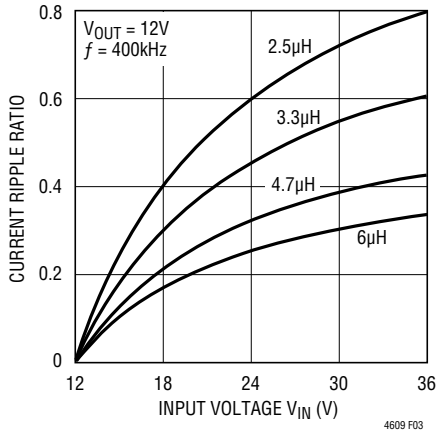

Figure 3. Current Ripple Ratio at Different Inputs for Buck Mode

For the input capacitor, use a low ESR sized capacitor to handle the maximum RMS current. Input capacitors are required to be placed adjacent to the module. In Figure 16, the 10µF ceramic input capacitors are selected for their ability to handle the large RMS current into the converter. The 100µF bulk capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

For the output capacitor, the output voltage ripple and transient requirements require low ESR capacitors. If assuming that the ESR dominates the output ripple, the output ripple is as follows:

$$\Delta V_{OUT(P-P)} = ESR \bullet \Delta I_L$$

If a total low ESR of about 5mΩ is chosen for output capacitors, the maximum output ripple of 21.5mV occurs at the input voltage of 36V with the current ripple at 4.3A.

Boost Mode Operation

For boost mode operation, use input voltage V_{IN} = 5V to 12V, V_{OUT} = 12V and f = 400kHz.

Set the PLLFLTR pin and R_{FB} as in buck mode.

If the maximum output power P is 50W at boost mode and the module efficiency η is about 90%, we can get the current ripple ratio of the current ripple ΔI_L to the maximum inductor current I_L as follows:

$$\frac{\Delta I_L}{I_L} = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}^2 \eta}{V_{OUT} \bullet L \bullet f \bullet P}$$

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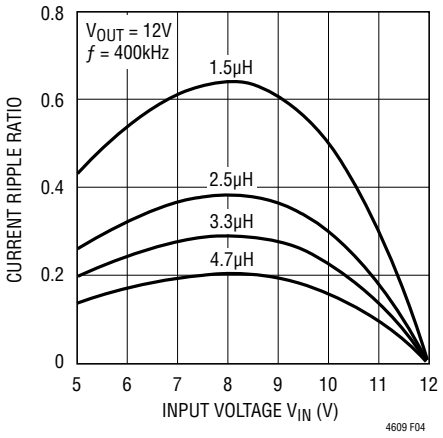

Figure 4. Current Ripple Ratio at Different Inputs for Boost Mode

Figure 4 shows the current ripple ratio at different input voltages based on the inductor values: 1.5µH, 2.5µH, 3.3µH and 4.7µH. If we need 30% ripple current ratio at all inputs, the 3.3µH inductor can be selected.

At boost mode, sensing resistor selection is based on the maximum input current and the allowed maximum sensing threshold 160mV.

$$R_{SENSE} = \frac{2 \bullet 160mV}{2 \bullet \frac{P}{\eta \bullet V_{IN(MIN)}} + \Delta I_L}$$

Consider the safety margin about 30%, we can choose the sensing resistor as 8mΩ.

For the input capacitor, only minimum capacitors are needed to handle the maximum RMS current, since it is a continuous input current at boost mode. A 100µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

Since the output capacitors at boost mode need to filter the square wave current, more capacitors are expected to achieve the same output ripples as the buck mode. If assuming that the ESR dominates the output ripple, the output ripple is as follows:

$$\Delta V_{OUT(P-P)} = ESR \bullet I_{L(MAX)}$$

If a total low ESR about 5mΩ is chosen for output capacitors, the maximum output ripple of 70mV occurs at the input voltage of 5V with the peak inductor current at 14A.

An RC snubber is recommended on SW1 to obtain low switching noise, as shown in Figure 17.

Wide Input Mode Operation

If a wide input range is required from 5V to 36V, the module will work in different operation modes. If input voltage V_{IN} = 5V to 36V, V_{OUT} = 12V and f = 400kHz, the design needs to consider the worst case in buck or boost mode design. Therefore, the maximum output power is limited to 60W. The sensing resistor is chosen at 8mΩ, the input capacitor is the same as the buck mode design and the output capacitor uses the boost mode design. Since the maximum output ripple normally occurs at boost mode in the wide input mode design, more inductor ripple current, up to 150% of the inductor current, is allowed at buck mode to meet the ripple design requirement. Thus, a 3.3µH inductor is chosen at the wide input mode. The maximum output ripple voltage is still 70mV if the total ESR is about 5mΩ.

Additionally, the current limit may become very high when the module runs at buck mode due to the low sensing resistor used in the wide input mode operation.

Safety Considerations

The LTM4609 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

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Table 3. Typical Components (f = 400kHz)

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
TDK	C4532X7R1E226M (22µF, 25V)	Sanyo	16SVP180MX (180µF, 16V), 20SVP150MX (150µF, 20V)
INDUCTOR VENDORS	**PART NUMBER**	**R_{SENSE} VENDORS**	**PART NUMBER**
Toko	FDA1254	Vishay	Power Metal Strip Resistors WSL1206-18
Sumida	CDEP134, CDEP145, CDEP147	Panasonic	Thick Film Chip Resistors ERJ12

V_{IN} (V)	V_{OUT} (V)	R_{SENSE} (0.5W RATING)	Inductor (µH)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	$I_{OUT(MAX)}$* (A)
5	10	2 × 16mW 0.5W	2.2	None	150µF 35V	4 × 22µF 25V	2 × 180µF 16V	4
15	10	2 × 18mW 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
20	10	2 × 20mW 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10
24	10	2 × 18mΩ 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10
32	10	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	9
36	10	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 180µF 16V	9
6	12	2 × 14mΩ 0.5W	2.2	None	150µF 35V	4 × 22µF 25V	2 × 180µF 16V	4
16	12	2 × 16mW 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
20	12	2 × 18mW 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10
24	12	2 × 18mΩ 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	9
32	12	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	9
36	12	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 180µF 16V	9
5	16	2 × 18mW 0.5W	3.3	None	150µF 35V	4 × 22µF 25V	2 × 150µF 20V	2.5
8	16	2 × 16mW 0.5W	3.3	None	150µF 35V	4 × 22µF 25V	2 × 150µF 20V	4
12	16	2 × 14mW 0.5W	2.2	None	150µF 35V	4 × 22µF 25V	2 × 150µF 20V	8
20	16	2 × 20mW 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 150µF 20V	10
24	16	2 × 20mΩ 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 150µF 20V	10
32	16	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 150µF 20V	9
36	16	2 × 22mΩ 0.5W	6	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 150µF 20V	9
5	20	2 × 18mΩ 0.5W	3.3	NONE	150µF 50V	4 × 22µF 25V	2 × 150µF 50V	2
10	20	2 × 18mΩ 0.5W	3.3	NONE	150µF 50V	4 × 22µF 25V	2 × 150µF 50V	5
32	20	1 × 12mΩ 0.5W	6	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 150µF 50V	9
36	20	1 × 13mΩ 0.5W	8	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 150µF 50V	8
5	24	2 × 16mΩ 0.5W	3.3	NONE	150µF 50V	4 × 22µF 25V	2 × 150µF 50V	1.5
12	24	2 × 18mΩ 0.5W	4.7	NONE	150µF 50V	4 × 22µF 25V	2 × 150µF 50V	5
32	24	1 × 14mΩ 0.5W	4.7	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 150µF 50V	8
36	24	1 × 13mΩ 0.5W	7	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 150µF 50V	8

APPLICATIONS INFORMATION

Table 3. Typical Components (f = 400kHz) Continued

V_{IN} (V)	V_{OUT} (V)	R_{SENSE} (0.5W RATING)	Inductor (µH)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	$I_{OUT(MAX)}$* (A)
5	30	2 × 16mΩ 0.5W	3.3	NONE	150µF 50V	4 × 22µF 50V	2 × 150µF 50V	1.3
12	30	2 × 14mΩ 0.5W	4.7	NONE	150µF 50V	4 × 22µF 50V	2 × 150µF 50V	3
32	30	1 × 12mΩ 0.5W	2.5	2 × 10µF 50V	150µF 50V	2 × 22µF 50V	2 × 150µF 50V	8
36	30	1 × 13mΩ 0.5W	4.7	2 × 10µF 50V	150µF 50V	2 × 22µF 50V	2 × 150µF 50V	8
5	34	2 × 18mΩ 0.5W	3.3	NONE	150µF 50V	4 × 22µF 50V	2 × 150µF 50V	1
12	34	2 × 16mΩ 0.5W	4.7	NONE	150µF 50V	4 × 22µF 50V	2 × 150µF 50V	3
24	34	1 × 12mΩ 0.5W	5.6	NONE	150µF 50V	4 × 22µF 50V	2 × 150µF 50V	5
36	34	1 × 12mΩ 0.5W	2.5	2 × 10µF 50V	150µF 50V	2 × 22µF 50V	2 × 150µF 50V	8

INDUCTOR MANUFACTURER	WEBSITE	PHONE NUMBER
Sumida	www.sumida.com	408-321-9660
Toko	www.toko.com	847-297-0070

SENSING RESISTOR MANUFACTURER	WEBSITE	PHONE NUMBER
Panasonic	www.panasonic.com/industrial/components	949-462-1816
KOA	www.koaspeer.com	814-362-5536
Vishay	www.vishay.com	800-433-5700

*Maximum load current is based on the Linear Technology DC1198A at room temperature with natural convection. Poor board layout design may decrease the maximum load current.

TYPICAL APPLICATIONS

(Power Loss includes all external components)

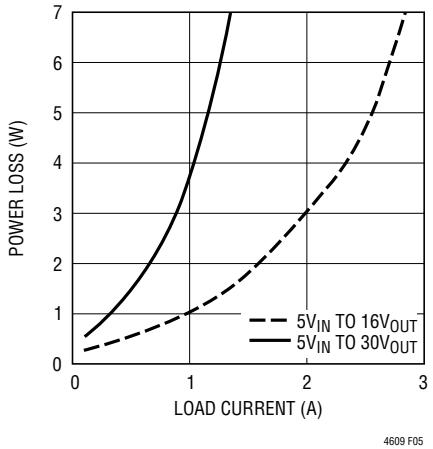


Figure 5. Boost Mode Operation

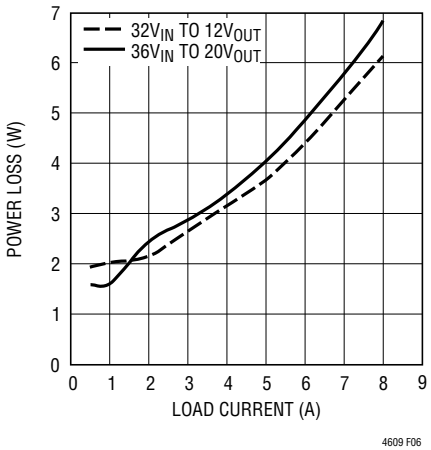


Figure 6. Buck Mode Operation

TYPICAL APPLICATIONS

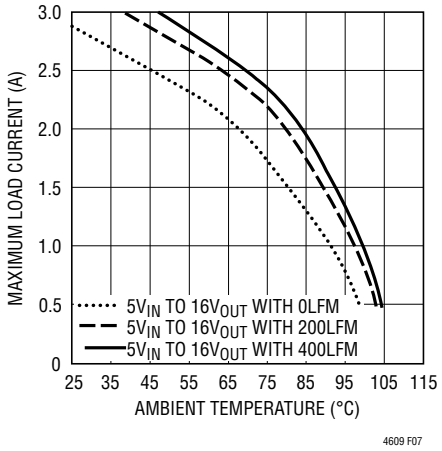


Figure 7. $5V_{IN}$ to $16V_{OUT}$ without Heat Sink

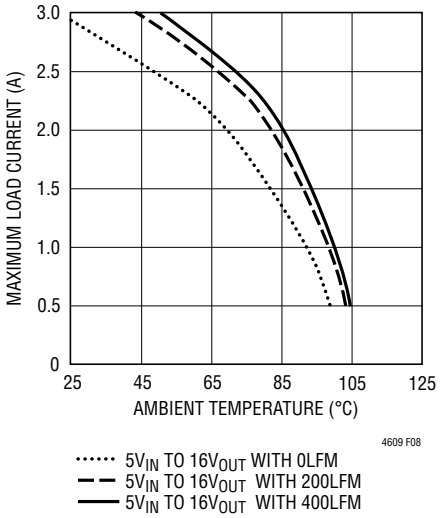


Figure 8. $5V_{IN}$ to $16V_{OUT}$ with Heat Sink

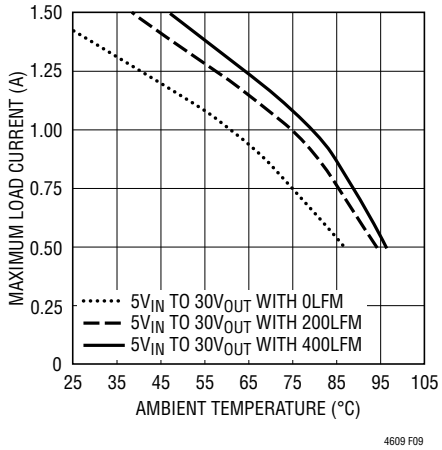


Figure 9. $5V_{IN}$ to $30V_{OUT}$ without Heat Sink

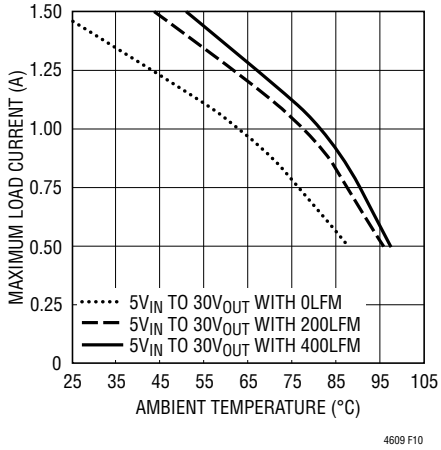


Figure 10. $5V_{IN}$ to $30V_{OUT}$ with Heat Sink

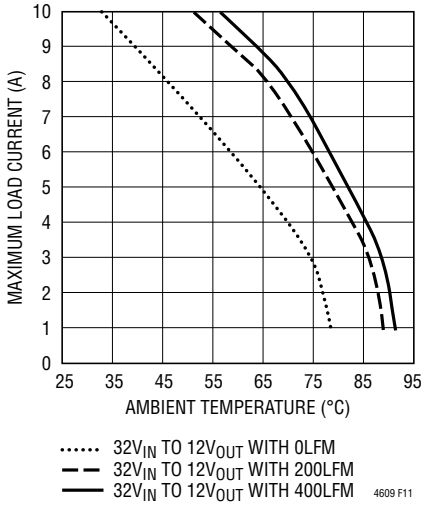


Figure 11. $32V_{IN}$ to $12V_{OUT}$ without Heat Sink

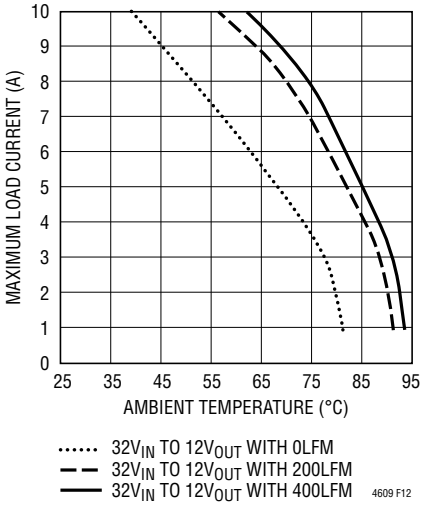


Figure 12. $32V_{IN}$ to $12V_{OUT}$ with Heat Sink

TYPICAL APPLICATIONS

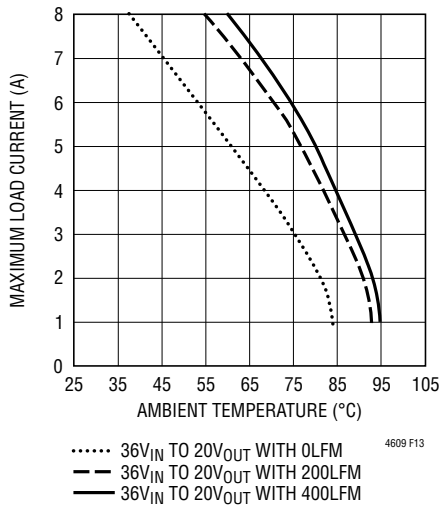


Figure 13. $36V_{IN}$ to $20V_{OUT}$ without Heat Sink

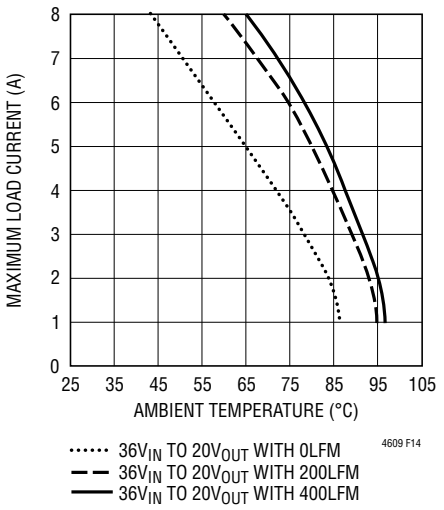


Figure 14. $36V_{IN}$ to $20V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

Table 4. Boost Mode

DERATING CURVE	V_{OUT} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)*
Figure 7, 9	16, 30	Figure 5	0	None	11.4
Figure 7, 9	16, 30	Figure 5	200	None	8.5
Figure 7, 9	16, 30	Figure 5	400	None	7.5
Figure 8, 10	16, 30	Figure 5	0	BGA Heat Sink	11.0
Figure 8, 10	16, 30	Figure 5	200	BGA Heat Sink	7.9
Figure 8, 10	16, 30	Figure 5	400	BGA Heat Sink	7.1

Table 5. Buck Mode

DERATING CURVE	V_{OUT} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)*
Figure 11, 13	12, 20	Figure 6	0	None	8.2
Figure 11, 13	12, 20	Figure 6	200	None	5.9
Figure 11, 13	12, 20	Figure 6	400	None	5.4
Figure 12, 14	12, 20	Figure 6	0	BGA Heat Sink	7.5
Figure 12, 14	12, 20	Figure 6	200	BGA Heat Sink	5.3
Figure 12, 14	12, 20	Figure 6	400	BGA Heat Sink	4.8

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavidthermalloy.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

*The results of thermal resistance from junction to ambient θ_{JA} are based on the demo board DC 1198A. Thus, the maximum temperature on board is treated as the junction temperature (which is in the µModule regulator for most cases) and the power losses from all components are counted for calculations. It has to be mentioned that poor board design may increase the θ_{JA}.

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4609 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, R_{SENSE}, SW1, SW2, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency input and output ceramic capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise
- Route $SENSE^-$ and $SENSE^+$ leads together with minimum PC trace spacing. Avoid sense lines passing through noisy areas, such as switch nodes.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers
- Do not put vias directly on pads, unless the vias are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 15. gives a good example of the recommended layout.

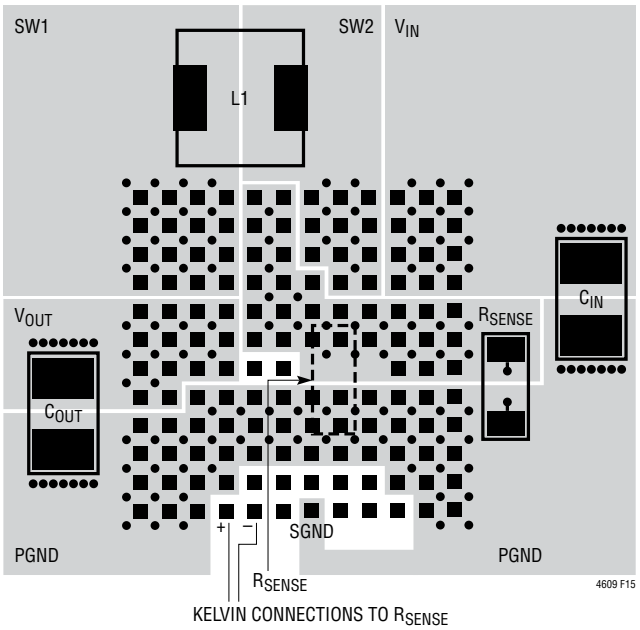


Figure 15. Recommended PCB Layout (LGA Shown, for BGA Use Circle Pads)

TYPICAL APPLICATIONS

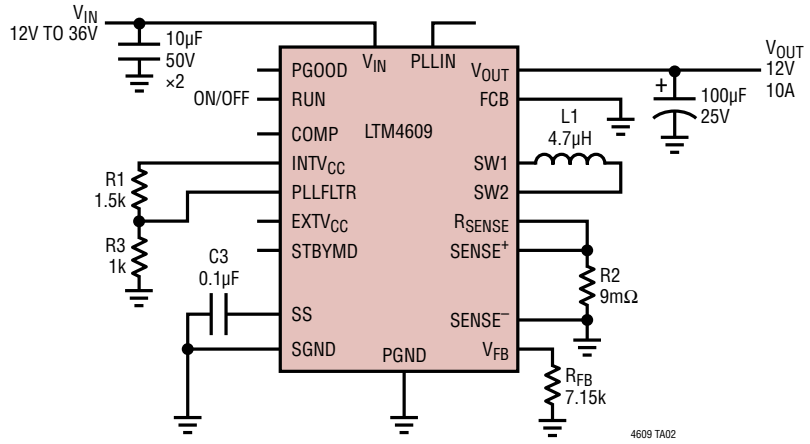


Figure 16. Buck Mode Operation with 12V to 36V Input

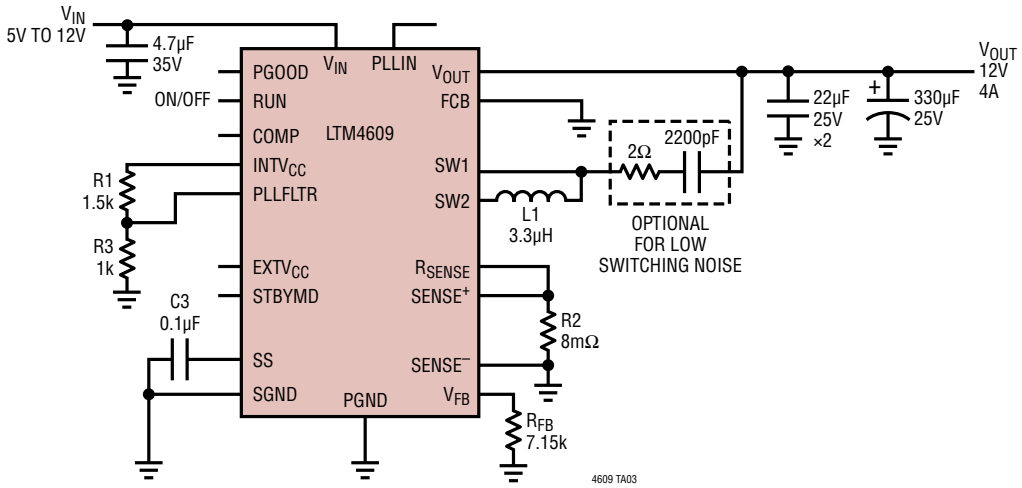


Figure 17. Boost Mode Operation with 5V to 12V Input with Low Switching Noise (Optional)

TYPICAL APPLICATIONS

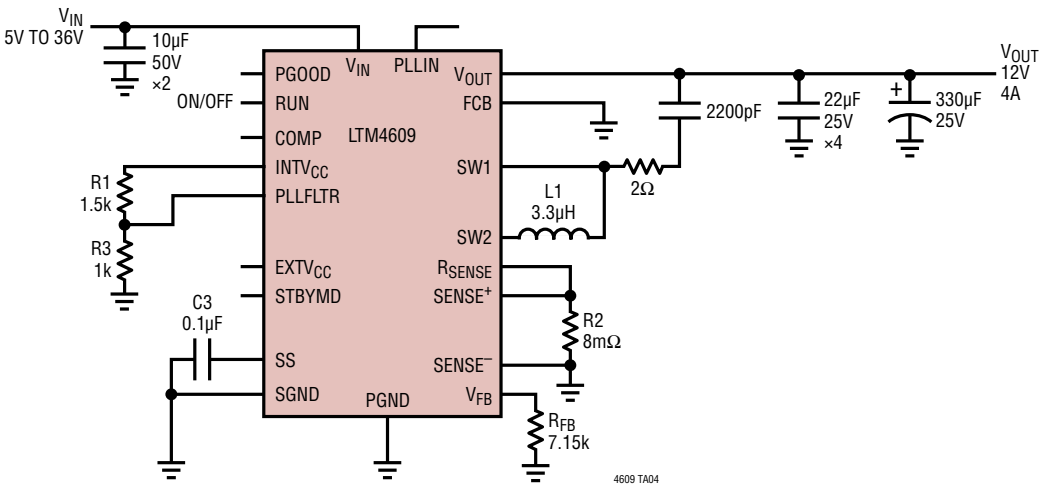


Figure 18. Wide Input Mode with 5V to 36V Input, 12V at 4A Output

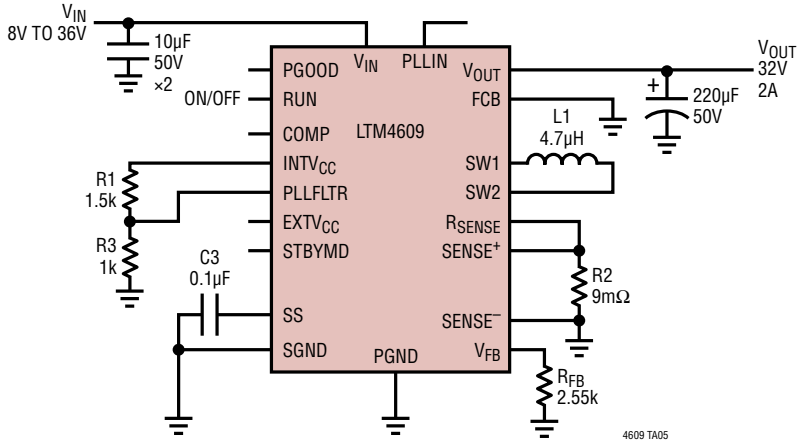


Figure 19. 32V at 2A Design

TYPICAL APPLICATIONS

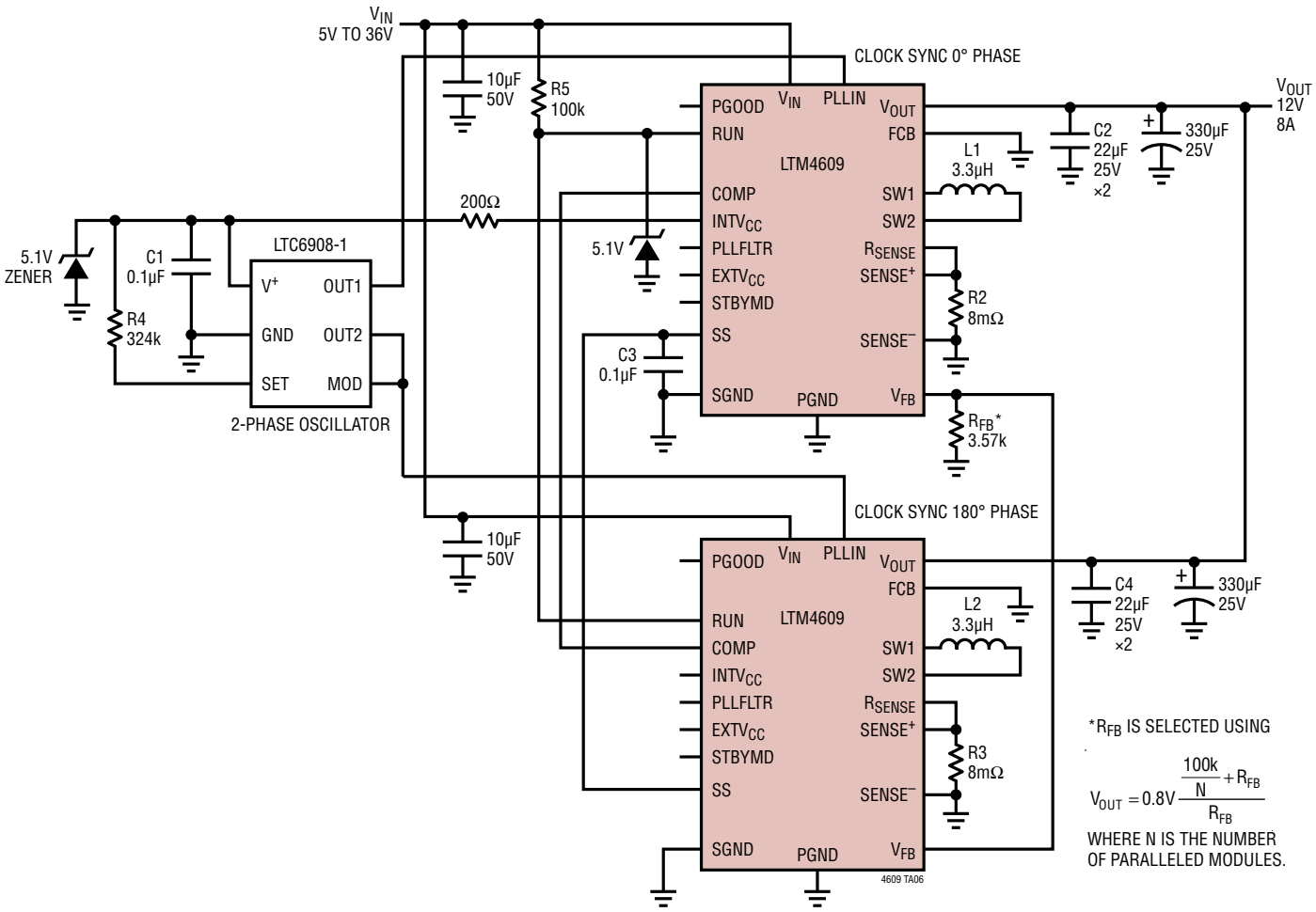
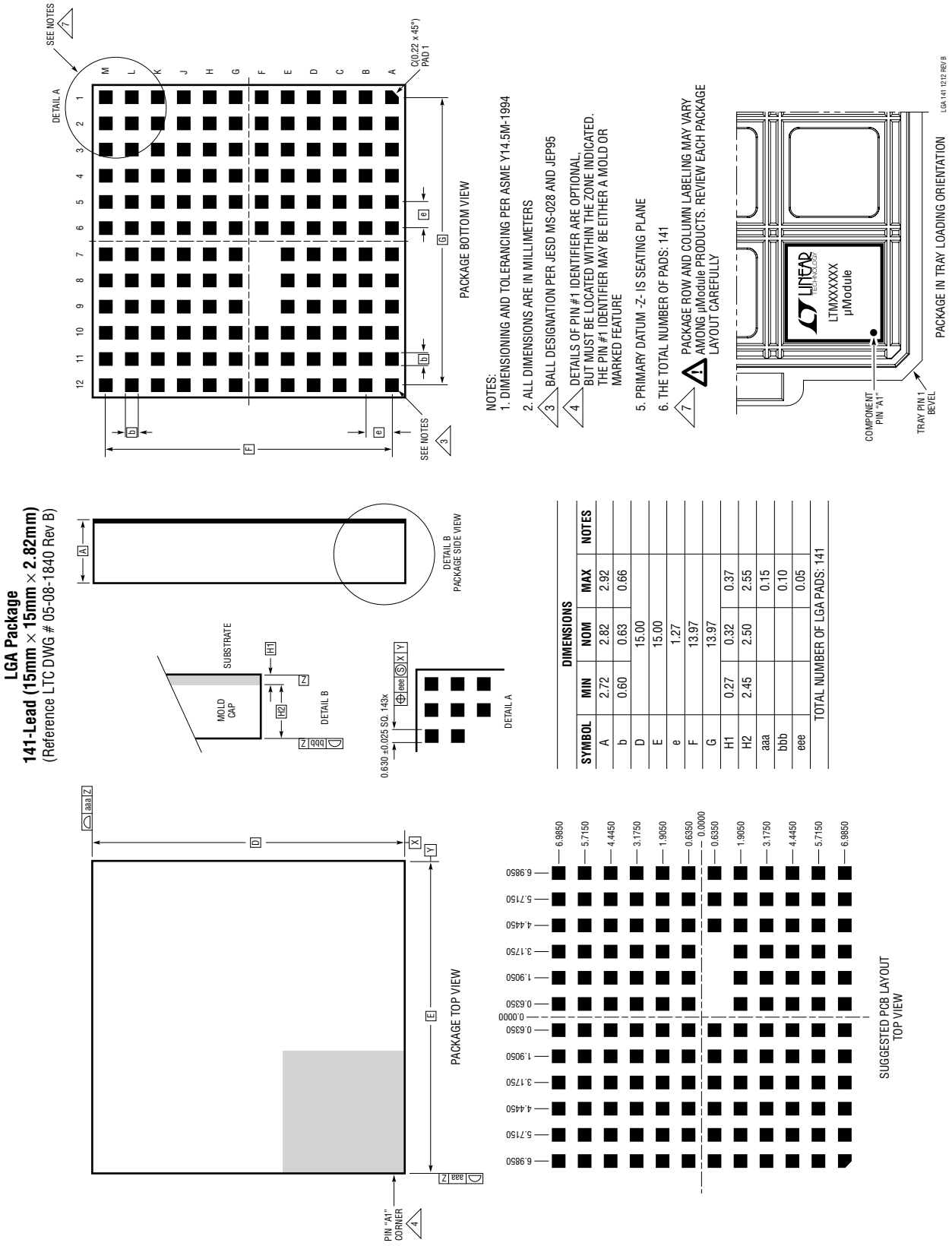


Figure 20. Two-Phase Parallel, 12V at 8A Design

PACKAGE DESCRIPTION

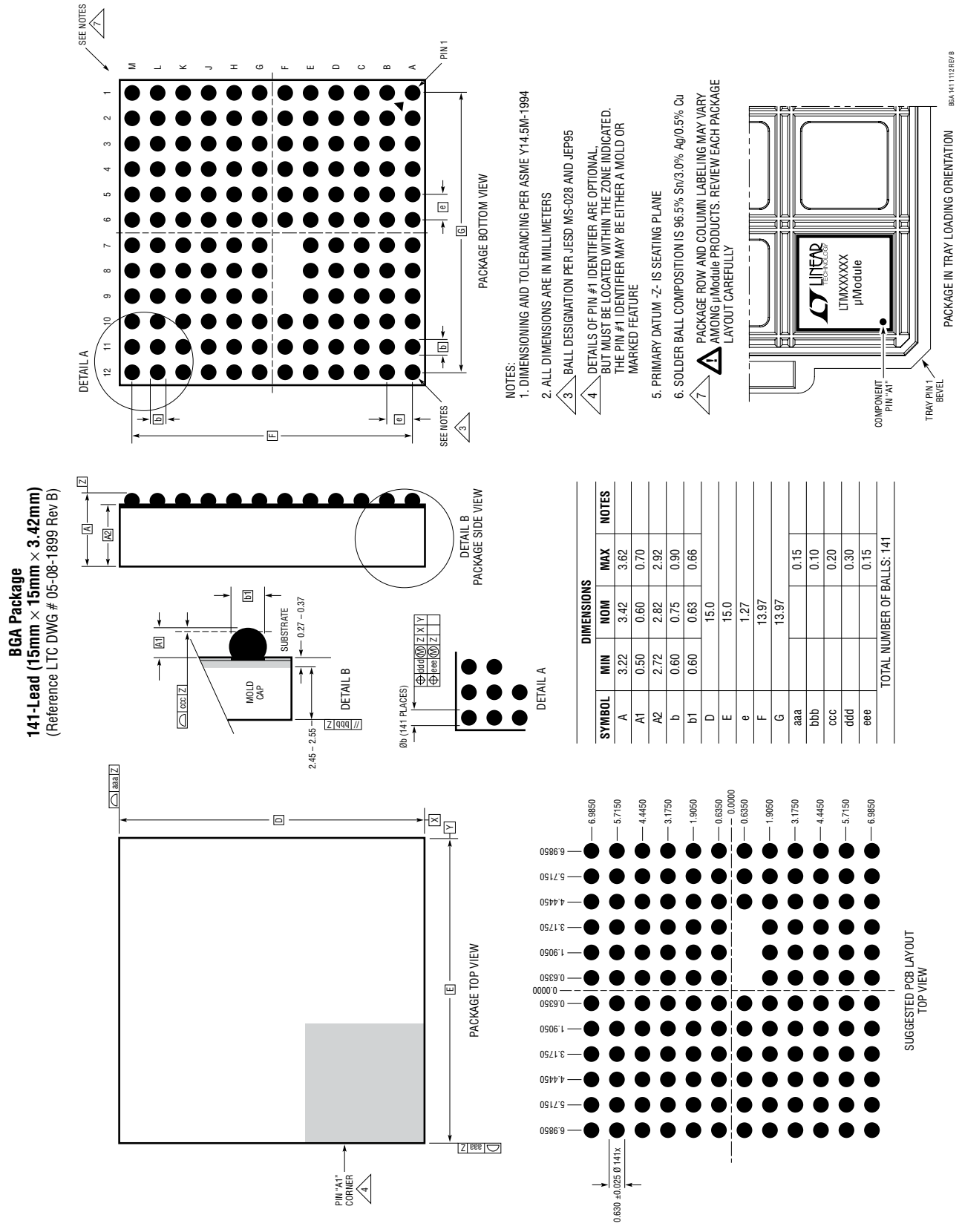
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 141				

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 141				

PACKAGE DESCRIPTION

Pin Assignment Table 6 (Arranged by Pin Number)

PIN NAME	FUNCTION	PIN NAME	FUNCTION	PIN NAME	FUNCTION	PIN NAME	FUNCTION	PIN NAME	FUNCTION	PIN NAME	FUNCTION
A1	PGND	C1	PGND	E1	V_{OUT}	G1	V_{OUT}	J1	SW1	L1	SW1
A2	PGND	C2	PGND	E2	V_{OUT}	G2	V_{OUT}	J2	SW1	L2	SW1
A3	PGND	C3	PGND	E3	PGND	G3	V_{OUT}	J3	SW1	L3	SW1
A4	$SENSE^+$	C4	PGND	E4	PGND	G4	V_{OUT}	J4	SW1	L4	SW1
A5	$SENSE^-$	C5	PGND	E5	PGND	G5	R_{SENSE}	J5	R_{SENSE}	L5	R_{SENSE}
A6	SS	C6	PGND	E6	PGND	G6	R_{SENSE}	J6	R_{SENSE}	L6	R_{SENSE}
A7	SGND	C7	PGND	E7	PGND	G7	R_{SENSE}	J7	R_{SENSE}	L7	SW2
A8	RUN	C8	PGND	E8	PGND	G8	R_{SENSE}	J8	SW2	L8	SW2
A9	FCB	C9	PGND	E9	PGND	G9	R_{SENSE}	J9	SW2	L9	SW2
A10	STBYMD	C10	PGND	E10	PGND	G10	R_{SENSE}	J10	V_{IN}	L10	V_{IN}
A11	PGND	C11	PGND	E11	PGND	G11	R_{SENSE}	J11	V_{IN}	L11	V_{IN}
A12	PGND	C12	PGND	E12	PGND	G12	R_{SENSE}	J12	V_{IN}	L12	V_{IN}
B1	PGND	D1	PGND	F1	V_{OUT}	H1	V_{OUT}	K1	SW1	M1	SW1
B2	PGND	D2	PGND	F2	V_{OUT}	H2	V_{OUT}	K2	SW1	M2	SW1
B3	PGND	D3	PGND	F3	V_{OUT}	H3	V_{OUT}	K3	SW1	M3	SW1
B4	PGND	D4	PGND	F4	V_{OUT}	H4	V_{OUT}	K4	SW1	M4	SW1
B5	PGOOD	D5	PGND	F5	$INTV_{CC}$	H5	R_{SENSE}	K5	R_{SENSE}	M5	R_{SENSE}
B6	V_{FB}	D6	PGND	F6	$EXTV_{CC}$	H6	R_{SENSE}	K6	R_{SENSE}	M6	R_{SENSE}
B7	COMP	D7	PGND	F7	–	H7	R_{SENSE}	K7	SW2	M7	SW2
B8	PLLFLTR	D8	PGND	F8	–	H8	R_{SENSE}	K8	SW2	M8	SW2
B9	PLLIN	D9	PGND	F9	–	H9	R_{SENSE}	K9	SW2	M9	SW2
B10	PGND	D10	PGND	F10	R_{SENSE}	H10	R_{SENSE}	K10	V_{IN}	M10	V_{IN}
B11	PGND	D11	PGND	F11	R_{SENSE}	H11	R_{SENSE}	K11	V_{IN}	M11	V_{IN}
B12	PGND	D12	PGND	F12	R_{SENSE}	H12	R_{SENSE}	K12	V_{IN}	M12	V_{IN}

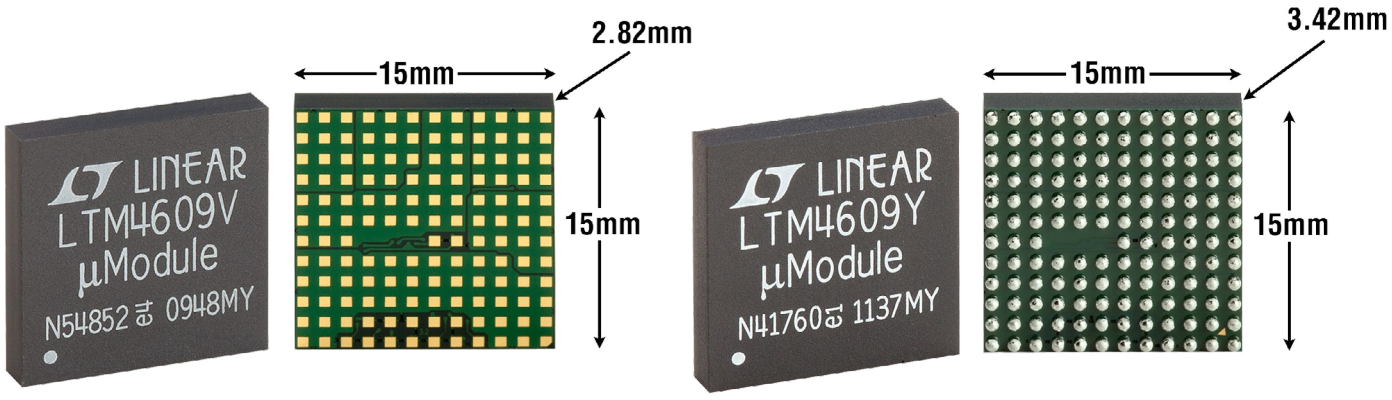
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/10	MP-grade part added. Reflected throughout the data sheet.	1-26
C	03/12	Added the BGA Package option and updated the Typical Application.	1
		Updated the Pin Configuration and Order Information sections.	2
		Updated Note 2.	4
		Added $INTV_{CC}$ maximum load current.	7
		Updated the recommended heat sinks table.	19
		Added BGA Package drawing.	25
		Updated the Related Parts table.	28
D	12/12	Add to Absolute Maximum Ratings and Thermal Resistance figures	2
		Augment $INTV_{CC}$ limits	4
		Update Note 2 and Note 3	4
		Update Related Parts table	28
E	1/14	Added SnPb terminal finish product option	1, 2
F	4/14	Removed CLOCK SYNC, Figures 16, 17, 18, 19	21, 22

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE PHOTOS



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3780	36V Buck-Boost Controller	Synchronous Operation; Single Inductor, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 30V
LTC3785	10V Buck-Boost Controller	Synchronous, No R_{SENSE}™, 2.7V ≤ V_{IN} ≤ 10V, 2.7V ≤ V_{OUT} ≤ 10V
LTM4601/LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase® Operation to 48A, LTM4601-1 Has No Remote Sensing
LTM4603	6A DC/DC µModule with PLL and Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version Has No Remote Sensing, Pin Compatible with the LTM4601
LTM4604A	4A, Low V_{IN}, DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.32mm
LTM4605/LTM4607	5A High Efficiency Buck-Boost DC/DC µModule Regulators	Pin Compatible with LTM4609, Lower Voltage Versions of the LTM4609
LTM4606/LTM4612	Ultralow Noise DC/DC µModule Regulators	Low EMI, LTM4606 Verified by Xilinx to Power Rocket IO™, CISPR22 Compliant
LTM4608A	8A, Low V_{IN}, DC/DC µModule Regulator	2.7V ≤ V_{IN} ≤ 5.5V, 0.6V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.82mm
LTM4627	20V, 15A DC/DC Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5V, PLL Input, V_{OUT} Tracking, Remote Sense Amplifier, 15mm × 15mm × 4.32mm LGA or 15mm × 15mm × 4.92mm BGA
LTC2978	Octal Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, 16-Bit ADC with ±0.25% TUE, 3.3V to 15V Operation
LTC2974	Quad Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements
LTC3880	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, ±0.5 Output Voltage Accuracy, MOSFET Gate Drivers

28 Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTM4609

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