THE DATASHEET OF

LT5401MPMSE#TRPBF

Matched Resistor Network for Precision Amplifiers

FEATURES

- **Optimized for Use with Fully Differential and Difference Amplifiers**
- **Excellent Matching**
  - **±0.003% Resistor Ratio Matching (Max)**
  - **96.5dB CMRR (Min)**
  - **±25ppm Gain Error (Max)**
  - **±0.5ppm/°C Matching Temperature Drift (Max)**
- ±35V Operating Voltage (±36V Abs Max)
- 8ppm/°C Absolute Resistor Value Temperature Drift
- Long-Term Stability: <8ppm at 6500Hours
- ESD Protected Inputs
- –55°C to 150°C Operating Temperature
- 10-Lead MSOP Package

APPLICATIONS

- Fully Differential Amplifiers
- Difference Amplifiers
- Reference Dividers
- Precision Summing/Subtracting

DESCRIPTION

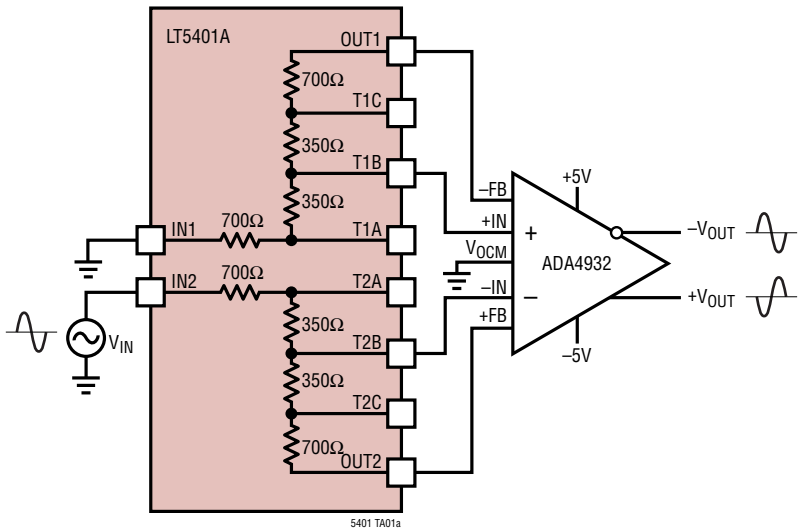
The LT®5401 is an ultra-precision matched resistor network optimized for use with fully differential or difference amplifiers, and with excellent matching specifications over the entire temperature range. The LT5401 contains two strings of matched resistors, each providing three tap points. The resulting matched ratios are well suited for precisely setting a differential amplifier's gain or attenuation.

When used to configure differential or difference gain, the LT5401's excellent ratio matching ensures high CMRR, low gain errors and low gain drift to levels far too difficult to achieve with discrete passive components. This high level of precision reduces calibration requirements in many applications and offers 10 times higher performance than a ±0.01% discrete solution.

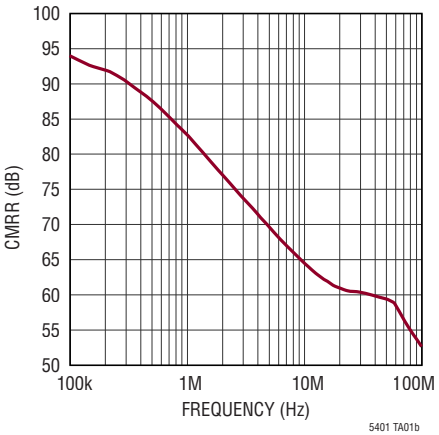
The LT5401 is available in a compact 10-lead MSOP package with exposed paddle for improved thermal performance over a temperature range of –55°C to 150°C.

TYPICAL APPLICATION

Using LT5401 with a Fully Differential Amplifier for Single-Ended to Differential Conversion, G = 1



Input Common Mode Rejection Ratio vs Frequency



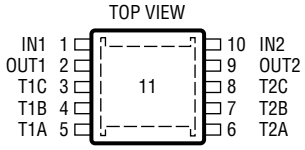
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Voltage IN1 to EPAD or IN2 to EPAD .....±36V
Total Voltage IN1 to OUT1 or IN2 to OUT2.....±36V
Total Voltage IN1 to T1A or OUT1 to T1C ..... ±12V
Total Voltage IN2 to T2A or OUT2 to T2C..... ±12V
Total Voltage T1B to T1A or T1C.....±6V
Total Voltage T2B to T2A or T2C.....±6V
Maximum Current T1A, T1B, T1C, T2A, T2B, T2C 9mA
Operating Temperature Range (Note 2)
LT5401I.....–40°C to 85°C
LT5401H .....–40°C to 125°C
LT5401MP .....–55°C to 150°C
Specified Temperature Range (Note 2)
LT5401I.....–40°C to 85°C
LT5401H .....–40°C to 125°C
LT5401MP .....–55°C to 150°C
Maximum Junction Temperature (Note 3)..... 150°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



MS10E PACKAGE
10-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, θ_{JC} = 20°C/W
EXPOSED PAD (PIN 11) IS ELECTRICALLY CONNECTED TO THE INPUT ESD AND MUST BE SOLDERED TO THE PCB, TYPICALLY CONNECTED TO GROUND PLANE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT5401AIMSE#PBF	LT5401AIMSE#TRPBF	LTHHJ	10-Lead Plastic MSOP	–40°C to 85°C
LT5401IMSE#PBF	LT5401IMSE#TRPBF	LTHHJ	10-Lead Plastic MSOP	–40°C to 85°C
LT5401AHMSE#PBF	LT5401AHMSE#TRPBF	LTHHJ	10-Lead Plastic MSOP	–40°C to 125°C
LT5401HMSE#PBF	LT5401HMSE#TRPBF	LTHHJ	10-Lead Plastic MSOP	–40°C to 125°C
LT5401MPMSE#PBF	LT5401MPMSE#TRPBF	LTHHJ	10-Lead Plastic MSOP	–55°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

Nominal Ratio of 1 only. The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LT5401A MIN	LT5401A TYP	LT5401A MAX	LT5401 MIN	LT5401 TYP	LT5401 MAX	UNITS
$(\Delta R/R)_{RE}$	Resistor Ratio Match	Note 4				±30			±60	ppm
		T_A = –40°C to 85°C	●			±60			±90	ppm
		T_A = –40°C to 125°C	●			±60			±95	ppm
		T_A = –55°C to 150°C	●						±120	ppm
$(\Delta R/R)_{RT}$	Resistor Ratio Match Tracking	Note 5				±30			±60	ppm
		T_A = –40°C to 85°C	●			±50			±80	ppm
		T_A = –40°C to 125°C	●			±60			±95	ppm
		T_A = –55°C to 150°C	●						±100	ppm
CMRR	Common Mode Rejection Ratio $CMRR = \frac{\left(\frac{\Delta R}{R}\right)_{RT}}{1+G}$ G is Nominal Ratio	Note 5		96.5			90.5			dB
		T_A = –40°C to 85°C	●	92			88			dB
		T_A = –40°C to 125°C	●	90.5			86.5			dB
		T_A = –55°C to 150°C	●				86			dB
$(\Delta R/R)_{AVE}$	Average Resistor Ratio Match	Note 6				±25			± 55	ppm
		T_A = –40°C to 85°C	●			±50			±80	ppm
		T_A = –40°C to 125°C	●			±50			±85	ppm
		T_A = –55°C to 150°C	●						±90	ppm
GE	Gain Error $GE = \left(\frac{\Delta R}{R}\right)_{AVE}$	Note 6				±25			±55	ppm
		T_A = –40°C to 85°C	●			±50			±80	ppm
		T_A = –40°C to 125°C	●			±50			±85	ppm
		T_A = –55°C to 150°C	●						±90	ppm
$(\Delta R/R)_{RE}/\Delta T$	Resistor Ratio Match Temperature Drift	Note 7	●		±0.2	±0.5		±0.2	±0.5	ppm/°C

ELECTRICAL CHARACTERISTICS

Nominal Ratio of 0.5 only. The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LT5401A MIN	LT5401A TYP	LT5401A MAX	LT5401 MIN	LT5401 TYP	LT5401 MAX	UNITS
$(\Delta R/R)_{RE}$	Resistor Ratio Match	Note 4				±30			±60	ppm
		T_A = –40°C to 85°C	●			±85			±115	ppm
		T_A = –40°C to 125°C	●			±85			±120	ppm
		T_A = –55°C to 150°C	●						±160	ppm
$(\Delta R/R)_{RT}$	Resistor Ratio Match Tracking	Note 5				±30			±60	ppm
		T_A = –40°C to 85°C	●			±55			±85	ppm
		T_A = –40°C to 125°C	●			±65			±100	ppm
		T_A = –55°C to 150°C	●						±110	ppm
CMRR	Common Mode Rejection Ratio $CMRR = \frac{\left(\frac{\Delta R}{R}\right)_{RT}}{1+G}$ G is Nominal Ratio	Note 5		94			88			dB
		T_A = –40°C to 85°C	●	88.7			84.9			dB
		T_A = –40°C to 125°C	●	87.3			83.5			dB
		T_A = –55°C to 150°C	●				82.7			dB
$(\Delta R/R)_{AVE}$	Average Resistor Ratio Match	Note 6				±25			± 55	ppm
		T_A = –40°C to 85°C	●			±65			±95	ppm
		T_A = –40°C to 125°C	●			±75			±110	ppm
		T_A = –55°C to 150°C	●						±130	ppm
GE	Gain Error $GE = \left(\frac{\Delta R}{R}\right)_{AVE}$	Note 6				±25			± 55	ppm
		T_A = –40°C to 85°C	●			±65			±95	ppm
		T_A = –40°C to 125°C	●			±75			±110	ppm
		T_A = –55°C to 150°C	●						±130	ppm
$(\Delta R/R)_{RE}/\Delta T$	Resistor Ratio Match Temperature Drift	Note 7	●		±0.2	±0.7		±0.2	±0.7	ppm/°C

ELECTRICAL CHARACTERISTICS

Nominal Ratio of 2 only. The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LT5401A MIN	LT5401A TYP	LT5401A MAX	LT5401 MIN	LT5401 TYP	LT5401 MAX	UNITS
$(\Delta R/R)_{RE}$	Resistor Ratio Match	Note 4				±30			±60	ppm
		T_A = –40°C to 85°C	●			±80			±110	ppm
		T_A = –40°C to 125°C	●			±85			±120	ppm
		T_A = –55°C to 150°C	●						±155	ppm
$(\Delta R/R)_{RT}$	Resistor Ratio Match Tracking	Note 5				±30			±60	ppm
		T_A = –40°C to 85°C	●			±60			±90	ppm
		T_A = –40°C to 125°C	●			±70			±110	ppm
		T_A = –55°C to 150°C	●						±110	ppm
CMRR	Common Mode Rejection Ratio $CMRR = \frac{\left(\frac{\Delta R}{R}\right)_{RT}}{1+G}$ G is Nominal Ratio	Note 5		100			94			dB
		T_A = –40°C to 85°C	●	94			90.5			dB
		T_A = –40°C to 125°C	●	92.6			88.7			dB
		T_A = –55°C to 150°C	●				88.7			dB
$(\Delta R/R)_{AVE}$	Average Resistor Ratio Match	Note 6				±30			±60	ppm
		T_A = –40°C to 85°C	●			±75			±105	ppm
		T_A = –40°C to 125°C	●			±75			±110	ppm
		T_A = –55°C to 150°C	●						±120	ppm
GE	Gain Error $GE = \left(\frac{\Delta R}{R}\right)_{AVE}$	Note 6				±30			± 60	ppm
		T_A = –40°C to 85°C	●			±75			±105	ppm
		T_A = –40°C to 125°C	●			±75			±110	ppm
		T_A = –55°C to 150°C	●						±120	ppm
$(\Delta R/R)_{RE}/\Delta T$	Resistor Ratio Match Temperature Drift	Note 7	●		±0.4	±0.8		±0.4	±0.8	ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LT5401A MIN	LT5401A TYP	LT5401A MAX	LT5401 MIN	LT5401 TYP	LT5401 MAX	UNITS
$(\Delta R/R)_{SS}$	Side-to-Side Resistor Match	Note 8				±0.3			±0.4	%
			●			±0.4			±0.5	%
ΔR	Absolute Resistor Tolerance		●			±7.5			±15	%
ΔR/ΔT	Absolute Resistor Value Temperature Drift	Note 7	●	–10	8	25	–10	8	25	ppm/°C
	Maximum Operating Voltage		●	–35		35	–35		35	V
	Distributed Capacitance	Resistor to Exposed Pad			3.4			3.4		pF
		Resistor to Resistor (Same Side)			1			1		pF
	Resistor Voltage Coefficient		●		< 0.1			< 0.1		ppm/V
	Excess Current Noise	Mil-Std-202 Method 308			< –55			< –55		dB
	Resistor Ratio Matching Long-Term Drift	35°C 6500Hours, 25mW			< 8			< 8		ppm
	Resistor Ratio Matching Thermal Shock/Hysteresis	–50°C to 150°C, 5 Cycles			< 3			< 3		ppm
	Resistor Ratio Matching IR Reflow	25°C to 260°C, 3 Cycles			< 3			< 3		ppm
	Resistor Ratio Matching Accelerated Shelf Life	150°C, 1000Hours			10			10		ppm
	Harmonic Distortion	$20V_{P-P}$, 1kHz, Difference Amplifier			–120			–120		dBc

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT5401I is guaranteed to meet specified performance from –40°C to 85°C. The LT5401H is guaranteed to meet specified performance from –40°C to 125°C and is 100% tested at these temperature extremes. The LT5401MP is guaranteed to meet specified performance from –55°C to 150°C and is 100% tested at these temperature extremes.

Note 3: In order to keep the junction temperature within the Absolute Maximum Rating, maximum power dissipation should be derated at elevated ambient temperatures.

Note 4: $(\Delta R/R)_{RE}$ specifies the following ratio matches:

RESISTOR RATIO	NOMINAL RATIO
(R1C + R1D)/(R1A + R1B)	1
(R2C + R2D)/(R2A + R2B)	1
(R1B + R1C + R1D)/(R1A)	2
(R2B + R2C + R2D)/(R2A)	2
(R1D)/(R1A + R1B + R1C)	0.5
(R2D)/(R2A + R2B + R2C)	0.5

Note 5: $(\Delta R/R)_{RT}$ specifies how well the $(\Delta R/R)_{RE}$ ratios match each other when the 2 sets of LT5401 resistors are configured for nominally equal ratios. This specification determines CMRR performance when the LT5401 is used to configure difference and fully differential amplifiers.

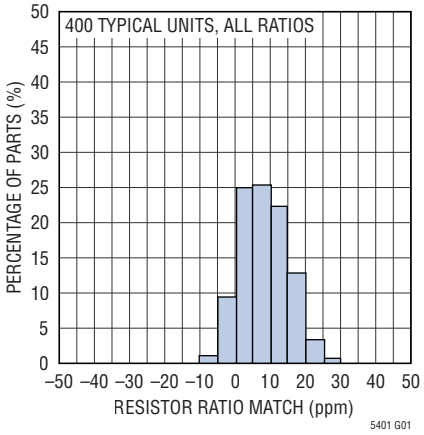
Note 6: $(\Delta R/R)_{AVE}$ specifies average $(\Delta R/R)_{RE}$ ratio matching when the 2 sets of LT5401 resistors are configured for nominally equal ratios. This specification determines gain accuracy performance when the LT5401 is used to configure difference and fully differential amplifiers.

Note 7: This parameter is not 100% tested.

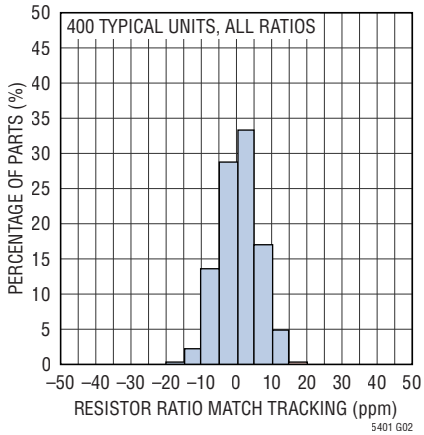
Note 8: $(\Delta R/R)_{SS}$ specifies matching between the sum of R1 and R2 where R1 = R1A + R1B + R1C + R1D and R2 = R2A + R2B + R2C + R2D.

TYPICAL PERFORMANCE CHARACTERISTICS

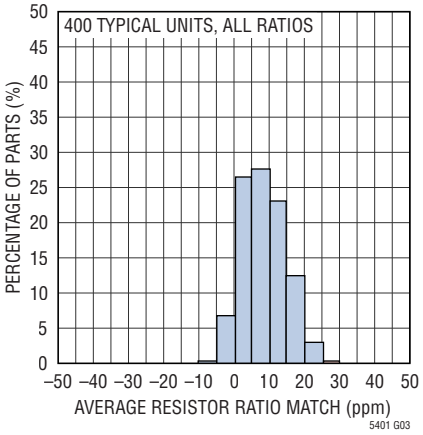
Resistor Ratio Match



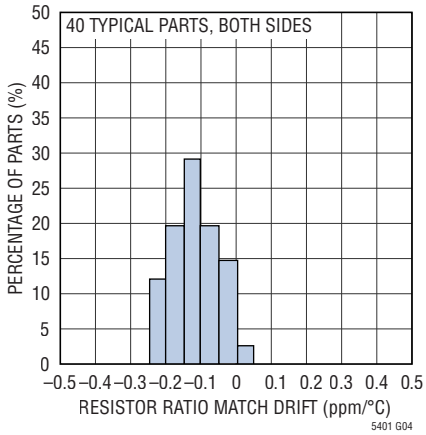
Resistor Ratio Match Tracking



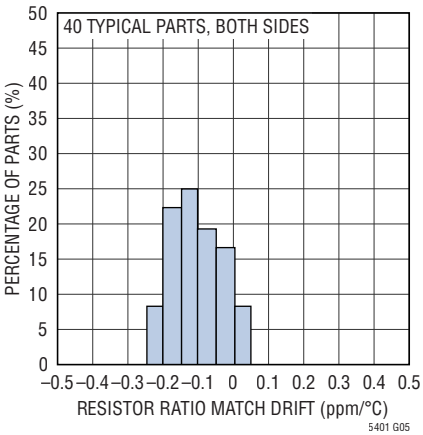
Average Resistor Ratio Match



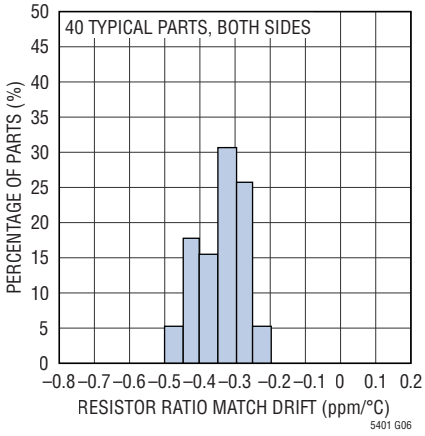
Resistor Ratio Matching Temperature Drift, G = 0.5V/V



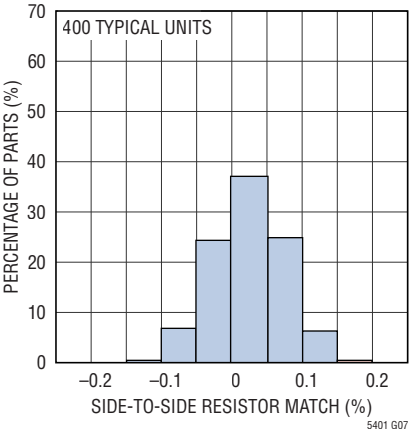
Resistor Ratio Matching Temperature Drift, G = 1V/V



Resistor Ratio Matching Temperature Drift, G = 2V/V



Side-to-Side Resistor Match



PIN FUNCTIONS

IN1 (Pin 1): Connection to R1A. ESD protection on this pin is provided through a 36V bidirectional ESD clamp to the exposed pad.

OUT1 (Pin 2): Connection to R1D.

T1C (Pin 3): Connection to R1C and R1D resistors. This tap point has series parasitic resistance and should not conduct current.

T1B (Pin 4): Connection to R1B and R1C resistors. This tap point has series parasitic resistance and should not conduct current.

T1A (Pin 5): Connection to R1A and R1B resistors. This tap point has series parasitic resistance and should not conduct current.

T2A (Pin 6): Connection to R2A and R2B resistors. This tap point has series parasitic resistance and should not conduct current.

T2B (Pin 7): Connection to R2B and R2C resistors. This tap point has series parasitic resistance and should not conduct current.

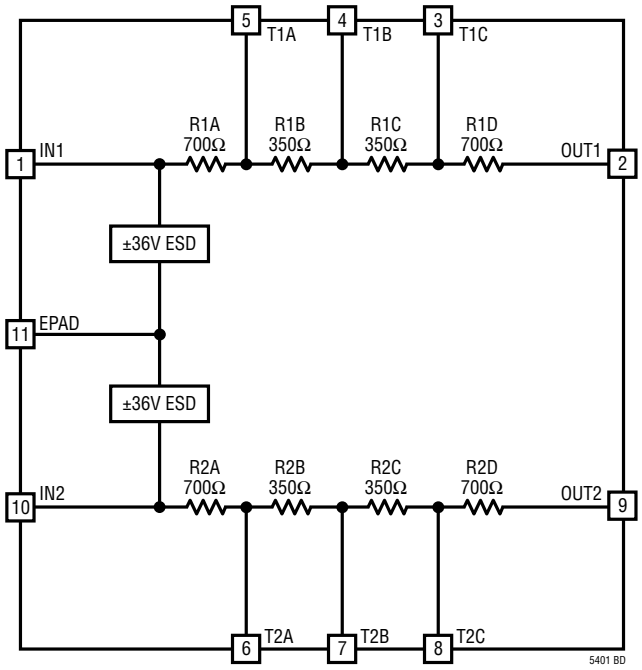
T2C (Pin 8): Connection to R2C and R2D resistors. This tap point has series parasitic resistance and should not conduct current.

OUT2 (Pin 9): Connection to R2D.

IN2 (Pin 10): Connection to R2A. ESD protection on this pin is provided through a 36V bidirectional ESD clamp to the exposed pad.

EPAD (Exposed Pad Pin 11): Connection to 36V bidirectional ESD clamps. This pad is typically connected to a ground plane and provides a return path for current during ESD events.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Matching and Tolerance Specifications

$(\Delta R/R)_{RE}$ specifies the resistor ratio combinations shown in Table 1.

Table 1. Resistor Ratio Combinations

RESISTOR RATIO	NOMINAL RATIO
(R1C + R1D)/(R1A + R1B)	1
(R2C + R2D)/(R2A + R2B)	1
(R1B + R1C + R1D)/(R1A)	2
(R2B + R2C + R2D)/(R2A)	2
(R1D)/(R1A + R1B + R1C)	0.5
(R2D)/(R2A + R2B + R2C)	0.5

$(\Delta R/R)_{RE}/\Delta T$ specifies the rate at which the resistor ratio match shown in Table 1 varies over temperature. The LT5401 specifies a maximum resistor ratio match drift of 0.5ppm/°C, which is 20 times better than discrete 10ppm/°C resistors.

$(\Delta R/R)_{RT}$ specifies the match of the ratio formed with R1A, R1B, R1C and R1D to the same ratio formed with R2A, R2B, R2C and R2D. The LT5401 specifies 0.003% ratio matching, which guarantees 96.5dB of CMRR when the LT5401 is used to configure difference and fully differential amplifiers. This level of performance is 133 times better than typical 0.1% resistors might achieve.

$(\Delta R/R)_{AVE}$ specifies the average match of the ratio formed with R1A, R1B, R1C and R1D and the ratio formed with R2A, R2B, R2C and R2D. When using the LT5401 to configure difference and fully differential amplifiers, this specification guarantees 25ppm gain accuracy. This level of performance is 80 times better than typical 0.1% resistors might achieve.

$(\Delta R/R)_{SS}$ specifies the match of (R1A + R1B + R1C + R1D) to (R2A + R2B + R2C + R2D).

ΔR specifies the LT5401's absolute resistor tolerance. $\Delta R/\Delta T$ specifies the rate at which the LT5401's absolute resistance varies over temperature.

General Considerations of LT5401 with a Fully Differential Amplifier (FDA)

The LT5401 can be used with a variety of fully differential amplifiers from low power to high speed. The outstanding resistor ratio matching of LT5401 provides for very high common mode rejection and highly accurate gain over the specified operating temperature range.

Noise

For low noise design of an LT5401 and FDA, the noise contribution of the LT5401 resistor values with the amplifier's voltage and current noise must be considered. Figure 1 shows a simplified noise model for a fully differential amplifier. Table 2 lists the LT5401 resistor values for its three nominal gains, 0dB, 6dB and –6dB. Table 3 is a partial list of recommended differential amplifiers for use with an LT5401. Equation 1 shows the output noise as function of FDA noise and resistor noise. Using Table 2 resistor values and the Table 3 noise sources, the output noise can be calculated for an LT5401 and FDA pair. In addition, the terms of Equation 1 provide an intuitive guide to low noise design. For a high gain circuit, the amplifier's voltage noise and input resistors noise can be the dominant noise, for low gains the amplifier's current noise can increase the output noise even if the amplifier's voltage noise is low. For example, for 0dB gain the LT5401 R_F and R_I are 1050Ω. The ADA4938 and ADA4932 voltage and current noise are ($2.8nV/\sqrt{Hz}$, $5pA/\sqrt{Hz}$) and ($3.6nV/\sqrt{Hz}$, $1pA/\sqrt{Hz}$) respectively. The calculated output noise of an LT5401 with an ADA4938 or with an ADA4932 is $12.5nV/\sqrt{Hz}$ and $11.1nV/\sqrt{Hz}$ respectively. So, despite the lower voltage noise that ADA4938 has, it still results in higher output noise due to its higher current noise compared to ADA4932.

APPLICATIONS INFORMATION

Table 2. Typical LT5401 Resistor Values

GAIN (dB)	R_F (Ω)	R_I (Ω)
0	1050	1050
6	1400	700
–6	700	1400

Table 3. FDA Noise, $2V_{P-P}$ BW and I_{SUPPLY}

FDA	e_{ni} (nV/√Hz)	I_n (pA/√Hz)	BW (MHz)	I_S (mA)
LTC6404-1	1.5	3	72	27
ADA4945-1	1.8	1	60	4
LTC6403-1	2.8	1.8	32	11
ADA4938-1	2.8	5	800	34
LTC6363	2.9	0.55	35	1.75
ADA4932-1	3.6	1	360	8.8
LTC6362	3.9	0.8	7	1
ADA4940-1	3.9	0.8	25	1.25

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet (I_n \bullet R_F)^2 + 2 \bullet \left(e_{nRI} \bullet \left(\frac{R_F}{R_I}\right)\right)^2 + 2 \bullet e_{nRF}{}^2} \quad (1)$$

Bandwidth

Figure 2 shows an FDA circuit model with the LT5401 resistors and parasitic capacitors C_P and an external feedback capacitor C_F. The gain setting resistors and C_P form distributed input and feedback poles. The input poles provide a useful attenuation at very high frequencies and the feedback poles add gain peaking (without any feedback capacitor). In addition, C_P at the FDA inputs and the gain setting resistors form a parasitic pole that increases gain peaking and can cause instability. A feedback capacitor C_F is required to mitigate the excessive gain peaking of multiple parasitic poles. A $C_F \geq 3.3$pF is recommended for 6dB gain (use higher C_F values for 0dB and –6dB gains).

The C_P capacitor at the FDA outputs is a C_{LOAD} and can lower the amplifier's phase margin (consider the gain peaking sensitivity of the Frequency Response vs C_{LOAD} plot in the FDA data sheet).

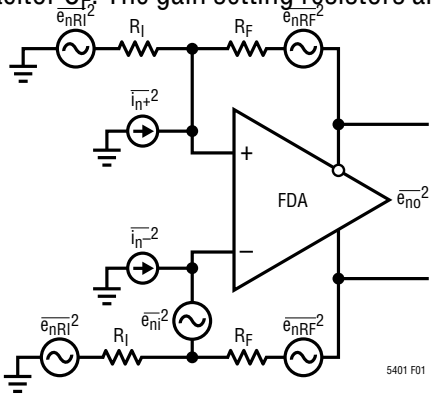


Figure 1. A Simplified FDA Noise Model

PCB Layout

A PCB layout for an FDA must be differentially symmetrical and matched from input to output using short traces and striping copper from under the trace to minimize

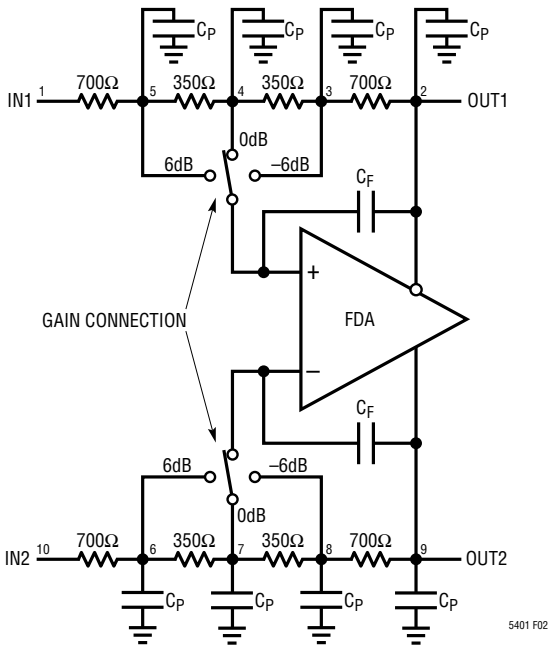


Figure 2. Simplified LT5401 and FDA Model. C_P is a 3.4pF Parasitic Capacitance and C_F is an External Feedback Capacitor

APPLICATIONS INFORMATION

stray capacitance. The layout of an LT5401 and FDA must preserve the outstanding resistor network matching to minimize the error due to any trace resistance matching. The copper trace resistance is 0.25mΩ ±15% and 0.5mΩ ±15% per square trace area for 2oz and 1oz copper, respectively. For example, for 0dB gain, ±30ppm matching of 1050Ω resistors is ±31.5mΩ. If the trace length is 0.2-inch, the resistance of a 20mil wide trace for 2oz copper is 2.5mΩ. Even an arbitrary ±30% matching the error is ±0.75mΩ, adding less than ±1ppm error. In addition, the trace resistance ratio temperature drift will not degrade the LT5401 ratio temperature drift (1ppm/°C max). For example, the temperature coefficient of a copper resistance 0.4%/°C. A 100°C temperature rise from 25°C to 125°C increases the 2.5mΩ trace to 3.5mΩ. An arbitrary ±30% matching error is ±0.3mΩ, adding less than ±0.3ppm temperature error.

Configuring the LT5401

The LT5401 consists of two sets of matched 4-segment resistors. Each resistor string has three tap points which are intended to connect to a high impedance such as an amplifier's input. Each tap point has parasitic metal resistance R_P as shown in Figure 3. To preserve the matching performance of the LT5401, no current should be conducted in any of the tap points. Figure 3 illustrates the correct (Figure 3a) and incorrect (Figure 3b) ways to configure the LT5401 as a fully differential amplifier.

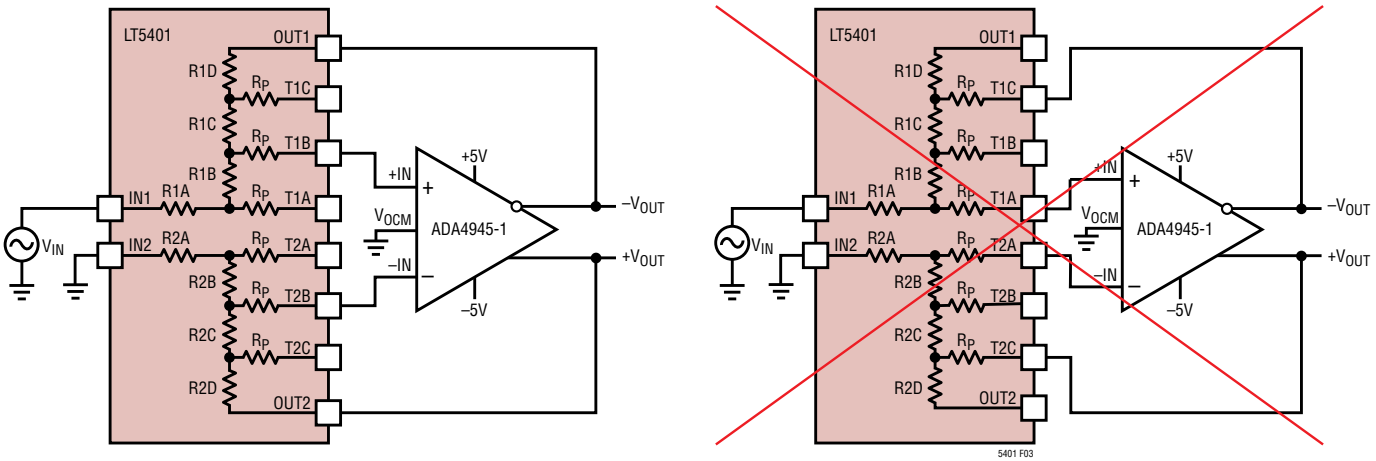
Figure 3a correctly connects tap points T1B and T2B to the amplifier's high impedance inputs and uses the IN and OUT pins.

Figure 3b incorrectly uses tap points T1C and T2C to connect to the amplifier's outputs. This incorrect configuration will incur significant gain, CMRR and drift errors because of the parasitic resistance in series with T1C and T2C.

Figure 4 shows the LT5401 being used to setup two buffered voltage dividers.

The top example in Figure 4 is correctly configured because no current is conducted in any of the tap points. T1B is connected to a high impedance amplifier input and current only flows in IN1 and OUT1.

The bottom example in Figure 4 is incorrectly configured because tap point T2C has been grounded and will conduct current. When incorrectly configured like this, the parasitic resistance in series with tap point T2C will cause a significant error and drift in the divider ratio. Also, had T2A not been buffered with the amplifier shown, any loading on T2A would cause current flow in T2A and result in significant error and drift in the divider ratio.



(a) CORRECT Way to Configure

(b) INCORRECT Way to Configure

Figure 3. Fully Differential Amplifier

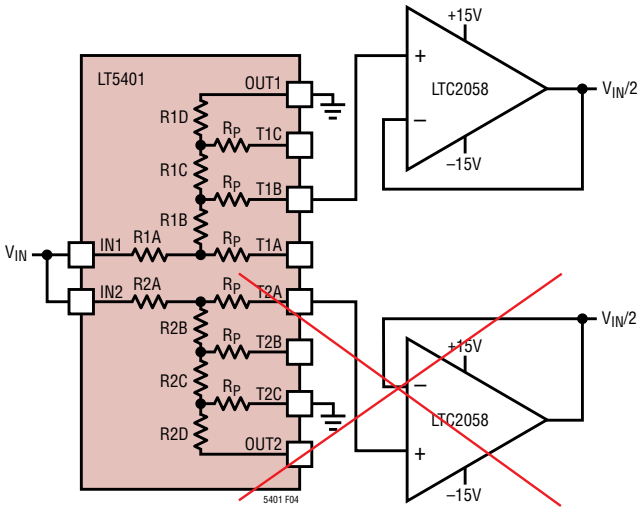


Figure 4. Voltage Divider

Where to Connect the Exposed Pad

The exposed pad is electrically connected to the IN1 and IN2 pins through 36V bidirectional ESD clamps. Its main purpose is to reduce the internal temperature rise in applications dissipating large amounts of power and to provide a return path to ground for ESD currents. The exposed pad should be tied to a ground plane though a low resistive path to provide the best level of thermal relief and ESD protection. The exposed pad can be tied to a low impedance voltage other than ground as long as the absolute maximum ratings are satisfied.

Thermal Considerations

Each resistor is rated for relatively high power dissipation, as listed in the Absolute Maximum Ratings section of this data sheet. To calculate the internal temperature rise inside the package, add together the power dissipated in all of the resistors, and multiply by the thermal resistance coefficient of the package (θ_{JA} or θ_{JC} as applicable).

For example Equation 2, if 32V is placed across IN1 and OUT1, the total power dissipation will be:

$$\frac{V_{TOTAL}^{2}}{R_{TOTAL}} = \frac{(32)^2}{(R1A+R1B+R1C+R1D)} \approx 0.5W \qquad (2)$$

and the total temperature rise inside the package equals 20°C. All 8 resistors will be at the same temperature, regardless of which resistor dissipates more power. The junction temperature must be kept within the Absolute Maximum Rating. At elevated ambient temperatures, this requirement places a limit on the maximum power dissipation. Figure 5 shows maximum power dissapation versus ambient temperature for various θ_{JA} values.

In addition to limiting the maximum power dissipation, the maximum voltage across any two pins must also be kept less than the absolute maximum rating.

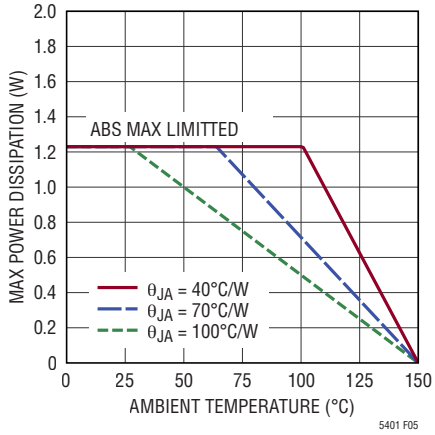


Figure 5. Safe Operating Area for Various θ_{JA}

ESD

The LT5401 can withstand up to ±500V of electrostatic discharge (ESD, human body). ESD beyond this voltage can damage or degrade the device performance.

To protect the LT5401 against large ESD strikes, external protection can be added using diodes to the circuit supply rails or bidirectional Zeners to ground (Figure 6).

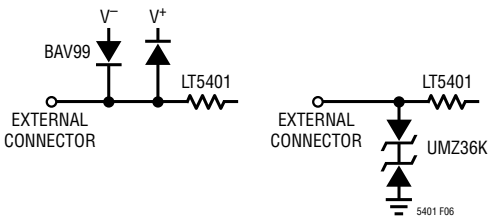
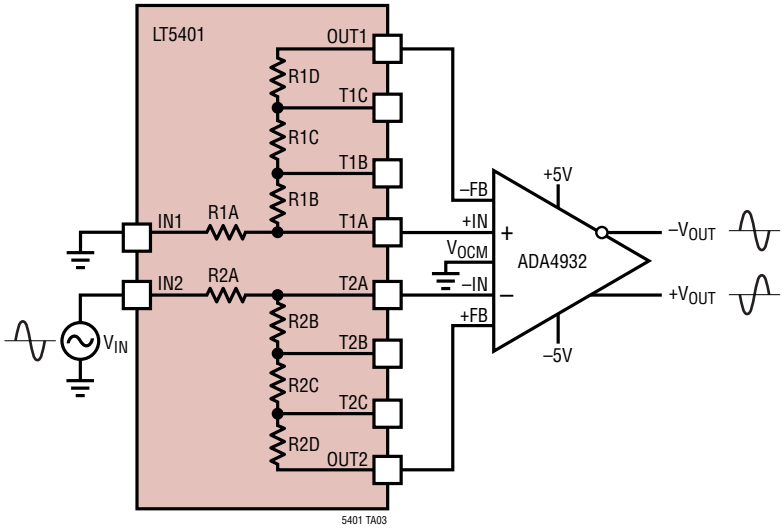


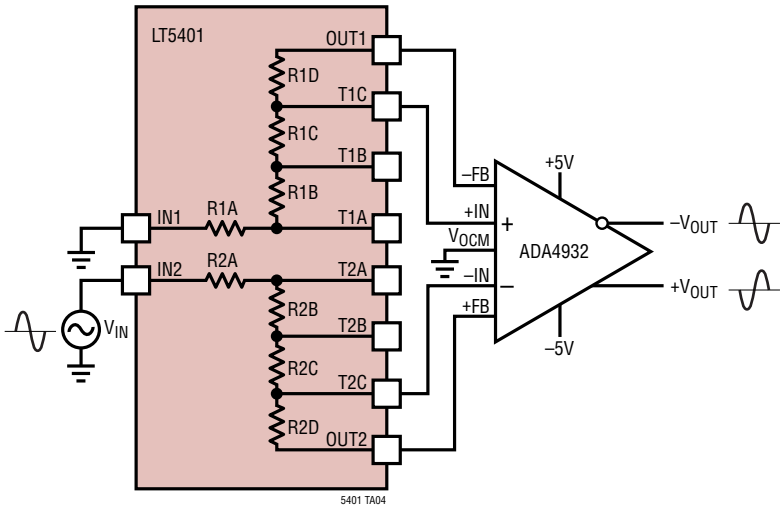
Figure 6.

TYPICAL APPLICATIONS

Single-Ended to Differential Conversion, G = 2V

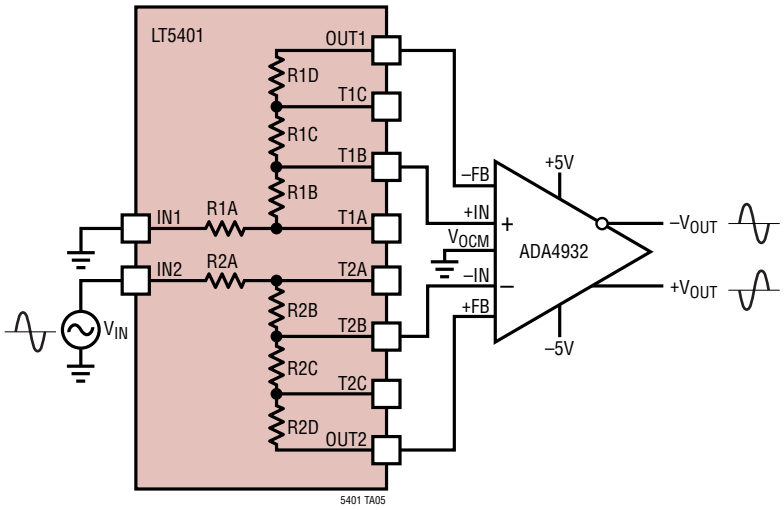


Single-Ended to Differential Conversion, G = 0.5V

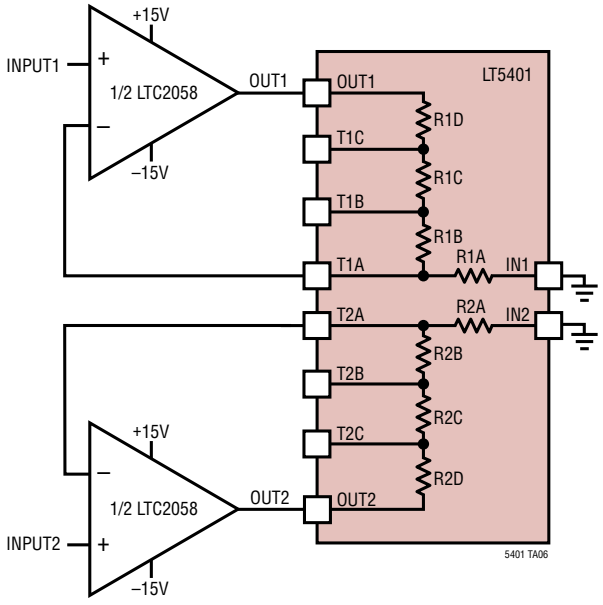


TYPICAL APPLICATIONS

Single-Ended to Differential Conversion, G = 1V

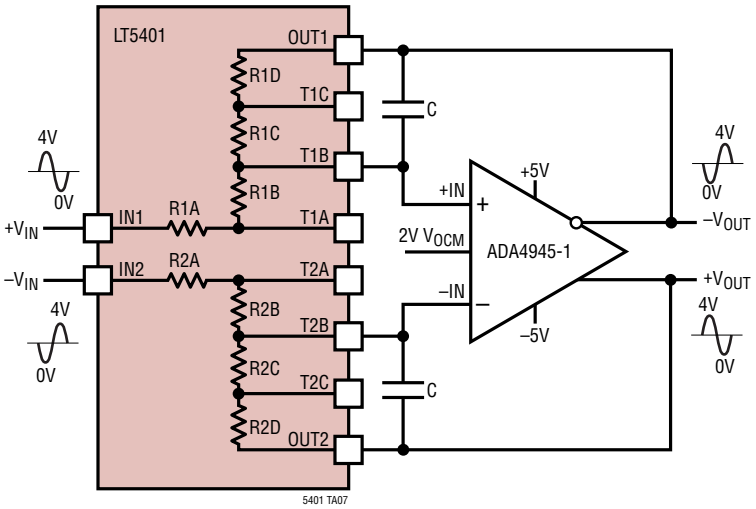


Dual Precision Amplifier Configuration, G = 3V



TYPICAL APPLICATIONS

Precision Fully Differential Single Pole Low Pass Filter

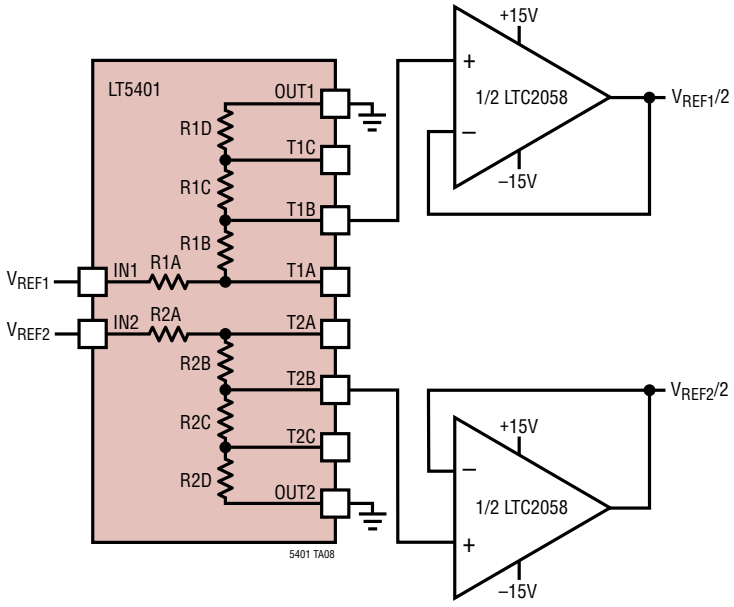


$$H(s) = H_0 \bullet \frac{w_P}{s + w_P}$$

$$\text{WHERE } H_0 = \frac{R_{FB}}{R_{IN}}, w_P = \frac{1}{R_{FB} \bullet C}$$

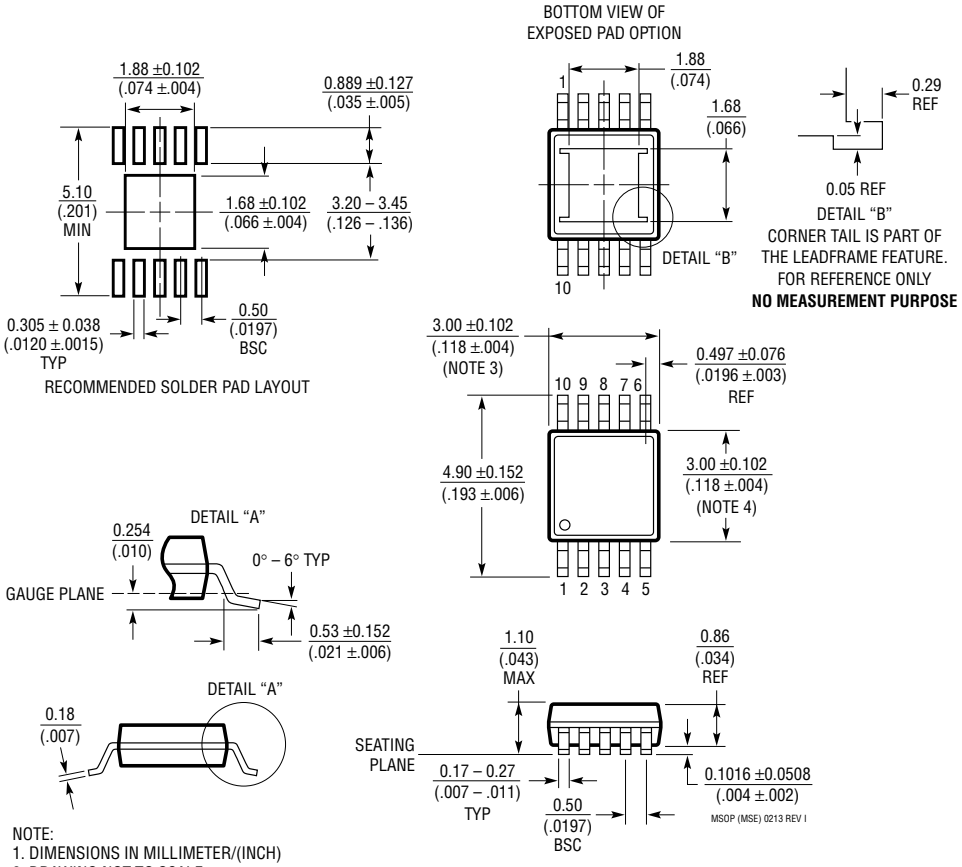
$$R_{FB} = R1C + R1D = R2C + R2D \qquad R_{IN} = R1A + R1B = R2A + R2B$$

Dual-Buffered Precision Voltage Divider



PACKAGE DESCRIPTION

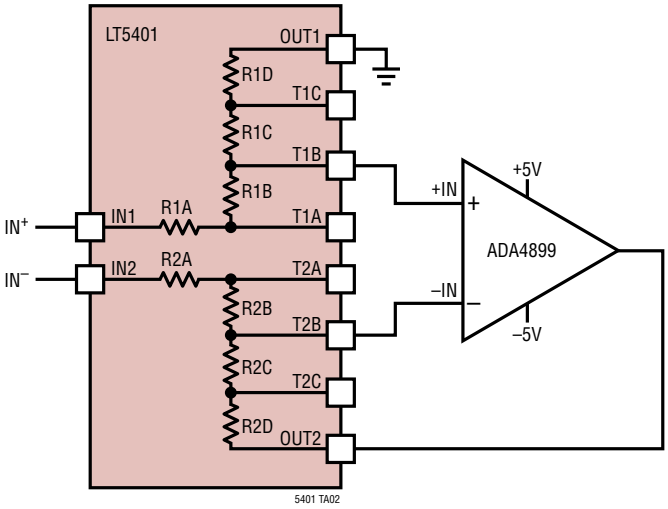
MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Precision Difference Amplifier, G = 1V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fully Differential Amplifiers		
AD8139	Low Noise, Rail-to-Rail, Differential ADC Driver	24.5mA, –95dBc Distortion at 2MHz, $2V_{P-P}$ Output
AD8138	Low Distortion, Differential ADC Driver	20mA, –94dBc Distortion at 5MHz, $2V_{P-P}$ Output
LT1994	70MHz Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	13mA, –94dBc Distortion at 1MHz, $2V_{P-P}$ Output
AD8132	Low Cost, High Speed Differential Amplifier	10.7mA, –96dBc Distortion at 1MHz, $2V_{P-P}$ Output
ADA4932-1/ADA4932-2	Low Power, Differential ADC Driver	9.6mA, –110dBc Distortion at 1MHz, $2V_{P-P}$ Output
AD8137	Low Cost, Low Power, Differential ADC Driver	2.6mA, –84dBc Distortion at 1MHz, $2V_{P-P}$ Output
LTC6363	Precision, Low Power Differential Amplifier/ADC Driver	1.75mA, –123dBc Distortion at 1kHz, $18V_{P-P}$ Output
LTC6363-1/LTC6363-2/ LTC6363-0.5	Precision, Fixed Gain, Low Power Differential Amplifier/ADC Driver Family	1.75mA, –123dBc Distortion at 1kHz, $18V_{P-P}$ Output
ADA4945	High Speed, Low Drift Fully Differential ADC Driver	1.4mA/4mA, –116dBc Distortion at 100kHz, $8V_{P-P}$ Output
ADA4940-1/ADA4940-2	Ultralow Power, Low Distortion, Fully Differential ADC Drivers	1.25mA, –96dBc Distortion at 1MHz, $2V_{P-P}$ Output
LTC6362	Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver	1mA, –116dBc Distortion at 1kHz, $8V_{P-P}$ Output
Operational Amplifiers		
LTC6228/LTC6229	Single/Dual 700MHz Low Noise Op Amp	16mA/Amplifier, $0.88nV/\sqrt{Hz}$
ADA4899-1	Single 600MHz Ultralow Distortion and Noise Op Amp	14.7mA, $1nV/\sqrt{Hz}$
ADA4896-2/ADA4897-1/ ADA4897-2	Single/Dual 230MHz Low Power and Noise Op Amp	3mA/Amplifier, $1nV/\sqrt{Hz}$
LTC6252/LTC6253/ LTC6254	Single/Dual/Quad 720MHz RRIO Power Efficient Op Amps	3.5mA/Amplifier, $2.75nV/\sqrt{Hz}$
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 180MHz Rail-to-Rail Low Power Op Amps	1mA/Amplifier, $4.2nV/\sqrt{Hz}$
Matched Resistor Networks		
LT5400	Precision Quad Matched Resistor Network	Ratios = 1:1, 1:4, 1:5, 1:9, 1:10

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- Analog Devices Inc. Information

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- Shortage Management
- Alternative Solution
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