



**THE DATASHEET OF
ZXGD3107N8TC**



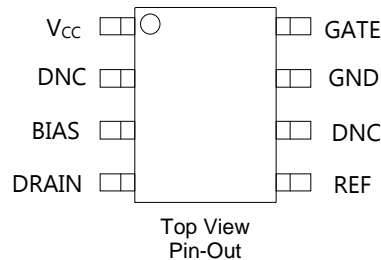
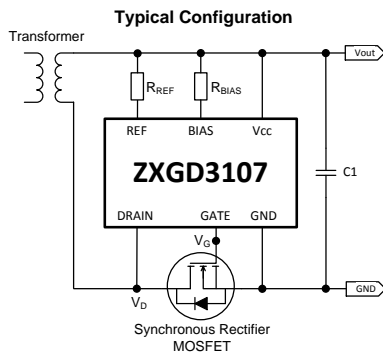
Description

ZXGD3107N8 synchronous controller is designed for driving a MOSFET as an ideal rectifier. This is to replace a diode for increasing the power transfer efficiency.

Proportional Gate drive control monitors the reverse voltage of the MOSFET such that if body diode conduction occurs, a positive voltage is applied to the MOSFET's GATE pin. Once the positive voltage is applied to the Gate, the MOSFET switches on allowing reverse current flow. The controllers' output voltage is then proportional to the MOSFET drain-source voltage and this is applied to the Gate via the driver. This action minimizes body diode conduction while enabling a rapid MOSFET turn-off as drain current decays to zero.

Applications

- Flyback Converters in:
 - AC-DC Adaptors
 - Set-Top Boxes
 - PoE Power Devices
- Resonant Converters in:
 - Telecoms PSU
 - Laptop Adaptors
 - Computing Power Supplies – ATX and Server PSU



Pin Name	Pin Function
VCC	Power Supply
DNC	Do Not Connect
BIAS	Bias Current
DRAIN	Drain Sense
REF	Reference Current
GND	Power Ground
GATE	Gate Drive

Features

- Proportional Gate Drive to Minimize Body Diode Conduction
- Low Standby Power with Quiescent Supply Current < 1mA
- 4.5V Operation Enables Low Voltage Supply
- 40V V_{CC} Rating
- 200V Drain Voltage Rating
- Operation up to 500kHz
- Critical Conduction Mode (CrCM) & Continuous Mode (CCM)
- Compliant with Eco-Design Directive
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony free. "Green" Device (Note 3)**

Mechanical Data

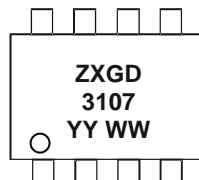
- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish. Solderable per MIL-STD-202, Method 208 [Ⓔ]
- Weight: 0.074 grams (Approximate)

Ordering Information (Note 4)

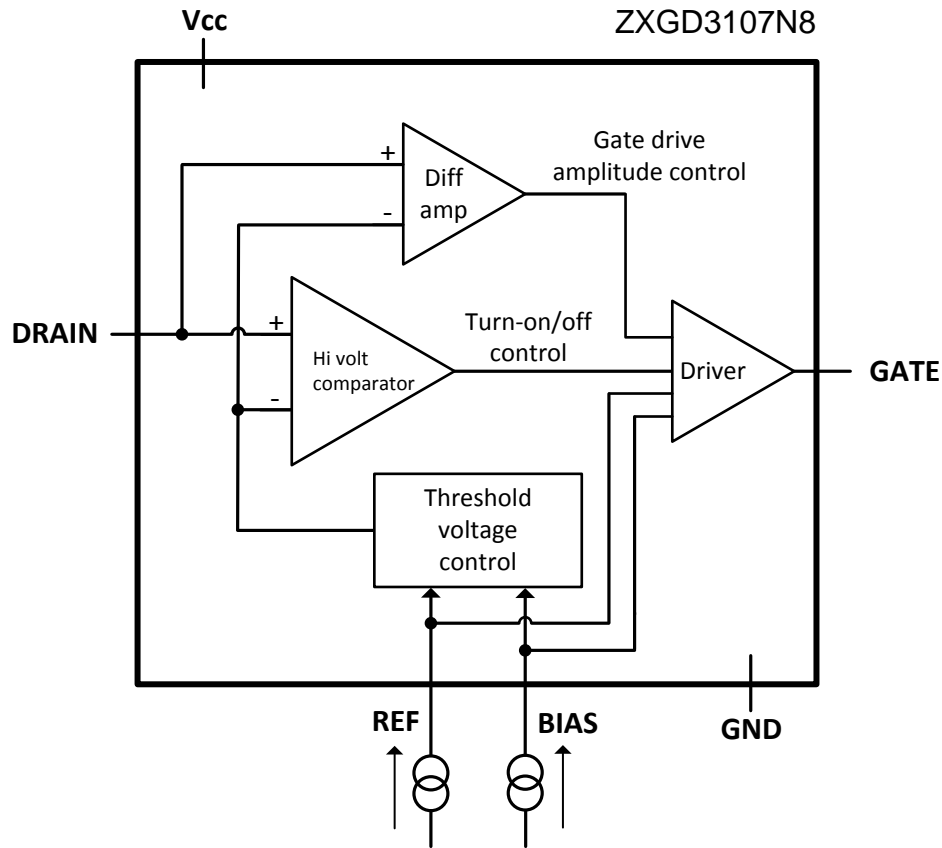
Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
ZXGD3107N8TC	ZXGD3107	13	12	2,500

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 - See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 - For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



ZXGD = Product Type Marking Code, Line 1
 3107 = Product Type Marking Code, Line 2
 YY = Year (ex: 17 = 2017)
 WW = Week (01 to 53)

Functional Block Diagram


Pin Number	Pin Name	Pin Function and Description
1	V _{CC}	Power supply This supply pin should be closely decoupled to ground with a ceramic capacitor.
2, 6	DNC	Do not connect Leave pin floating.
3	BIAS	Bias Connect this pin to V _{CC} via R _{BIAS} resistor. Select R _{BIAS} to source 0.56mA into this pin. Refer to Table 1 and 2, in Application Information section.
4	DRAIN	Drain sense Connect directly to the synchronous MOSFET drain terminal.
5	REF	Reference Connect this pin to V _{CC} via R _{REF} resistor. Select R _{REF} to source 1.23mA into this pin. Refer to Table 1 and 2, in Application Information section.
7	GND	Ground Connect this pin to the synchronous MOSFET source terminal and ground reference point.
8	GATE	Gate drive This pin sinks and sources the I _{SINK} and I _{SOURCE} current to the synchronous MOSFET Gate.

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply Voltage, Relative to GND	V _{CC}	40	V
Drain Pin Voltage	V _D	-3 to 200	V
Gate Output Voltage	V _G	-3 to V _{CC} + 3	V
Gate Driver Peak Source Current	I _{SOURCE}	4	A
Gate Driver Peak Sink Current	I _{SINK}	9	A
Reference Voltage	V _{REF}	V _{CC}	V
Reference Current	I _{REF}	25	mA
Bias Voltage	V _{BIAS}	V _{CC}	V
Bias Current	I _{BIAS}	100	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

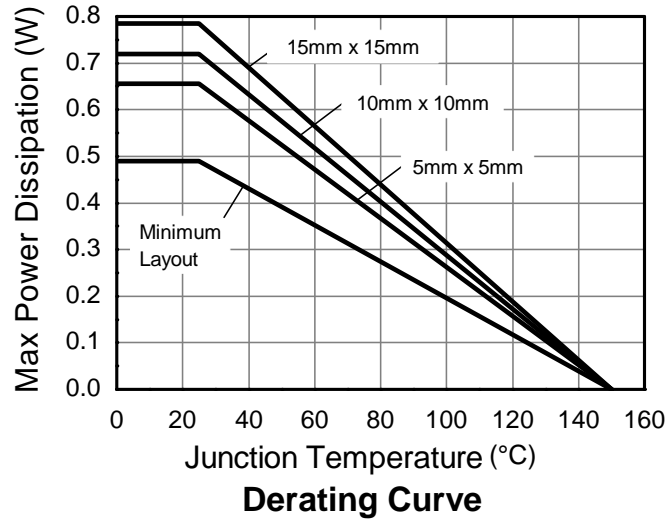
Characteristic	Symbol	Value	Unit	
Power Dissipation Linear Derating Factor	P _D	490	mW mW/°C	
		(Note 5)		3.92
		(Note 6)		655
		(Note 7)		5.24
		(Note 8)		720
Thermal Resistance, Junction to Ambient	R _{θJA}	5.76	°C/W	
		(Note 5)		785
		(Note 6)		6.28
		(Note 7)		255
(Note 8)	191			
(Note 9)	173			
(Note 10)	159			
Thermal Resistance, Junction to Lead	R _{θJL}	55	°C/W	
Thermal Resistance, Junction to Case	R _{θJC}	45	°C/W	
Operating Temperature Range	T _J	-40 to +150	°C	
Storage Temperature Range	T _{STG}	-50 to +150		

ESD Ratings (Note 11)

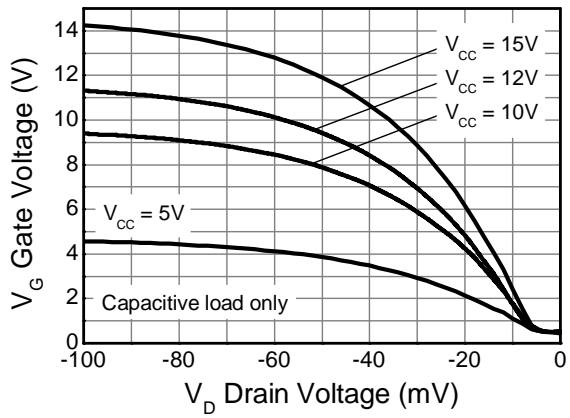
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	1,500	V	1C
Electrostatic Discharge - Machine Model	ESD MM	200	V	B

- Notes:
- For a device surface mounted on minimum recommended pad layout FR-4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 - Same as note (5), except pin 1 (V_{CC}) and pin 7 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
 - Same as note (6), except both heatsinks are 10mm x 10mm.
 - Same as note (6), except both heatsinks are 15mm x 15mm.
 - Thermal resistance from junction to solder-point at the end of each lead on pin 1 (V_{CC}) or pin 7 (GND).
 - Thermal resistance from junction to top of the case.
 - Refer to JEDEC specification JESD22-A114 and JESD22-A115.

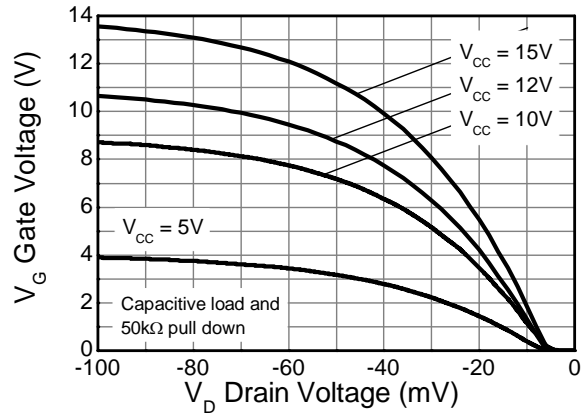
Thermal Derating Curve



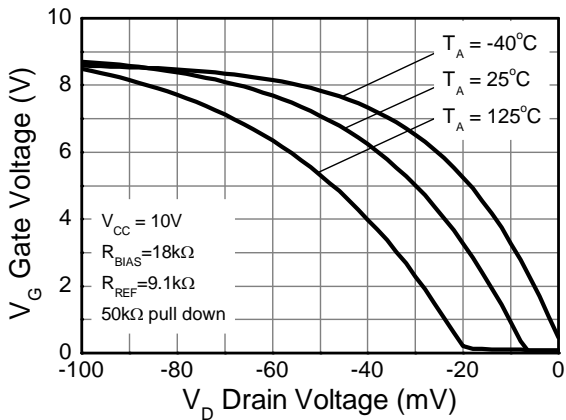
Typical Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)



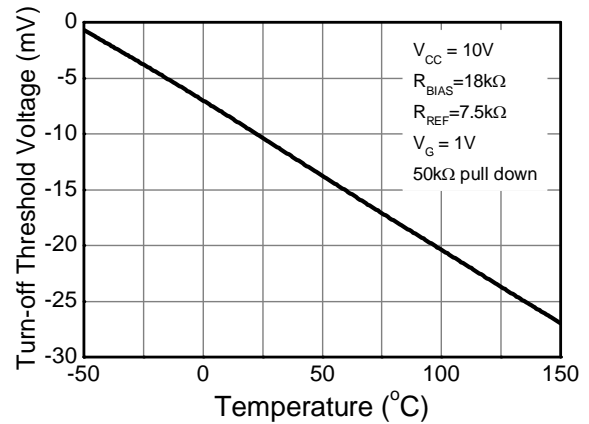
Transfer Characteristic



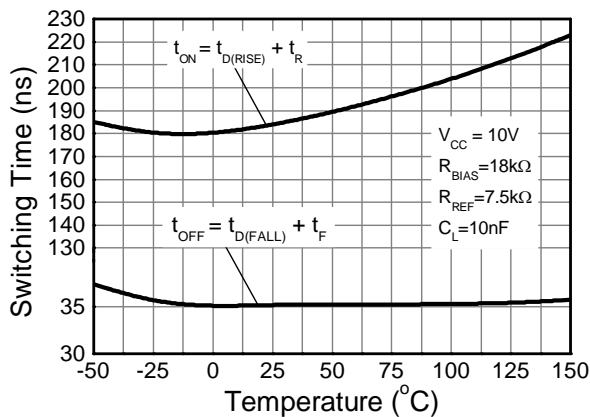
Transfer Characteristic



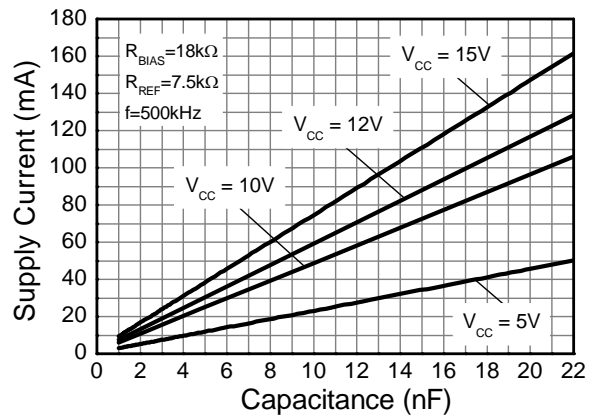
Transfer Characteristic



Turn-off Threshold Voltage vs Temperature

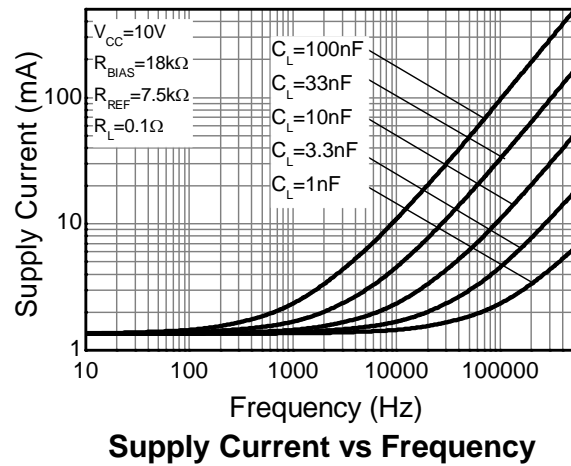
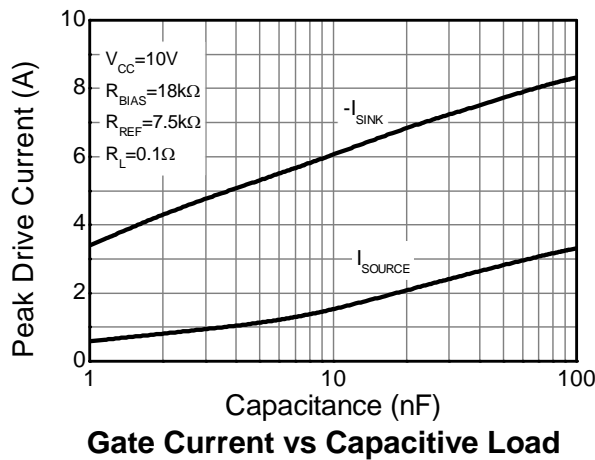
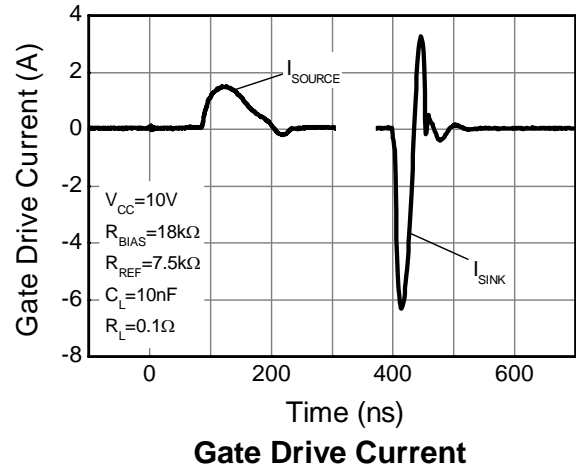
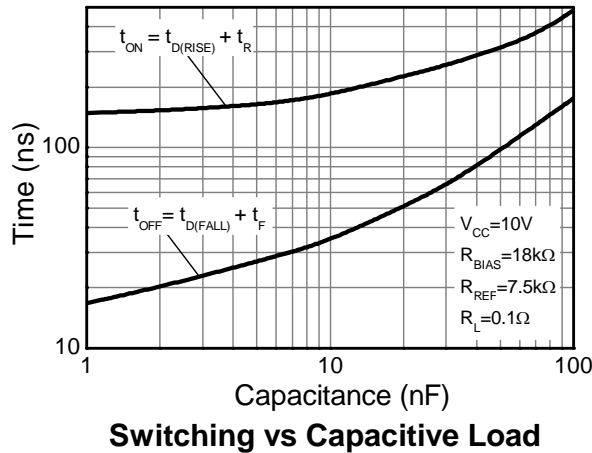
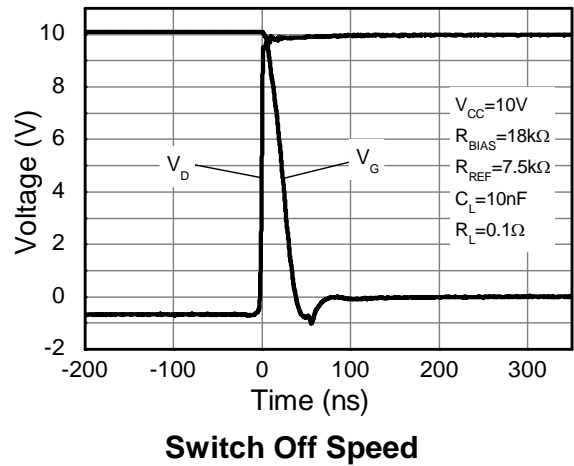
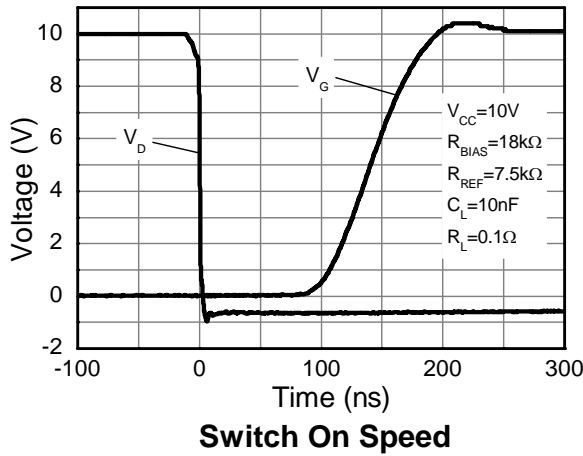


Switching vs Temperature



Supply Current vs Capacitive Load

Typical Electrical Characteristics (Cont.) (@T_A = +25°C, unless otherwise specified.)



Application Information

The purpose of the ZXGD3107N8 is to drive a MOSFET as a low- V_F Schottky diode replacement in isolated AC-DC converter. When combined with a low $R_{DS(ON)}$ MOSFET, the controller can yield significant power-efficiency improvement, while maintaining design simplicity and incurring minimal component count. Figure 1 shows the typical configuration of ZXGD3107N8 for synchronous rectification in a low output voltage flyback converter.

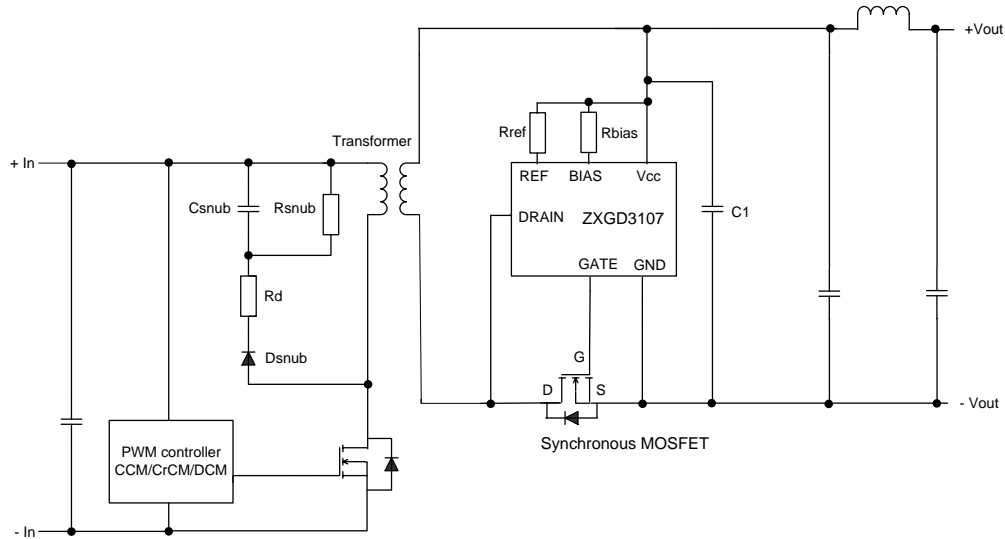


Figure 1. Typical Flyback Application Schematic

Threshold Voltage and Resistor Setting

Proper selection of external resistors R_{REF} and R_{BIAS} is important for optimum device operation. R_{REF} and R_{BIAS} supply fixed current into the REF and BIAS pins of the controller. I_{REF} and I_{BIAS} combines to set the turn-off threshold voltage level, V_T . In order to set V_T to $-10mV$, the recommended I_{REF} and I_{BIAS} are $1.23mA$ and $0.56mA$ respectively.

The values for R_{REF} and R_{BIAS} are selected based on the V_{CC} voltage. If the V_{CC} pin is connected to the power converter's output, the resistors should be selected based on the nominal converter's output voltage. Table 1 provides the recommended resistor values for different V_{CC} voltages to achieve a V_T of $-10mV$.

Supply, V_{CC}	Bias Resistor, R_{BIAS}	Reference Resistor, R_{REF}
5V	9.6k Ω	4k Ω
10V	18k Ω	7.5k Ω
12V	24k Ω	9.6k Ω
15V	30k Ω	12k Ω

Table 1. Recommended Resistor Values for Different V_{CC} Voltages

Application Information (Cont.)

Functional Descriptions

The operation of the device is described step-by-step with reference to the timing diagram in Figure 2.

1. The detector stage monitors the MOSFET drain-source voltage.
2. When, due to transformer action, the MOSFET body diode is forced to conduct there is a negative voltage on the drain pin due to the body diode forward voltage.
3. When the negative drain voltage crosses the turn-off Threshold voltage V_T , the detector stage outputs a positive voltage with respect to ground after the turn-on delay time $t_{D(FALL)}$. This voltage is then fed to the MOSFET driver stage and current is sourced out of the GATE pin.
4. The controller goes into Proportional Gate drive control — the Gate output voltage is proportional to the MOSFET on-resistance-induced drain-source voltage. Proportional Gate drive ensures that MOSFET conducts during majority of the conduction cycle to minimize power loss in the body diode.
5. As the drain current decays linearly toward zero, Proportional Gate drive control reduces the Gate voltage so the MOSFET can be turned off rapidly at zero current crossing. The Gate voltage falls to 1V when the drain-source voltage crosses the detection threshold voltage to minimize reverse current flow.
6. At zero drain current, the controller Gate output voltage is pulled low to $V_{G(OFF)}$ to ensure that the MOSFET is off.

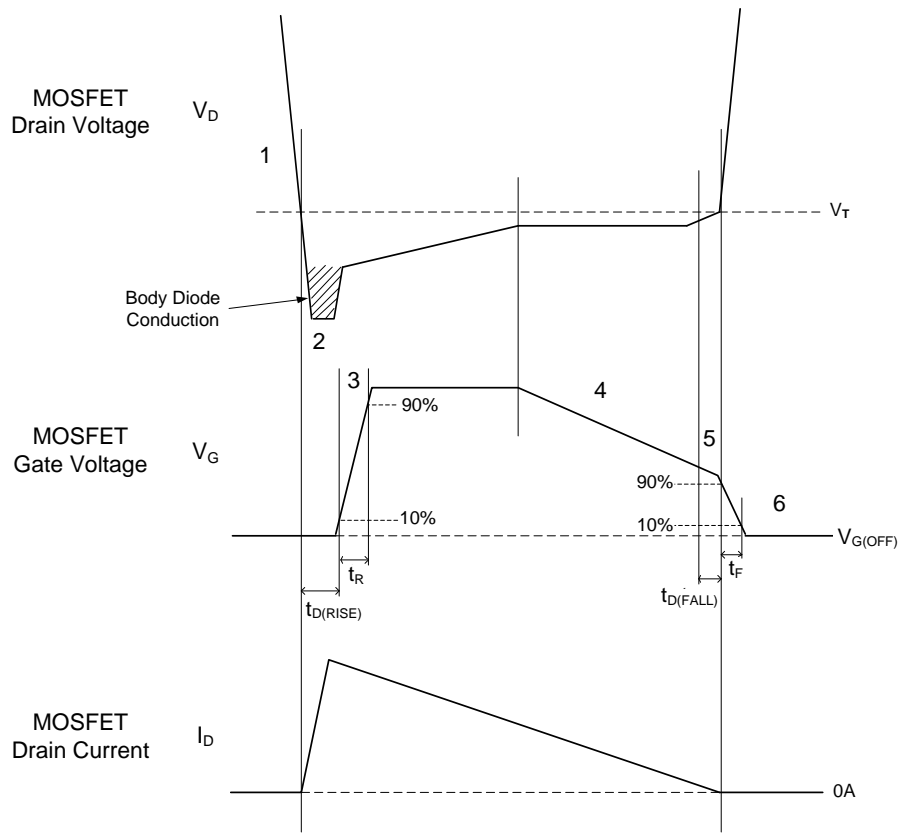


Figure 2. Timing Diagram for a Critical Conduction Mode Flyback Converter

Application Information (Cont.)

Quiescent Current Consumption

The quiescent current consumption of the controller is the sum of I_{REF} and I_{BIAS} . For an application that requires ultra-low standby power consumption, I_{REF} and I_{BIAS} can be further reduced by increasing the value of resistor R_{REF} and R_{BIAS} .

Bias Current I_{BIAS}	Ref Current I_{REF}	Bias Resistor R_{BIAS}	Ref Resistor R_{REF}	Quiescent Current I_q
0.25	0.78	39.8k Ω	11.9k Ω	1.03mA
0.35	0.94	28.4k Ω	9.8k Ω	1.29mA
0.45	1.1	22.1k Ω	8.4k Ω	1.55mA
0.56	1.23	18k Ω	7.5k Ω	1.79mA
0.6	1.34	16.6k Ω	6.9k Ω	1.94mA
0.8	1.6	12.4k Ω	5.8k Ω	2.4mA

Table 2. Quiescent Current Consumption for Different Resistor Values at $V_{CC} = 10V$

I_{REF} also controls the Gate driver peak sink current whilst I_{BIAS} controls the peak source current. At the default current value of I_{REF} and I_{BIAS} of 1.23mA and 0.56mA, the Gate driver is able to provide 2A source and 6A sink current. The Gate current decreases if I_{REF} and I_{BIAS} are reduced. Care must be taken in reducing the controller quiescent current so that sufficient drive current is still delivered to the MOSFET particularly for high-switching frequency application.

Layout Guidelines

When laying out the PCB, care must be taken in decoupling the ZXGD3107N8 closely to V_{CC} and ground with 1 μ F low-ESR, low-ESL X7R type ceramic bypass capacitor. If the converter's output voltage is higher than 40V, a series voltage regulator between the converter's output voltage and the V_{CC} pin can be used to get a stable V_{CC} voltage.

GND is the ground reference for the internal high-voltage amplifier as well as the current return for the Gate driver. So the ground return loop should be as short as possible. Sufficient PCB copper area should be allocated to the V_{CC} and GND pin for heat dissipation especially for high-switching frequency application.

Any stray inductance involved by the load current may cause distortion of the drain-to-source voltage waveform, leading to premature turn-off of the synchronous MOSFET. In order to avoid this issue, drain-voltage sensing should be done as physically close to the drain terminals as possible. The PCB track length between the controller drain pin and MOSFET's terminal should be kept less than 10mm. MOSFET packages with low internal-wire-bond inductance are preferred for high-switching frequency power conversion to minimize body diode conduction.

After the primary MOSFET turns-off, its drain voltage oscillates due to reverse recovery of the snubber diode. These high-frequency oscillations are reflected across the transformer to the drain terminal of the synchronous MOSFET. The synchronous controller senses the drain-voltage ringing, causing its Gate output voltage to oscillate. The synchronous MOSFET cannot be fully enhanced until the drain voltage stabilizes.

In order to prevent this issue, the oscillations on the primary MOSFET can be damped with either a series resistor R_d to the snubber diode or an R-C network across the diode. Both methods reduce the oscillations by softening the snubber diode's reverse recovery characteristic.

Application Information (Cont.)

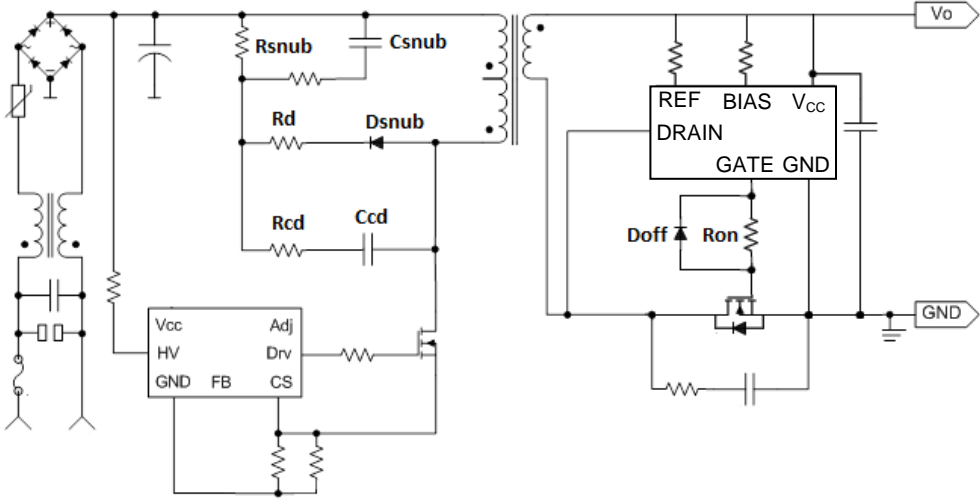
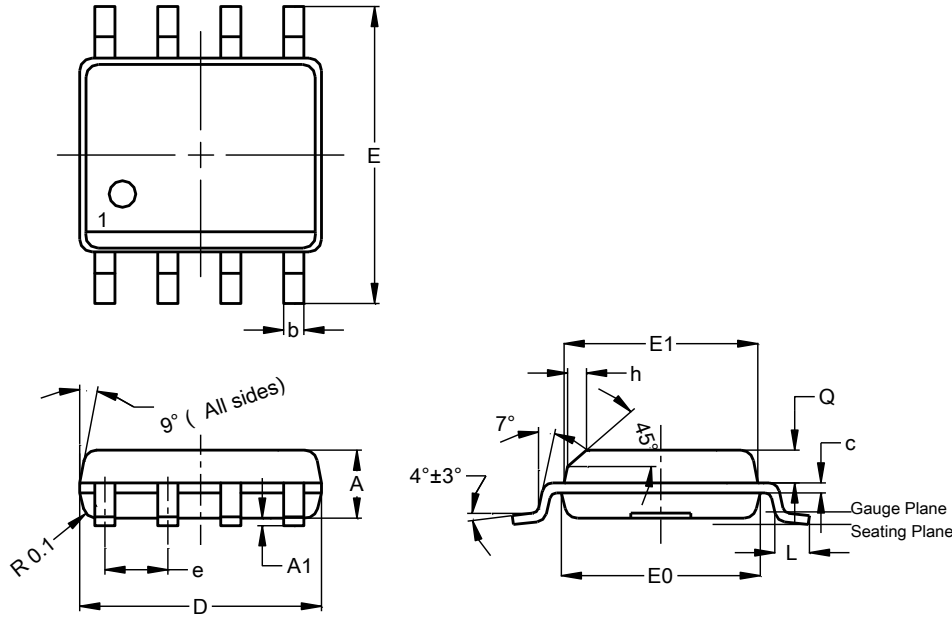


Figure 5. Primary Side Snubber Network to Reduce Drain Voltage Oscillations

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



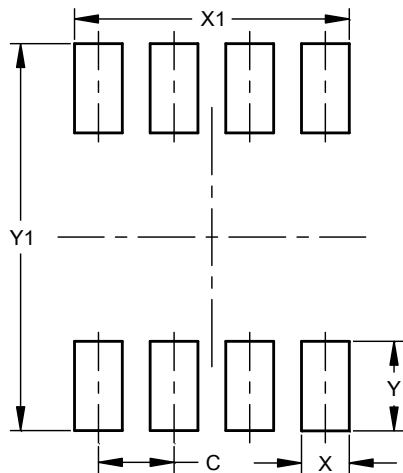
SO-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	-	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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