THE DATASHEET OF

LTC1623IS8#TRPBF

SMBus Dual High Side Switch Controller

FEATURES

- **SMBus and I²C Compatible**
- **Built-In Charge Pumps Drive N-Channel Switches**
- **16 Available Switches on the Same Bus**
- **0.6V V_{IL} and 1.4V V_{IH} for DATA and CLK**
- **Available in 8-Lead MSOP and S0 Packages**
- Low Standby Current: 14µA
- Eight Addresses from Two Three-State Address Pins
- Internal Power-On Reset Timer
- Internal Undervoltage Lockout
- No Need for External Pull-Up Resistors at Output
- No Need for Secondary Power Source

APPLICATIONS

- Computer Peripheral Control
- Laptop Computer Power Plane Switching
- Portable Equipment Power Control
- Industrial Control Systems
- Handheld Equipment

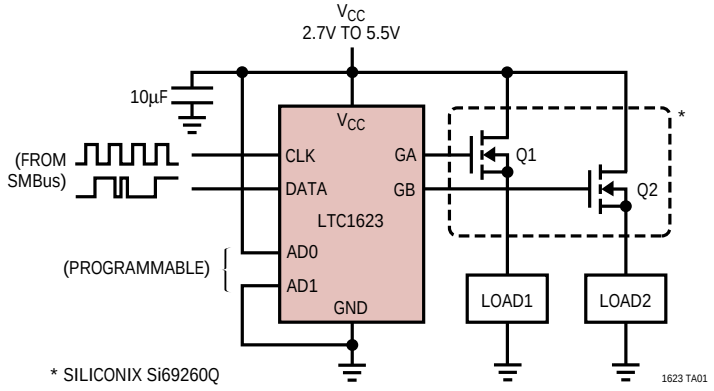
DESCRIPTION

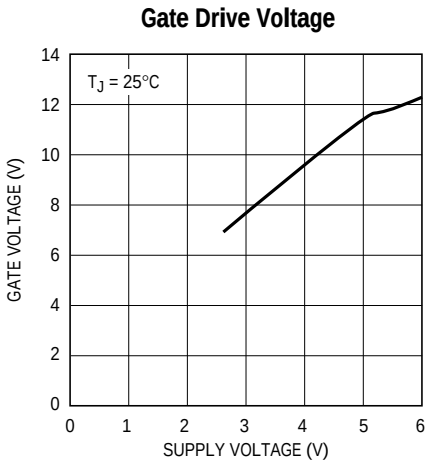
The LTC®1623 SMBus switch controller is a slave device that controls two high-side N-channel MOSFETs on either the SMBus or the I²C bus. The LTC1623 operates with an input voltage from 2.7V to 5.5V with a low standby current of 14µA (at 3.3V). In accordance with the SMBus specification, the LTC1623 maintains the 0.6V V_{IL} and 1.4V V_{IH} input thresholds throughout the supply voltage range.

Using the 2-wire interface, CLK and DATA, the LTC1623 monitors the bus for a start condition (DATA going from high to low while CLK is high). Once detected, the LTC1623 compares its address with the first (address) byte sent over the bus from the master. If matched, the LTC1623 will execute the second (command) byte from the master and independently control the built-in charge pumps to drive two external switches.

The LTC1623 has two three-state programmable address pins, thus allowing eight different addresses and a total of sixteen available switches on the same bus.

TYPICAL APPLICATION





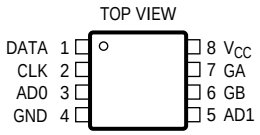
ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin)

Input Supply Voltage (V_{CC}) ..... –0.3V to 6V
DATA, CLK (Bus Pins 1, 2) ..... –0.3V to 6V
AD0, AD1 (Address Pins 3, 5) ..... –0.3V to (V_{CC} + 0.3V)
GA,GB (Gate Drive Pins 6, 7) ..... –0.3V to (V_{CC} + 7V)
Junction Temperature ..... 125°C

Operating Temperature Range
LTC1623C ..... 0° to 70°C
LTC1623I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

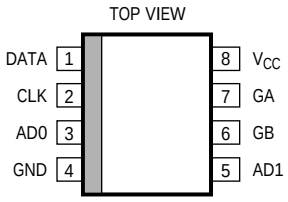
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1623CMS8
MS8 PART MARKING
LTCH



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1623CS8 LTC1623IS8
S8 PART MARKING
1623 1623I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise specified. C_{GA} = 1000pF, C_{GB} = 1000pF

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{CC}	Operating Supply Voltage Range				2.7		5.5	V
I_{VCC}	Supply Current	Charge Pump Off, AD0 and AD1High or Low, DATA and CLK High	V_{CC} = 2.7V	●		12	30	µA
			V_{CC} = 3.3V	●		14	30	µA
			V_{CC} = 5V	●		17	30	µA
I_{VCC}	Supply Current	GA or GB High (Command Byte 00000001 or 00000010)		●		140	250	µA
		Both GA and GB High (Command Byte 00000011)		●		162	250	µA
V_{GS}	Gate Voltage Above Supply	V_{CC} = 2.7V		●	2.7	4.2	7	V
		V_{CC} = 3.3V		●	4.5	5.4	7	V
		V_{CC} = 5.5V		●	4.5	6.4	7	V
V_{UVLO}	Undervoltage Lockout	Falling Edge (Note1)		●	1.5	2.0	2.5	V
t_{POR}	Power-On Reset Delay Time	V_{CC} = 2.7V (Note2)				300	1000	µs
		V_{CC} = 5.5V				300	1000	µs
f_{OSC}	Charge Pump Oscillator Frequency (Note 3)					300		kHz
t_{ON}	Turn-On Time into 1000pF	V_{CC} = 2.7V (From ON to GA, GB = V_{CC} + 1V) (Note 4)				170		µs
		V_{CC} = 5.5V (From ON to GA, GB = V_{CC} + 2V) (Note 4)				180		µs
t_{OFF}	Turn-Off Time into 1000pF	V_{CC} = 2.7V (From OFF to GA, GB = 100mV) (Note 5)				17		µs
		V_{CC} = 5.5V (From OFF to GA, GB = 100mV) (Note 5)				12		µs
V_{IL}	DATA/CLK Input Low Voltage	V_{CC} = 2.7V to 5.5V					0.6	V
V_{IH}	DATA/CLK Input High Voltage	V_{CC} = 2.7V to 5.5V			1.4			V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise specified. C_{GA} = 1000pF, C_{GB} = 1000pF

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	AD0 and AD1 Input Low Voltage	V_{CC} = 2.7V to 5.5V	●			0.2	V
V_{IH}	AD0 and AD1 Input High Voltage	V_{CC} = 2.7V to 5.5V	●	V_{CC} – 0.2			V
V_{OL}	Data Output Low Voltage	V_{CC} = 2.7 to 5.5V, I_{PULLUP} = 350µA	●		0.22	0.4	V
C_{IN}	Input Capacitance (DATA, CLK, AD0, AD1)				5		pF
I_{IN}	Input Leakage Current (DATA, CLK)					±1	µA
	Input Leakage Current(AD0, AD1)					±250	nA
SMBus Related Specs (Note 6)							
f_{SMB}	SMBus Operating Frequency			10		100	kHz
t_{SUSTA}	Start Condition Setup Time			4.7			µs
t_{BUF}	Bus Free Time Between Stop and Start			4.7			µs
t_{HDSTA}	Start Condition Hold Time			4.0			µs
t_{SUSTP}	Stop Condition Setup Time			4.0			µs
t_{HDDAT}	Data Hold Time			300			ns
t_{SUDAT}	Data Setup Time			250			ns
t_{LOW}	Clock Low Period			4.7			µs
t_{HIGH}	Clock High Period			4.0		50	µs
t_f	Clock /Data Fall Time					300	ns
t_r	Clock/Data Rise Time					1000	ns
I_{PULLUP}	Current Through External Pull-Up Resistor on DATA Pin	(Data Pull-Down Current Capacity) V_{CC} = 2.7V to 5.5V		100		350	µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Approximately 3% hysteresis is provided to ensure stable operation and eliminate false triggering by minor V_{CC} glitches.

Note 2: Measured from $V_{CC} > V_{UVLO}$ to SMBus ready for data input.

Note 3: The oscillator frequency is not tested directly but is inferred from turn-on time.

Note 4: ON is enabled upon receiving the Stop condition from the SMBus master.

Note 5: OFF is enabled upon receiving the Stop condition from the SMBus master.

Note 6: SMBus timing specs are guaranteed but not tested.

PIN FUNCTIONS

DATA: (Pin 1) Open-Drain Connected Serial Data Interface. Must be pulled high to V_{CC} with external resistor. The pull-up current must be limited to 350µA.

CLK: (Pin 2) Serial Clock Interface. Must be pulled high to V_{CC} with external resistor. The pull-up current must be limited to 350µA.

AD0: (Pin 3) Lower Three-State Programmable Address Pin. Must be connected directly to V_{CC}, GND, or $V_{CC}/2$ (using two resistors ≤ 1M). Do not float this pin.

GND: (Pin 4) Ground.

AD1: (Pin 5) Higher Three-State Programmable Address Pin. Must be connected directly to V_{CC}, GND, or $V_{CC}/2$ (using two resistors ≤ 1M). Do not float this pin.

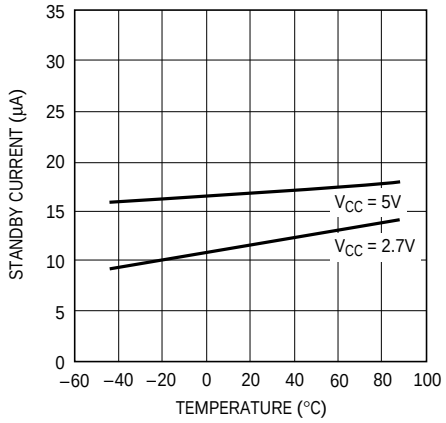
GB: (Pin 6) Gate Drive to External High-Side Switch. Fully enhanced by internal charge pump. Controlled by 2nd LSB of command byte.

GA: (Pin 7) Gate Drive to External High-Side Switch. Fully enhanced by internal charge pump. Controlled by LSB of command byte.

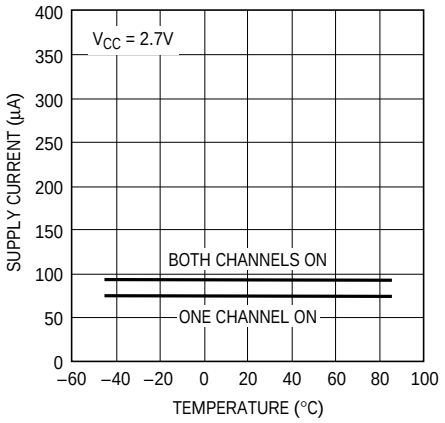
V_{CC}: (Pin 8) Input Supply Voltage. Range from 2.7V to 5.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

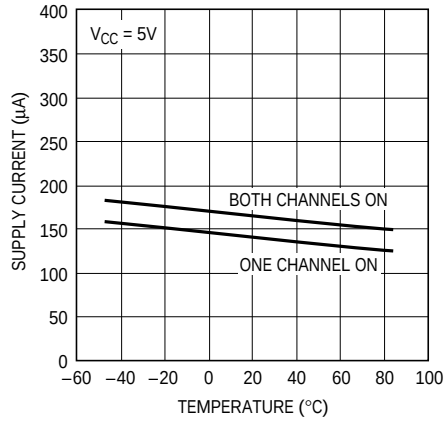
Standby Current



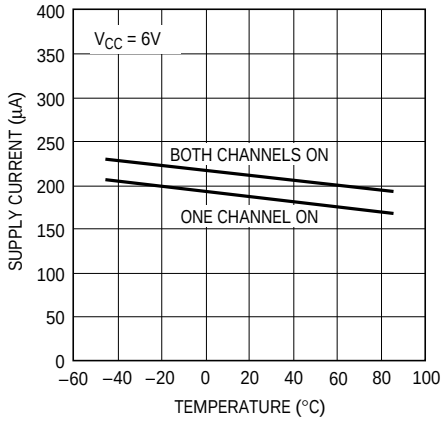
Supply Current



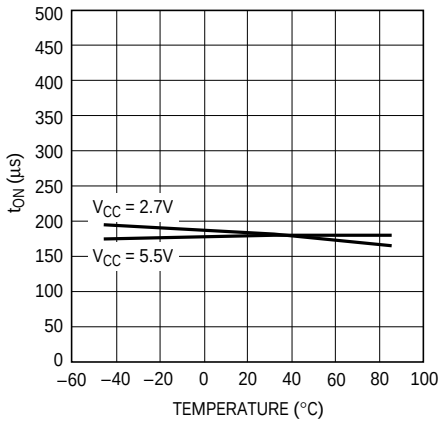
Supply Current



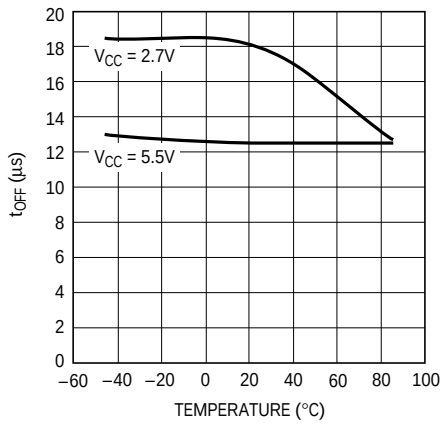
Supply Current



t_{ON} vs Temperature

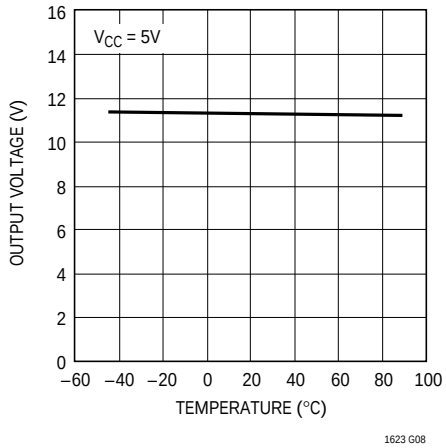


t_{OFF} vs Temperature

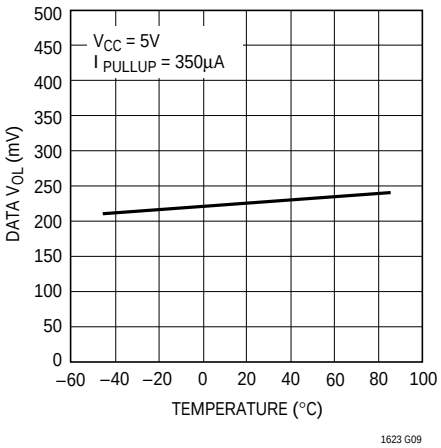


TYPICAL PERFORMANCE CHARACTERISTICS

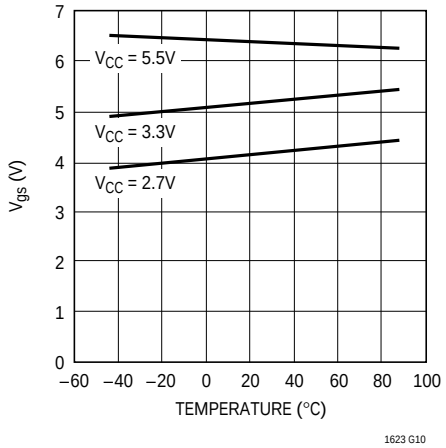
GA, GB Output Voltage



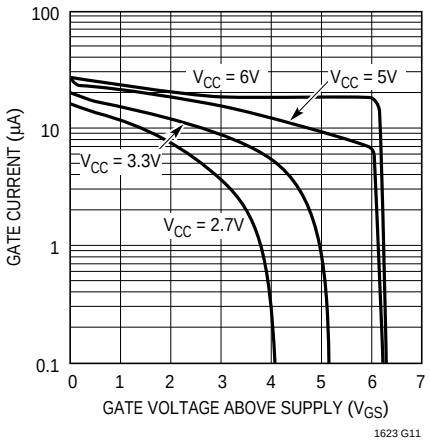
DATA V_{OL} vs Temperature



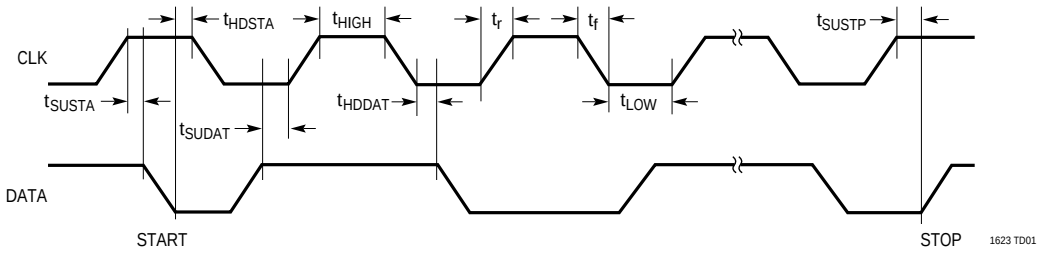
V_{GS} vs Temperature



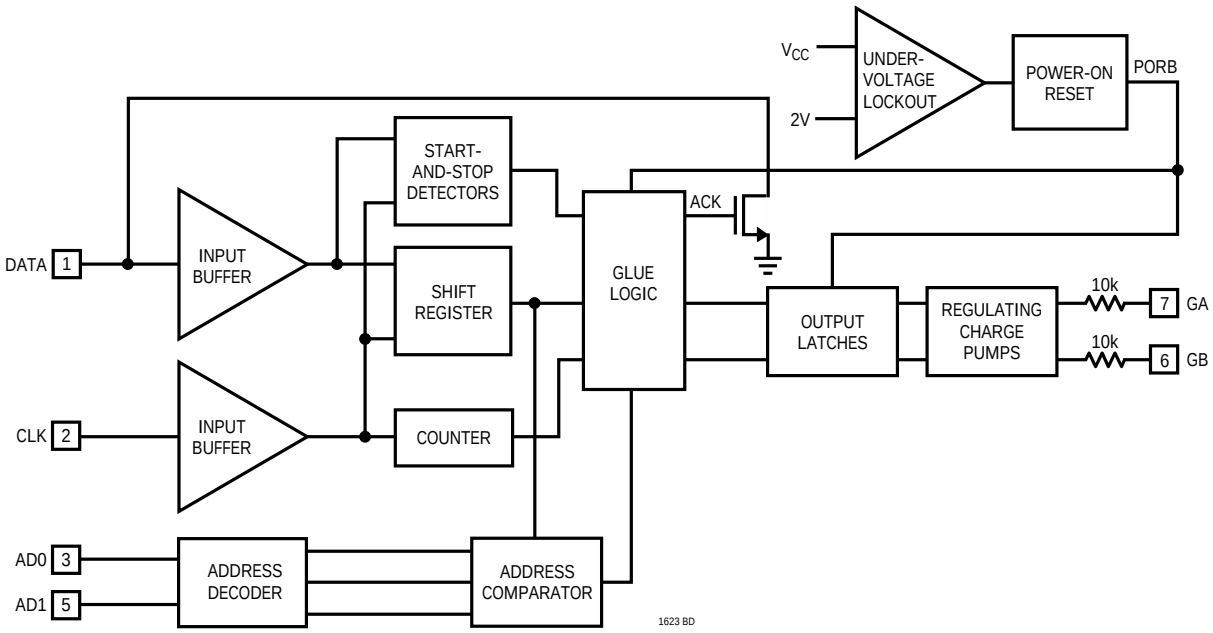
Gate Drive Current



TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



OPERATION

SMBus Operation

SMBus is a serial bus interface that uses only two bus lines, DATA and CLK, to control low power peripheral devices in portable equipment. It consists of masters, also known as hosts, and slave devices. The master of the SMBus is always the one to initiate communications to its slave devices by varying the status of the DATA and CLK lines. The SMBus specification establishes a set of protocols that devices on the bus must follow during communications.

The protocol that the LTC1623 uses is the Send Byte Protocol. In this protocol, the master first sends out a Start signal by switching the DATA line from high to low while CLK is high. (Because there may be more than one master on the same bus, an arbitration process takes place if two masters attempt to take control of the DATA line simultaneously; the first master that outputs a one while the other master is zero loses the arbitration and becomes a slave itself.) Upon detecting this Start signal, all slave devices on the bus wake up and get ready to shift in the next byte of data.

The master then sends out the first byte. The first seven bits of this byte consist of the address of the device that the master wishes to communicate with. The last bit indicates whether the command will be a read (logic one) or write (logic zero). Because the LTC1623 is a slave device that can only be written to by a master, it will ignore the ensuing commands of the master if it wants to read from the LTC1623, even if the address sent by the master matches that of the LTC1623. After reception of the first byte, the slave device (LTC1623) with the matching address then acknowledges the master by pulling the data line low before the rising edge of the ninth clock cycle.

By now, all other nonmatching slave devices will have gone back to their original standby states to wait for the next start signal. Meanwhile, upon receiving the acknowledge from the matching slave, the master then sends out the command byte. In the case of the LTC1623, the two LSBs of this second byte from the master are the signals controlling the status of the external switches; a digital "one" turns on the charge pump to drive up the output gate voltage while a digital "zero" shuts down the charge pump and discharges the output gate voltage to zero.

After receiving the command byte, the slave device (LTC1623) needs to again acknowledge the master by pulling the DATA line low on the following clock cycle. The master then ends this Send Byte Protocol by sending the Stop signal, which is a transition from low to high on the DATA line while the CLK line is high. Valid data is shifted into the output latch on the last acknowledge signal; the external switch will not be enabled, however, until the Stop signal is detected. This double-buffering feature allows the user to daisy-chain several differently addressed SMBus devices such that their output executions are synchronous to the Stop signal even though valid data were loaded into their output latches at different times. Figure 1 shows an example of this special protocol. If somehow either the Start or the Stop signal is detected in the middle of a byte, the slave device (LTC1623) will regard this as an error and reject all previous data. Other than the Stop and Start conditions, DATA must be stable during CLK high; DATA can change state only during CLK low.

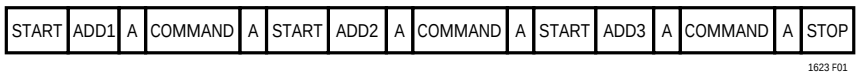
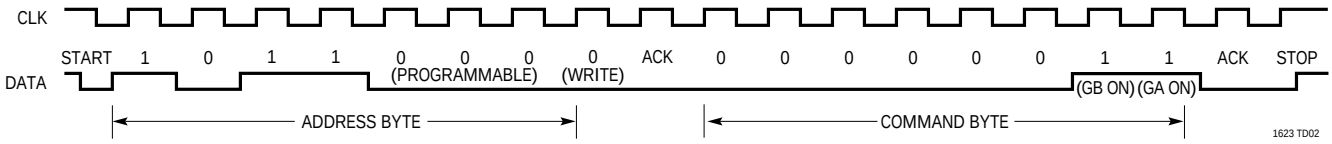


Figure 1. Daisy-Chaining Multiple SMBus Devices

Example of Send Byte Protocol to Slave Address 1011000 Turning GA and GB On



OPERATION

Address

The LTC1623 has an address of 1011XXX; the four MSBs are hard-wired, but the 3 LSBs are programmed by the user with the help of two three-state address pins. Refer to Table 1 for the pin configurations and their corresponding addresses.

To conserve standby current, it is preferable to tie the address pins to either V_{CC} or GND. If more than four addresses are needed, then either one of the address pins can be tied to the third state of $V_{CC}/2$ by using two equal value resistors (≤1M) shown in Figure 2. Do not connect both address pins to the $V_{CC}/2$ state simultaneously because this is not a valid address.

Table 1. Address Pin Truth Table

AD0	AD1	ADDRESS
GND	GND	1011000
GND	$V_{CC}/2$	1011001
GND	V_{CC}	1011010
$V_{CC}/2$	GND	1011011
$V_{CC}/2$	$V_{CC}/2$	UNUSED
$V_{CC}/2$	V_{CC}	1011100
V_{CC}	GND	1011101
V_{CC}	$V_{CC}/2$	1011110
V_{CC}	V_{CC}	1011111

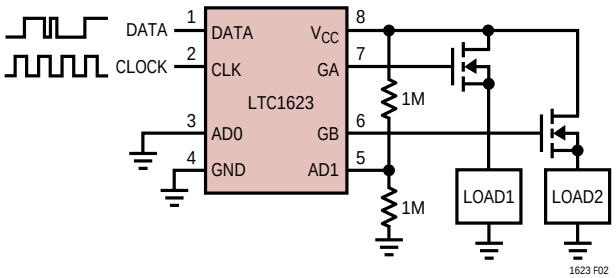


Figure 2. LTC1623 Programmed with Address 1011001

Charge Pump

To fully enhance the external N-channel switches, an internal charge pump is used to boost the output gate drive to a minimum of 2.7V and a maximum of 6V above V_{CC}, depending on V_{CC} itself. The reason for the maximum output voltage limit is to avoid switch gate source breakdown due to excessive gate overdrive. A feedback network is used to limit the charge pump output to 6V above V_{CC}. Because the output will only need to drive the gate of the external switch by charging and discharging the parasitic gate capacitances, the internal charge pump, clocked by an approximately 300KHz oscillator, is appropriately sized to source less than 100µA.

Power-On Reset and Undervoltage Lockout

The LTC1623 starts up with both gate drives low. An internal power-on reset (POR) signal inhibits operation until about 300µs after V_{CC} crosses the undervoltage lockout threshold (typically 2V). The circuit includes some hysteresis and delay to avoid nuisance resets. Once operation begins, V_{CC} must drop below the threshold for at least 100µs to trigger another POR sequence.

During standby, when both gate drive outputs are disabled, quiescent current is kept to a minimum (13µA typical) because only the UVLO block is active.

Input Threshold

Anticipating the trend toward lower supply voltages, the SMBus is specified with a V_{IH} of 1.4V and a V_{IL} of 0.6V. While some SMBus parts may violate this stringent SMBus specification by allowing a higher V_{IH} value for a correspondingly higher input supply voltage, the LTC1623 meets and maintains the constant SMBus input threshold specification across the entire supply voltage range of 2.7V to 5.5V.

APPLICATIONS INFORMATION

To avoid turning on the external power MOSFETs too quickly, an internal 10k resistor has been placed in series with each of the output gate drive pins (see Functional Block Diagram). Therefore, it only needs an external 0.1µF capacitor to create enough RC delay (10k • 0.1µF = 1ms) to slow down the ramp rate of the output gate drive. In other words, it will take a minimum of 1ms to charge up the external MOSFET. An additional external 1k resistor between the 0.1µF capacitor and the gate of the MOSFET (Figure 3) is required to eliminate possible MOSFET self oscillations.

For active-low applications in which the load needs to be on upon power-up, an external P-channel switch can be used (Figure 3). This load can be switched off later after the proper protocol has been sent.

Used with the LT®1431, the LTC1623 makes a 3.3V/3A extremely low voltage drop regulator (Figures 4 and 5). In this application, the other output channel can be used to drive a separate load, or it can also be used to control the output of the LDO so that the user has total control over the switching in and switching out of the LDO (Figure 5). Also, with the help of the LT1304-5, the LTC1623 can be used to make a boost switching regulator with a low standby current of 22µA (Figure 6).

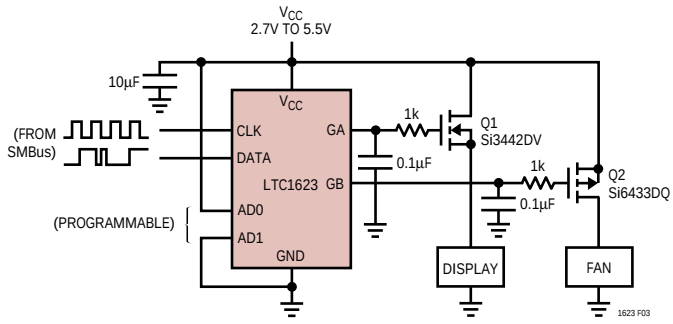


Figure 3. Dual Load Switch with Q2 On upon Power-Up

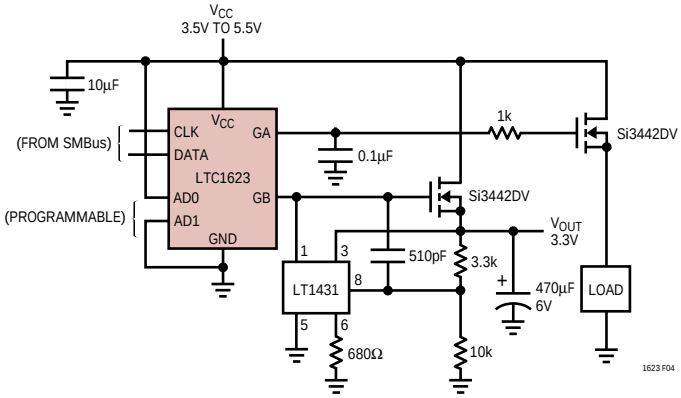


Figure 4. 3.3V/3A Extremely Low Voltage Drop Regulator and Load Switch

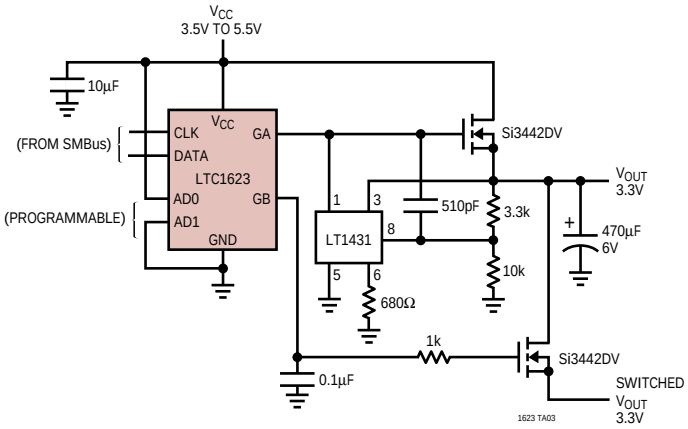


Figure 5. SMBus Controlled Low Dropout Regulator

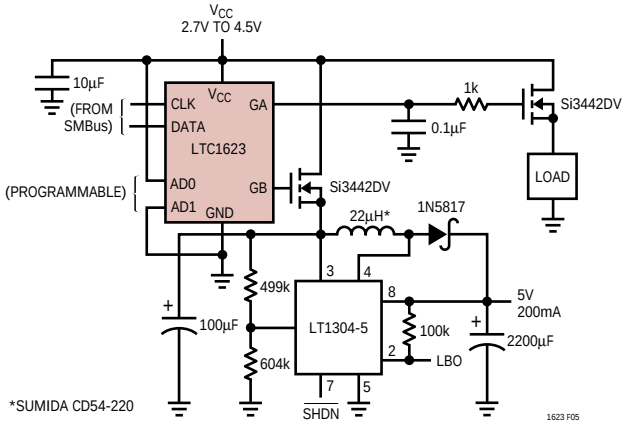
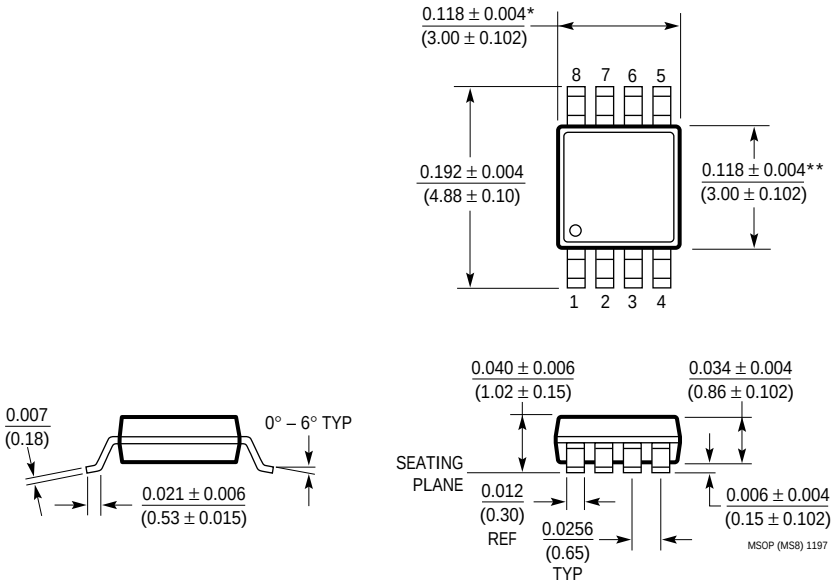


Figure 6. Switching Regulator with Low-Battery Detect Using 22µA Standby Current

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



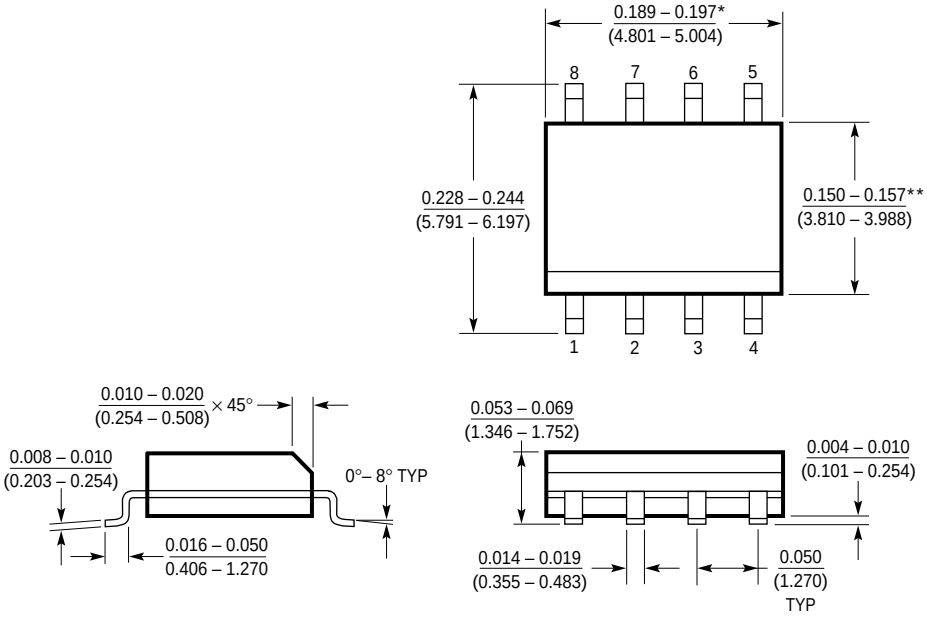
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



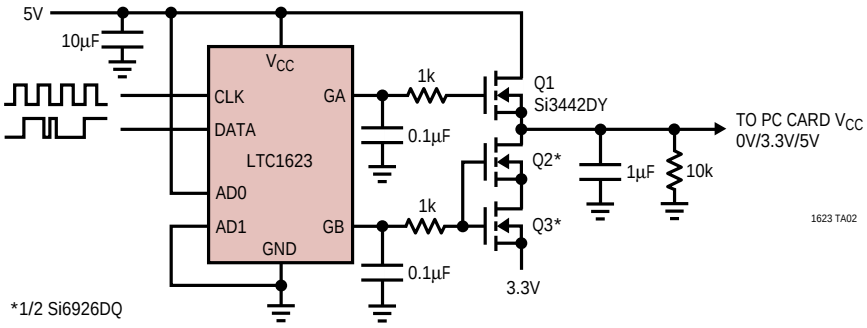
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

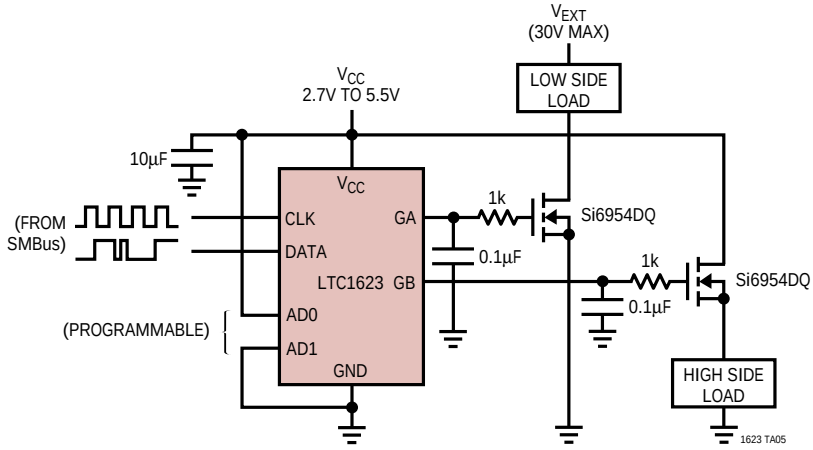
SO8 0996

TYPICAL APPLICATIONS

Single Slot PCMCIA 3.3V/5V Switch



LTC1623 Driving Both High Side and Low Side Switches



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1153/LTC1154	Single High Side Micropower MOSFET Drivers	Circuit Breaker with Auto Reset
LTC1155/LTC1255	Dual High Side Micropower MOSFET Drivers	Latch-Off Current Limit
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	Three MOSFET Drivers in 8-Lead SO Package
LT1304	Micropower DC/DC Converter	Low-Battery Detector Active in Shutdown
LTC1473	Dual PowerPath™ Switch Matrix	Current Limit with Timer
LTC1479	PowerPath Controller for Dual Battery Systems	Complete Smart Battery Controller

PowerPath is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1623f LT/TP 0598 4K • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC1623IS8#TRPBF on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management