THE DATASHEET OF

APA600-FG256

ProASIC^PLUS® Flash Family FPGAs

FlashLock

Features and Benefits

High Capacity

Commercial and Industrial

- 75,000 to 1 Million System Gates
- 27 K to 198 Kbits of Two-Port SRAM
- 66 to 712 User I/Os

Military

- 300, 000 to 1 Million System Gates
- 72 K to 198 Kbits of Two Port SRAM
- 158 to 712 User I/Os

Reprogrammable Flash Technology

- 0.22 µm 4 LM Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Up Cycles
- Mil/Aero Devices Operate over Full Military Temperature Range

Performance

- 3.3 V, 32-Bit PCI, up to 50 MHz (33 MHz over military temperature)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming

- The Industry's Most Effective Security Key (FlashLock®)

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy

- Ultra-Fast Local and Long-Line Network
- High-Speed Very Long-Line Network
- High-Performance, Low Skew, Splittable Global Network
- 100% Routability and Utilization

I/O

- Schmitt-Trigger Option on Every Input
- 2.5 V / 3.3 V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin-Compatible Packages across the ProASIC^PLUS Family

Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide, and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs

- SmartGen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

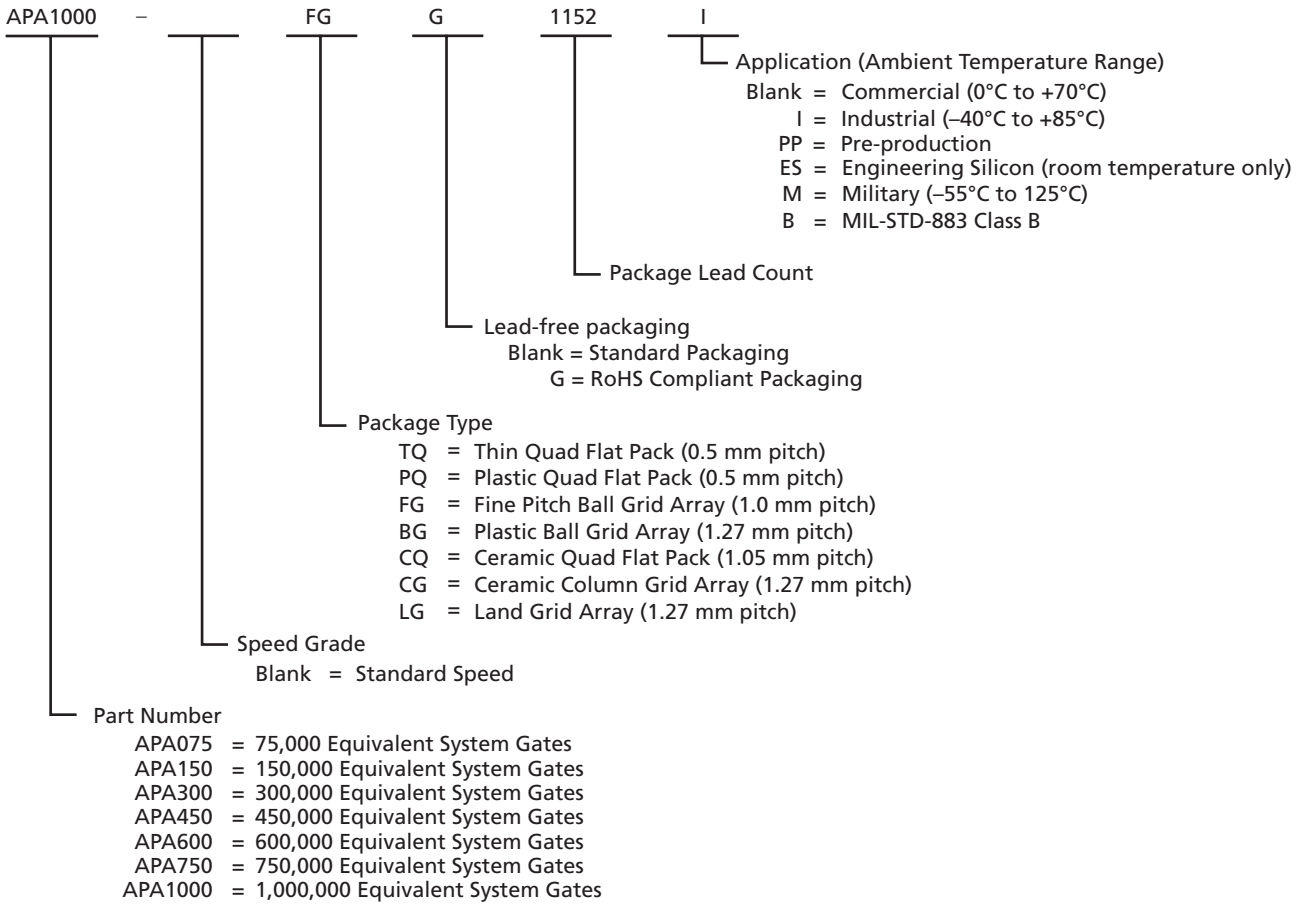
Table 1 • **ProASIC^PLUS Product Profile**

Device	APA075	APA150	APA300[1]	APA450	APA600[1]	APA750	APA1000[1]
Maximum System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Tiles (Registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits (k=1,024 bits)	27 k	36k	72 k	108 k	126 k	144 k	198 k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2	2
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	24	32	32	48	56	64	88
Maximum User I/Os	158	242	290	344	454	562	712
JTAG ISP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)							
TQFP	100, 144	100	–	–	–	–	–
PQFP	208	208	208	208	208	208	208
PBGA	–	456	456	456	456	456	456
FBGA	144	144, 256	144, 256	144, 256, 484	256, 484, 676	676, 896	896, 1152
CQFP[2]			208, 352		208, 352		208, 352
CCGA/LGA[2]					624		624

Notes:

1. *Available as Commercial/Industrial and Military/MIL-STD-883B devices.*
2. *These packages are available only for Military/MIL-STD-883B devices.*

Ordering Information



Device Resources

	User I/Os[2]												
	Commercial/Industrial										Military/MIL-STD-883B		
Device	TQFP[3] 100-Pin	TQFP[3] 144-Pin	PQFP[3] 208-Pin	PBGA[3] 456-Pin	FBGA[3] 144-Pin	FBGA[3] 256-Pin	FBGA[3] 484-Pin	FBGA[3] 676-Pin	FBGA[3] 896-Pin	FBGA[3] 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 [4]							
APA300			158 [5]	290 [5]	100 [5]	186 [4, 5]					158	248	
APA450			158	344	100	186 [4]	344 [4]						
APA600			158 [5]	356 [5]		186 [4, 5]	370 [4]	454			158	248	440
APA750			158	356				454	562 [6]				
APA1000			158 [5]	356 [5]					642 [5, 6]	712 [6]	158	248	440

Notes:

1. *Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*
2. *Each pair of PECL I/Os is counted as one user I/O.*
3. *Available in RoHS compatible packages. Ordering code is "G."*
4. *FG256 and FG484 are footprint-compatible packages.*
5. *Military Temperature Plastic Package Offering*
6. *FG896 and FG1152 are footprint-compatible packages.*

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

Temperature Grade Offerings

Package	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
TQ100	C, I	C, I					
TQ144	C, I						
PQ208	C, I	C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
BG456		C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
FG144	C, I	C, I	C, I, M	C, I			
FG256		C, I	C, I, M	C, I	C, I, M		
FG484				C, I	C, I, M		
FG676					C, I, M	C, I	
FG896						C, I	C, I, M
FG1152							C, I
CQ208			M, B		M, B		M, B
CQ352			M, B		M, B		M, B
CG624					M, B		M, B

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Speed Grade and Temperature Matrix

	Std.
C	✓
I	✓
M, B	✓

Note: *C = Commercial*
I = Industrial
M = Military
B = MIL-STD-883

Device Family Overview

The ProASIC^PLUS family of devices, Actel's second-generation family of flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^PLUS a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^PLUS family achieves its nonvolatility and reprogrammability through an advanced flash-based 0.22 µm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant flash switches allows 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the flash FPGA implementation, please refer to the "Boundary Scan (JTAG)" section on page 2-8.

ProASIC^PLUS devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

ProASIC^PLUS Architecture

The proprietary ProASIC^PLUS architecture provides granularity comparable to gate arrays.

The ProASIC^PLUS device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^PLUS devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user-defined depth and width, and parity generation or checking. Refer to the "Embedded Memory Specifications" section on page 2-54 for more information.

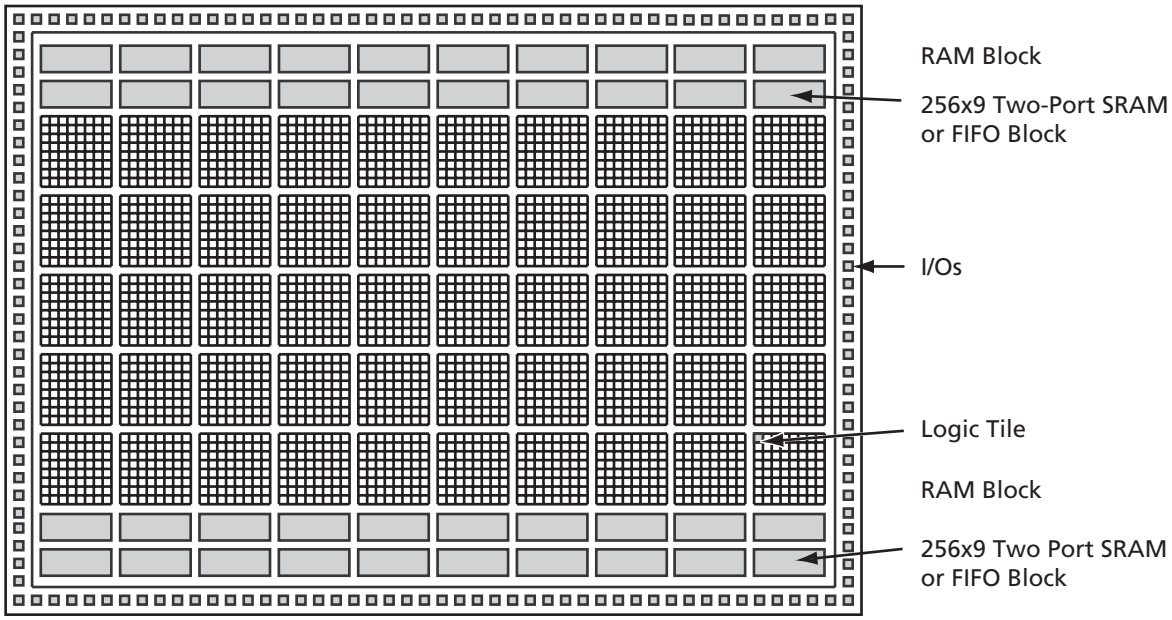


Figure 1-1 • **The ProASIC^PLUS Device Architecture**

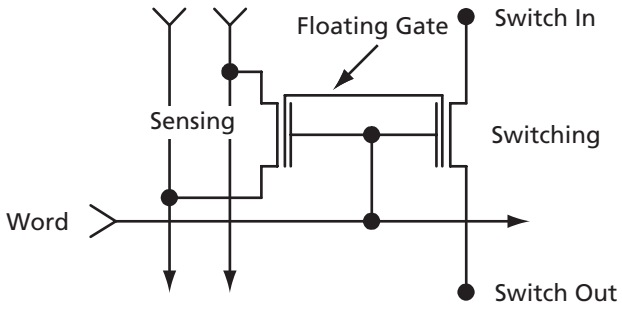


Figure 1-2 • **Flash Switch**

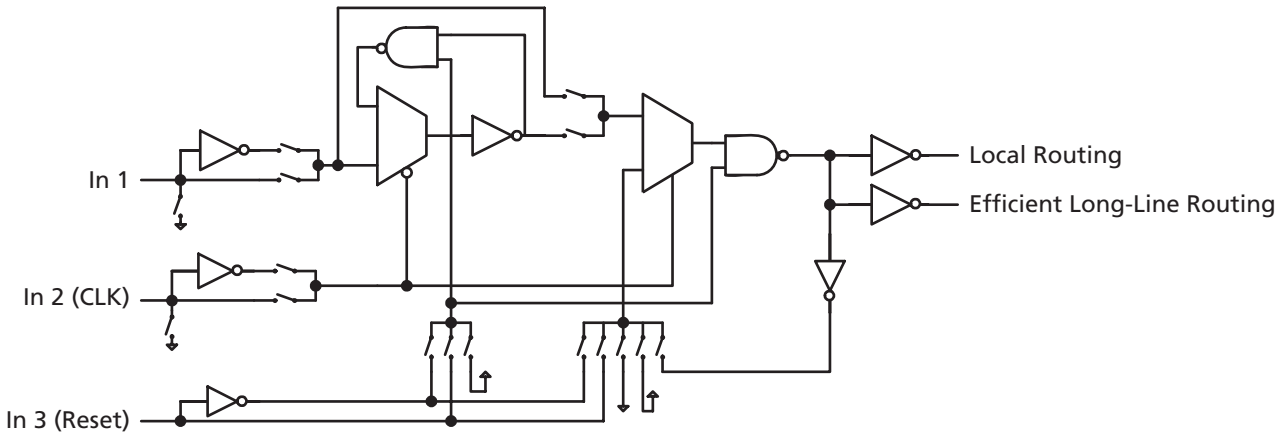


Figure 1-3 • **Core Logic Tile**

Live at Power-Up

The Actel flash-based ProASIC^PLUS devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, executing critical tasks before the processor wakes up, setting up and configuring memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC^PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for complex programmable logic device (CPLD) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC^PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC^PLUS devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Flash Switch

Unlike SRAM FPGAs, ProASIC^PLUS uses a live-at-power-up ISP flash switch as its programming element.

In the ProASIC^PLUS flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-2).

Logic Tile

The logic tile cell (Figure 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

Data Sheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advance

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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