THE DATASHEET OF

ADA4075-2ACPZ-R7

Ultralow Noise Amplifier at Lower Power

Data Sheet

ADA4075-2

FEATURES

Ultralow noise: 2.8 nV/√Hz at 1 kHz typical
Ultralow distortion: 0.0002% typical
Low supply current: 1.8 mA per amplifier typical
Offset voltage: 1 mV maximum
Bandwidth: 6.5 MHz typical
Slew rate: 12 V/µs typical
Dual-supply operation: ±4.5 V to ±18 V
Unity-gain stable
Extended industrial temperature range
8-lead SOIC and 2 mm × 2 mm LFCSP packages

APPLICATIONS

Precision instrumentation
Professional audio
Active filters
Low noise amplifier front end
Integrators

PIN CONFIGURATIONS

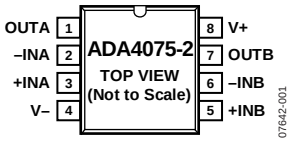

Figure 1. 8-Lead SOIC

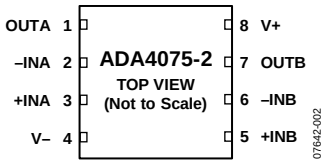

Figure 2. 8-Lead, 2 mm × 2 mm LFCSP

GENERAL DESCRIPTION

The ADA4075-2 is a dual, high performance, low noise operational amplifier combining excellent dc and ac characteristics on the Analog Devices, Inc., *i*Polar® process. The *i*Polar process is an advanced bipolar technology implementing vertical junction isolation with lateral trench isolation. This allows for low noise performance amplifiers in smaller die size at faster speed and lower power. Its high slew rate, low distortion, and ultralow noise make the ADA4075-2 ideal for high fidelity audio and high performance instrumentation applications. It is also especially useful for lower power demands, small enclosures, and high density applications. The ADA4075-2 is specified for the −40°C to +125°C temperature range and is available in a standard SOIC package and a 2 mm × 2 mm LFCSP package.

Table 1. Low Noise Precision Op Amps

Supply	44 V	36 V	12 V to 16 V	5 V
Single	OP27	AD8671 AD8675 AD8597 ADA4004-1 AD797	AD8665 OP162	AD8605 AD8655 AD8691
Dual	OP275	AD8672 AD8676 AD8599 ADA4004-2	AD8666 OP262	AD8606 AD8656 AD8692
Quad		AD8674 ADA4004-4	AD8668 OP462	AD8608 AD8694

Rev. C
Document Feedback

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10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, SOIC package, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	1	mV
		−40°C ≤ T_A ≤ +125°C			1.2	mV
Input Bias Current	I_B			30	100	nA
		−40°C ≤ T_A ≤ +125°C			150	nA
Input Offset Current	I_{OS}			5	50	nA
		−40°C ≤ T_A ≤ +125°C			75	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	110	118		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −11 V to +11 V	114	117		dB
		−40°C ≤ T_A ≤ +125°C	108			dB
		R_L = 600 Ω, V_O = −10 V to +10 V	112	117		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.3		µV/°C
Input Resistance, Differential Mode	R_{INDM}			1.5		MΩ
Input Resistance, Common Mode	R_{INCM}			500		MΩ
Input Capacitance, Differential Mode	C_{INDM}			2.4		pF
Input Capacitance, Common Mode	C_{INCM}			2.1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	12.8	13		V
		−40°C ≤ T_A ≤ +125°C	12.5			V
		R_L = 600 Ω to GND	12.4	12.8		V
		−40°C ≤ T_A ≤ +125°C	12			V
		V_{SY} = ±18 V, R_L = 600 Ω to GND	15	15.8		V
		−40°C ≤ T_A ≤ +125°C	14			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		−14	−13.6	V
		−40°C ≤ T_A ≤ +125°C			−13	V
		R_L = 600 Ω to GND		−13.6	−13	V
		−40°C ≤ T_A ≤ +125°C			−12.5	V
		V_{SY} = ±18 V, R_L = 600 Ω to GND		−16.6	−16	V
		−40°C ≤ T_A ≤ +125°C			−15	V
Short-Circuit Current	I_{SC}			40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V	106	110		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Supply Current per Amplifier	I_{SY}	V_{SY} = ±4.5 V to ±18 V, I_O = 0 mA		1.8	2.25	mA
		−40°C ≤ T_A ≤ +125°C			3.35	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, A_V = 1		12		V/µs
Settling Time	t_S	To 0.01%, V_{IN} = 10 V step, R_L = 1 kΩ		3		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 35 pF, A_V = 1		6.5		MHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 35 pF, A_V = 1		60		Degrees
THD + NOISE						
Total Harmonic Distortion and Noise	THD + N	R_L = 2 kΩ, A_V = 1, V_{IN} = 3 V rms, f = 1 kHz		0.0002		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		60		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.2		pA/√Hz

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, LFCSP package, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	1	mV
		−40°C ≤ T_A ≤ +125°C			1.5	mV
Input Bias Current	I_B			30	100	nA
		−40°C ≤ T_A ≤ +125°C			150	nA
Input Offset Current	I_{OS}			5	50	nA
		−40°C ≤ T_A ≤ +125°C			75	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	110	116		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −11 V to +11 V	110	117		dB
		−40°C ≤ T_A ≤ +125°C	102			dB
		R_L = 600 Ω, V_O = −10 V to +10 V	108	117		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		3		µV/°C
Input Resistance, Differential Mode	R_{INDM}			1.5		MΩ
Input Resistance, Common Mode	R_{INCM}			500		MΩ
Input Capacitance, Differential Mode	C_{INDM}			2.4		pF
Input Capacitance, Common Mode	C_{INCM}			2.1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	12.8	13		V
		−40°C ≤ T_A ≤ +125°C	12.5			V
		R_L = 600 Ω to GND	12.4	12.8		V
		−40°C ≤ T_A ≤ +125°C	12			V
		V_{SY} = ±18 V, R_L = 600 Ω to GND	15	15.8		V
		−40°C ≤ T_A ≤ +125°C	14			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		−14	−13.6	V
		−40°C ≤ T_A ≤ +125°C			−13	V
		R_L = 600 Ω to GND		−13.6	−13	V
		−40°C ≤ T_A ≤ +125°C			−12.5	V
		V_{SY} = ±18 V, R_L = 600 Ω to GND		−16.6	−16	V
		−40°C ≤ T_A ≤ +125°C			−15	V
Short-Circuit Current	I_{SC}			40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V	100	104		dB
		−40°C ≤ T_A ≤ +125°C	95			dB
Supply Current per Amplifier	I_{SY}	V_{SY} = ±4.5 V to ±18 V, I_O = 0 mA		1.8	2.25	mA
		−40°C ≤ T_A ≤ +125°C			3.35	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, A_V = 1		12		V/µs
Settling Time	t_S	To 0.01%, V_{IN} = 10 V step, R_L = 1 kΩ		3		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 35 pF, A_V = 1		6.5		MHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 35 pF, A_V = 1		60		Degrees
THD + NOISE						
Total Harmonic Distortion and Noise	THD + N	R_L = 2 kΩ, A_V = 1, V_{IN} = 3 V rms, f = 1 kHz		0.0002		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		60		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.2		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±20 V
Input Voltage	$\pm V_{SY}$
Input Current[1]	±10 mA
Differential Input Voltage	±1.2 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	158	43	°C/W
8-Lead LFCSP	115	40	°C/W

POWER SEQUENCING

The op amp supplies must be established simultaneously with, or before, any input signals are applied. If this is not possible, limit the input current to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

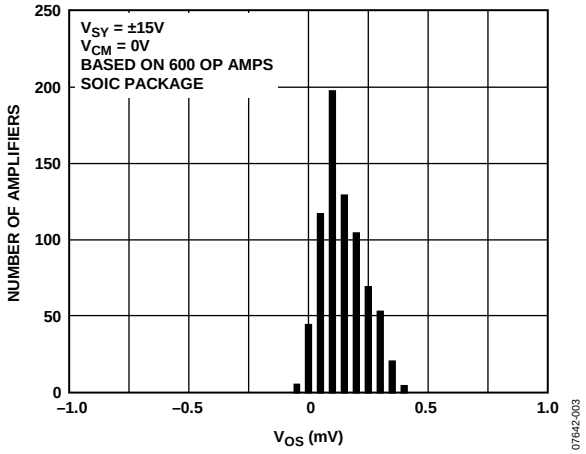

Figure 3. Input Offset Voltage Distribution

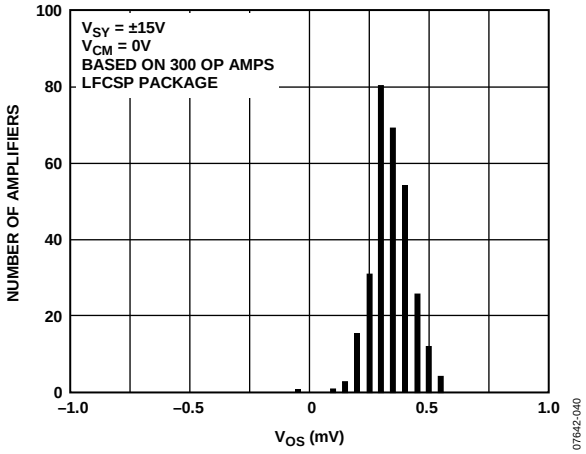

Figure 4. Input Offset Voltage Distribution

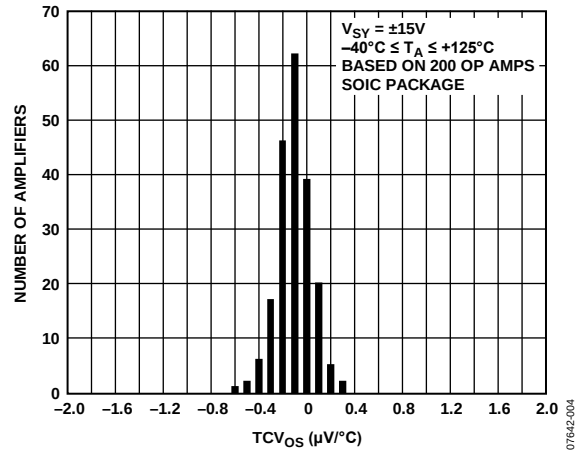

Figure 5. Input Offset Voltage Drift Distribution

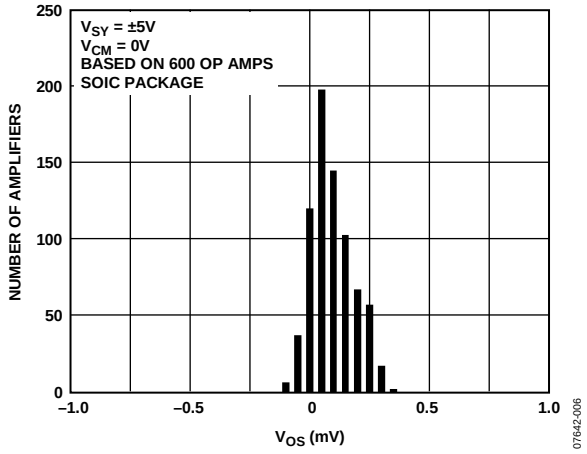

Figure 6. Input Offset Voltage Distribution

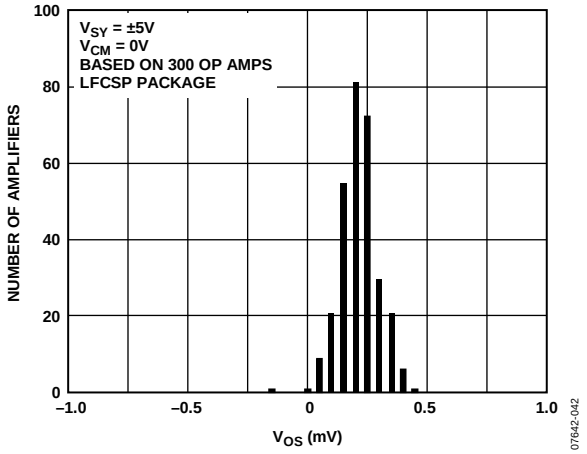

Figure 7. Input Offset Voltage Distribution

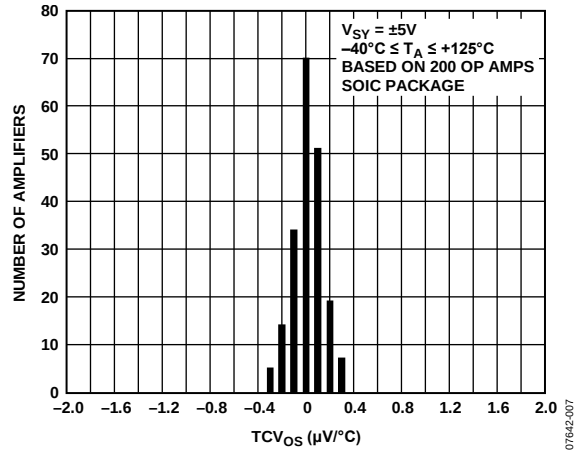

Figure 8. Input Offset Voltage Drift Distribution

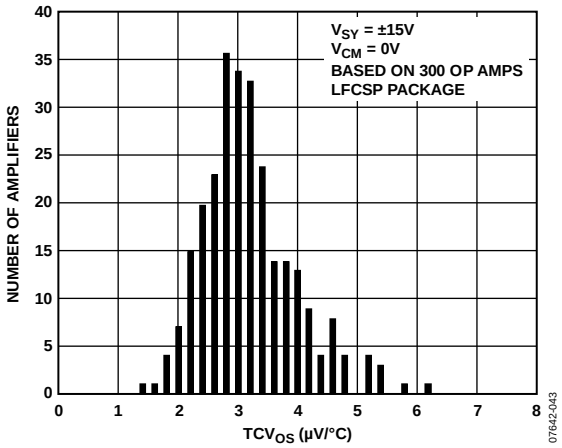

Figure 9. Input Offset Voltage Drift Distribution

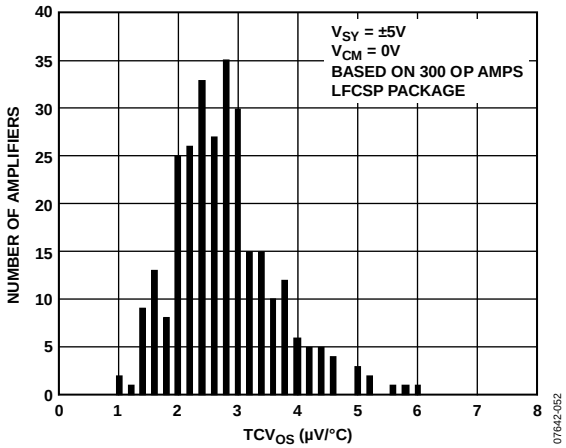

Figure 12. Input Offset Voltage Drift Distribution

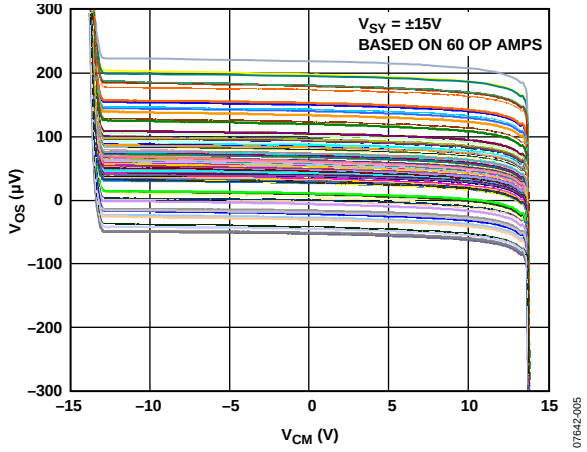

Figure 10. Input Offset Voltage vs. Common-Mode Voltage

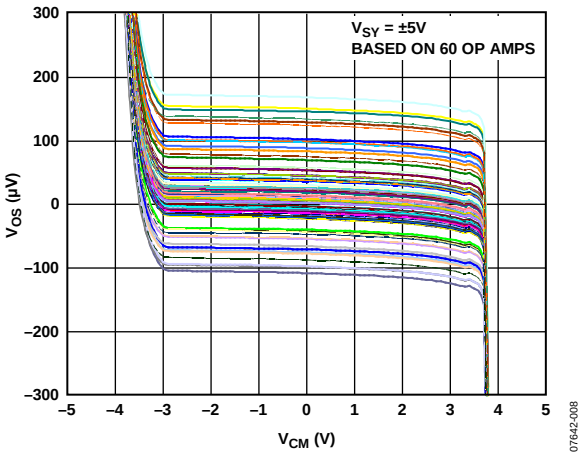

Figure 13. Input Offset Voltage vs. Common-Mode Voltage

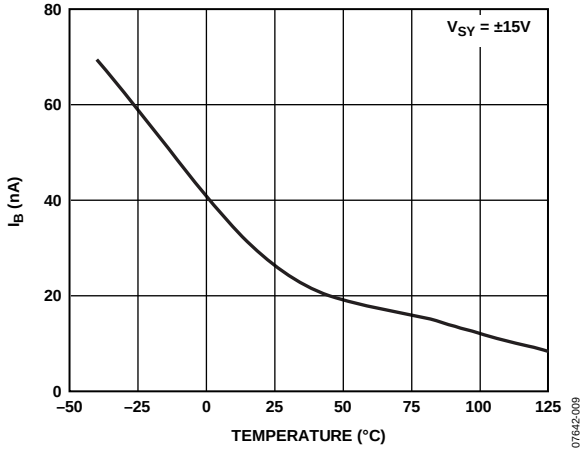

Figure 11. Input Bias Current vs. Temperature

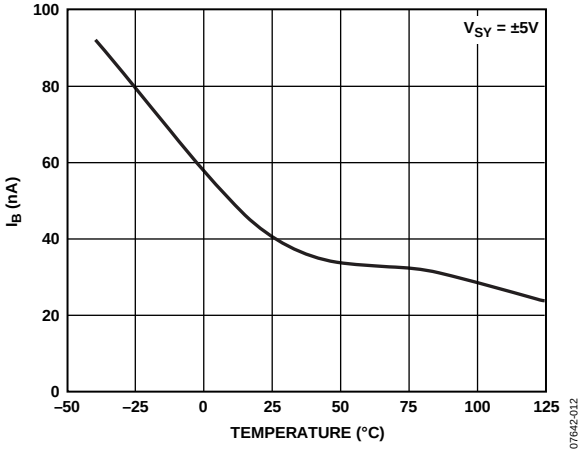

Figure 14. Input Bias Current vs. Temperature

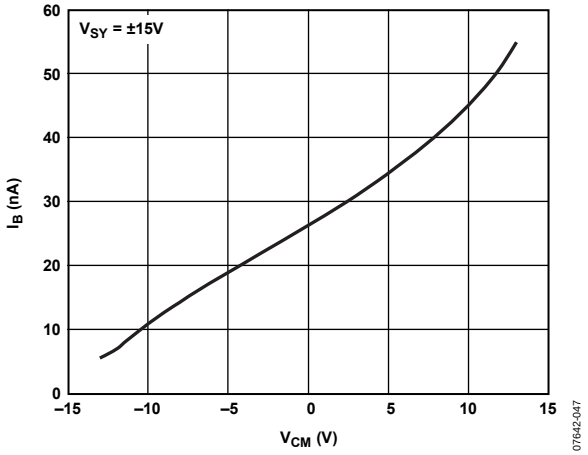

Figure 15. Input Bias Current vs. Input Common-Mode Voltage

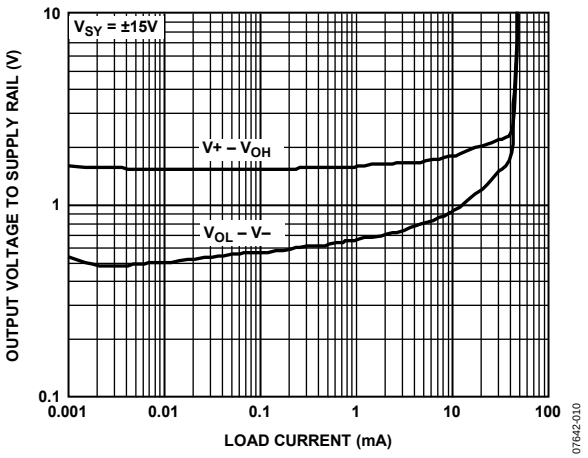

Figure 16. Output Voltage to Supply Rail vs. Load Current

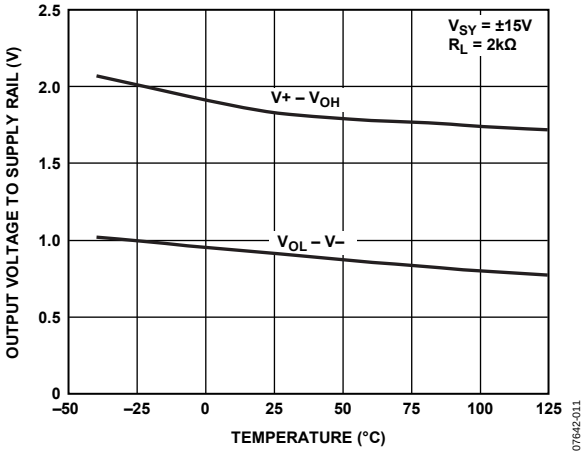

Figure 17. Output Voltage to Supply Rail vs. Temperature

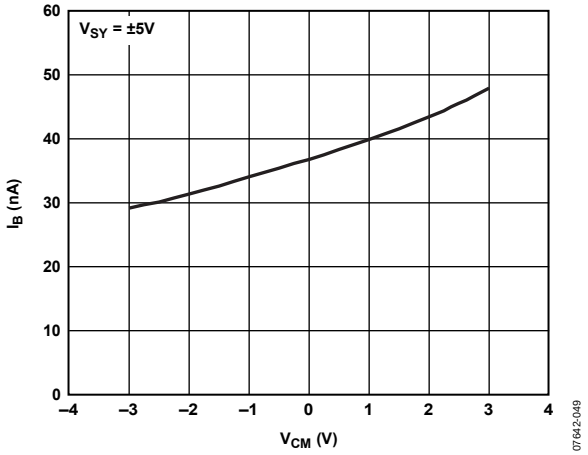

Figure 18. Input Bias Current vs. Input Common-Mode Voltage

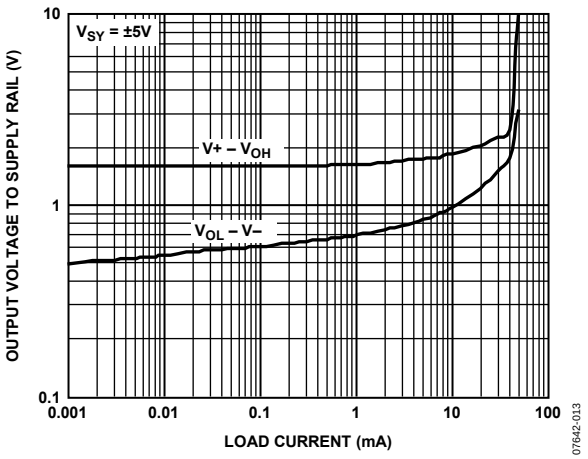

Figure 19. Output Voltage to Supply Rail vs. Load Current

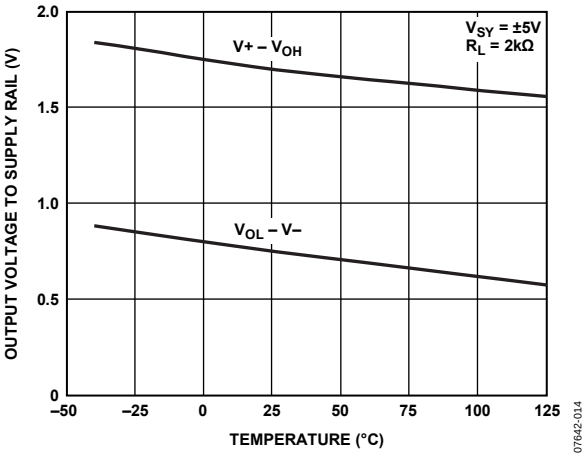

Figure 20. Output Voltage to Supply Rail vs. Temperature

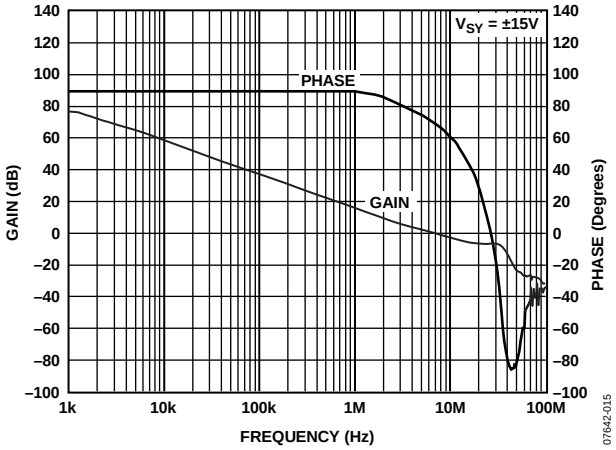

Figure 21. Open-Loop Gain and Phase vs. Frequency

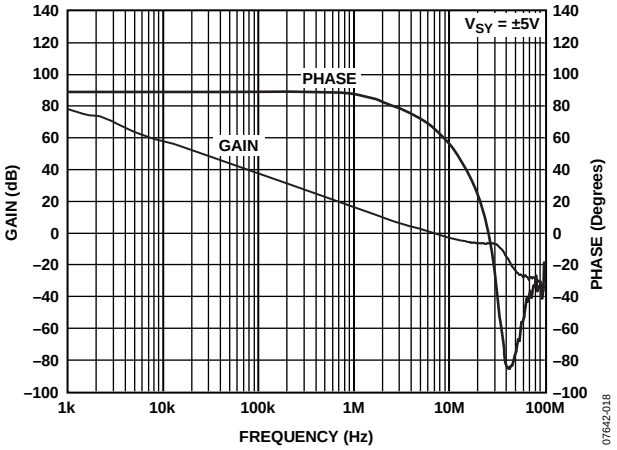

Figure 24. Open-Loop Gain and Phase vs. Frequency

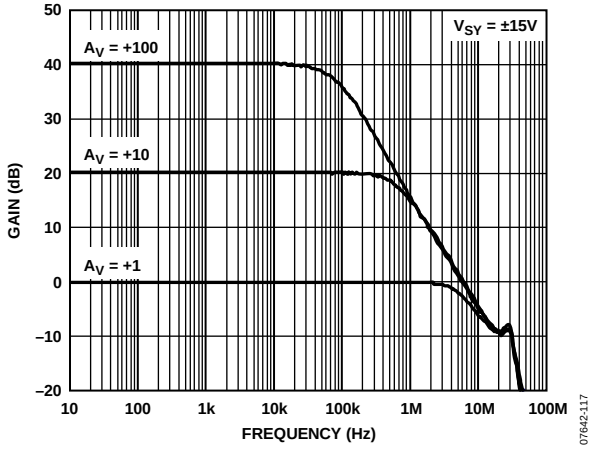

Figure 22. Closed-Loop Gain vs. Frequency

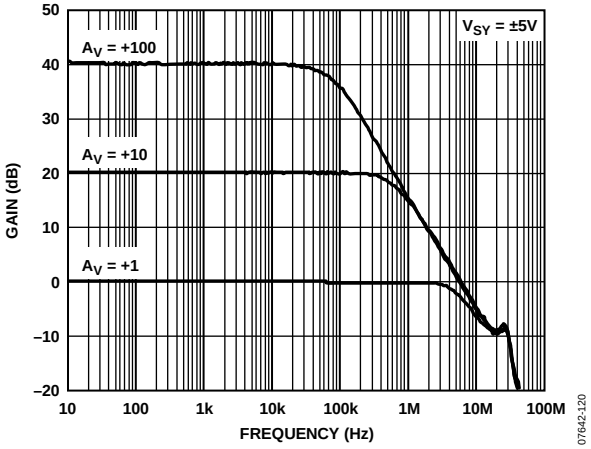

Figure 25. Closed-Loop Gain vs. Frequency

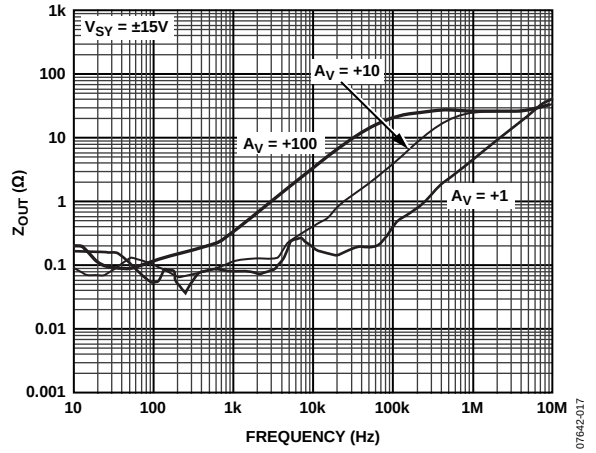

Figure 23. Output Impedance vs. Frequency

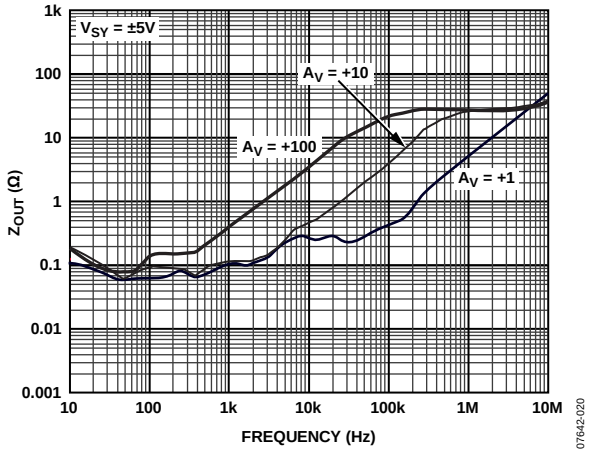

Figure 26. Output Impedance vs. Frequency

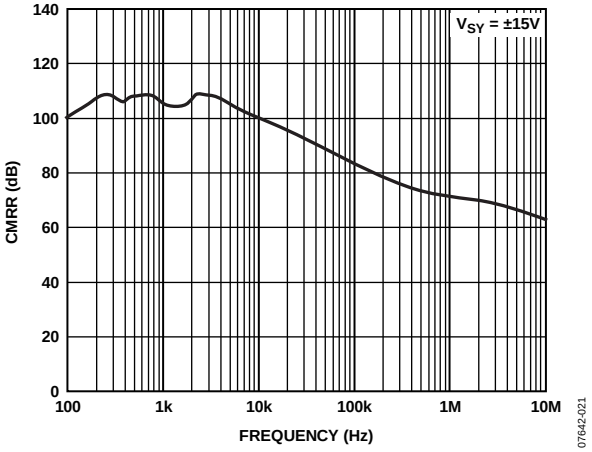

Figure 27. CMRR vs. Frequency

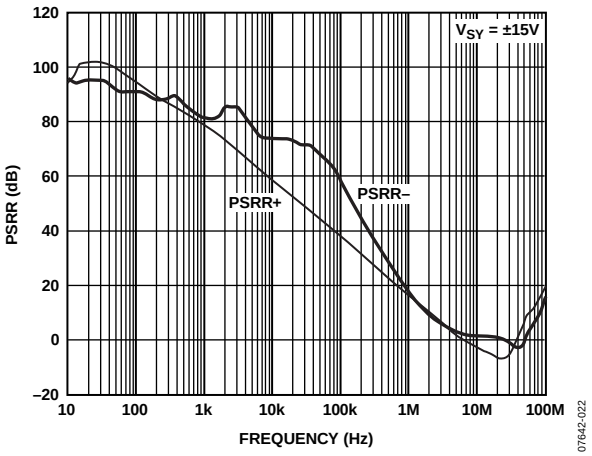

Figure 28. PSRR vs. Frequency

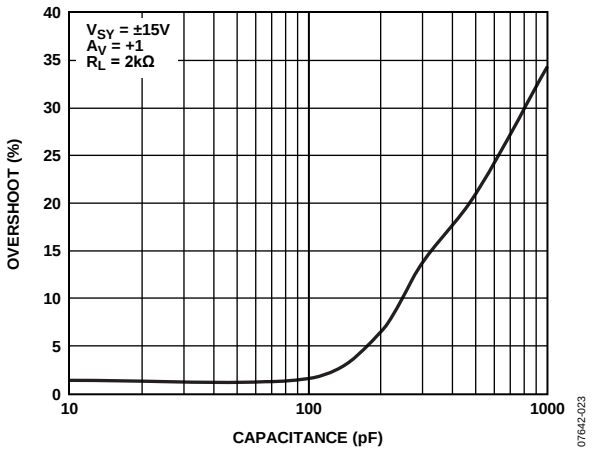

Figure 29. Small Signal Overshoot vs. Load Capacitance

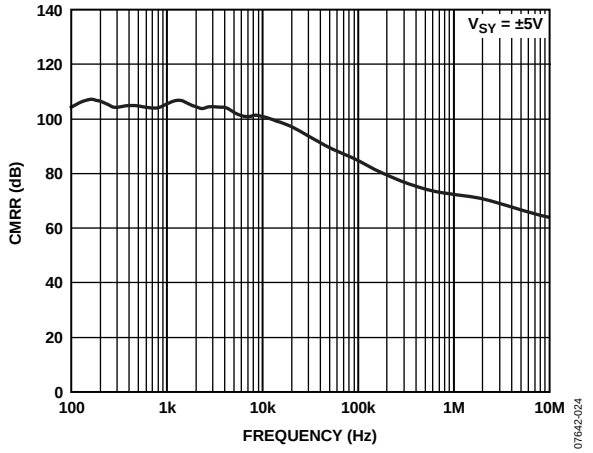

Figure 30. CMRR vs. Frequency

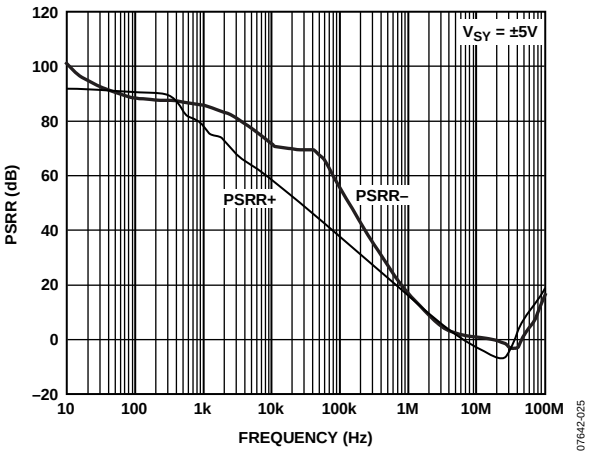

Figure 31. PSRR vs. Frequency

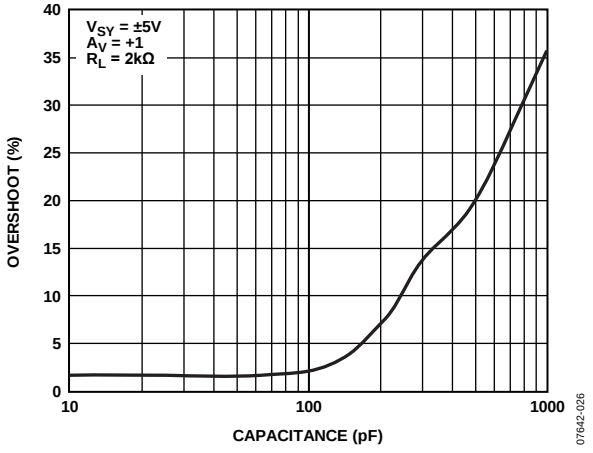

Figure 32. Small Signal Overshoot vs. Load Capacitance

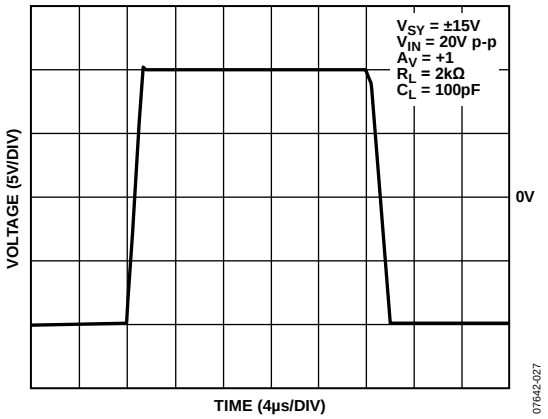

Figure 33. Large Signal Transient Response

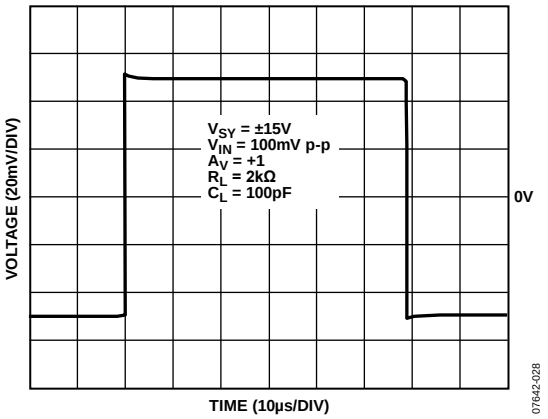

Figure 34. Small Signal Transient Response

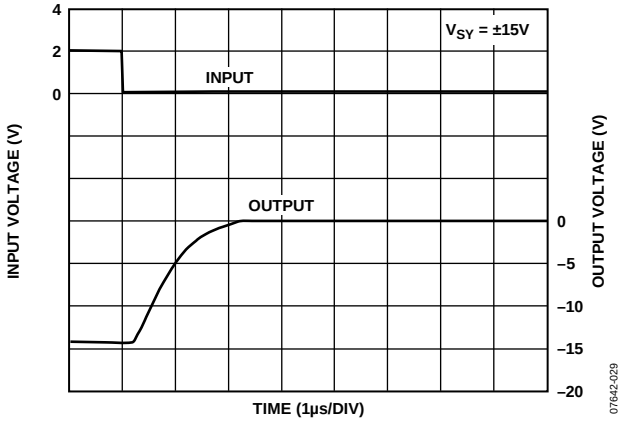

Figure 35. Negative Overload Recovery

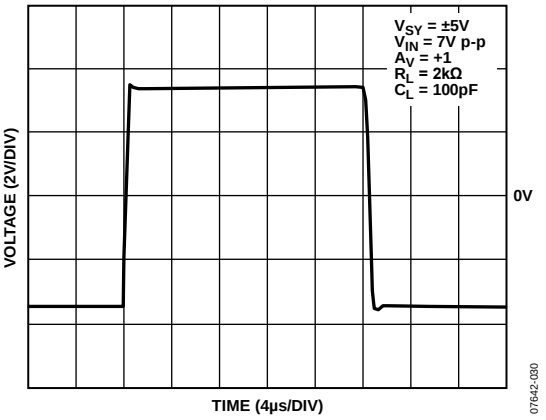

Figure 36. Large Signal Transient Response

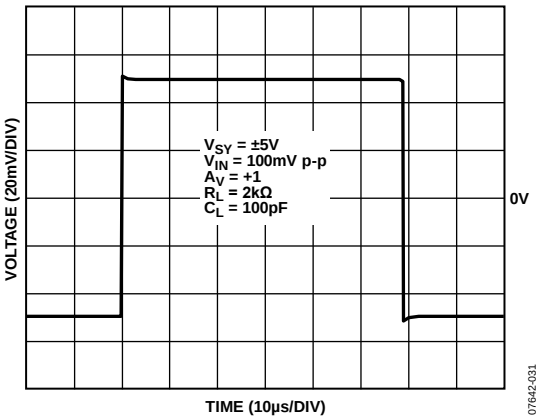

Figure 37. Small Signal Transient Response

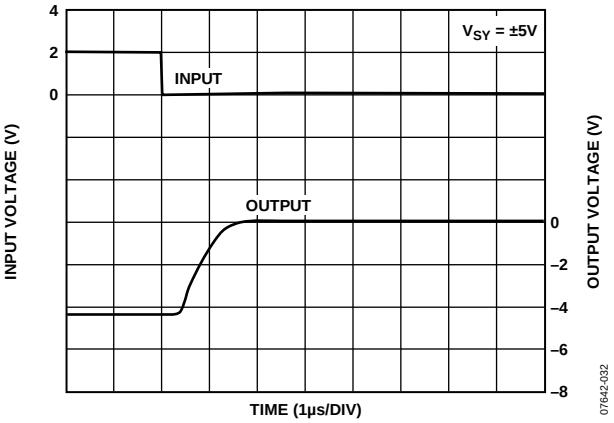

Figure 38. Negative Overload Recovery

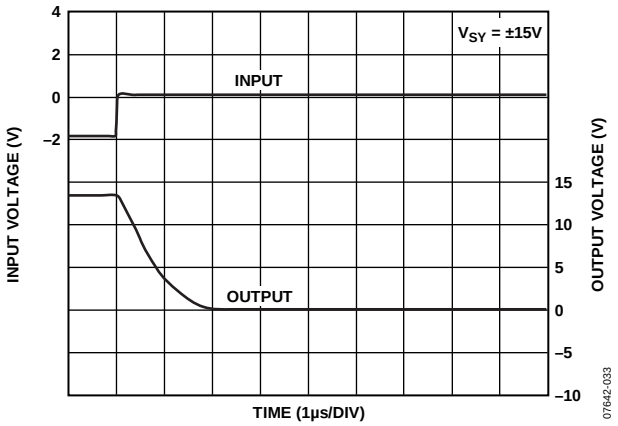

Figure 39. Positive Overload Recovery

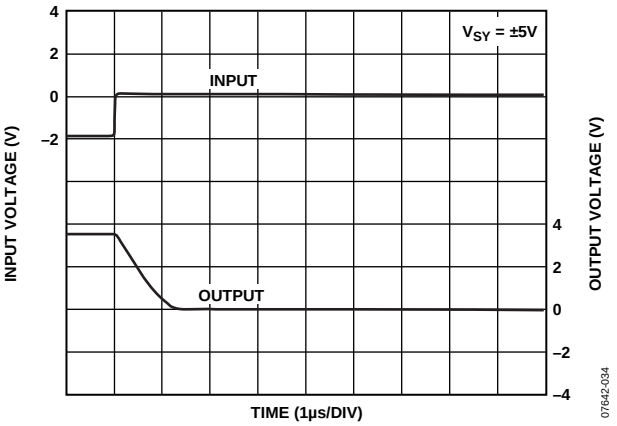

Figure 42. Positive Overload Recovery

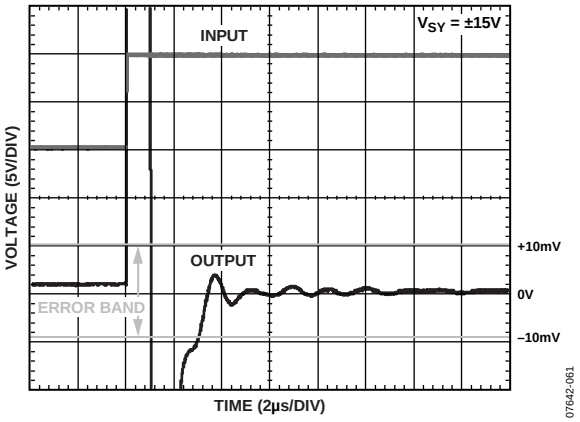

Figure 40. Positive Settling Time to 0.01%

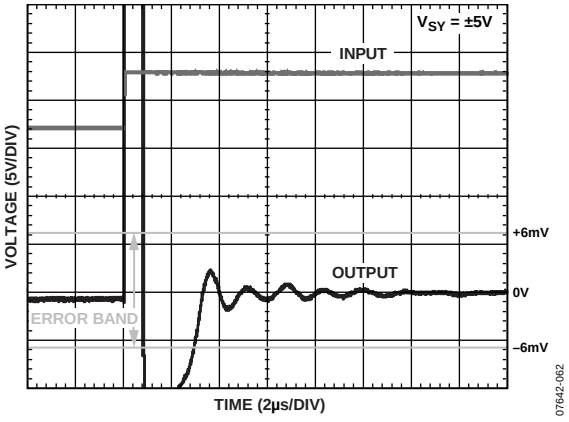

Figure 43. Positive Settling Time to 0.01%

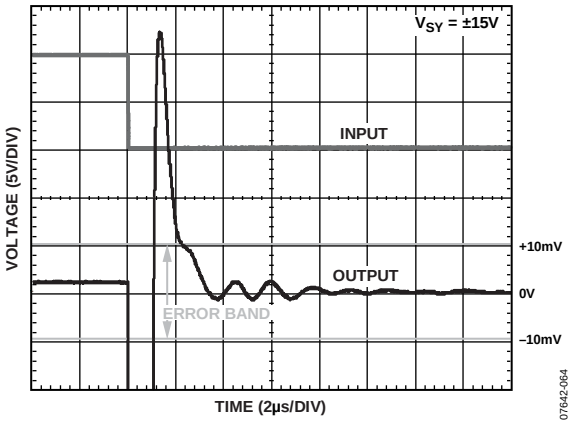

Figure 41. Negative Settling Time to 0.01%

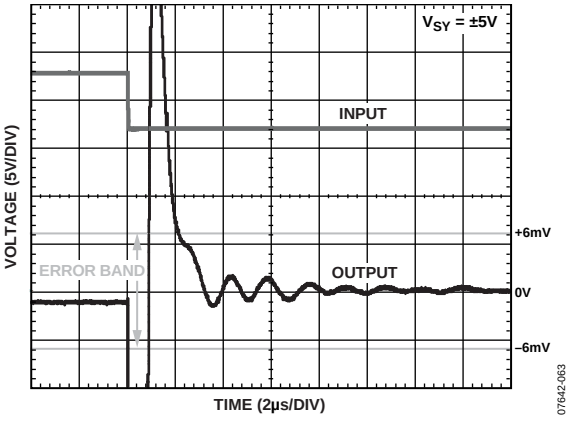

Figure 44. Negative Settling Time to 0.01%

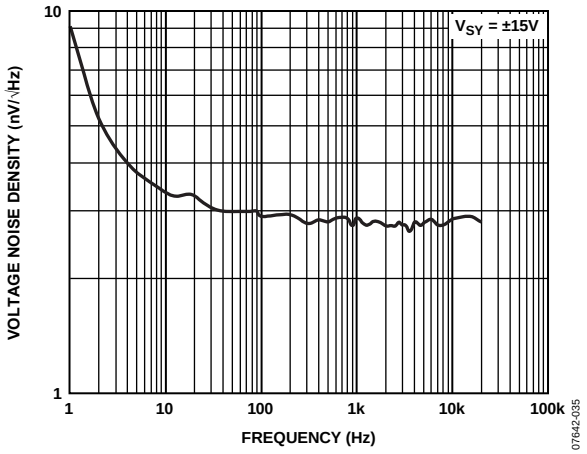

Figure 45. Voltage Noise Density

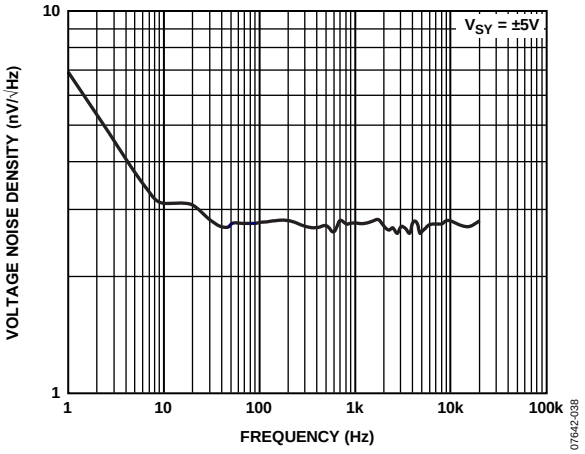

Figure 48. Voltage Noise Density

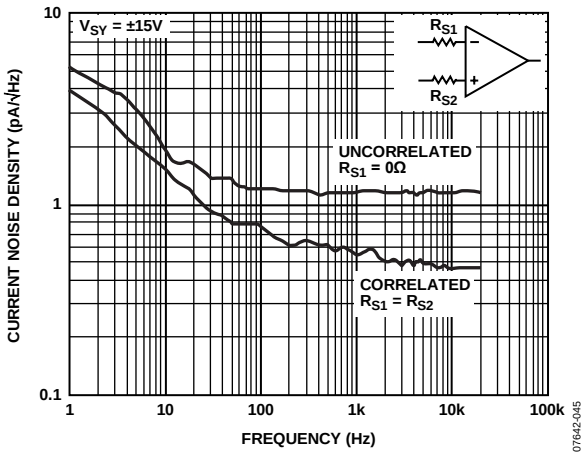

Figure 46. Current Noise Density

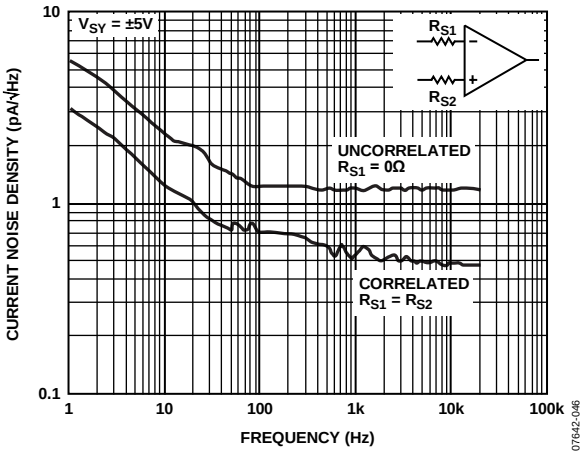

Figure 49. Current Noise Density

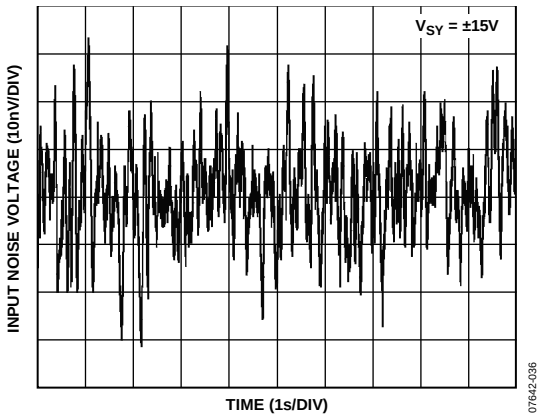

Figure 47. 0.1 Hz to 10 Hz Noise

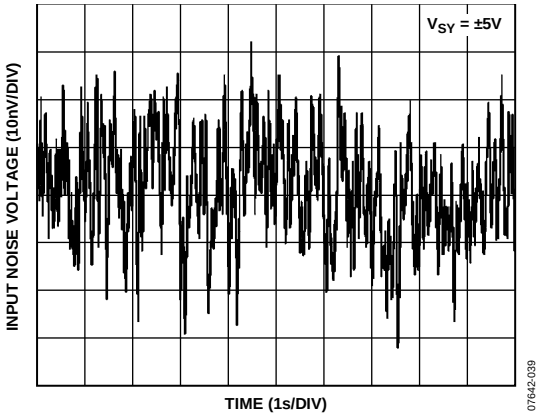

Figure 50. 0.1 Hz to 10 Hz Noise

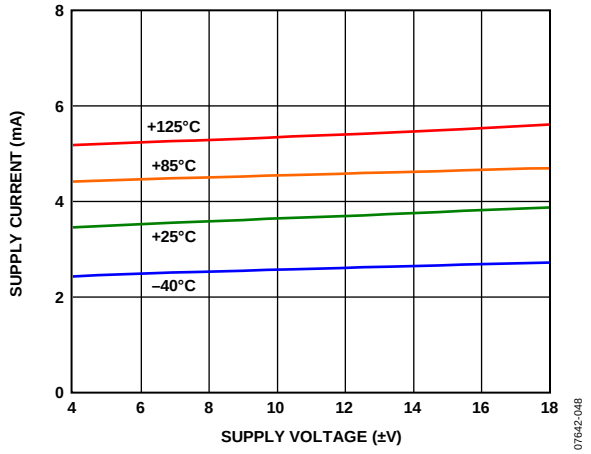

Figure 51. Supply Current vs. Supply Voltage

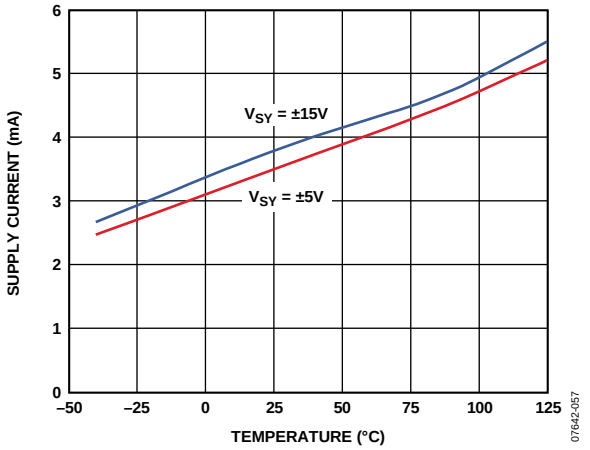

Figure 54. Supply Current vs. Temperature

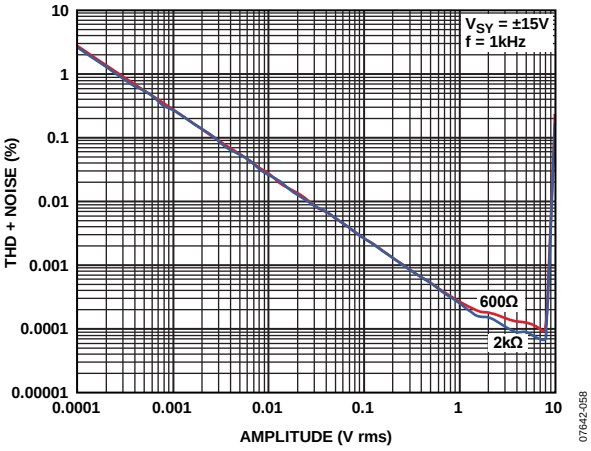

Figure 52. THD + Noise vs. Amplitude

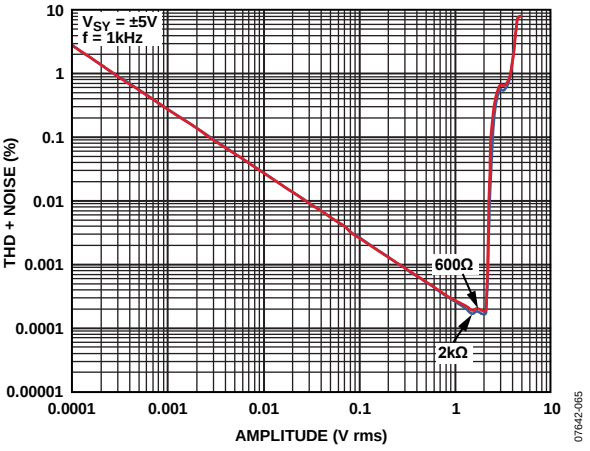

Figure 55. THD + Noise vs. Amplitude

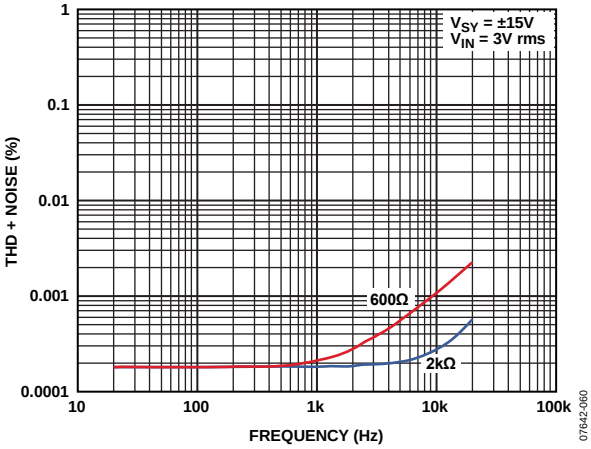

Figure 53. THD + Noise vs. Frequency

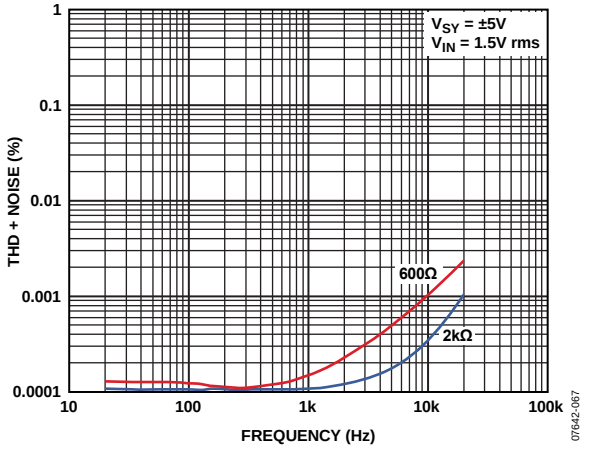

Figure 56. THD + Noise vs. Frequency

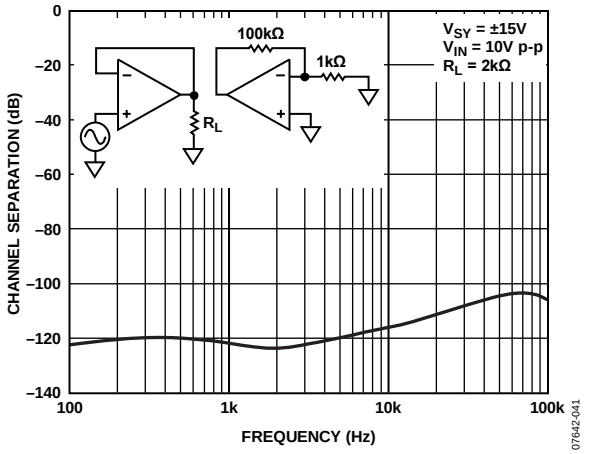

Figure 57. Channel Separation vs. Frequency

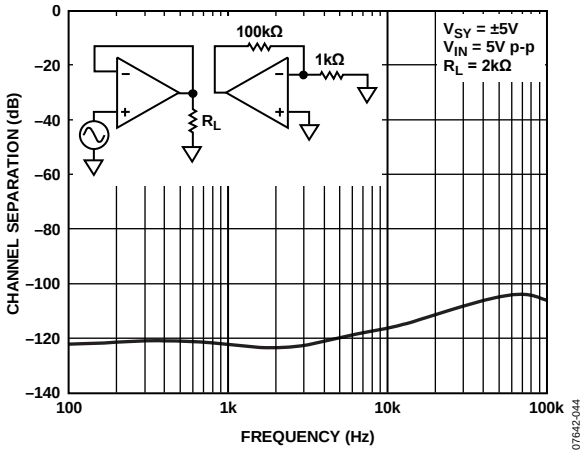

Figure 60. Channel Separation vs. Frequency

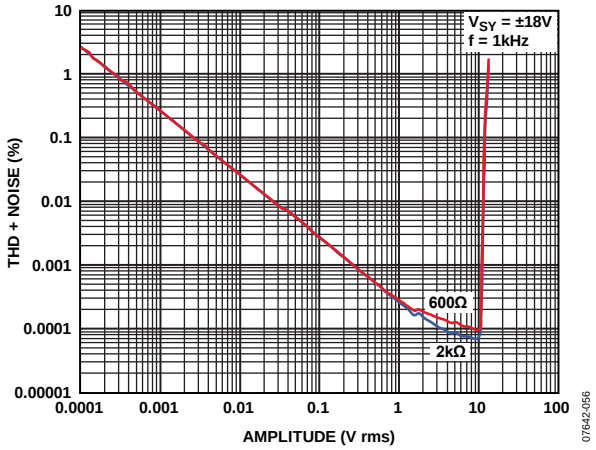

Figure 58. THD + Noise vs. Amplitude

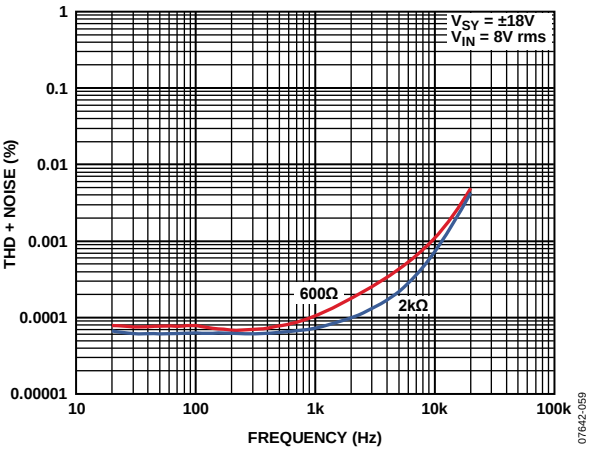

Figure 61. THD + Noise vs. Frequency

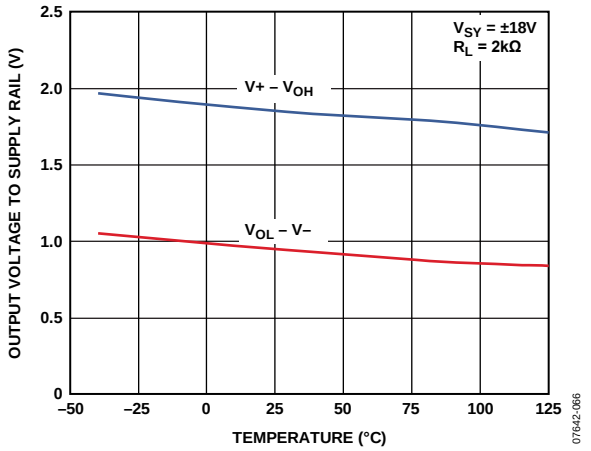

Figure 59. Output Voltage to Supply Rail vs. Temperature

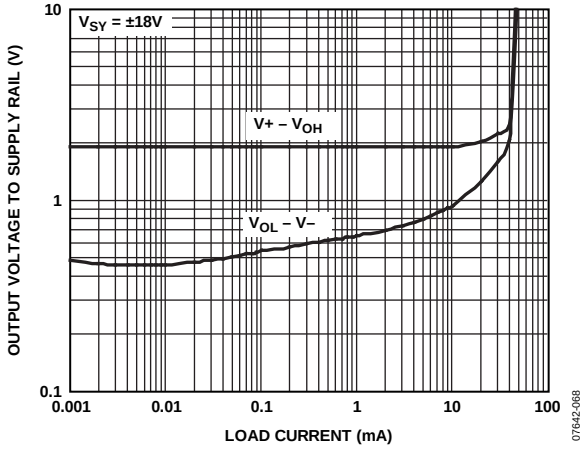

Figure 62. Output Voltage to Supply Rail vs. Load Current

APPLICATIONS INFORMATION

INPUT PROTECTION

To prevent base-emitter junction breakdown from occurring in the input stage of the ADA4075-2 when a very large differential voltage is applied, the inputs are clamped by the internal diodes to ±1.2 V. To preserve the ultralow voltage noise feature of the ADA4075-2, the commonly used internal current-limiting resistors in series with the inputs are not used.

In small signal applications, current limiting is not required; however, in applications where the differential voltage of the ADA4075-2 exceeds ±1.2 V, large currents may flow through these diodes. Employ external current-limiting resistors as shown in Figure 63 to reduce the input currents to less than ±10 mA. Note that depending on the value of these resistors, the total voltage noise will most likely be degraded. For example, a 1 kΩ resistor at room temperature has a thermal noise of 4 nV/√Hz, whereas the ADA4075-2 has an ultralow voltage noise of only 2.8 nV/√Hz typical.

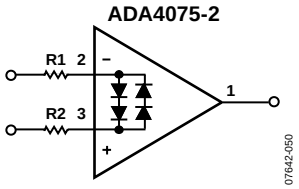

Figure 63. Input Protection

TOTAL HARMONIC DISTORTION

The total harmonic distortion + noise (THD + N) of the ADA4075-2 is 0.0002% typical with a load resistance of 2 kΩ. Figure 64 shows the performance of the ADA4075-2 driving a 2 kΩ load with supply voltages of ±4 V and ±15 V. Notice that there is more distortion for the supply voltage of ±4 V than for a supply voltage of ±15 V. Therefore, it is important to operate the ADA4075-2 at a supply voltage greater than ±5 V for optimum distortion. The THD + noise graphs for supply voltages of ±5 V and ±18 V are available in Figure 56 and Figure 61.

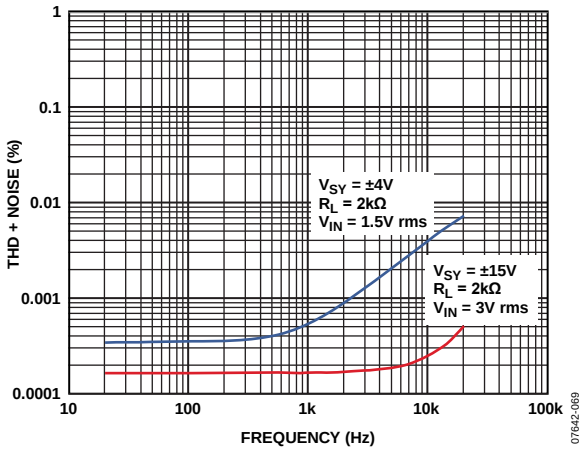

Figure 64. THD + Noise vs. Frequency

PHASE REVERSAL

An undesired phenomenon, phase reversal (also known as phase inversion) occurs in many op amps when one or both of the inputs are driven beyond the specified input common-mode voltage (V_{ICM}) range, in effect reversing the polarity of the output. In some cases, phase reversal can induce lockups and cause equipment damage as well as self destruction.

The ADA4075-2 incorporates phase reversal prevention circuitry that clamps the output to 2 V typical from the supply rails when one or both inputs exceed the V_{ICM} range. Figure 65 shows the input/output waveforms of the ADA4075-2 configured as a unity-gain buffer for a supply voltage of ±15 V.

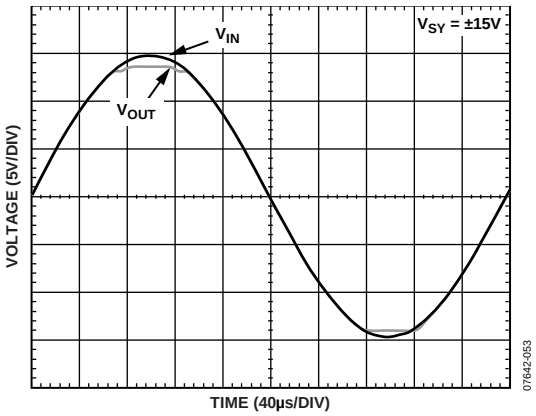

Figure 65. No Phase Reversal

DAC OUTPUT FILTER

The ultralow voltage noise, low distortion, and high slew rate of the ADA4075-2 make it an ideal choice for professional audio signal processing. Figure 66 shows the ADA4075-2 used in a typical audio DAC output filter configuration. The differential outputs of the DAC are fed into the ADA4075-2. The ADA4075-2 is configured as a differential Sallen-Key filter. It operates as an external low-pass filter to remove high frequency noise present on the output pins of the DAC. It also provides differential-to-single-ended conversion from the differential outputs of the DAC.

For a DAC output filter, an op amp with reasonable slew rate and bandwidth is required. The ADA4075-2 has a high slew rate of the 12 V/µs and a relatively wide bandwidth of 6.5 MHz. The cutoff frequency of the low-pass filter is approximately 167 kHz. In addition, the 100 kΩ – 47 µF RC network provides ac coupling to block out the dc components at the output.

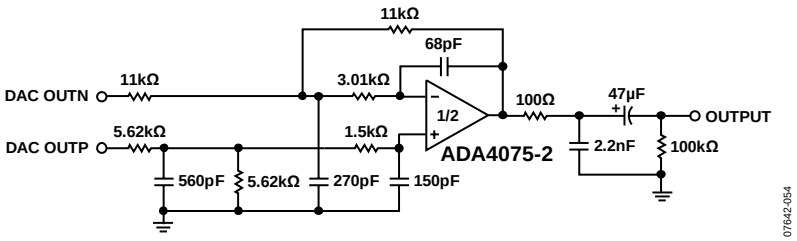

Figure 66. Typical DAC Output Filter Circuit (Differential)

BALANCED LINE DRIVER

The circuit of Figure 67 shows a balanced line driver designed for audio use. Such drivers are intended to mimic an output transformer in operation, whereby the common-mode voltage can be impressed by the load. Furthermore, either output can be shorted to ground in single-ended applications without affecting the overall operation.

Circuits of this type use positive and negative feedback to obtain a high common-mode output impedance, and they are somewhat notorious for component sensitivity and susceptibility to latch-up. This circuit uses several techniques to avoid spurious behavior.

First, the 4-op-amp arrangement ensures that the input impedance is load independent (the input impedance can become negative with some configurations). Note that the output op amps are packaged with the input op amps to maximize drive capability.

Second, the positive feedback is ac-coupled by C2 and C3, which eliminates the need for offset trim. Because the circuit is ac-coupled at the input, these capacitors do not have significant dc voltage across them, thus tantalum types of capacitors can be used.

Finally, even with these precautions, it is vital that the positive feedback be accurately controlled. This is partly achieved by using 1% resistors. In addition, the following setup procedure ensures that the positive feedback does not become excessive:

1. Set R11 to its midposition (or short the ends together, whichever is easier) and temporarily short the negative output to ground.
2. Apply a 10 V p-p sine wave at approximately 1 kHz to the input and adjust R7 to provide 930 mV p-p at TEST (see Figure 67).
3. Remove the short from the negative output (and across R11, if used) and adjust R11 until the output waveforms are symmetric.

The overall gain of the driver is equal to 2, which provides an extra 6 dB of headroom in balanced differential mode. The output noise is about −109 dBV in a 20 kHz bandwidth.

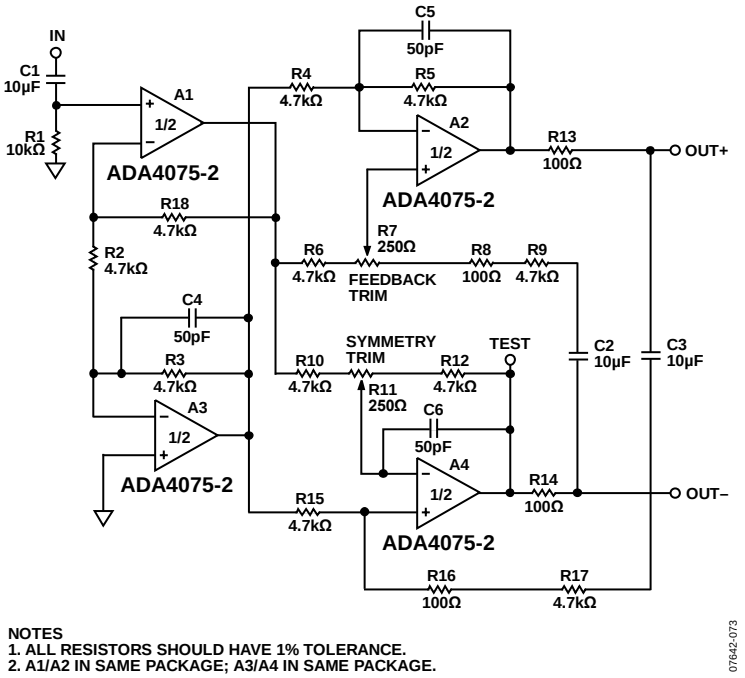

Figure 67. Balanced Line Driver

BALANCED LINE RECEIVER

Figure 68 depicts a unity-gain balanced line receiver capable of a high degree of hum rejection. The CMRR is approximately given by

$$20 \log_{10} \left| \frac{R_1 R_4 + 2R_3 R_4 + R_2 R_3}{2(R_1 R_4 - R_2 R_3)} \right|$$

Therefore, R1 to R4 should be close tolerance components to obtain the best possible CMRR without adjustment. The presence of A2 ensures that the impedances are symmetric at the two inputs (unlike many other designs), and, as a bonus, A2 also provides a complementary output. A3 raises the common-mode input impedance from approximately 7.5 kΩ to approximately 70 kΩ, reducing the degradation of CMRR due to mismatches in source impedance.

Note that A3 is not in the signal path, and almost any op amp works well here. Although it may seem as though the inverting output should be noisier than the noninverting one, they are in fact symmetric at about −111 dBV (20 kHz bandwidth).

Sometimes an overall gain of ½ is desired to provide an extra 6 dB of differential input headroom. This can be attained by reducing R3 and R4 to 5 kΩ and increasing R9 to 22 kΩ.

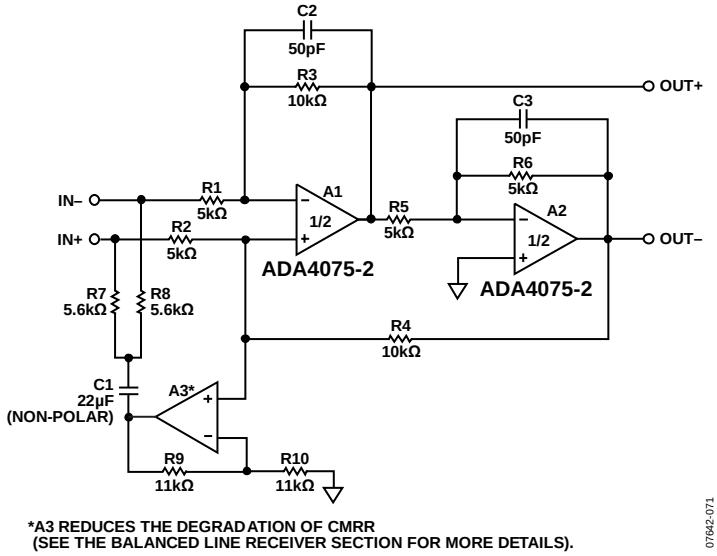

Figure 68. Balanced Line Receiver

LOW NOISE PARAMETRIC EQUALIZER

The circuit in Figure 69 is a reciprocal parametric equalizer yielding ±20 dB of cut or boost with variable bandwidth and frequency. The frequency control range is 6.9:1, with the geometric mean center frequency conveniently occurring at the midpoint of the potentiometer setting. The center frequency is equal to 48 Hz/Ct, where Ct is the value of C1 and C2 in microfarads.

The bandwidth control adjusts the Q from 0.9 to about 11. The overall noise is setting dependent, but with all controls centered, it is about −104 dBV in a 20 kHz bandwidth. Such a low noise level can obviate the need for a bypass switch in many applications.

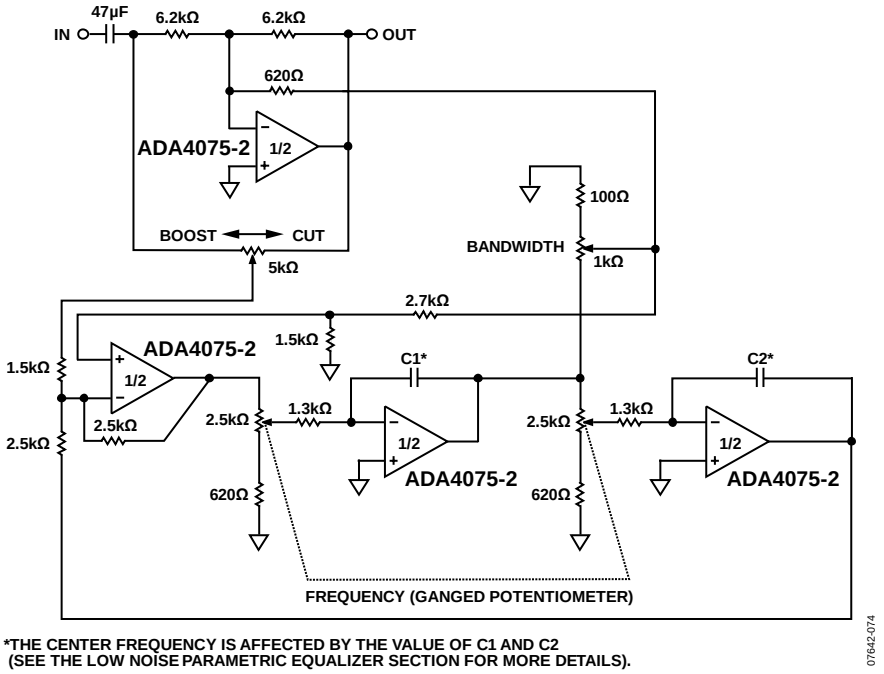

Figure 69. Low Noise Parametric Equalizer

SCHEMATIC

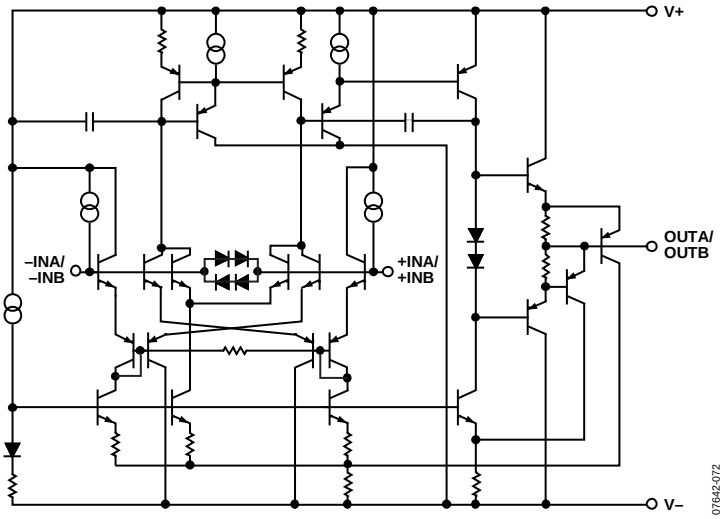

Figure 70. Simplified Schematic

OUTLINE DIMENSIONS

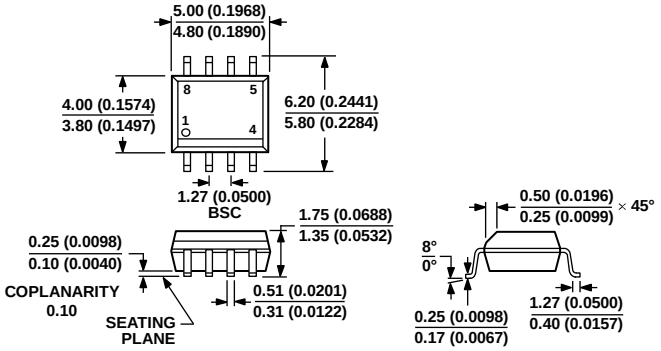

Figure 71. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

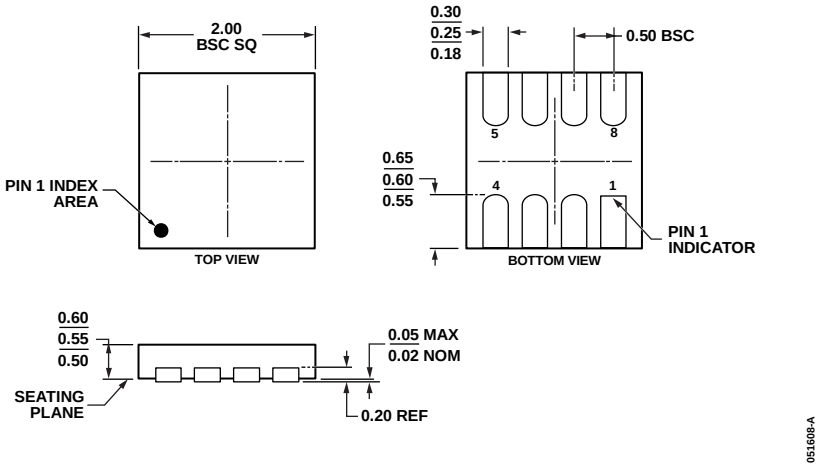

Figure 72. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
2 mm × 2 mm Body, Very Very Thin, Dual Lead
(CP-8-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4075-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4075-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4075-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4075-2ACPZ-R7	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-6	A0
ADA4075-2ACPZ-RL	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-6	A0

[1] Z = RoHS Compliant Part.

NOTES

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Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ADA4075-2ACPZ-R7 on WIN SOURCE
- Analog Devices Inc. Information

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