THE DATASHEET OF

AD5161BRM5

256-Position SPI/I²C Selectable Digital Potentiometer

Data Sheet

AD5161

FEATURES

256-position
End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Compact MSOP-10 (3 mm × 4.9 mm) package
Pin selectable SPI/I²C compatible interface
Extra package address decode pin AD0
Full read/write of wiper register
Power-on preset to midscale
Single supply 2.7 V to 5.5 V
Low temperature coefficient 45 ppm/°C
Low power, I_{DD} = 8 µA
Wide operating temperature −40°C to +125°C
SDO output allows multiple device daisy-chaining
Evaluation board available

APPLICATIONS

Mechanical potentiometer replacement in new designs
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier biasing
Gain control and offset adjustment

FUNCTIONAL BLOCK DIAGRAM

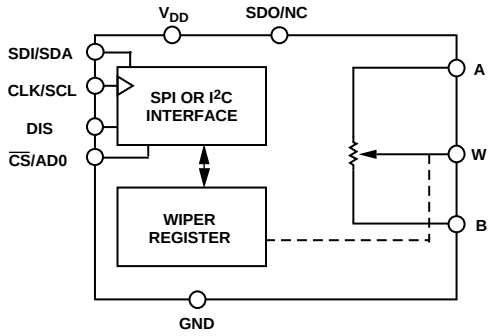

Figure 1.

PIN CONFIGURATION

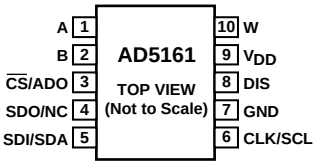

Figure 2.

GENERAL DESCRIPTION

The AD5161 provides a compact 3 mm × 4.9 mm packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The wiper settings are controllable through a pin selectable SPI or I²C compatible digital interface, which can also be used to read back the wiper register content. When the SPI mode is used, the device can be daisy-chained (SDO to SDI), allowing several parts to share the same control lines. In the I²C mode, address pin AD0 can be used to place up to two devices on the same bus. In this same mode, command bits are available to reset the wiper position to midscale or to shut down the device into a state of zero power consumption.

Operating from a 2.7 V to 5.5 V power supply and consuming less than 5 µA allows for usage in portable battery-operated applications.

Rev. C **Document Feedback**

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5/03—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		45		ppm/°C
Wiper Resistance	R_W			50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		−1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−6	−2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth −3dB	BW_5K	R_{AB} = 5 kΩ, Code = 0x80		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, RS = 0		6		nV/√Hz

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = no connect		45		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−3	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth −3dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV/√Hz

TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = +5V ± 10%, or +3V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS[6, 10] (Specifications Apply to All Parts)						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns
I^2C INTERFACE TIMING CHARACTERISTICS[6, 11] (Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES
[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.
[10] See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[11] See timing diagrams for locations of measured values.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Value
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
I_{MAX}[1]	±20 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2]	
θ_{JA} (10-Lead MSOP)	200°C/W

NOTES

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

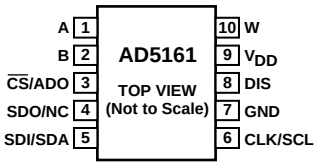


Figure 3. Pin Configuration

Table 5. Pin Function Description

Pin No.	Mnemonic	Description
1	A	A Terminal.
2	B	B Terminal.
3	$\overline{CS}$/AD0	Chip Select ($\overline{CS}$) Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the DAC register. Programmable address bit 0 (AD0) for multiple package decoding.
4	SDO/NC	Serial Data Output (SDO). Open-drain transistor requires pull-up resistor. No Connect (NC).
5	SDI/SDA	Serial Data Input (SDI). Serial Data Input/Output (SDA).
6	CLK/SCL	Serial Clock Input. Positive edge triggered.
7	GND	Digital Ground.
8	DIS	Digital Interface Select (SPI/I^2C Select). SPI when DIS = 0, I^2C when DIS = 1.
9	V_{DD}	Positive Power Supply.
10	W	W Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

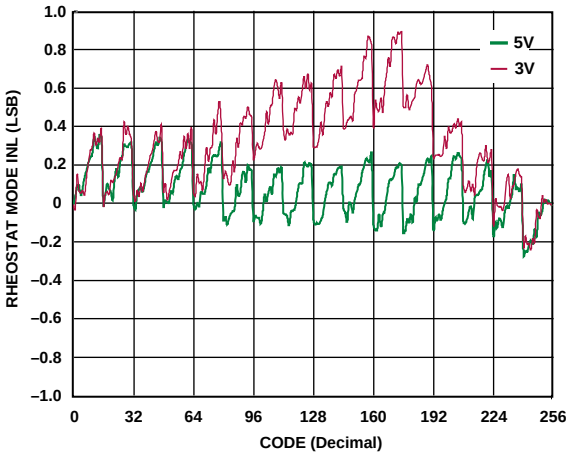


Figure 4. R-INL vs. Code vs. Supply Voltages

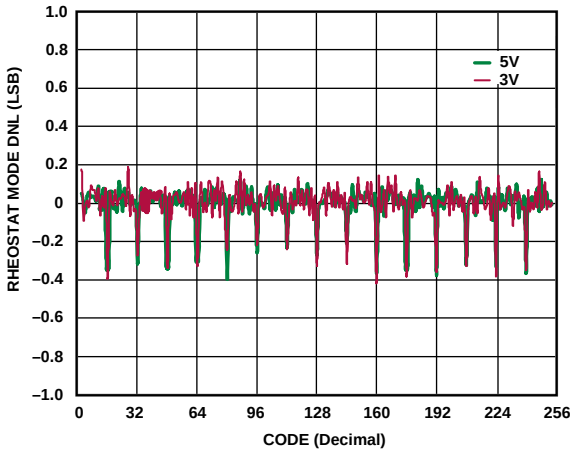


Figure 5. R-DNL vs. Code vs. Supply Voltages

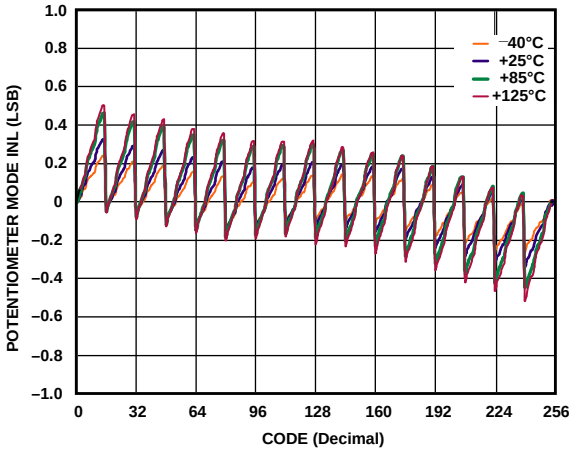


Figure 6. INL vs. Code, V_{DD} = 5 V

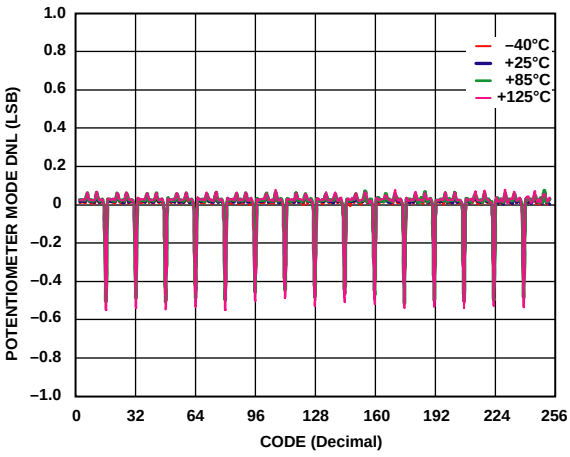


Figure 7. DNL vs. Code, V_{DD} = 5 V

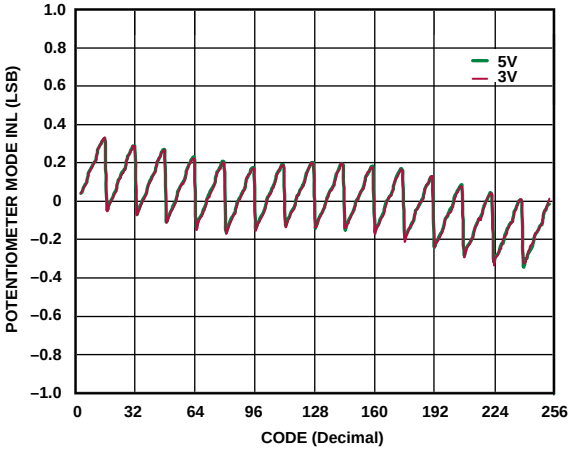


Figure 8. INL vs. Code vs. Supply Voltages

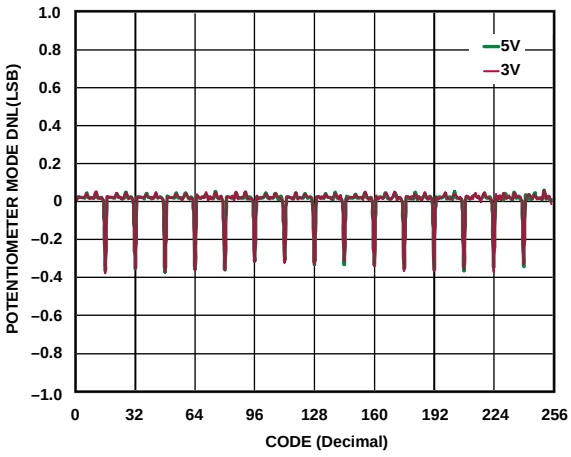


Figure 9. DNL vs. Code vs. Supply Voltages

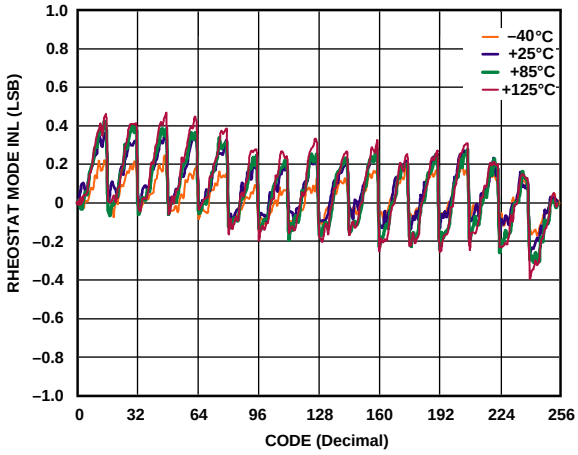


Figure 10. R-INL vs. Code, V_{DD} = 5 V

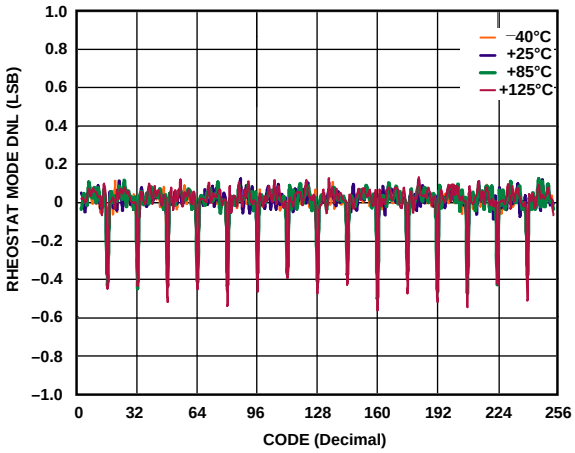


Figure 11. R-DNL vs. Code, V_{DD} = 5 V

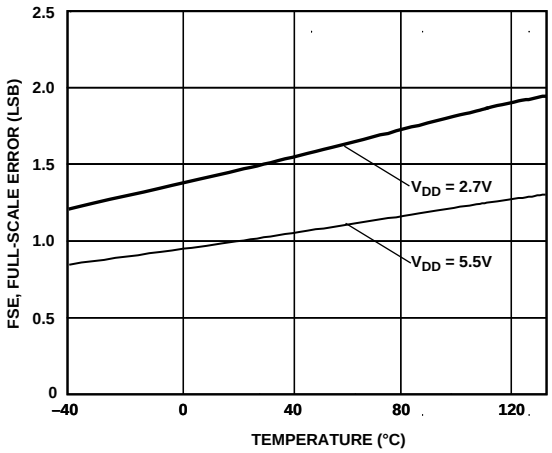


Figure 12. Full-Scale Error vs. Temperature

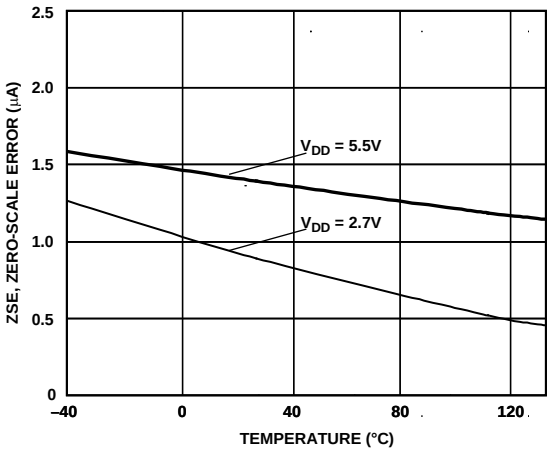


Figure 13. Zero-Scale Error vs. Temperature

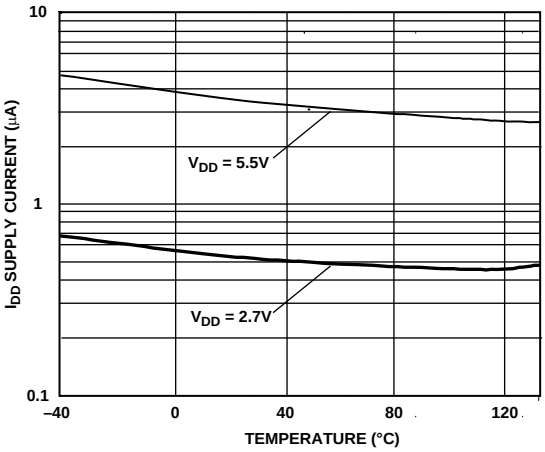


Figure 14. Supply Current vs. Temperature

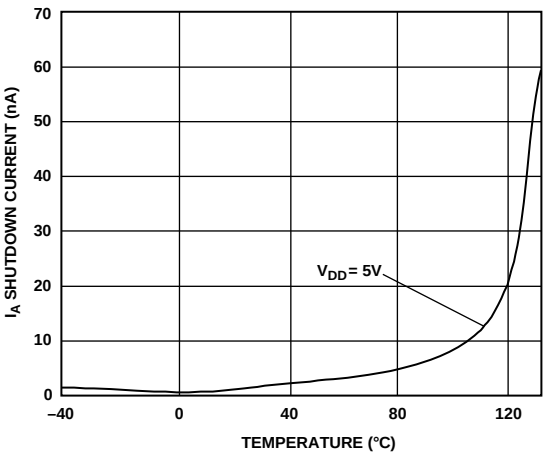


Figure 15. Shutdown Current vs. Temperature

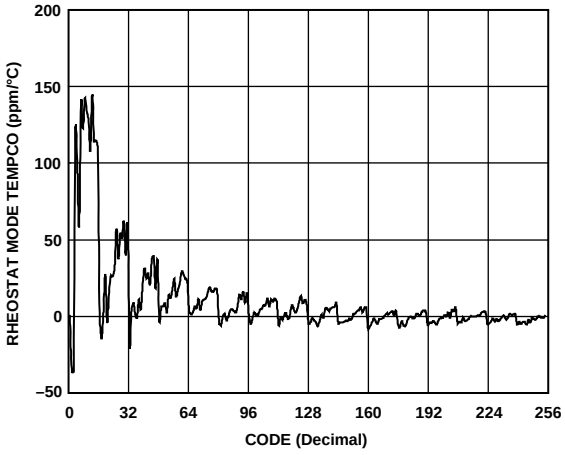


Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

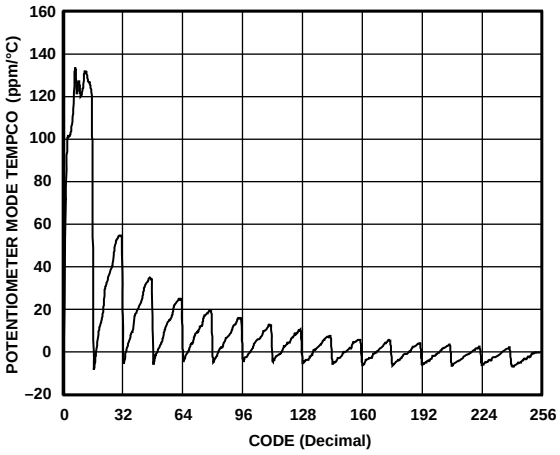


Figure 17. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

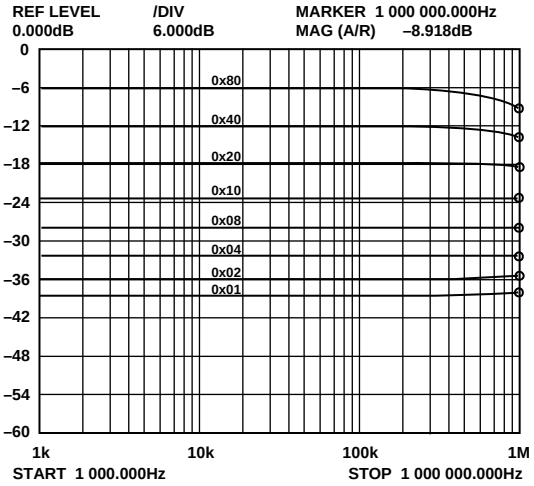


Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

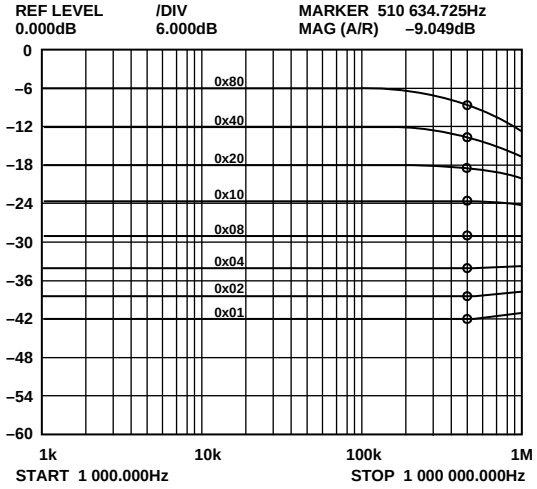


Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

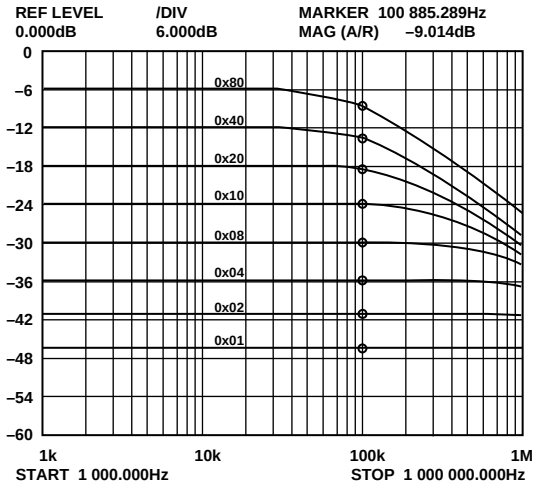


Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

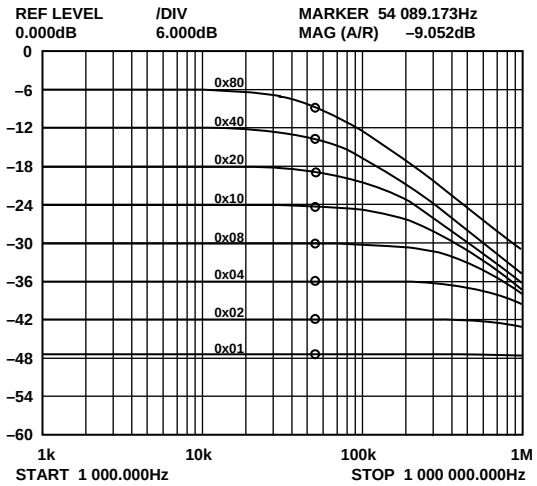


Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

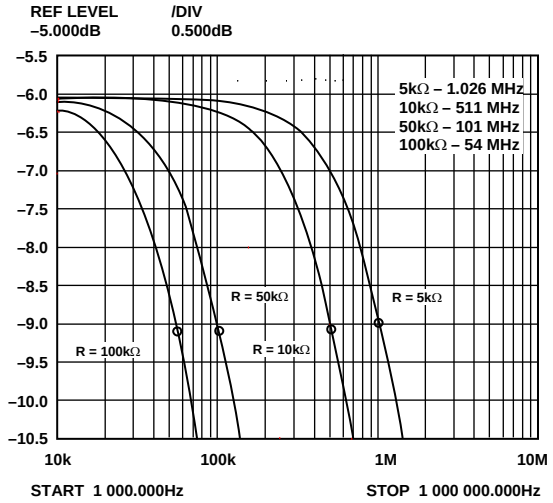


Figure 22. –3 dB Bandwidth @ Code = 0x80

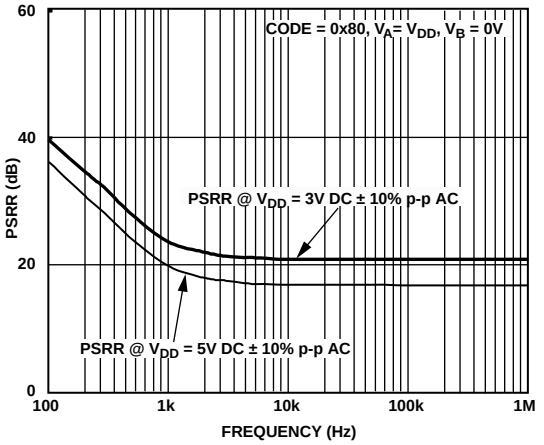


Figure 23. PSRR vs. Frequency

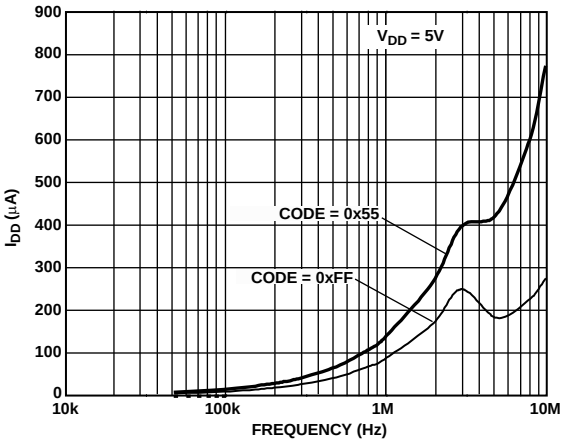


Figure 24. I_{DD} vs. Frequency

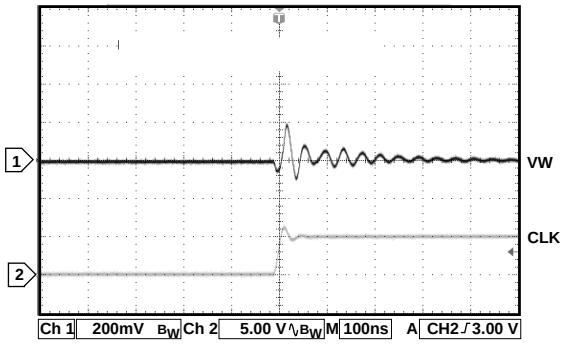


Figure 25. Digital Feedthrough

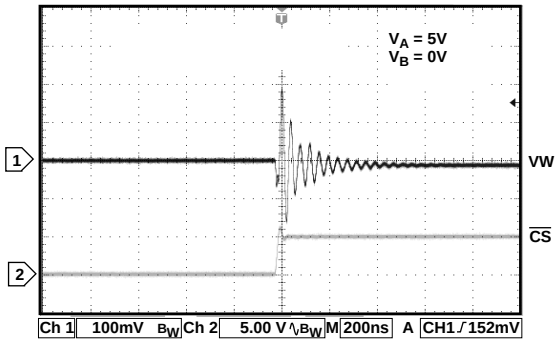


Figure 26. Midscale Glitch, Code 0x80–0x7F

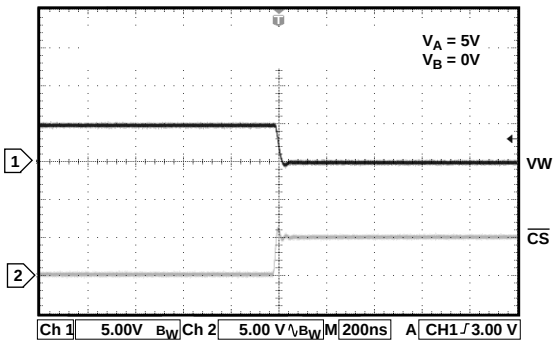


Figure 27. Large Signal Settling Time, Code 0xFF–0x00

TEST CIRCUITS

Figure 28 to Figure 36 illustrate the test circuits that define the test conditions used in the product specification tables.

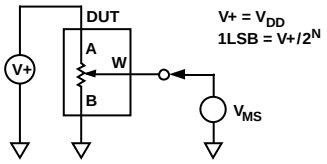


Figure 28. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

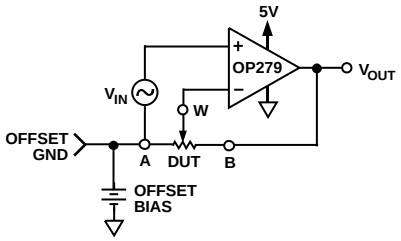


Figure 33. Test Circuit for Noninverting Gain

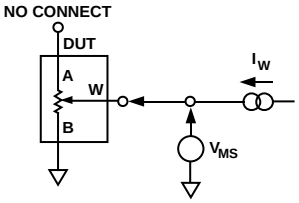


Figure 29. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

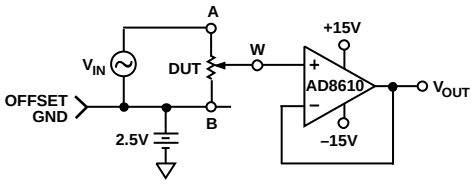


Figure 34. Test Circuit for Gain vs. Frequency

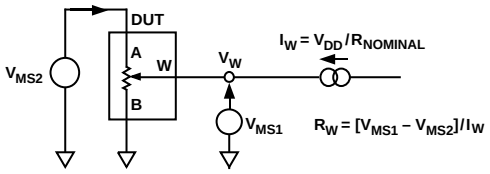


Figure 30. Test Circuit for Wiper Resistance

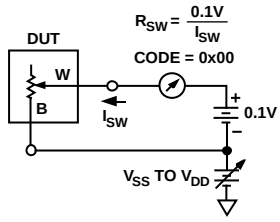


Figure 35. Test Circuit for Incremental ON Resistance

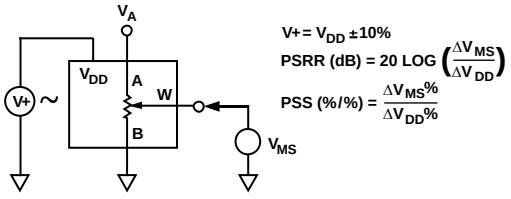


Figure 31. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

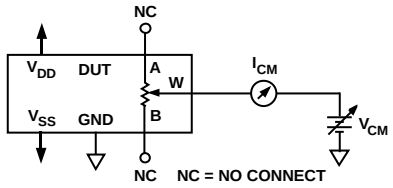


Figure 36. Test Circuit for Common-Mode Leakage Current

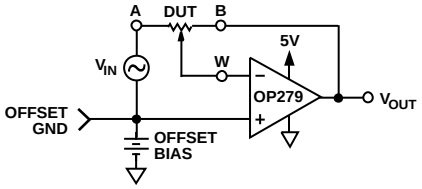


Figure 32. Test Circuit for Inverting Gain

SPI INTERFACE

Table 6. AD5161 Serial Data-Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
2^7							2^0

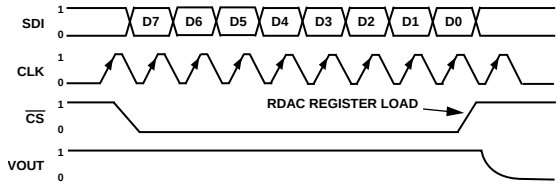


Figure 37. SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

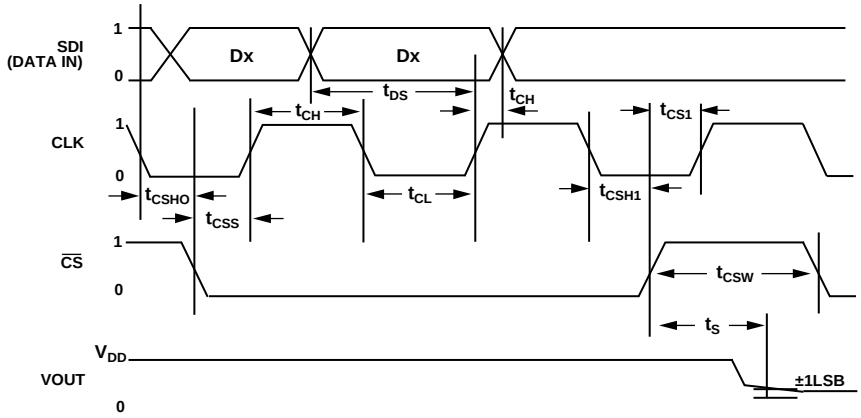


Figure 38. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

I²C INTERFACE

Table 7. Write Mode

S	0	1	0	1	1	0	AD0	$\overline{W}$	A	X	RS	SD	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 8. Read Mode

S	0	1	0	1	1	0	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

S = Start Condition

P = Stop Condition

A = Acknowledge

X = Don't Care

$\overline{W}$ = Write

R = Read

RS = Reset wiper to Midscale 80_H

SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits.

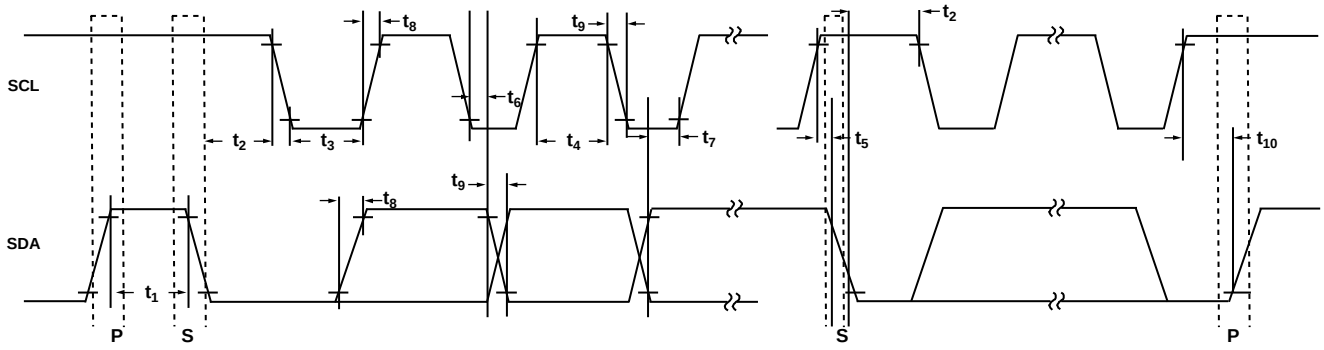


Figure 39. I²C Interface Detailed Timing Diagram

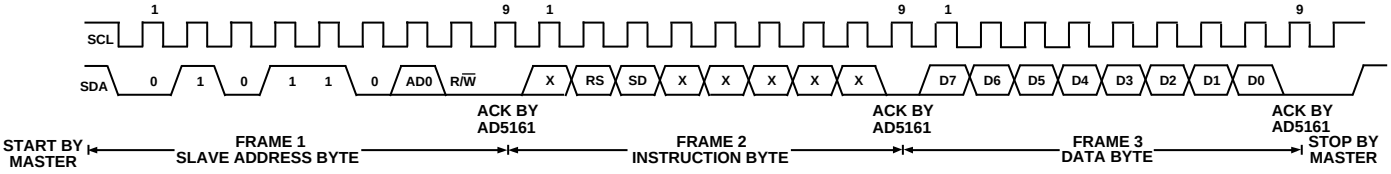


Figure 40. Writing to the RDAC Register

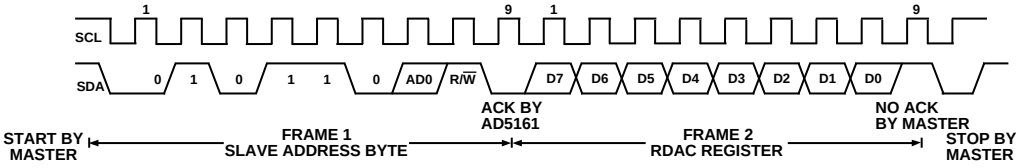


Figure 41. Reading Data from a Previously Selected RDAC Register in Write Mode

THEORY OF OPERATION

The AD5161 is a 256-position digitally controlled variable resistor (VR)[1] device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between Terminals W and B. The second connection is the first tap point, which corresponds to 99 Ω ($R_{WB} = R_{AB}/256 + R_W = 39\ \Omega + 60\ \Omega$) for data 0x01. The third connection is the next tap point, representing 177 Ω ($2 \times 39\ \Omega + 60\ \Omega$) for data 0x02 and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9961 Ω ($R_{AB} - 1$ LSB + R_W). Figure 42 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

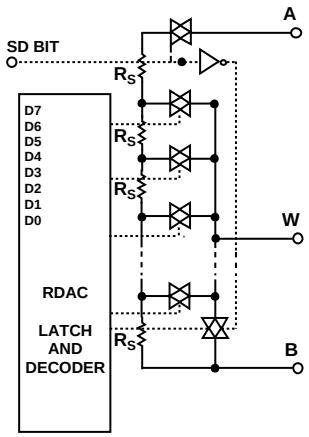


Figure 42. AD5161 Equivalent RDAC Circuit

[1] The terms digital potentiometer, VR, and RDAC are used interchangeably.

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} will be set for the indicated RDAC latch codes.

Table 9. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9,961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5,060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the following output resistance R_{WA} will be set for the indicated RDAC latch codes.

Table 10. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	99	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device to device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W, can be found as

$$V_W(D) = \frac{R_{WB}(D)}{256}V_A + \frac{R_{WA}(D)}{256}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

PIN SELECTABLE DIGITAL INTERFACE

The AD5161 provides the flexibility of a selectable interface. When the digital interface select (DIS) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high, the I²C mode is engaged.

SPI Compatible 3-Wire Serial Bus (DIS = 0)

The AD5161 contains a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table 6.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 37).

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5161 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

Daisy-Chain Operation

The serial data output (SDO) pin contains an open-drain N-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. This allows for daisy-chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be larger than the V_{DD} supply voltage. It is recommended to increase the clock period when using a pull-up resistor to the SDI pin of the following device because capacitive loading at the daisy-chain node SDO-SDI between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see Figure 43). If two AD5161s are daisy-chained, a total of at least 16 bits of data is required. The first eight bits, complying with the format shown in Table 6, go to U2 and the second eight bits with the same format go to U1. $\overline{CS}$ should be kept low until all 16 bits are clocked into their respective serial registers. After this, $\overline{CS}$ is pulled high to complete the operation and load the RDAC latch. If the data word during the $\overline{CS}$ low period is greater than 16 bits, any additional MSBs will be discarded.

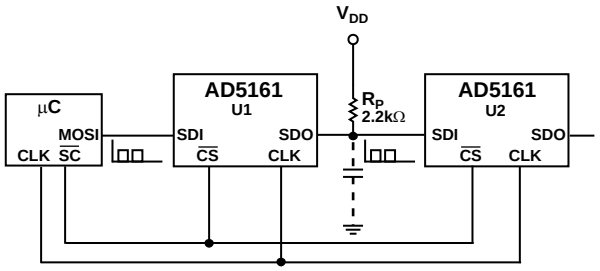


Figure 43. Daisy-Chain Configuration

I²C Compatible 2-Wire Serial Bus (DIS = 1)

The AD5161 can also be controlled via an I²C compatible serial bus with DIS tied high. The RDACs are connected to this bus as slave devices.

The first byte of the AD5161 is a slave address byte (see Table 7 and Table 8). It has a 7-bit slave address and a R/$\overline{W}$ bit. The six MSBs of the slave address are 010110, and the following bit is determined by the state of the AD0 pin of the device. AD0 allows the user to place up to two of the I²C compatible devices on one bus.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 40). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. A write operation contains an extra instruction byte that a read operation does not contain. Such an instruction byte in write mode follows the slave address byte. The first bit (MSB) of the instruction byte is a don't care.

   The second MSB, RS, is the midscale reset. A logic high on this bit moves the wiper to the center tap where $R_{WA} = R_{WB}$. This feature effectively writes over the contents of the register, and thus, when taken out of reset mode, the RDAC will remain at midscale.

   The third MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

   The remainder of the bits in the instruction byte are don't cares (see Table 7).

3. After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table 7).

4. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 41).

5. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 40). In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 41).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the write mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Readback RDAC Value

The AD5161 allows the user to read back the RDAC values in the read mode. Refer to Table 7 and Table 8 for the programming format.

Multiple Devices on One Bus

Figure 44 shows two AD5161 devices on the same serial bus. Each has a different slave address since the states of their AD0 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

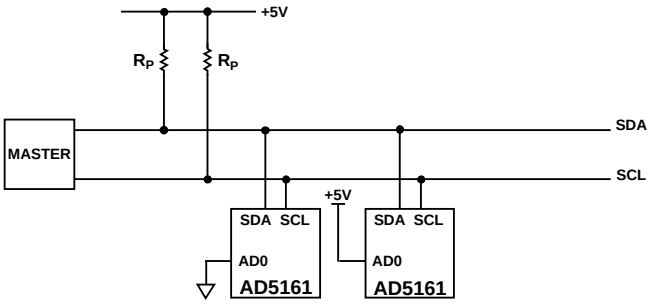


Figure 44. Multiple AD5161 Devices on One I²C Bus

LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3 V E²PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 45 shows one of the implementations. M1 and M2 can be any N-channel signal FETs, or if V_{DD} falls below 2.5 V, low threshold FETs such as the FDV301N.

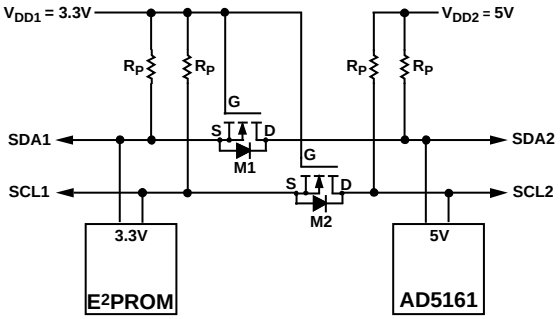


Figure 45. Level Shifting for Operation at Different Potentials

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 46 and Figure 47. This applies to the digital input pins SDI/SDA, CLK/SCL, and $\overline{CS}$/AD0.

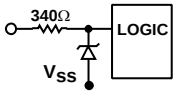


Figure 46. ESD Protection of Digital Pins

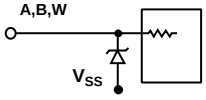


Figure 47. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5161 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or GND will be clamped by the internal forward biased diodes (see Figure 48).

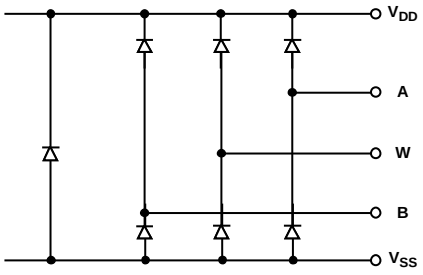


Figure 48. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 48), it is important to power V_{DD}/GND before applying any voltage to terminals A, B, and W; otherwise, the diode will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 49). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

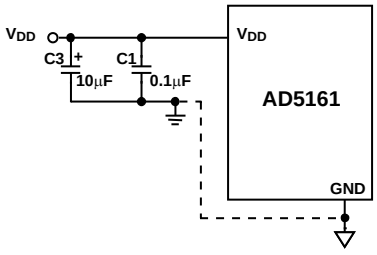
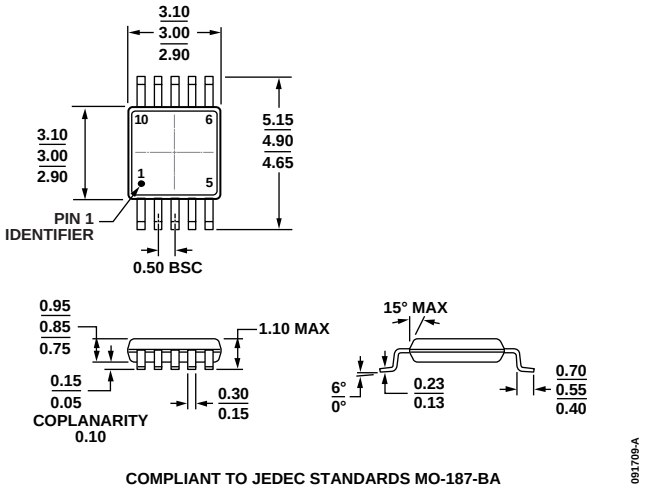


Figure 49. Power Supply Bypassing

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 50. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5161BRMZ5	5k	−40°C to +125°C	10-Lead MSOP	RM-10	D0C#
AD5161BRMZ5-RL7	5k	−40°C to +125°C	10-Lead MSOP	RM-10	D0C#
AD5161BRM10	10k	−40°C to +125°C	10-Lead MSOP	RM-10	D0D
AD5161BRM10-RL7	10k	−40°C to +125°C	10-Lead MSOP	RM-10	D0D
AD5161BRMZ10	10k	−40°C to +125°C	10-Lead MSOP	RM-10	D0D#
AD5161BRMZ10-RL7	10k	−40°C to +125°C	10-Lead MSOP	RM-10	D0D#
AD5161BRM50	50k	−40°C to +125°C	10-Lead MSOP	RM-10	D0E
AD5161BRM50-RL7	50k	−40°C to +125°C	10-Lead MSOP	RM-10	D0E
AD5161BRMZ50	50k	−40°C to +125°C	10-Lead MSOP	RM-10	D0E#
AD5161BRMZ50-RL7	50k	−40°C to +125°C	10-Lead MSOP	RM-10	D0E#
AD5161BRMZ100	100k	−40°C to +125°C	10-Lead MSOP	RM-10	D0F#
AD5161BRMZ100-RL7	100k	−40°C to +125°C	10-Lead MSOP	RM-10	D0F#
EVAL-AD5161DBZ	See Note 2		Evaluation Board		

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.
[2] The EVAL-AD5161DBZ evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

The AD5161 contains 2532 transistors. Die size: 30.7 mil × 76.8 mil = 2358 sq. mil.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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