

FEATURES

- 400 MHz bandwidth
- 2.7 V to 3.3 V power supply
- Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
- Programmable charge pump currents
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode
- 104 MHz phase frequency detector

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: -55°C to $+125^{\circ}\text{C}$
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Clock conditioning
- Clock generation
- IF LO generation

GENERAL DESCRIPTION

The ADF4002-EP frequency synthesizer is used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, and a programmable N divider. The 14-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). In addition, by programming R and N to 1, the part can be used as a stand-alone PFD and charge pump.

Additional application and technical information can be found in the [ADF4002](#) data sheet.

FUNCTIONAL BLOCK DIAGRAM

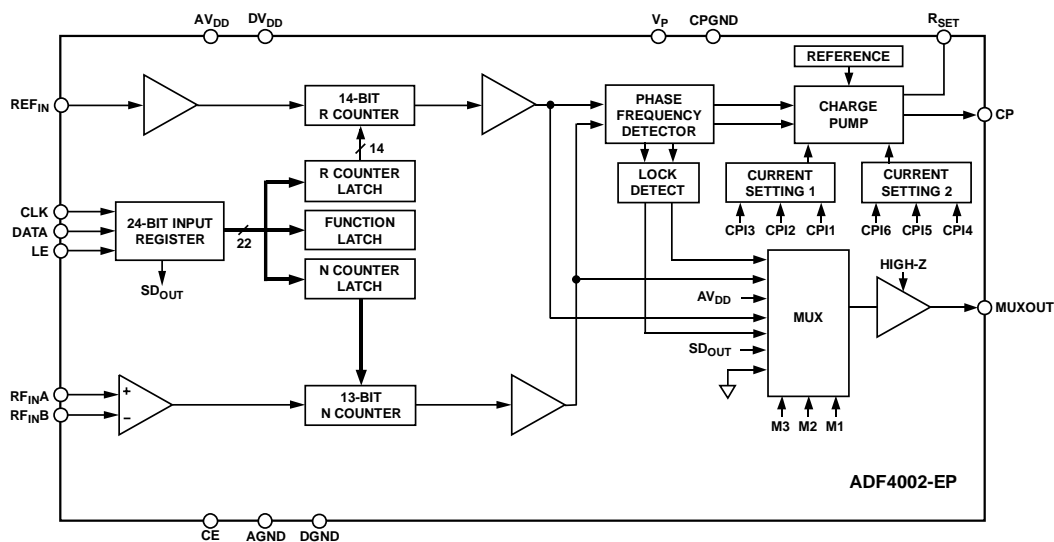


Figure 1.

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Rev. A

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REVISION HISTORY

9/2018—Rev. 0 to Rev. A

| | |
|--|---|
| Changes to Features Section..... | 1 |
| Added Enhanced Product Features Section..... | 1 |
| Changes to Figure 4 and Figure 5..... | 7 |
| Changes to Ordering Guide | 9 |

11/2010—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = 3\text{ V} \pm 10\%$, $AV_{DD} \leq V_P \leq 5.5\text{ V}$, $AGND = DGND = CPGND = 0\text{ V}$, $R_{SET} = 5.1\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MAX}$ to T_{MIN} , unless otherwise noted. Operating temperature range is -55°C to $+125^\circ\text{C}$.

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------------------------|------|------------------|--------|--|
| RF CHARACTERISTICS | | | | | |
| RF Input Sensitivity | -10 | | 0 | dBm | |
| RF Input Frequency (RF _{IN}) | 5 | | 400 | MHz | For RF _{IN} < 5 MHz, ensure slew rate (SR) > 4 V/μs |
| REF _{IN} CHARACTERISTICS | | | | | |
| REF _{IN} Input Frequency | 20 | | 300 | MHz | For REF _{IN} < 20 MHz, ensure SR > 50 V/μs |
| REF _{IN} Input Sensitivity ¹ | 0.8 | | AV _{DD} | V p-p | Biased at AV _{DD} /2 (ac coupling ensures AV _{DD} /2 bias) |
| REF _{IN} Input Capacitance | | | 10 | pF | |
| REF _{IN} Input Current | | | ±100 | μA | |
| PHASE FREQUENCY DETECTOR (PFD) | | | | | |
| Phase Detector Frequency ² | | | 104 | MHz | ABP[2:1] = 00 (2.9 ns antbacklash pulse width) |
| CHARGE PUMP | | | | | |
| I _{CP} Sink/Source | | | | | Programmable |
| High Value | | 5 | | mA | R _{SET} = 5.1 kΩ |
| Low Value | | 625 | | μA | |
| Absolute Accuracy | | 2.5 | | % | R _{SET} = 5.1 kΩ |
| R _{SET} Range | 3.0 | | 11 | kΩ | |
| I _{CP} Three-State Leakage | | 1 | | nA | T _A = 25°C |
| I _{CP} vs. V _{CP} | | 1.5 | | % | 0.5 V ≤ V _{CP} ≤ (V _P - 0.5 V) |
| Sink and Source Current Matching | | 2 | | % | 0.5 V ≤ V _{CP} ≤ (V _P - 0.5 V) |
| I _{CP} vs. Temperature | | 2 | | % | V _{CP} = V _P /2 |
| LOGIC INPUTS | | | | | |
| Input High Voltage, V _{IH} | 1.4 | | | V | |
| Input Low Voltage, V _{IL} | | | 0.6 | V | |
| Input Current, I _{INH} , I _{INL} | | | ±1 | μA | |
| Input Capacitance, C _{IN} | | | 10 | pF | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, V _{OH} | 1.4 | | | V | Open-drain output, 1 kΩ pull-up resistor to 1.8 V CMOS output |
| | DV _{DD} - 0.4 | | | V | |
| Output High Current, I _{OH} | | | 100 | μA | I _{OL} = 500 μA |
| Output Low Voltage, V _{OL} | | | 0.4 | V | |
| POWER SUPPLIES | | | | | |
| AV _{DD} | 2.7 | | 3.3 | V | AV _{DD} ≤ V _P ≤ 5.5 V |
| DV _{DD} | AV _{DD} | | | V | |
| V _P | AV _{DD} | | 5.5 | V | |
| I _{DD} ³ (AI _{DD} + DI _{DD}) | | 5.0 | 6.0 | mA | T _A = 25°C AI _{DD} + DI _{DD} |
| I _P | | | 0.4 | mA | |
| Power-Down Mode | | 1 | | μA | |
| NOISE CHARACTERISTICS | | | | | |
| Normalized Phase Noise Floor (PN _{SYNTH}) ^{4,5} | | -222 | | dBc/Hz | PLL loop bandwidth = 500 kHz |
| Normalized 1/f Noise (PN _{1/f}) ^{4,6} | | -119 | | dBc/Hz | Measured at 10 kHz offset; normalized to 1 GHz |

¹ AV_{DD} = DV_{DD} = 3 V.

² Guaranteed by design. Sample tested to ensure compliance.

³ T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; RF_{IN} = 350 MHz. The current for any other setup (25°C, 3.0 V) in mA is given by 2.35 + 0.0046 (REF_{IN}) + 0.0062 (RF); RF frequency and REF_{IN} frequency in MHz.

⁴ All phase noise measurements were performed with a Rohde & Schwarz FSUP26 phase noise test system using the EVAL-ADF4002EBZ1 evaluation board and the ultralow noise, 100 MHz OCXO from Wenzel (Part No. 501-16843) as the PLL reference.

⁵ The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value) and 10logf_{PFD}. PN_{SYNTH} = PN_{TOT} - 10logf_{PFD} - 20logN.

⁶ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1/f} + 10log(10 kHz/f) + 20log(f_{REF}/1 GHz). Both the normalized phase noise floor and the flicker noise are modeled in ADIsimPLL.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3\text{ V} \pm 10\%$, $AV_{DD} \leq V_P \leq 5.5\text{ V}$, $AGND = DGND = CPGND = 0\text{ V}$, $R_{SET} = 5.1\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MAX}$ to T_{MIN} , unless otherwise noted. Operating temperature range is -55°C to $+125^\circ\text{C}$.

Table 2.

| Parameter | Limit ¹ | Unit | Description |
|----------------|--------------------|--------|------------------------|
| t ₁ | 10 | ns min | DATA to CLK setup time |
| t ₂ | 10 | ns min | DATA to CLK hold time |
| t ₃ | 25 | ns min | CLK high duration |
| t ₄ | 25 | ns min | CLK low duration |
| t ₅ | 10 | ns min | CLK to LE setup time |
| t ₆ | 20 | ns min | LE pulse width |

¹ Guaranteed by design, but not production tested.

Timing Diagram

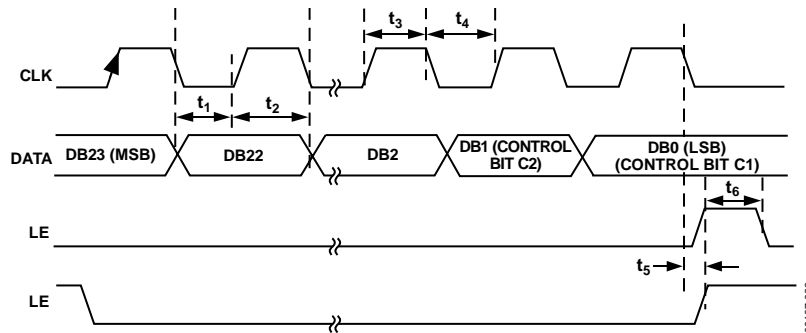


Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|--|-----------------------------|
| AV_{DD} to GND ¹ | -0.3 V to +3.6 V |
| AV_{DD} to DV_{DD} | -0.3 V to +0.3 V |
| V_P to GND ¹ | -0.3 V to +5.8 V |
| V_P to AV_{DD} | -0.3 V to +5.8 V |
| Digital I/O Voltage to GND ¹ | -0.3 V to $DV_{DD} + 0.3$ V |
| Analog I/O Voltage to GND ¹ | -0.3 V to $V_P + 0.3$ V |
| REF_{IN} , $RF_{IN A}$, $RF_{IN B}$ to GND ¹ | -0.3 V to $AV_{DD} + 0.3$ V |
| Operating Temperature Range | |
| Industrial | -55°C to +125°C |
| Storage Temperature Range | -65°C to +125°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| Transistor Count | |
| CMOS | 6425 |
| Bipolar | 303 |

¹ GND = AGND = DGND = CPGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL CHARACTERISTICS

Table 4. Thermal Impedance

| Package Type | θ_{JA} | Unit |
|---------------|---------------|------|
| TSSOP (RU-16) | 150.4 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

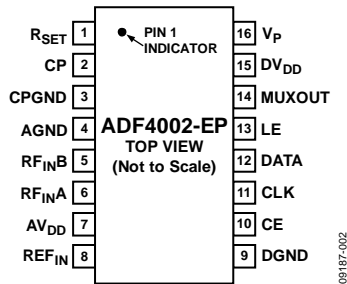


Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|---|
| 1 | R _{SET} | Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R _{SET} pin is 0.66 V. The relationship between I _{CP} and R _{SET} is $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ where R _{SET} = 5.1 kΩ and I _{CP} = 5 mA. |
| 2 | CP | Charge Pump Output. When enabled, this output provides ±I _{CP} to the external loop filter that, in turn, drives the external VCO. |
| 3 | CPGND | Charge Pump Ground. This is the ground return path for the charge pump. |
| 4 | AGND | Analog Ground. This is the ground return path of the RF input. |
| 5 | RF _{INB} | Complementary Input to the RF Input. This pin must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. |
| 6 | RF _{INA} | Input to the RF Input. This small-signal input is ac-coupled to the external VCO. |
| 7 | AV _{DD} | Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV _{DD} pin. AV _{DD} must be the same value as DV _{DD} . |
| 8 | REF _{IN} | Reference Input. This CMOS input has a nominal threshold of AV _{DD} /2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled. |
| 9 | DGND | Digital Ground. |
| 10 | CE | Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit PD1. |
| 11 | CLK | Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 12 | DATA | Serial Data Input. The serial data is loaded MSB first; the two LSBs are the control bits. This input is a high impedance CMOS input. |
| 13 | LE | Load Enable. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits. This input is a high impedance CMOS input. |
| 14 | MUXOUT | Multiplexer Output. This output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally. |
| 15 | DV _{DD} | Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to the DV _{DD} pin. DV _{DD} must be the same value as AV _{DD} . |
| 16 | V _P | Charge Pump Power Supply. This should be greater than or equal to AV _{DD} . In systems where AV _{DD} is 3 V, V _P can be set to 5.5 V and used to drive a VCO with a tuning voltage of up to 5 V. |

TYPICAL PERFORMANCE CHARACTERISTICS

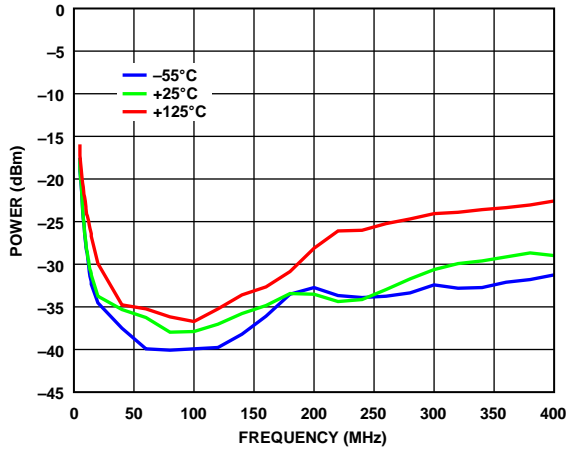


Figure 4. RF Input Sensitivity

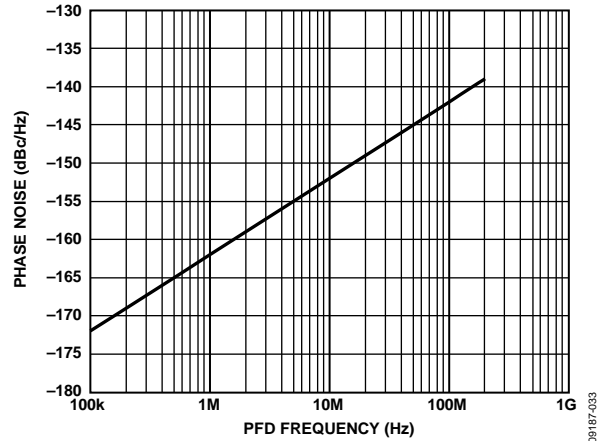


Figure 7. Phase Noise (Referred to CP Output) vs. PFD Frequency

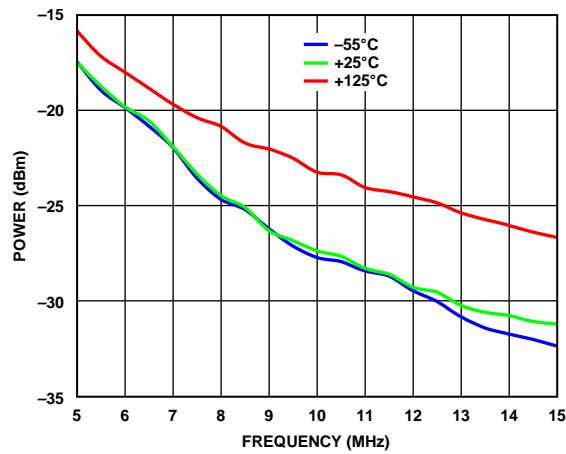


Figure 5. RF Input Sensitivity, Low Frequency

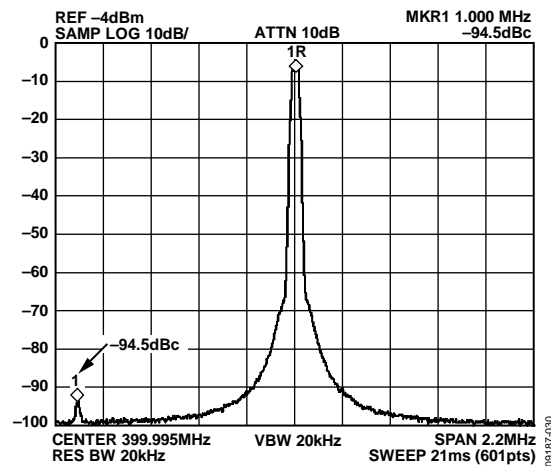


Figure 8. Reference Spurs (400 MHz, 1 MHz, 7 kHz)

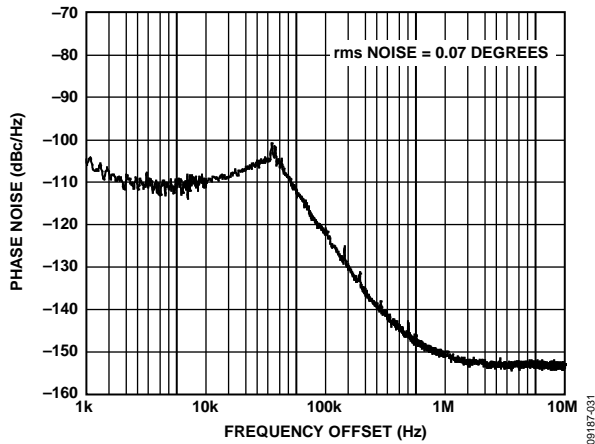
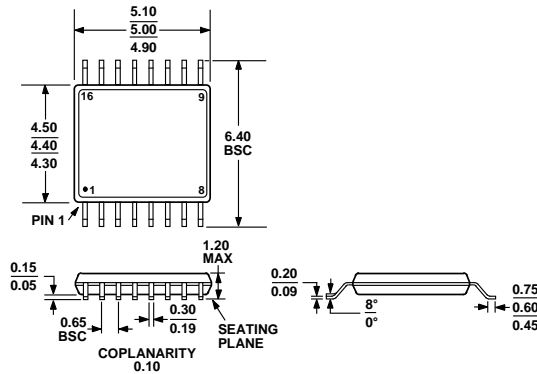


Figure 6. Integrated Phase Noise (400 MHz, 1 MHz, 50 kHz)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 9. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---------------------|----------------|
| ADF4002SRU-EP | -55°C to +125°C | 16-Lead TSSOP | RU-16 |
| ADF4002SRU-EP-RL7 | -55°C to +125°C | 16-Lead TSSOP | RU-16 |
| ADF4002SRUZ-EP | -55°C to +125°C | 16-Lead TSSOP | RU-16 |
| ADF4002SRUZ-EP-RL7 | -55°C to +125°C | 16-Lead TSSOP | RU-16 |

¹ Z = RoHS Compliant Part

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