THE DATASHEET OF

ADA4528-2TCPZ-EPR7

Precision, Ultralow Noise, RRIO, Zero-Drift Op Amp

Enhanced Product

ADA4528-2-EP

FEATURES

- Low offset voltage: 2.5 µV maximum
- Low offset voltage drift: 0.015 µV/°C maximum
- Low noise
  - 5.6 nV/√Hz at f = 1 kHz, A_V = +100
  - 97 nV p-p at f = 0.1 Hz to 10 Hz, A_V = +100
- Open-loop gain: 130 dB minimum
- CMRR: 135 dB minimum
- PSRR: 130 dB minimum
- Unity-gain crossover: 4 MHz
- Gain bandwidth product: 3 MHz at A_V = +100
- −3 dB closed-loop bandwidth: 6.2 MHz
- Single-supply operation: 2.2 V to 5.5 V
- Dual-supply operation: ±1.1 V to ±2.75 V
- Rail-to-rail input and output (RRIO)
- Unity-gain stable

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available upon request

APPLICATIONS

- Thermocouples/thermopiles
- Load cell and bridge transducers
- Precision instrumentation
- Electronic scales
- Medical instrumentation
- Handheld test equipment

PIN CONNECTION DIAGRAM

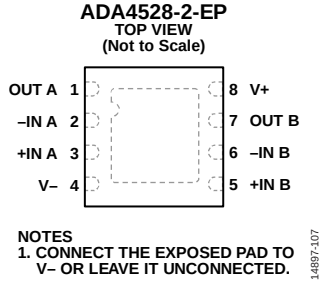

Figure 1.

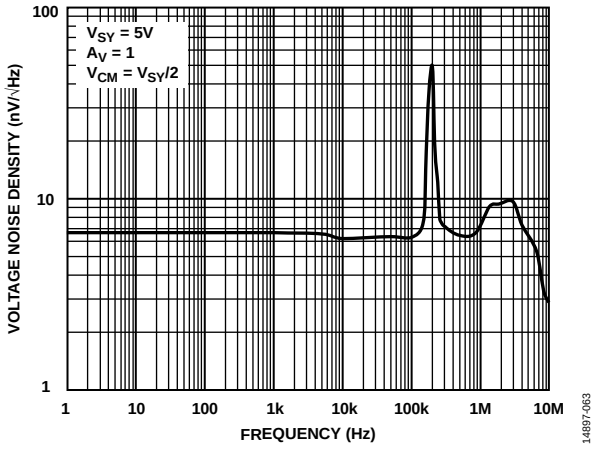

Figure 2. Voltage Noise Density vs. Frequency

GENERAL DESCRIPTION

The ADA4528-2-EP is an ultralow noise, zero-drift operational amplifier featuring rail-to-rail input and output swing. With an offset voltage of 2.5 µV, offset voltage drift of 0.015 µV/°C, and typical noise of 97 nV p-p (0.1 Hz to 10 Hz, A_V = +100), the ADA4528-2-EP is well suited for applications in which error sources cannot be tolerated.

The ADA4528-2-EP has a wide operating supply range of 2.2 V to 5.5 V, high gain, and excellent CMRR and PSRR specifications, which make it ideal for applications that require precision amplification of low level signals, such as position and pressure sensors, strain gages, and medical instrumentation.

The ADA4528-2-EP is specified over the extended industrial temperature range (−55°C to +125°C) and is available in an 8-lead LFCSP package.

Additional application and technical information can be found in the ADA4528-2 datasheet.

Rev. 0 Document Feedback

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REVISION HISTORY

8/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

V_{SY} = 2.5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.5 V		0.3	2.5	µV
		−55°C ≤ T_A ≤ +125°C			4.3	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C ≤ T_A ≤ +125°C		0.002	0.018	µV/°C
Input Bias Current	I_B			220	400	pA
		−55°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			440	800	pA
		−55°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	135	158		dB
		−55°C ≤ T_A ≤ +125°C	116			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	130	140		dB
		−55°C ≤ T_A ≤ +125°C	126			dB
		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	122	132		dB
		−55°C ≤ T_A ≤ +125°C	119			dB
Input Resistance						
Differential Mode	R_{INDM}			225		kΩ
Common Mode	R_{INCM}			1		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			15		pF
Common Mode	C_{INCM}			30		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.49	2.495		V
		−55°C ≤ T_A ≤ +125°C	2.485			V
		R_L = 2 kΩ to V_{CM}	2.46	2.48		V
		−55°C ≤ T_A ≤ +125°C	2.44			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−55°C ≤ T_A ≤ +125°C			15	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−55°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−55°C ≤ T_A ≤ +125°C	127			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.4	1.7	mA
		−55°C ≤ T_A ≤ +125°C			2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.45		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 1.5 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		7		µs
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100		3		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		6.2		MHz
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		97		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.6		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 2.0 V		5.5		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.7		pA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 5 V		0.3	2.5	µV
		−55°C ≤ T_A ≤ +125°C			4	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C ≤ T_A ≤ +125°C		0.002	0.015	µV/°C
Input Bias Current	I_B			125	250	pA
		−55°C ≤ T_A ≤ +125°C			400	pA
Input Offset Current	I_{OS}			250	500	pA
		−55°C ≤ T_A ≤ +125°C			650	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	137	160		dB
		−55°C ≤ T_A ≤ +125°C	122			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4.9 V	127	139		dB
		−55°C ≤ T_A ≤ +125°C	125			dB
		R_L = 2 kΩ, V_O = 0.1 V to 4.9 V	121	131		dB
		−55°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			190		kΩ
Common Mode	R_{INCM}			1		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			16.5		pF
Common Mode	C_{INCM}			33		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.99	4.995		V
		−55°C ≤ T_A ≤ +125°C	4.98			V
		R_L = 2 kΩ to V_{CM}	4.96	4.98		V
		−55°C ≤ T_A ≤ +125°C	4.94			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−55°C ≤ T_A ≤ +125°C			20	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−55°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−55°C ≤ T_A ≤ +125°C	127			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.5	1.8	mA
		−55°C ≤ T_A ≤ +125°C			2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.5		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 4 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		10		µs
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100		3.4		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		6.5		MHz
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		µs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		99		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.9		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 4.5 V		5.3		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.5		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure (still air).

θ_{JC} is the junction to case thermal resistance, measured on the exposed pad of the package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-8-19[1]	52	3.9	°C/W

[1] Thermal reporting per JEDEC JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

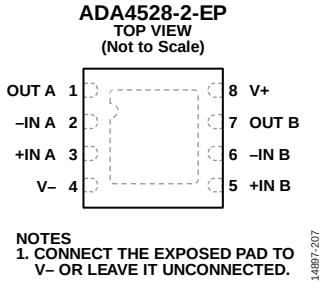

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
	EPAD	Exposed Pad. Connect the exposed pad to V− or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

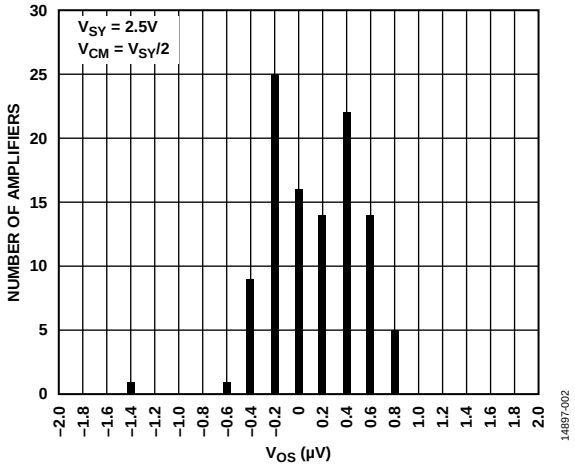

Figure 4. Input Offset Voltage (V_{OS}) Distribution

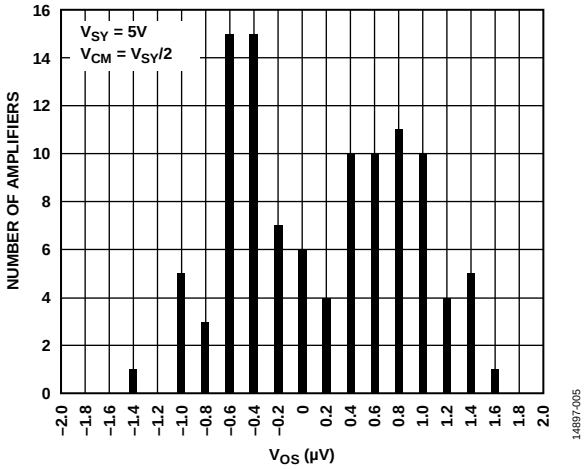

Figure 7. Input Offset Voltage (V_{OS}) Distribution

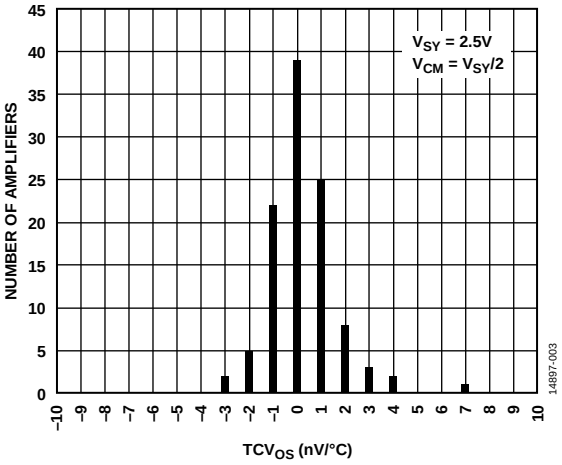

Figure 5. Input Offset Voltage Temperature Coefficient (TC_{VOS}) Drift Distribution

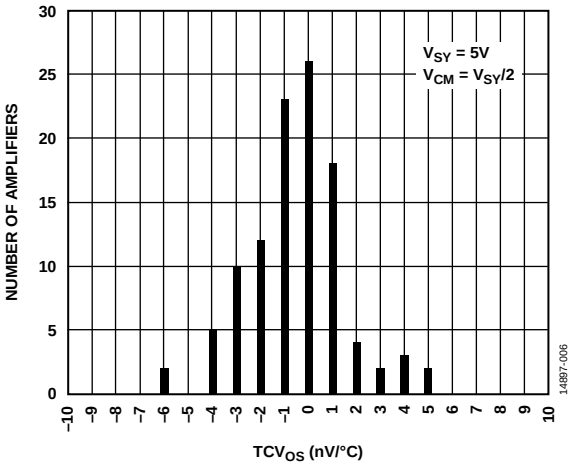

Figure 8. Input Offset Voltage Temperature Coefficient (TC_{VOS}) Drift Distribution

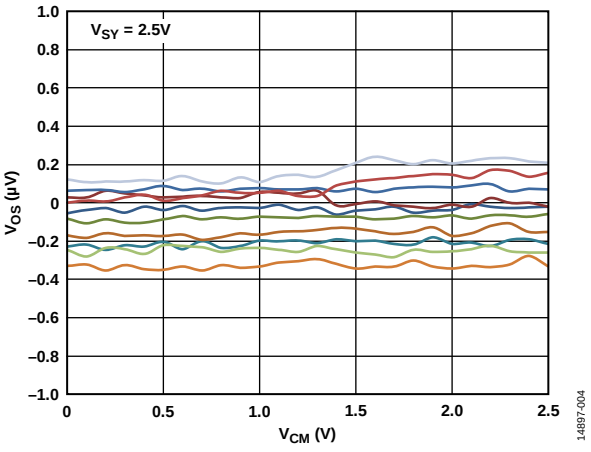

Figure 6. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

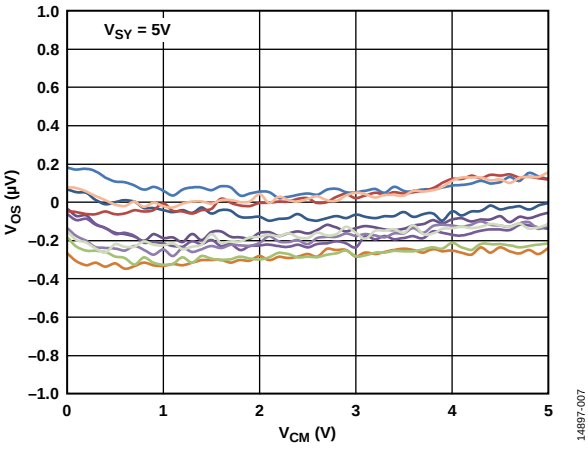

Figure 9. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM})

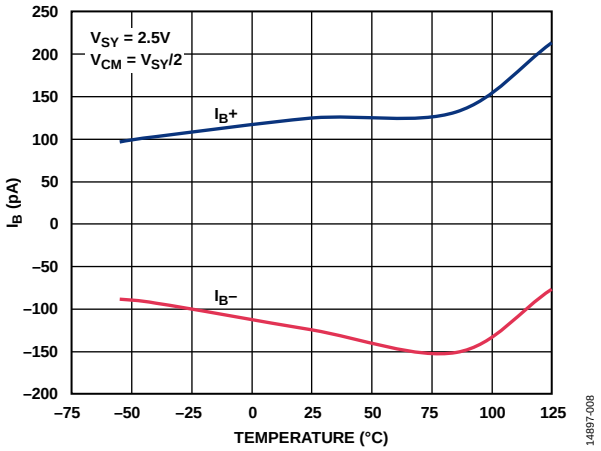

Figure 10. Input Bias Current (I_B) vs. Temperature

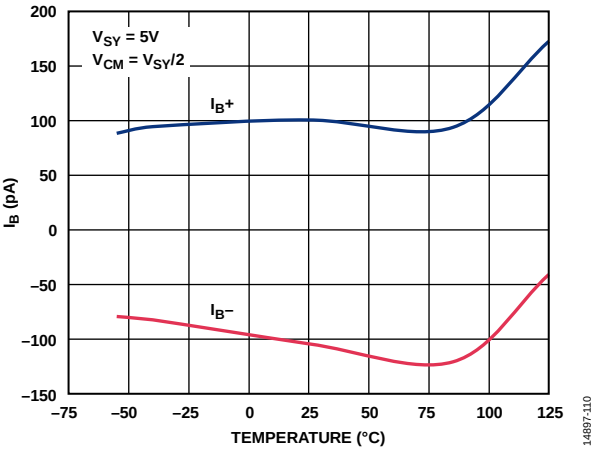

Figure 13. Input Bias Current (I_B) vs. Temperature

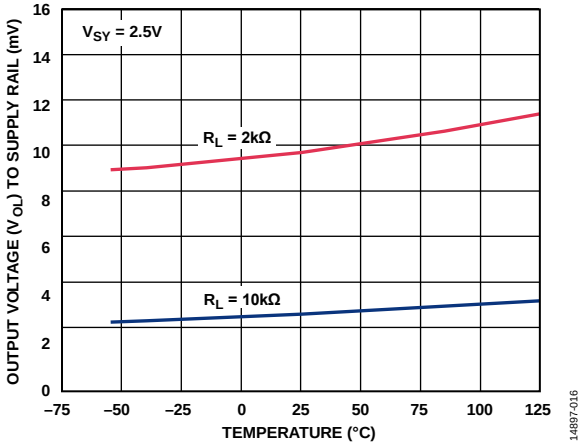

Figure 11. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

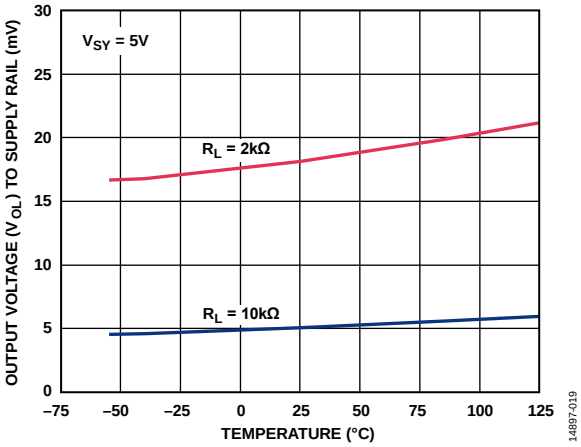

Figure 14. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

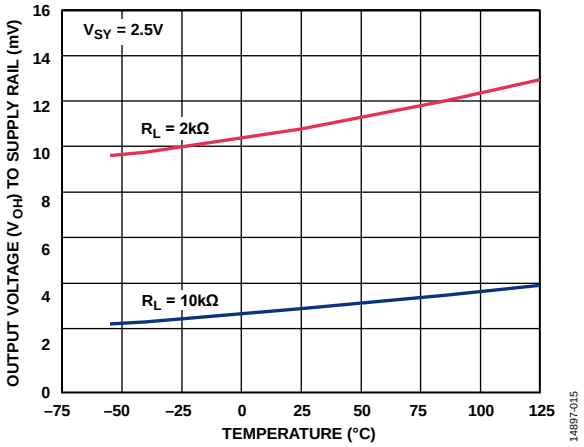

Figure 12. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

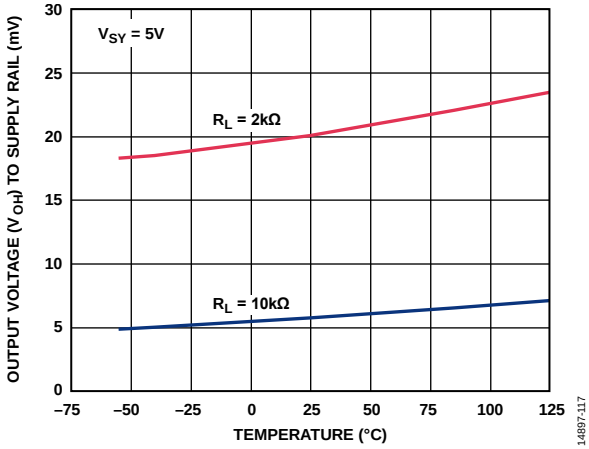

Figure 15. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

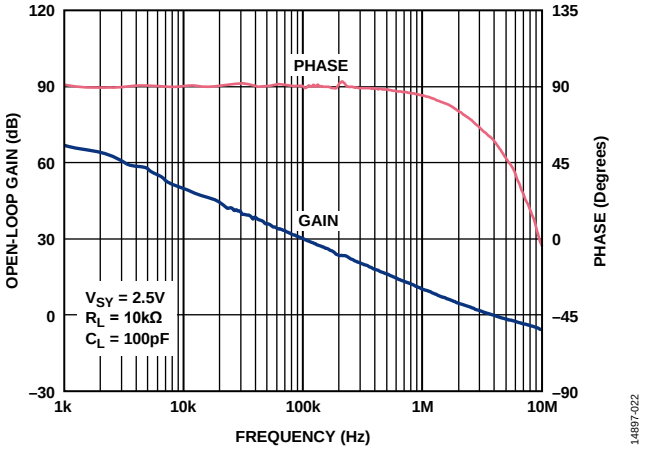

Figure 16. Open-Loop Gain and Phase vs. Frequency

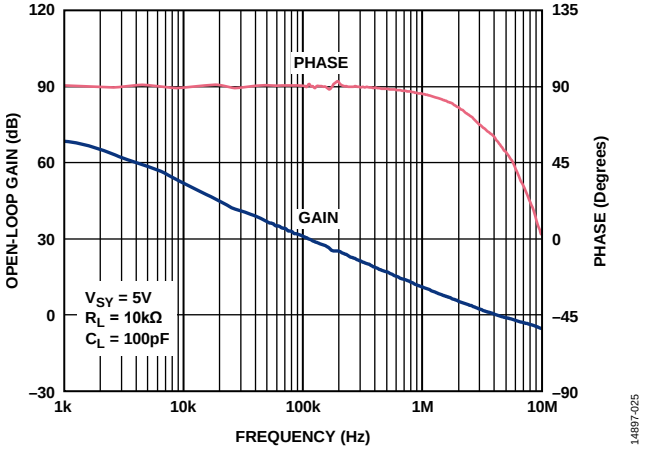

Figure 19. Open-Loop Gain and Phase vs. Frequency

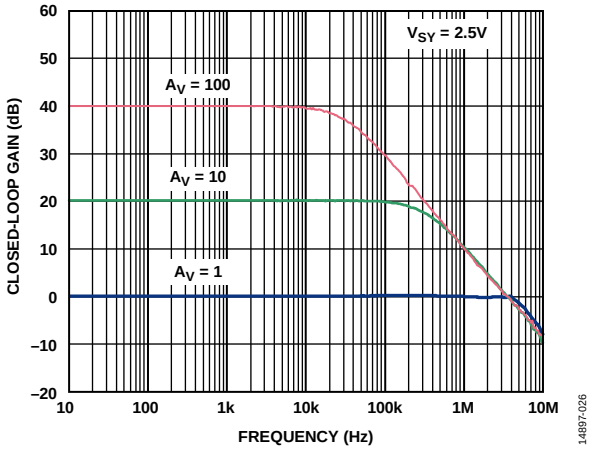

Figure 17. Closed-Loop Gain vs. Frequency

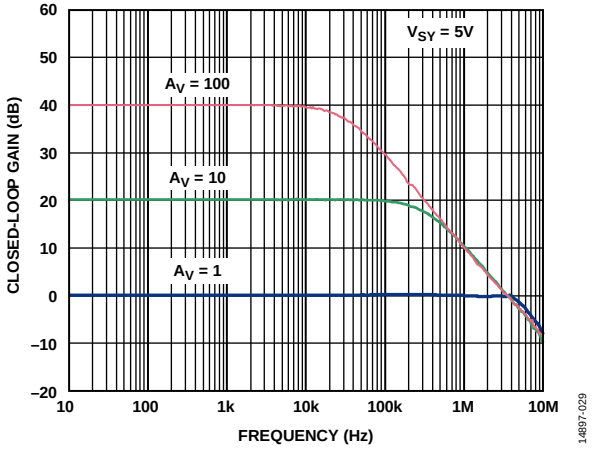

Figure 20. Closed-Loop Gain vs. Frequency

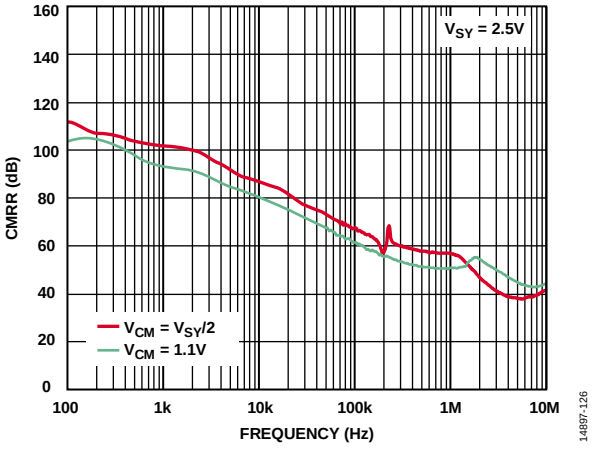

Figure 18. CMRR vs. Frequency

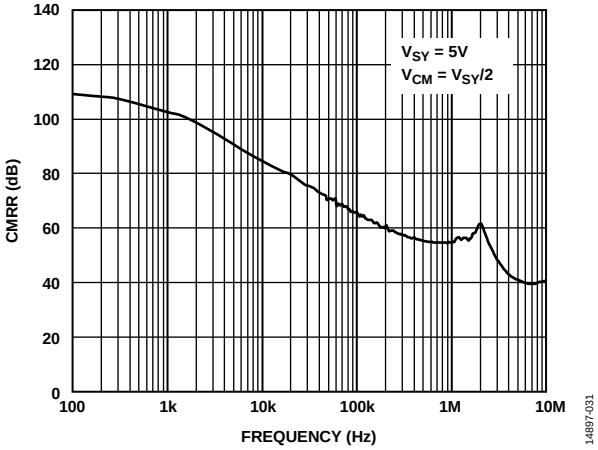

Figure 21. CMRR vs. Frequency

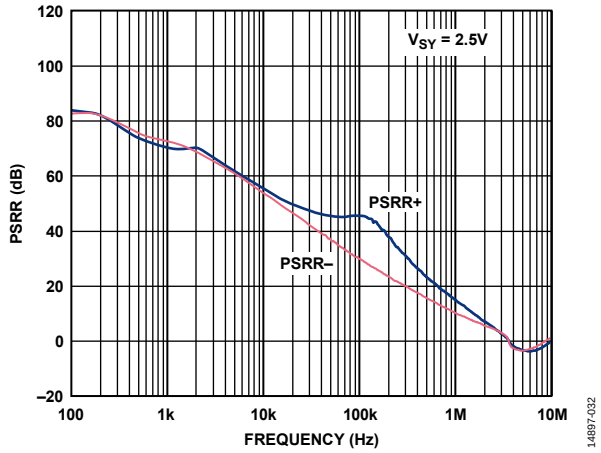

Figure 22. PSRR vs. Frequency

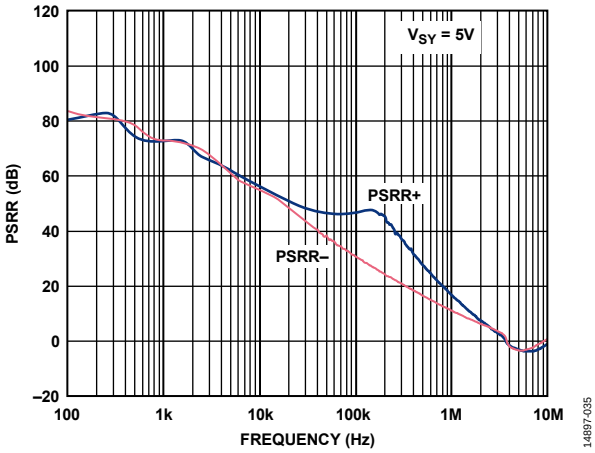

Figure 25. PSRR vs. Frequency

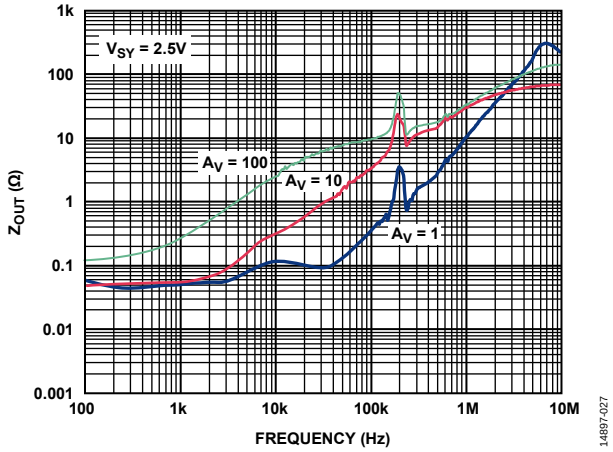

Figure 23. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency

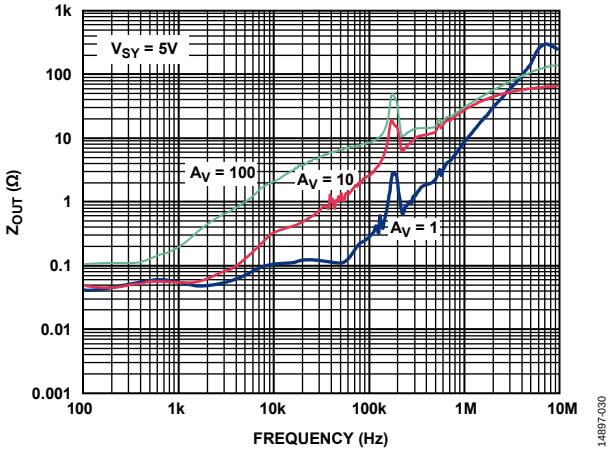

Figure 26. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency

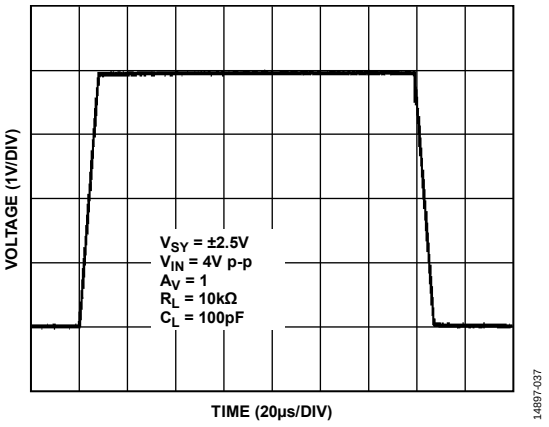

Figure 24. Large Signal Transient Response

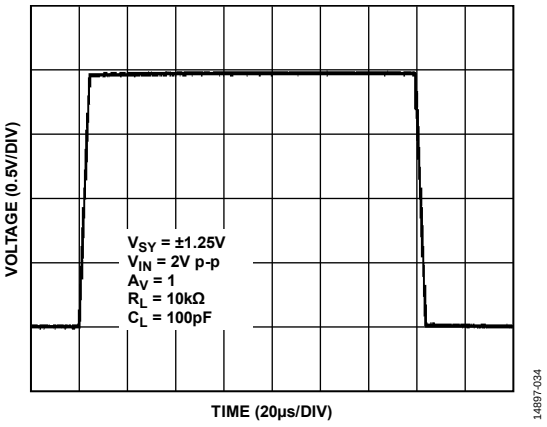

Figure 27. Large Signal Transient Response

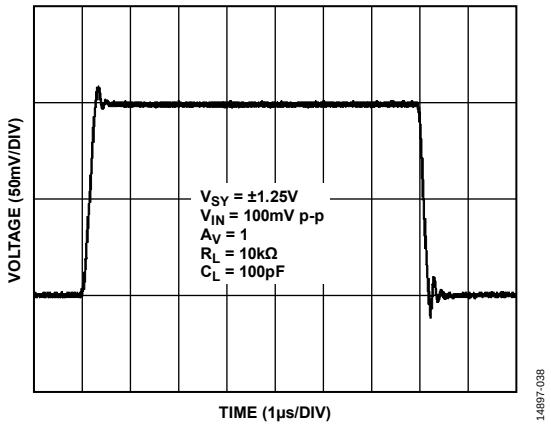

Figure 28. Small Signal Transient Response

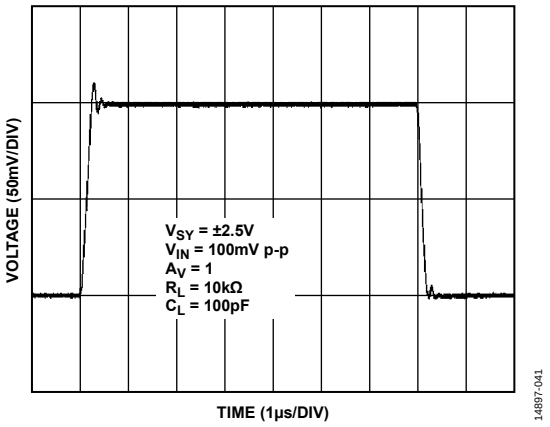

Figure 31. Small Signal Transient Response

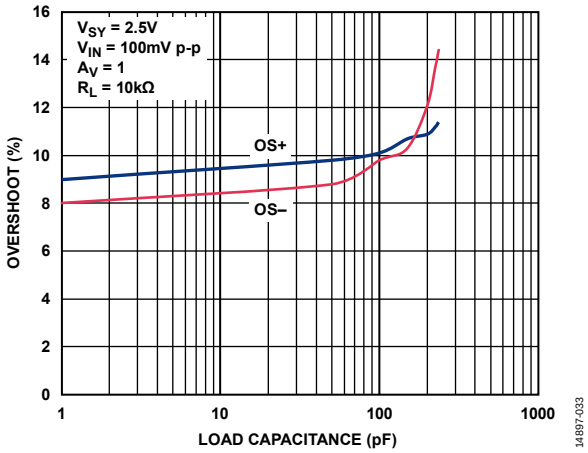

Figure 29. Small Signal Overshoot vs. Load Capacitance

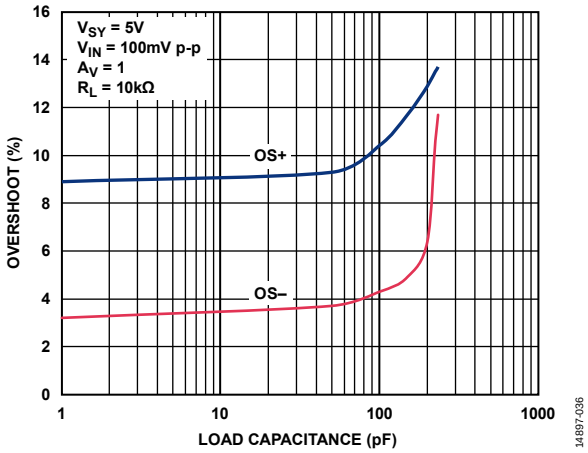

Figure 32. Small Signal Overshoot vs. Load Capacitance

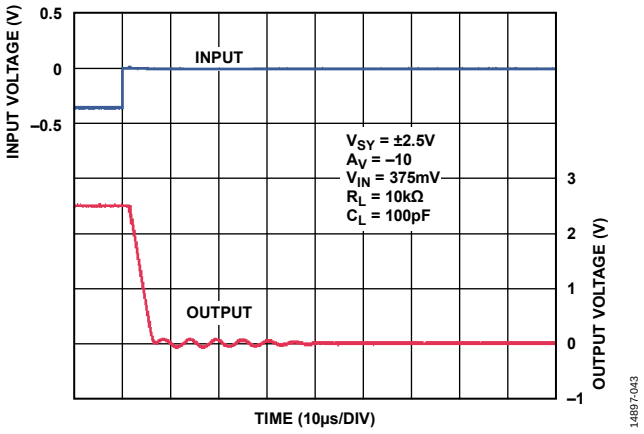

Figure 30. Positive Overload Recovery

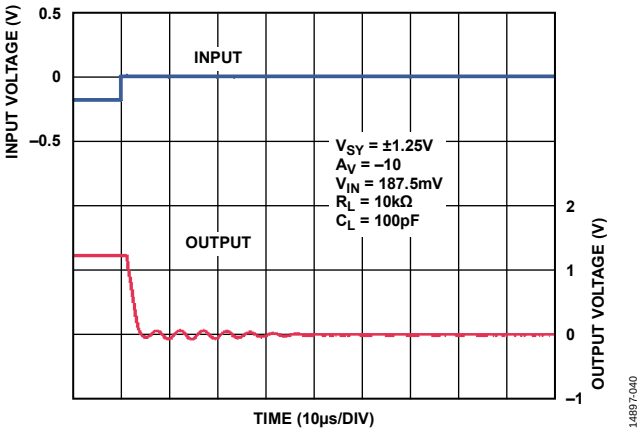

Figure 33. Positive Overload Recovery

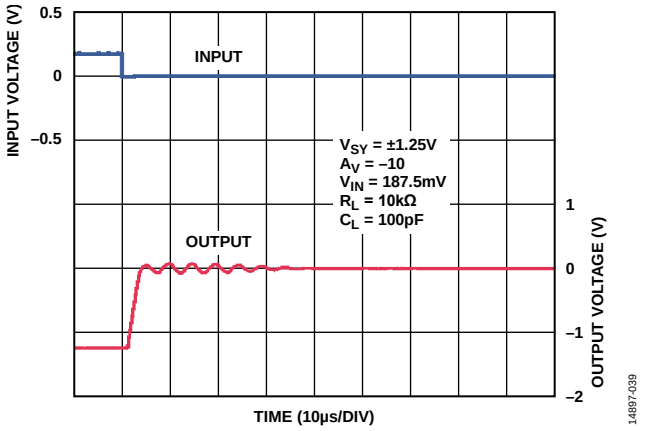

Figure 34. Negative Overload Recovery

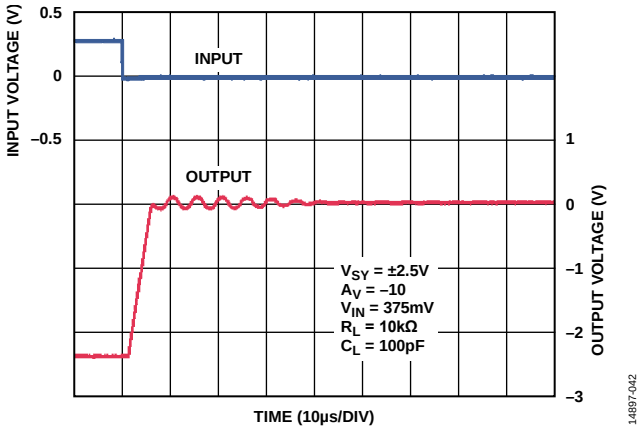

Figure 37. Negative Overload Recovery

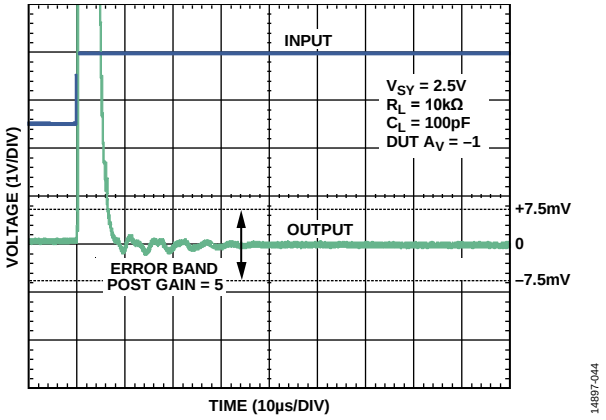

Figure 35. Positive Settling Time to 0.1%

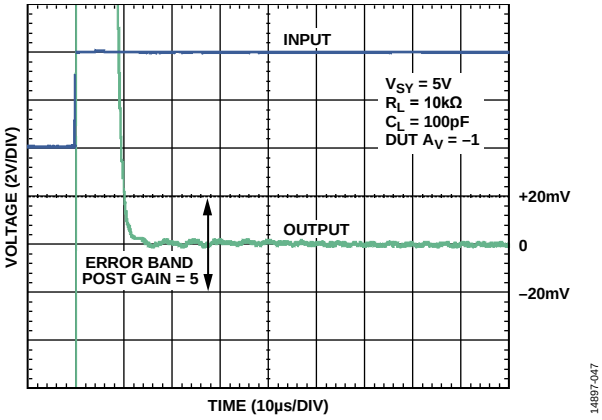

Figure 38. Positive Settling Time to 0.1%

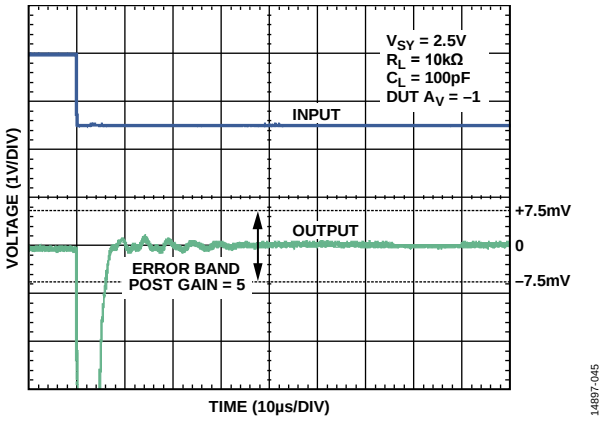

Figure 36. Negative Settling Time to 0.1%

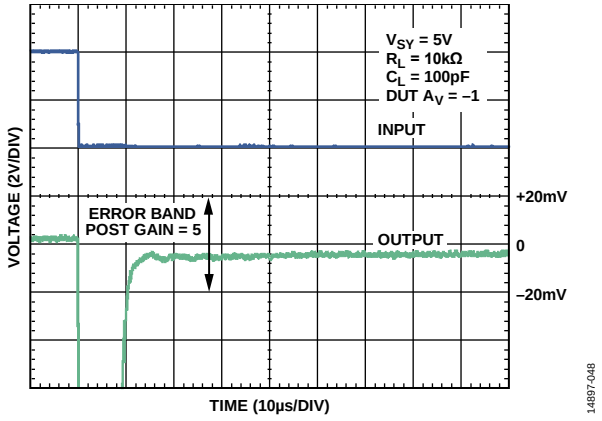

Figure 39. Negative Settling Time to 0.1%

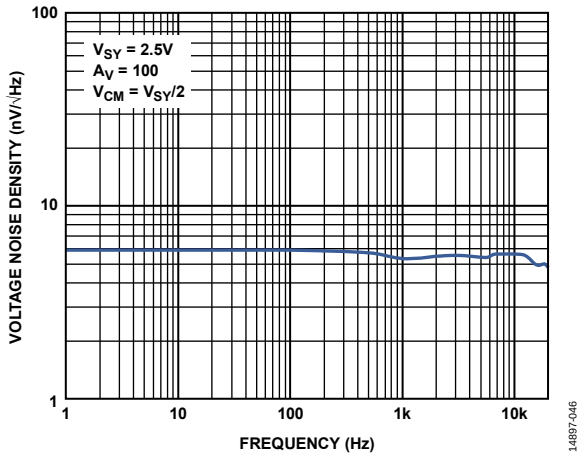

Figure 40. Voltage Noise Density vs. Frequency

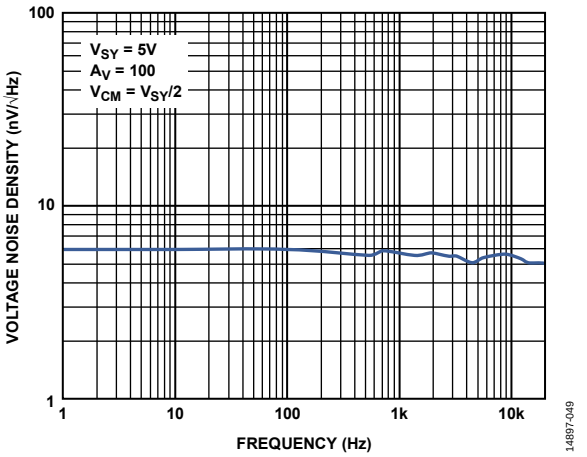

Figure 43. Voltage Noise Density vs. Frequency

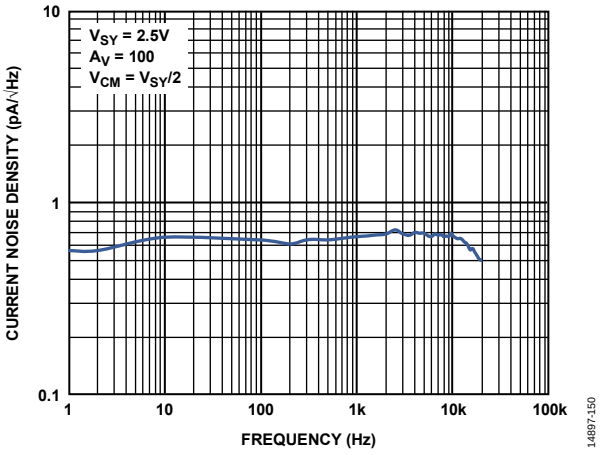

Figure 41. Current Noise Density vs. Frequency

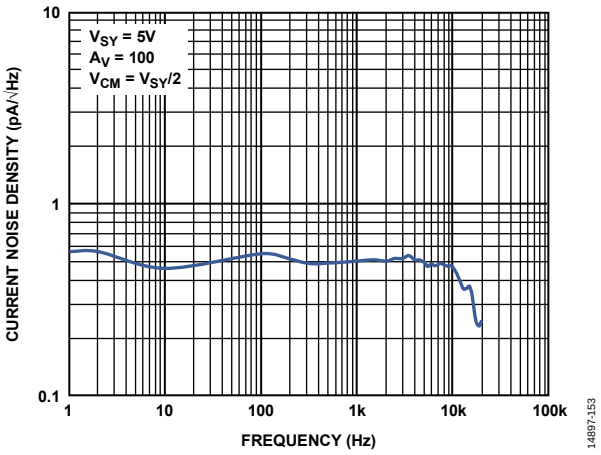

Figure 44. Current Noise Density vs. Frequency

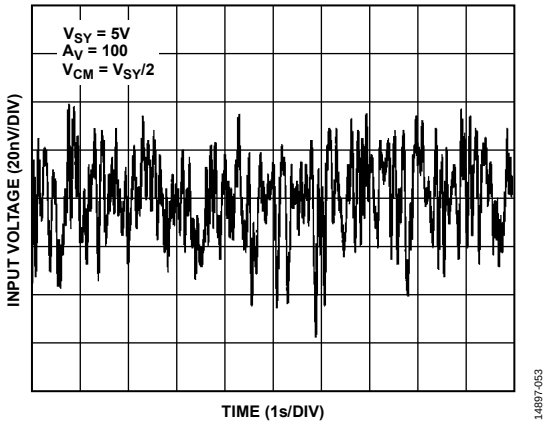

Figure 42. 0.1 Hz to 10 Hz Noise

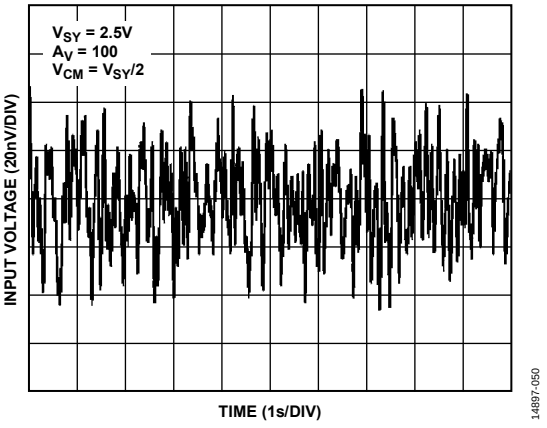

Figure 45. 0.1 Hz to 10 Hz Noise

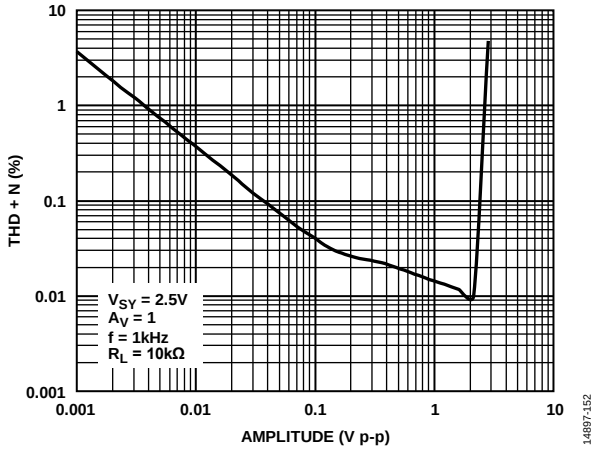

Figure 46. THD + N vs. Amplitude

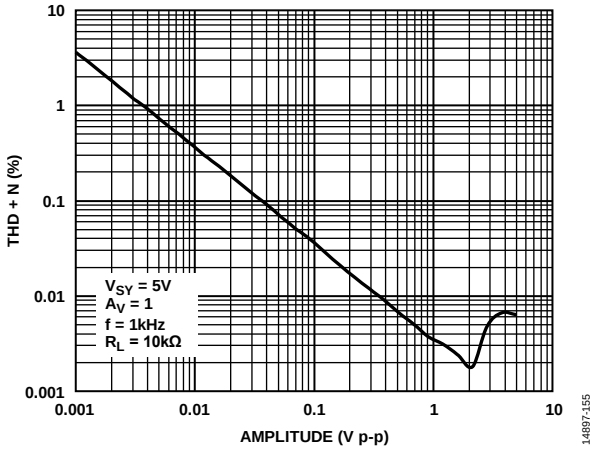

Figure 49. THD + N vs. Amplitude

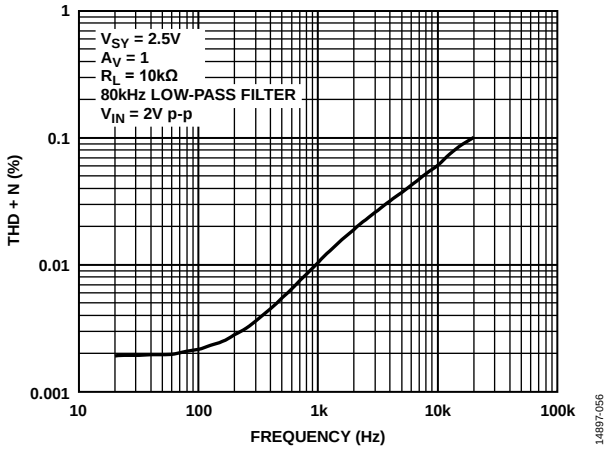

Figure 47. THD + N vs. Frequency

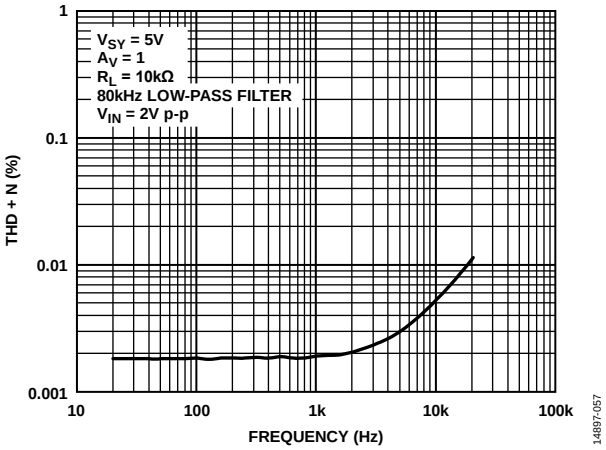

Figure 50. THD + N vs. Frequency

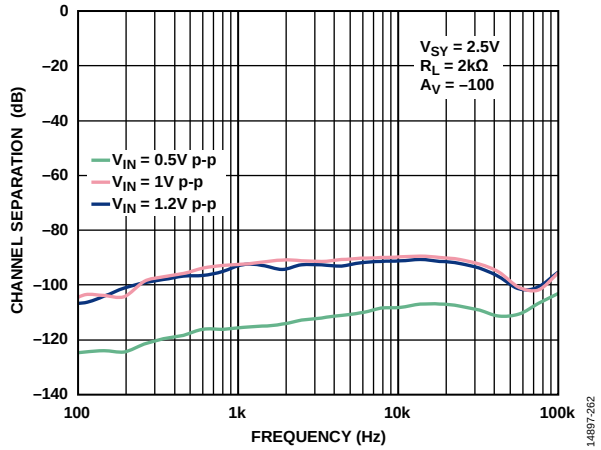

Figure 48.Channel Separation vs. Frequency

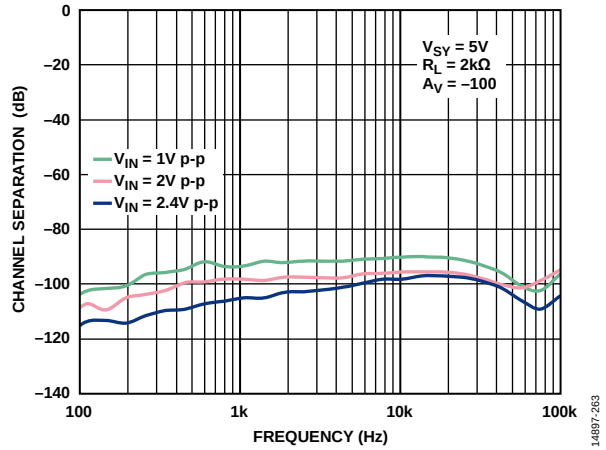

Figure 51. Channel Separation vs. Frequency

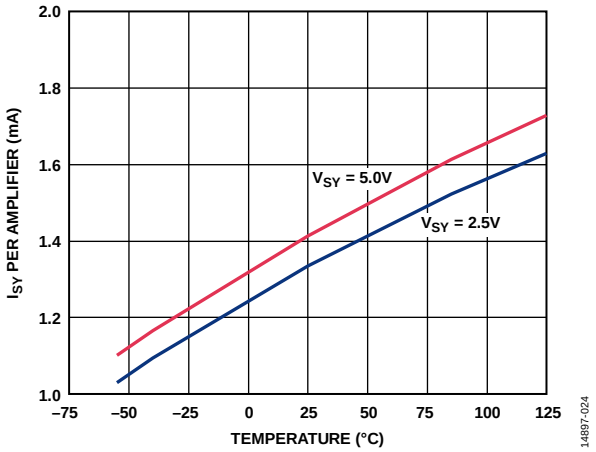

Figure 52. Supply Current (I_{SY}) per Amplifier vs. Temperature

OUTLINE DIMENSIONS

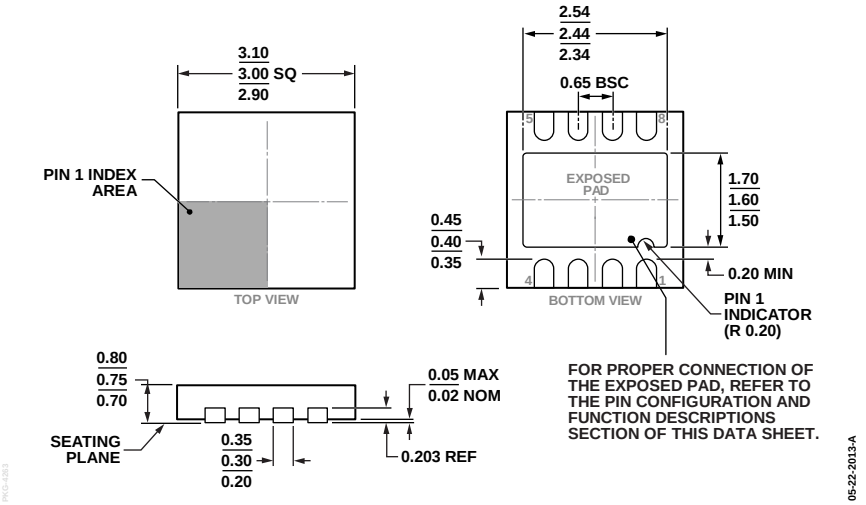

Figure 53. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4528-2TCPZ-EP	−55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	A3H
ADA4528-2TCPZ-EPR7	−55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-19	A3H

[1] Z = RoHS Compliant Part.

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