THE DATASHEET OF

ADL9006ACGZN

2 GHz to 28 GHz, GaAs, pHEMT, MMIC Low Noise Amplifier

Data Sheet **ADL9006**

FEATURES

P1dB: 20 dBm typical at 2 GHz to 6 GHz
P_{SAT}: 20.5 dBm typical at 2 GHz to 6 GHz
Gain: 15.5 dB typical at 6 GHz to 28 GHz
Noise figure: 2.5 dB typical at 2 GHz to 20 GHz
OIP3: 26 dBm typical at 2 GHz to 6 GHz
Supply voltage: 5 V at 53 mA
50 Ω matched input and output

APPLICATIONS

Test instrumentation
Military and space
Local oscillator driver amp

FUNCTIONAL BLOCK DIAGRAM

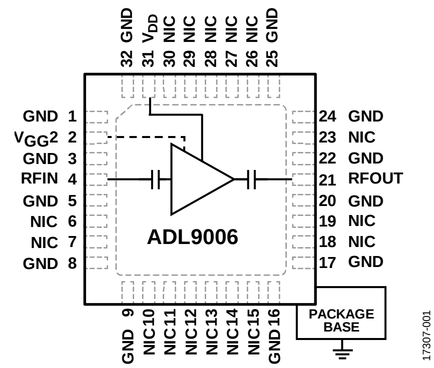


Figure 1.

GENERAL DESCRIPTION

The ADL9006 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), low noise amplifier that operates between 2 GHz and 28 GHz. The amplifier provides 15.5 dB of gain, 2.5 dB noise figure, 26 dBm output third-order intercept (OIP3), and 20 dBm of output power for 1 dB compression (P1dB) while requiring 53 mA from a 5 V supply. The ADL9006 is self biased with only a single positive supply needed to achieve a supply current (I_{DD}) of 53 mA.

The ADL9006 amplifier input and output are internally matched to 50 Ω.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

8/2020—Revision 0: Initial Version

SPECIFICATIONS

2 GHz TO 6 GHz

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 53 mA, $V_{GG}2$ = open, and a 50 Ω matched input and output, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			2		6	GHz
GAIN			13	15		dB
Gain Variation Over Temperature				0.007		dB/°C
RETURN LOSS						
Input				11		dB
Output				12		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB			20		dBm
Saturated Output Power	P_{SAT}		18	20.5		dBm
Output Third-Order Intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 0 dBm		26		dBm
NOISE FIGURE	NF			2.5	4	dB

6 GHz TO 20 GHz

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 53 mA, $V_{GG}2$ = open, and a 50 Ω matched input and output, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			6		20	GHz
GAIN			13	15.5		dB
Gain Variation Over Temperature				0.012		dB/°C
RETURN LOSS						
Input				12		dB
Output				17		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB			18		dBm
Saturated Output Power	P_{SAT}		16	18.5		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 0 dBm		23		dBm
NOISE FIGURE	NF			2.5	4.0	dB

20 GHz TO 28 GHz

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 53 mA, $V_{GG}2$ = open, and a 50 Ω matched input and output, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			20		28	GHz
GAIN			13	15.5		dB
Gain Variation Over Temperature				0.018		dB/°C
RETURN LOSS						
Input				15		dB
Output				15		dB
OUTPUT						
Saturated Output Power	P_{SAT}		15	17.5		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 0 dBm		19.5		dBm
NOISE FIGURE	NF			4	6	dB

DC SPECIFICATIONS

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY CURRENT						
Total Supply Current	I_{DD}	Nominal voltage = 5 V		53		mA
SUPPLY VOLTAGE	V_{DD}		4	5	7	V
GATE BIAS VOLTAGE	$V_{GG}2$	Normal condition is $V_{GG}2$ = open	−2.0		+2.6	V

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{DD}	8 V
$V_{GG}2$	−2.6 V to +3.6 V
RF Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 21.7 mW/°C Above 85°C)	1.96 W
Maximum Peak Reflow Temperature, Moisture Sensitivity Level 3 (MSL3)	260°C
Channel Temperature to Maintain 1,000,000 Hour Meant Time to Failure (MTTF)	175°C
Nominal Channel Temperature (T = 85°C, V_{DD} = 5 V)	98°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package	θ_{JC}	Unit
CG-32-2[1]	46	°C/W

[1] Thermal resistance (θ_{JC}) was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground paddle, to the PCB, and the ground paddle is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

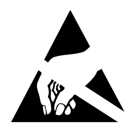
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL9006

Table 7. ADL9006, 32-Lead LFCSP_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

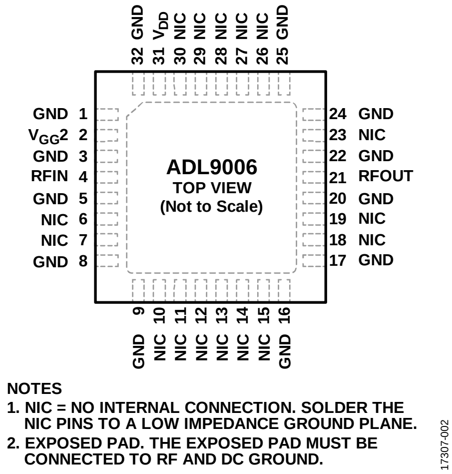


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground. Solder the GND pins to a low impedance ground plane.
2	$V_{GG}2$	Gain Control. $V_{GG}2$ is dc-coupled and accomplishes gain control by reducing the internal voltage and becoming more negative. Attach bypass capacitors to $V_{GG}2$, as shown in Figure 38. Under normal operating conditions, $V_{GG}2$ is left open.
4	RFIN	RF Input. RFIN is ac-coupled and matched to 50 Ω.
6, 7, 10 to 15, 18, 19, 23, 26 to 30	NIC	No Internal Connection. Solder the NIC pins to a low impedance ground plane.
21	RFOUT	RF Output. RFOUT is ac-coupled and matched to 50 Ω.
31	V_{DD}	Power Supply Voltage for the Amplifier.
EPAD		Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

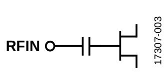


Figure 3. RFIN Interface Schematic

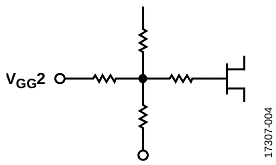


Figure 4. $V_{GG}2$ Interface Schematic

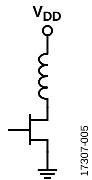


Figure 5. V_{DD} Interface Schematic

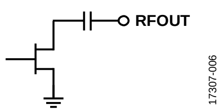


Figure 6. RFOUT Interface Schematic

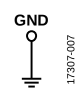


Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

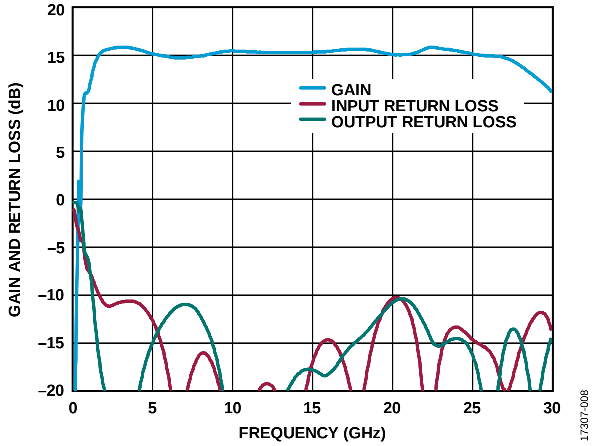


Figure 8. Gain and Return Loss vs. Frequency

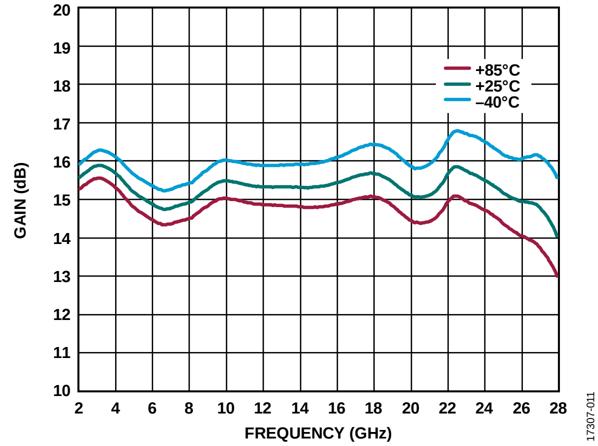


Figure 11. Gain vs. Frequency at Various Temperatures

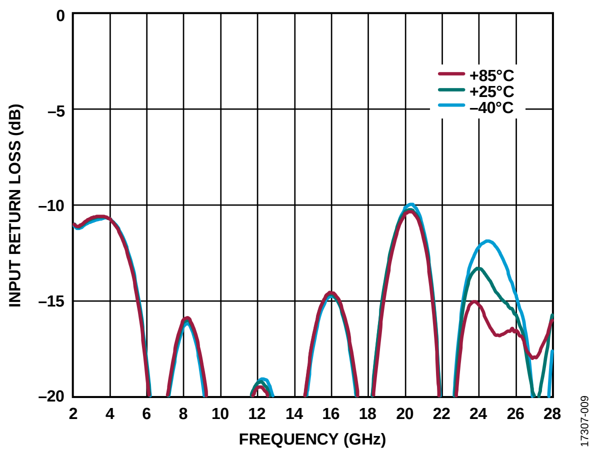


Figure 9. Input Return Loss vs. Frequency at Various Temperatures

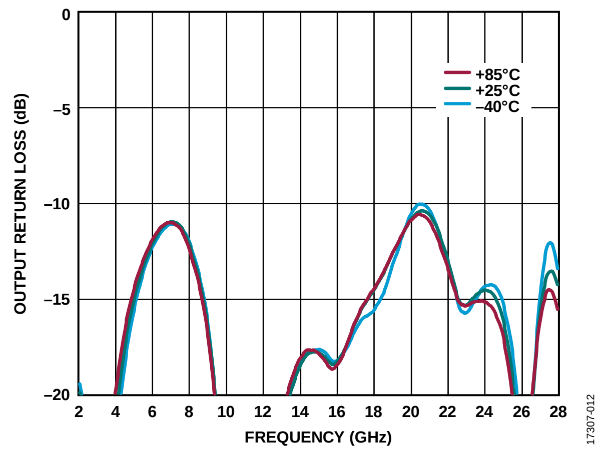


Figure 12. Output Return Loss vs. Frequency at Various Temperatures

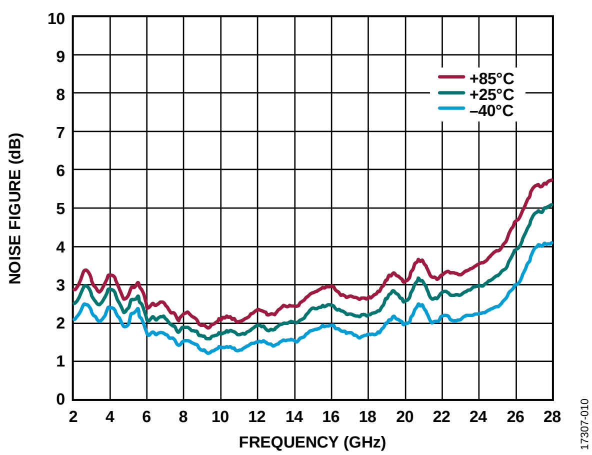


Figure 10. Noise Figure vs. Frequency at Various Temperatures

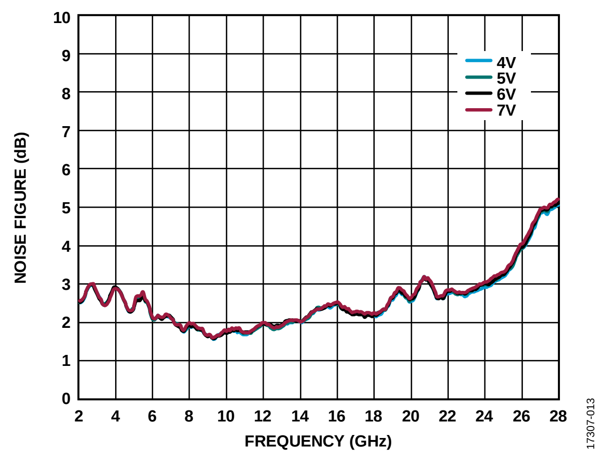


Figure 13. Noise Figure vs. Frequency at Various Supply Voltages

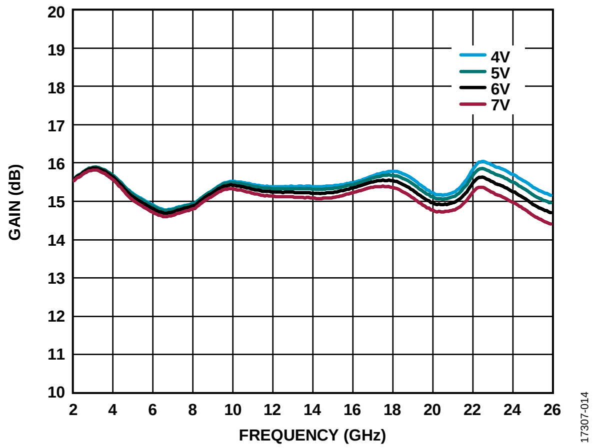


Figure 14. Gain vs. Frequency at Various Supply Voltages

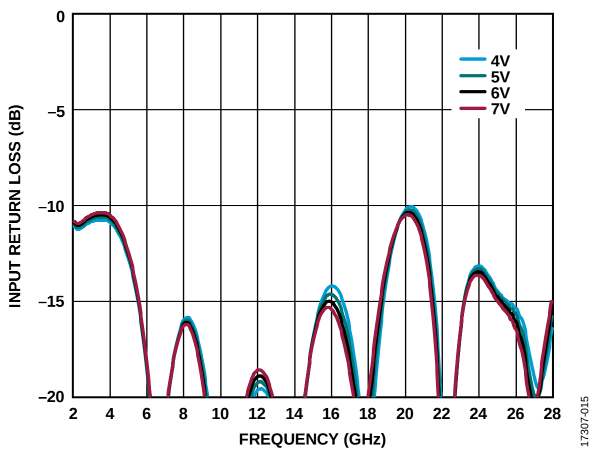


Figure 15. Input Return Loss vs. Frequency at Various Supply Voltages

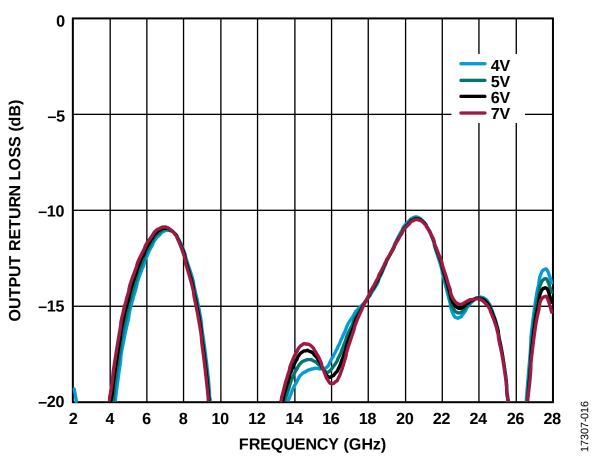


Figure 16. Output Return Loss vs. Frequency at Various Supply Voltages

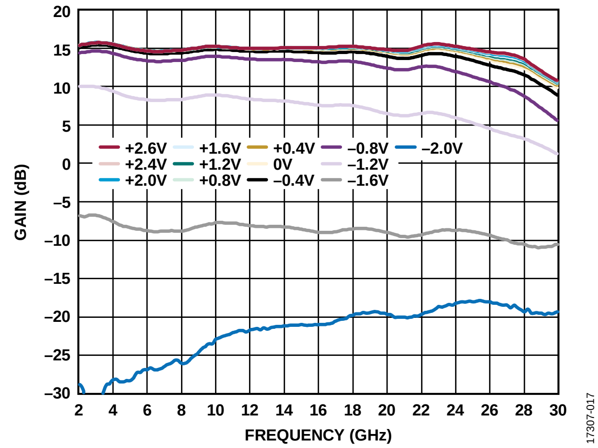


Figure 17. Gain vs. Frequency at Various $V_{GG}2$ Voltages

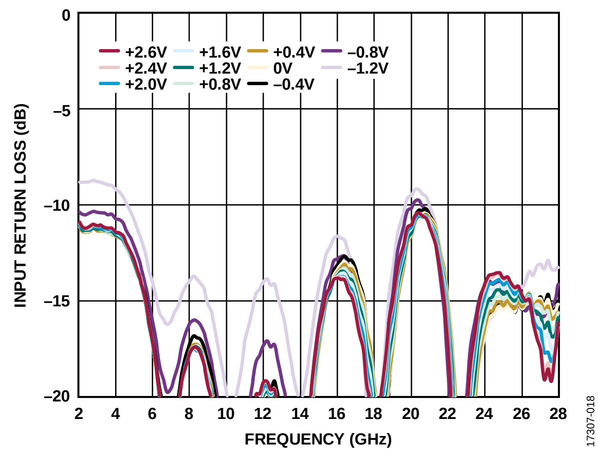


Figure 18. Input Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

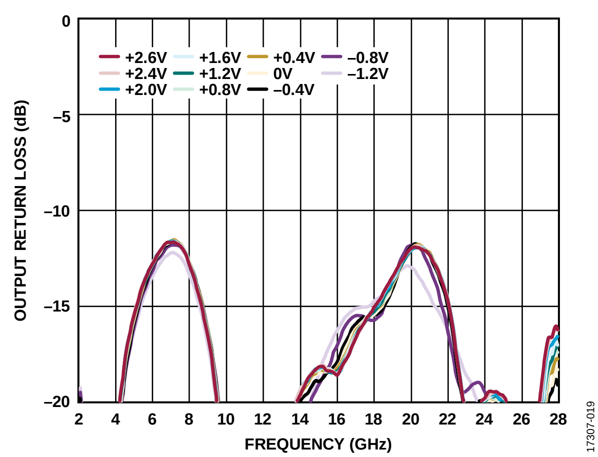


Figure 19. Output Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

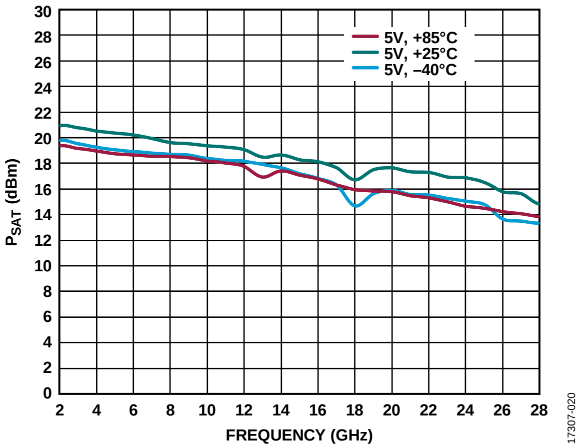


Figure 20. P_{SAT} vs. Frequency at Various Temperatures

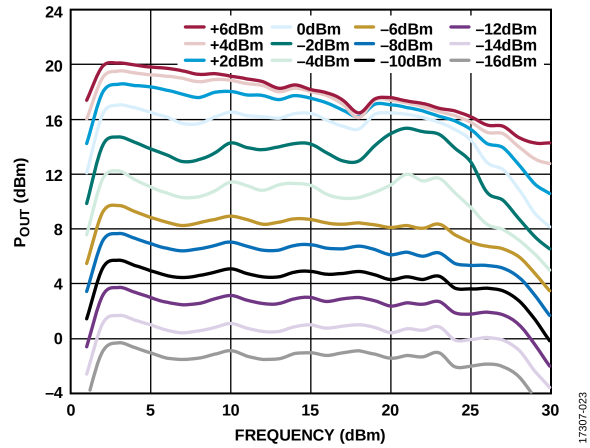


Figure 23. P_{OUT} vs. Frequency at Various Input Power Levels

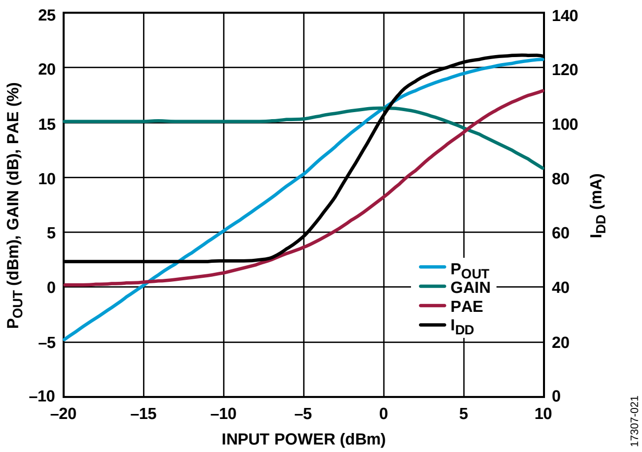


Figure 21. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 2 GHz, V_{DD} = 5 V

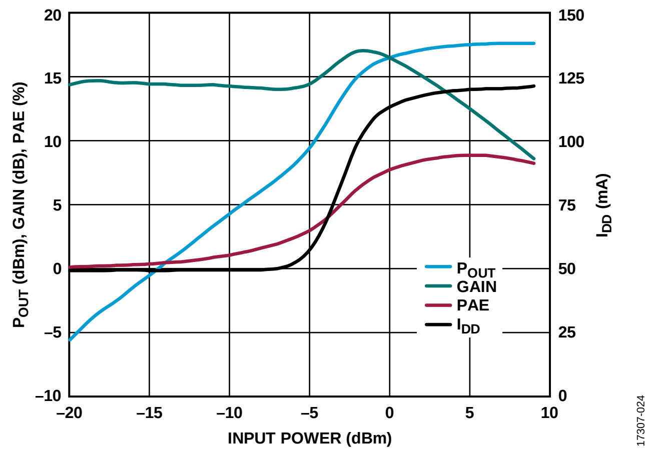


Figure 24. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 20 GHz, V_{DD} = 5 V

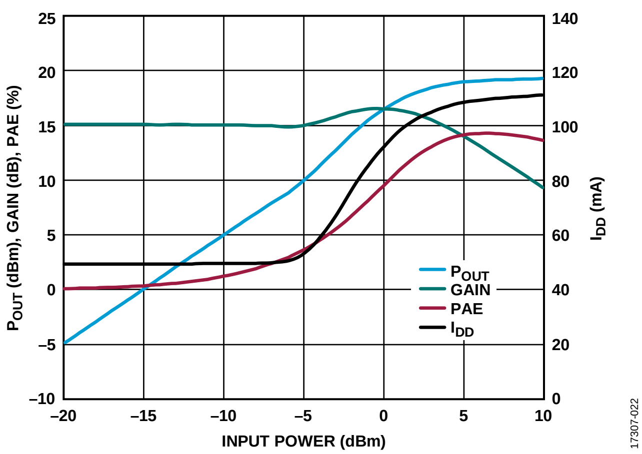


Figure 22. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 10 GHz, V_{DD} = 5 V

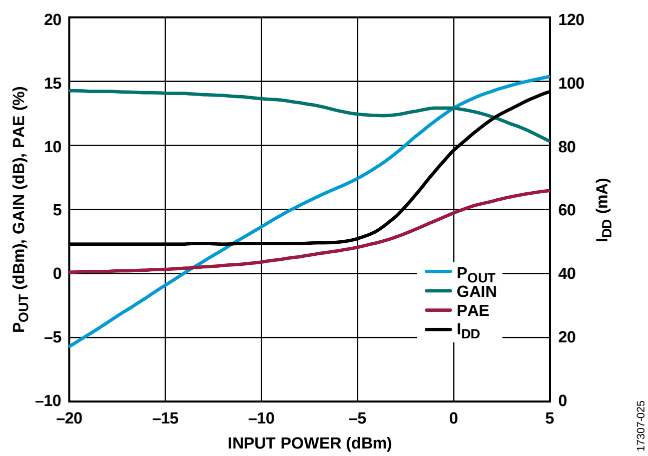


Figure 25. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 26 GHz, V_{DD} = 5 V

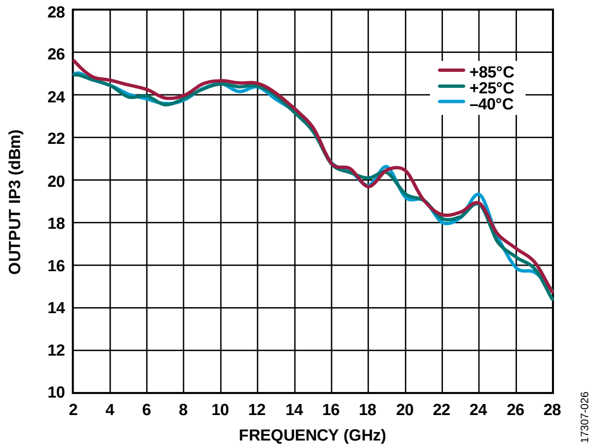


Figure 26. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 0 dBm

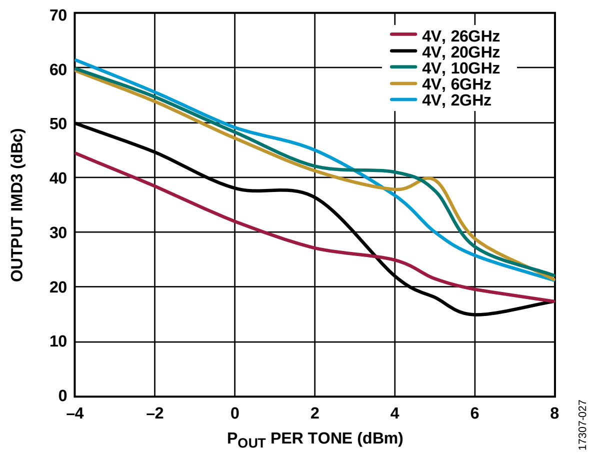


Figure 27. Output Third-Order Intermodulation Distortion Relative to Carrier (IMD3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 4 V

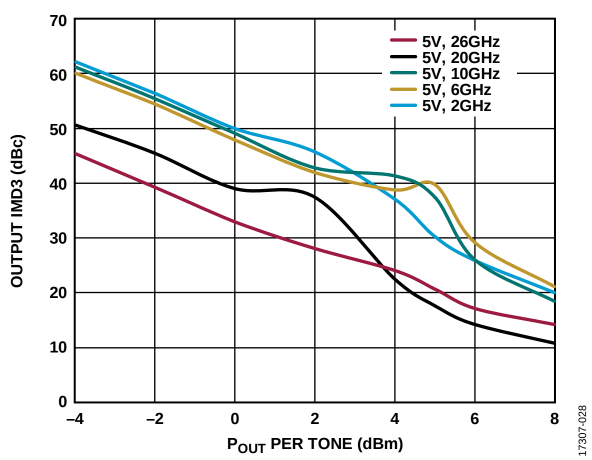


Figure 28. Output IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V

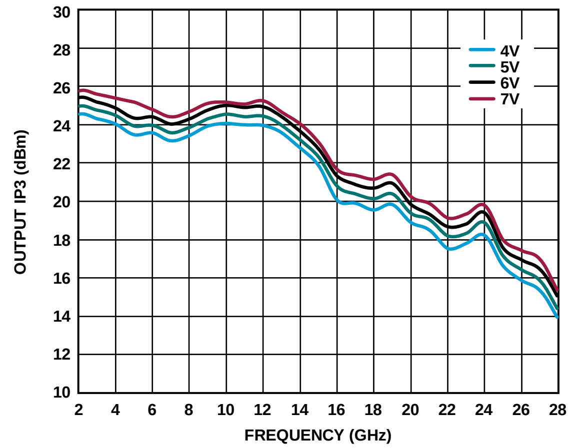


Figure 29. Output IP3 vs. Frequency at Various Supply Voltages

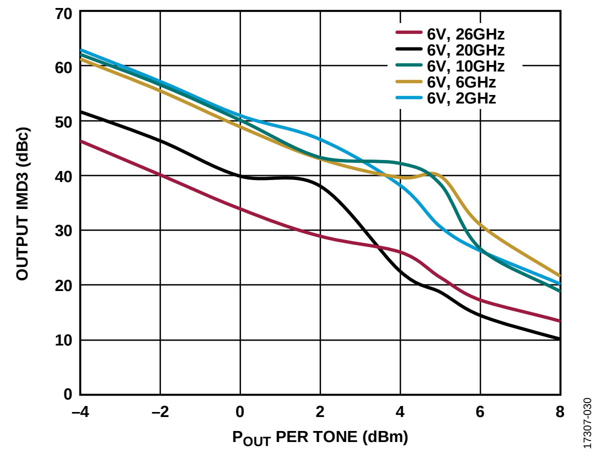


Figure 30. Output IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 6 V

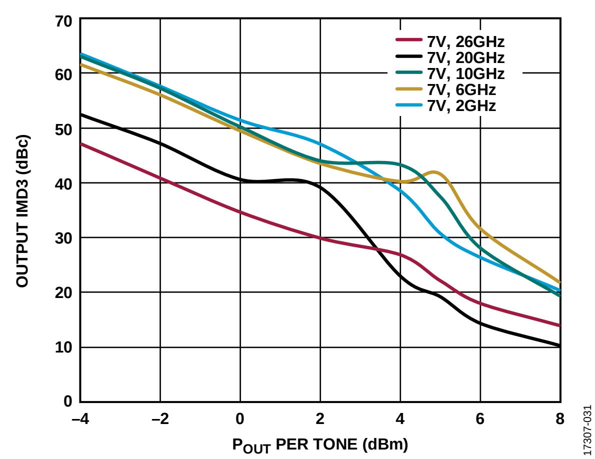


Figure 31. Output IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 7 V

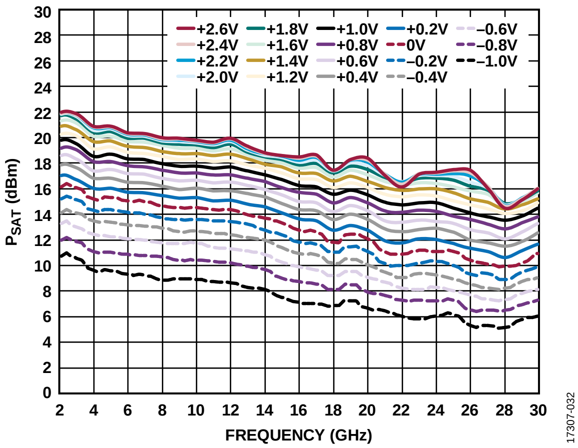


Figure 32. P_{SAT} vs. Frequency at Various $V_{GG}2$ Voltages

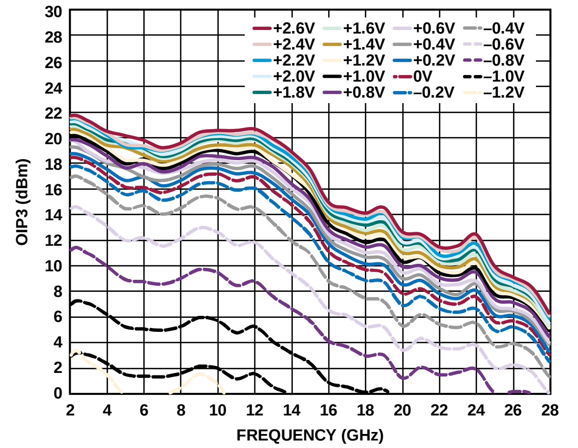


Figure 35. OIP3 vs. Frequency at Various $V_{GG}2$ Voltages

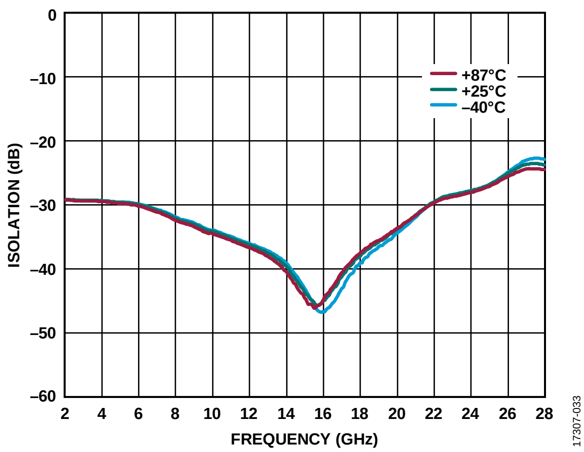


Figure 33. Isolation vs. Frequency over Various Temperatures

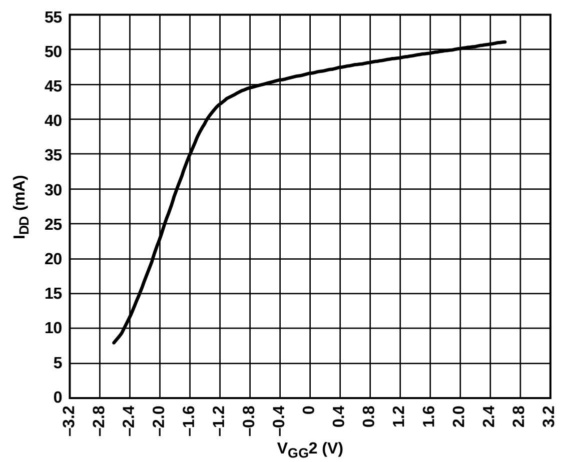


Figure 36. I_{DD} vs. $V_{GG}2$ Voltages, V_{DD} = 5 V

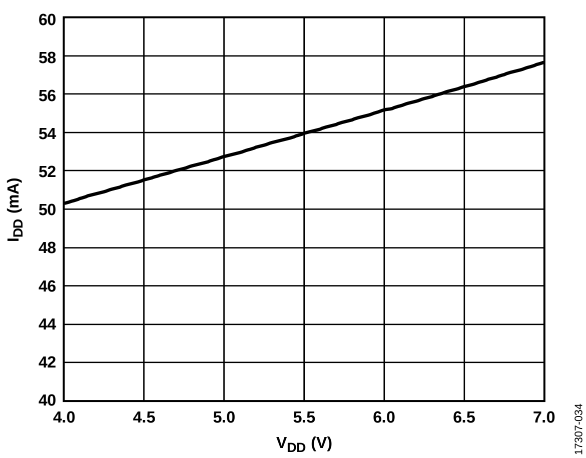


Figure 34. I_{DD} vs. V_{DD}

THEORY OF OPERATION

The ADL9006 is a GaAs, pHEMT, MMIC low noise amplifier. The basic architecture of the ADL9006 is that of a single-supply, biased, cascode distributed amplifier with an integrated RF choke for the drain. A simplified schematic of this architecture is shown in Figure 37.

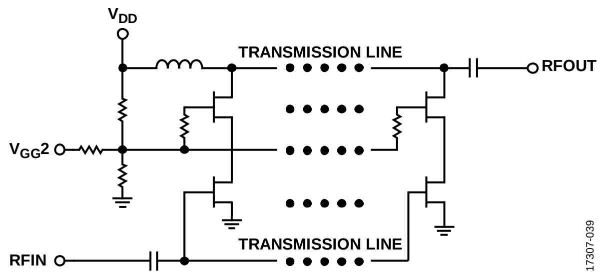


Figure 37. Architecture and Simplified Schematic

Though the gate bias voltages of the upper field effect transistors (FETs) are set internally by a resistive voltage divider tapped off of V_{DD}, the $V_{GG}2$ pin is provided to allow the user an optional means of changing the gate bias of the upper FETs. Adjustment of the $V_{GG}2$ pin voltage across the range of −2.0 V to +2.6 V changes the gate bias of the upper FETs, thus affecting gain changes, depending on the frequency (see Figure 17).

APPLICATIONS INFORMATION

BIASING PROCEDURES

Capacitive bypassing is required for V_{DD}, as shown in the typical application circuit in Figure 38. Gain control is possible through the application of a dc voltage to the $V_{GG}2$ pin. If gain control is used, $V_{GG}2$ must be bypassed by a 100 pF capacitor, a 0.01 µF capacitor, and a 4.7 µF capacitor. If gain control is not used, $V_{GG}2$ can be either left open or capacitively bypassed, as shown in Figure 38.

The recommended bias sequence during power-up is as follows:

1. Set V_{DD} to 5 V (this setting results in an I_{DD} near its specified typical value).
2. If the gain control function is used, apply a voltage within the range of −2.0 V to +2.6 V to $V_{GG}2$ until the desired gain is achieved.
3. Apply the RF input signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF input signal.
2. Remove the $V_{GG}2$ voltage or set it to 0 V.
3. Set V_{DD} to 0 V.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 38), biased per the conditions in the Specifications section. The bias conditions shown in the Specifications section are the operating points recommended to optimize the overall performance of the device. Operation using other bias conditions may provide performance that differs from what is shown in this data sheet. To obtain the optimal performance while not damaging the device, follow the recommended biasing sequences outlined in this section.

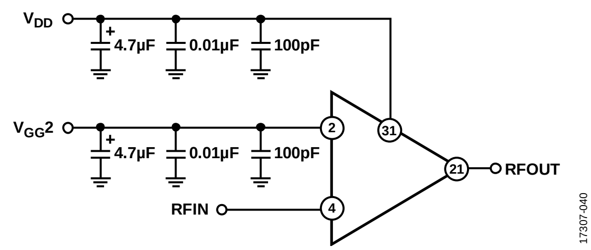


Figure 38. Typical Application Circuit

OUTLINE DIMENSIONS

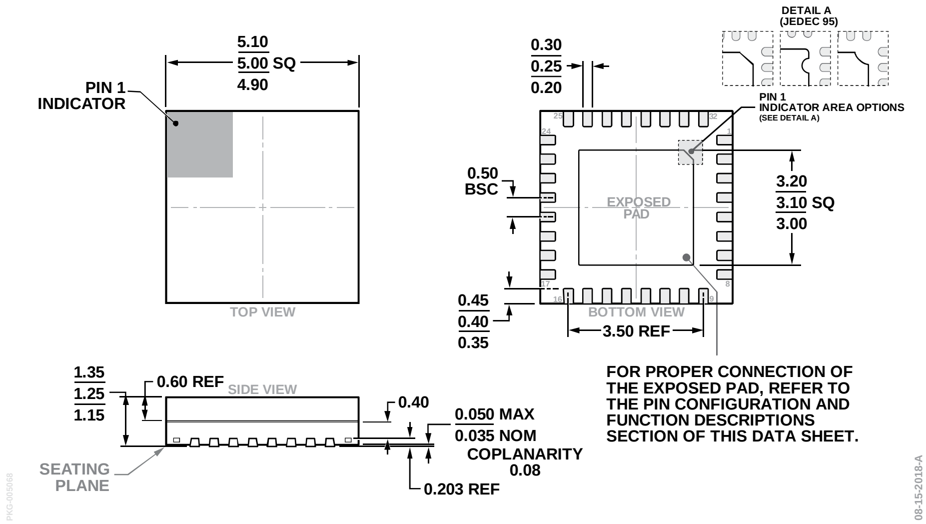


Figure 39. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description[3]	Package Option
ADL9006ACGZN	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
ADL9006ACGZN-R7	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
ADL9006-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section for additional information.
[3] The lead finish of the ADL9006ACGZN and the ADL9006ACGZN-R7 is nickel palladium gold (NiPdAu).