



**THE DATASHEET OF  
MC33152VDR2**



# MC34152, MC33152, NCV33152

## MOSFET Driver, High Speed, Dual

The MC34152/MC33152 are dual noninverting high speed drivers specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, dc-to-dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

This device is available in dual-in-line and surface mount packages.

### Features

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb-Free and Halide-Free Devices

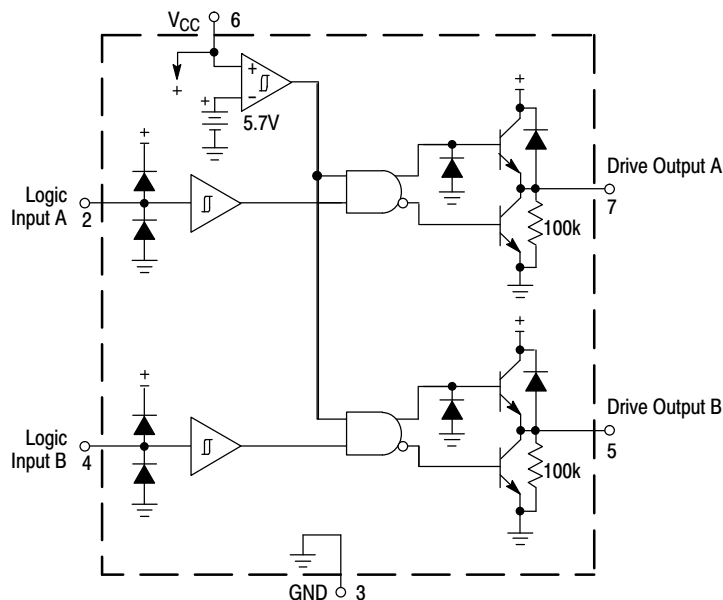


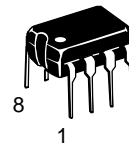
Figure 1. Representative Diagram



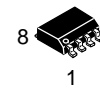
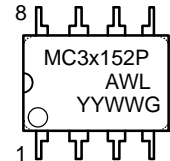
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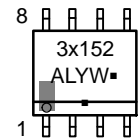
### MARKING DIAGRAMS



PDIP-8  
P SUFFIX  
CASE 626



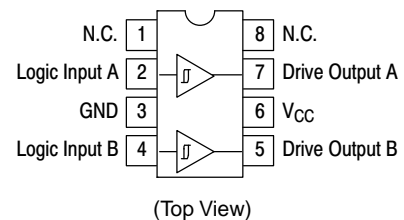
SOIC-8  
D SUFFIX  
CASE 751



x = 3 or 4  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	20	V
Logic Inputs (Note 1)	$V_{in}$	-0.3 to $+V_{CC}$	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to $V_{CC}$ )	$I_O$ $I_{O(clamp)}$	1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751 Maximum Power Dissipation @ $T_A = 50^\circ\text{C}$ Thermal Resistance, Junction-to-Air P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ $T_A = 50^\circ\text{C}$ Thermal Resistance, Junction-to-Air	$P_D$ $R_{\theta JA}$ $P_D$ $R_{\theta JA}$	0.56 180 1.0 100	W $^\circ\text{C/W}$ W $^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Operating Ambient Temperature MC34152 MC33152 MC33152V, NCV33152	$T_A$	0 to +70 -40 to +85 -40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Electrostatic Discharge Sensitivity (ESD) (Note 3) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	2000 200 1500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- For optimum switching speed, the maximum input voltage should be limited to 10 V or  $V_{CC}$ , whichever is less.
- Maximum package power dissipation limits must be observed.
- ESD protection per following tests:  
JEDEC Standard JESD22-A114-F for HBM  
JEDEC Standard JESD22-A115-A for MM  
JEDEC Standard JESD22-C101D for CDM.

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**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 12\text{ V}$ , for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
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## LOGIC INPUTS

Input Threshold Voltage					V
Output Transition High-to-Low State	$V_{IH}$	–	1.75	2.6	
Output Transition Low-to-High State	$V_{IL}$	0.8	1.58	–	
Input Current					$\mu\text{A}$
High State ( $V_{IH} = 2.6\text{ V}$ )	$I_{IH}$	–	100	300	
Low State ( $V_{IL} = 0.8\text{ V}$ )	$I_{IL}$	–	20	100	

## DRIVE OUTPUT

Output Voltage					V
Low State ( $I_{\text{sink}} = 10\text{ mA}$ )	$V_{OL}$	–	0.8	1.2	
( $I_{\text{sink}} = 50\text{ mA}$ )		–	1.1	1.5	
( $I_{\text{sink}} = 400\text{ mA}$ )		–	1.8	2.5	
High State ( $I_{\text{source}} = 10\text{ mA}$ )	$V_{OH}$	10.5	11.2	–	
( $I_{\text{source}} = 50\text{ mA}$ )		10.4	11.1	–	
( $I_{\text{source}} = 400\text{ mA}$ )		10	10.8	–	
Output Pull-Down Resistor	$R_{PD}$	–	100	–	$\text{k}\Omega$

## SWITCHING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Propagation Delay ( $C_L = 1.0\text{ nF}$ )					ns
Logic Input to: Drive Output Rise (10% Input to 10% Output)	$t_{PLH}$ (IN/OUT)	–	55	120	
Drive Output Fall (90% Input to 90% Output)	$t_{PHL}$ (IN/OUT)	–	40	120	
Drive Output Rise Time (10% to 90%)	$t_r$	–	14	30	ns
$C_L = 1.0\text{ nF}$		–	36	–	
$C_L = 2.5\text{ nF}$		–	–	–	
Drive Output Fall Time (90% to 10%)	$t_f$	–	15	30	ns
$C_L = 1.0\text{ nF}$		–	32	–	
$C_L = 2.5\text{ nF}$		–	–	–	

## TOTAL DEVICE

Power Supply Current	$I_{CC}$				mA
Standby (Logic Inputs Grounded)		–	6.0	8.0	
Operating ( $C_L = 1.0\text{ nF}$ Drive Outputs 1 and 2, $f = 100\text{ kHz}$ )		–	10.5	15	
Operating Voltage	$V_{CC}$	6.1	–	18	V

## UNDERVOLTAGE LOCKOUT

Startup Threshold	$V_{th}$	–	5.8	6.1	V
Minimum Operating Voltage After Turn-On ( $V_{CC}$ )	$V_{CC(\text{min})}$	–	5.3	–	V

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

$T_{\text{low}} = 0^\circ\text{C}$  for MC34152,  $-40^\circ\text{C}$  for MC33152,  $-40^\circ\text{C}$  for MC33152V

$T_{\text{high}} = +70^\circ\text{C}$  for MC34152,  $+85^\circ\text{C}$  for MC33152,  $+125^\circ\text{C}$  for MC33152V

NCV33152:  $T_{\text{low}} = -40^\circ\text{C}$ ,  $T_{\text{high}} = +125^\circ\text{C}$ . Guaranteed by design.

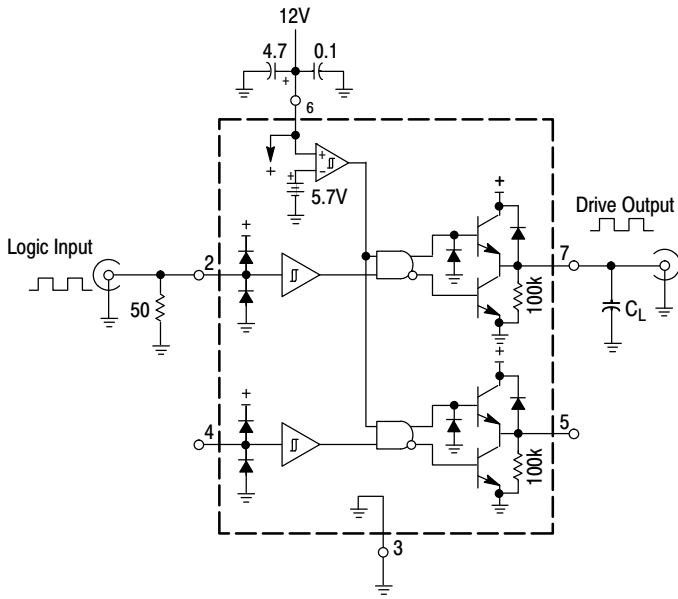


Figure 2. Switching Characteristics Test Circuit

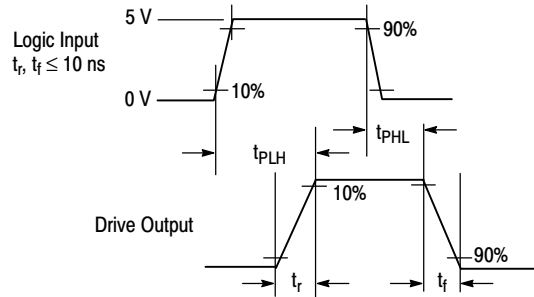


Figure 3. Switching Waveform Definitions

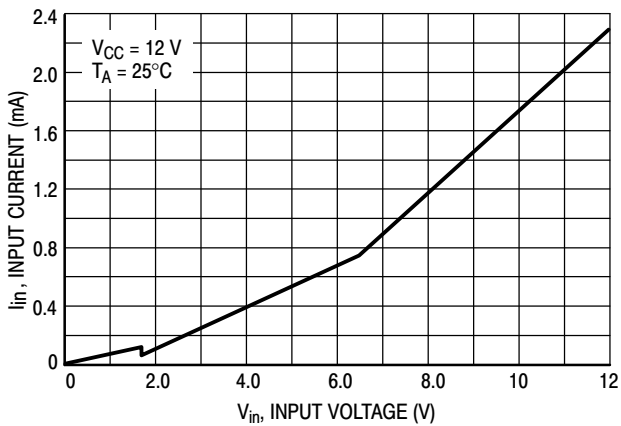


Figure 4. Logic Input Current versus Input Voltage

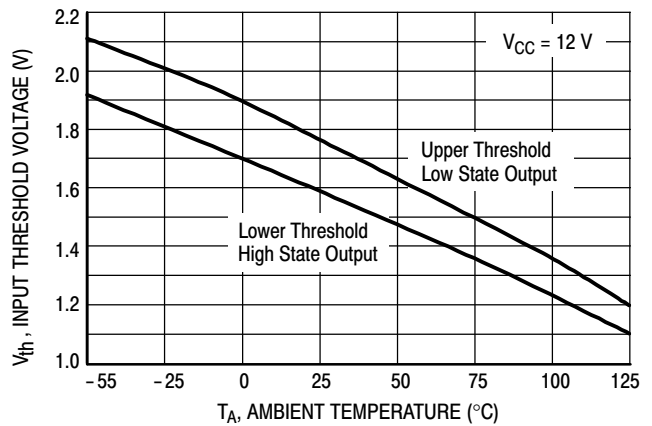


Figure 5. Logic Input Threshold Voltage versus Temperature

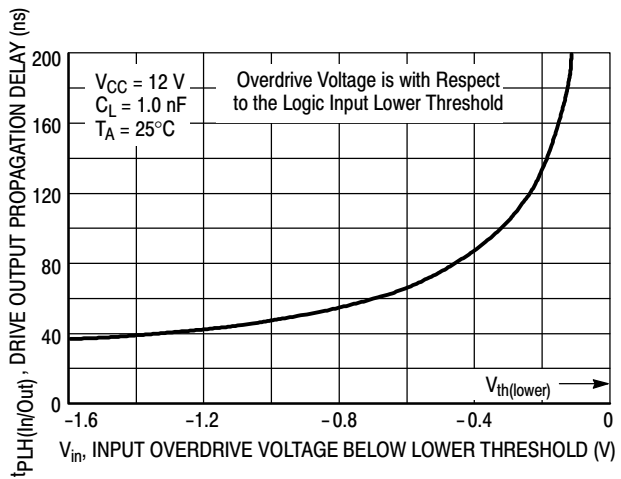


Figure 6. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage

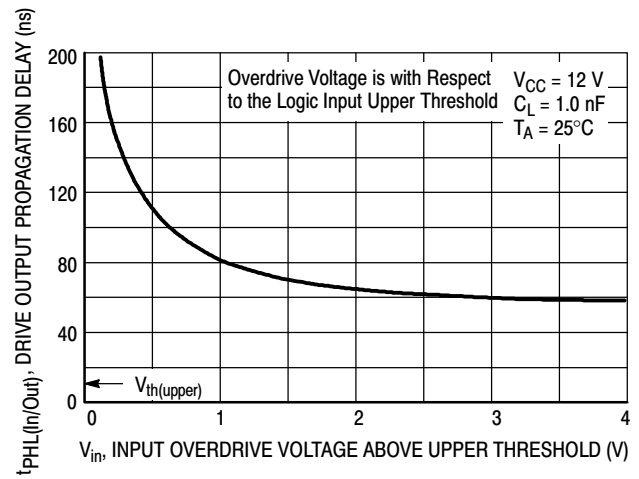
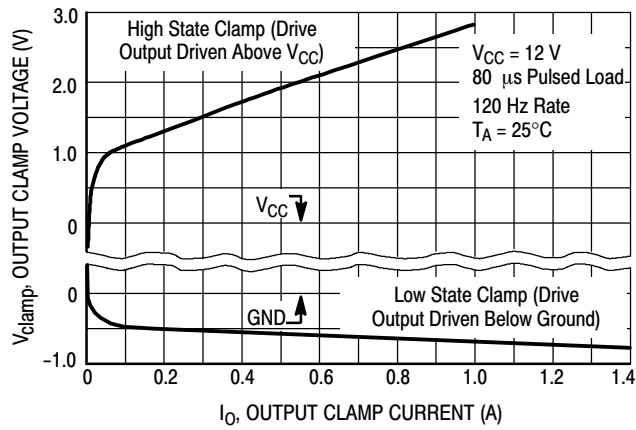
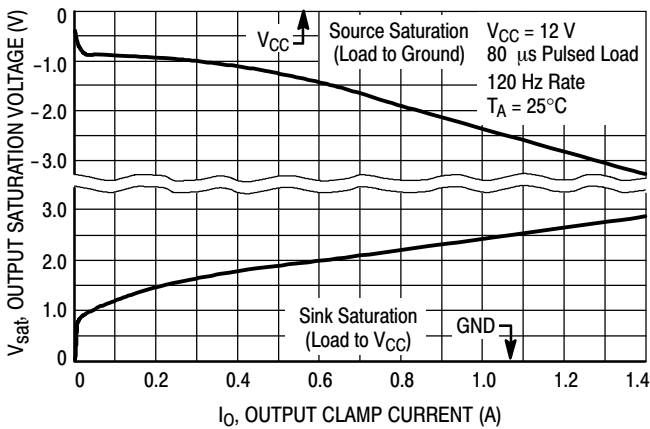


Figure 7. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage

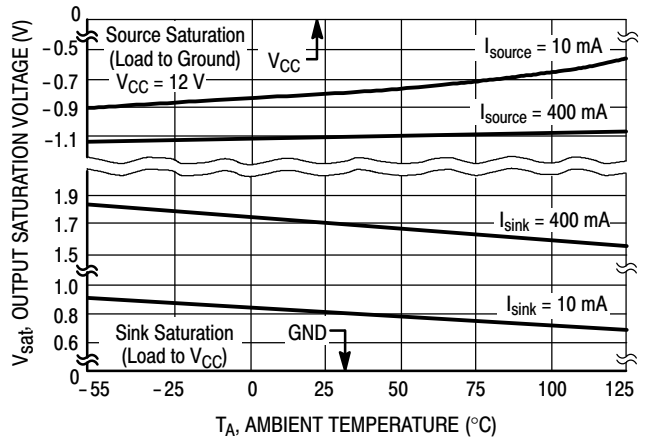
# MC34152, MC33152, NCV33152



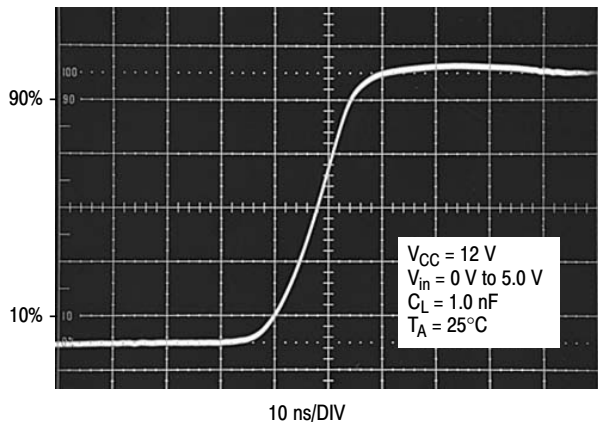
**Figure 8. Drive Output Clamp Voltage versus Clamp Current**



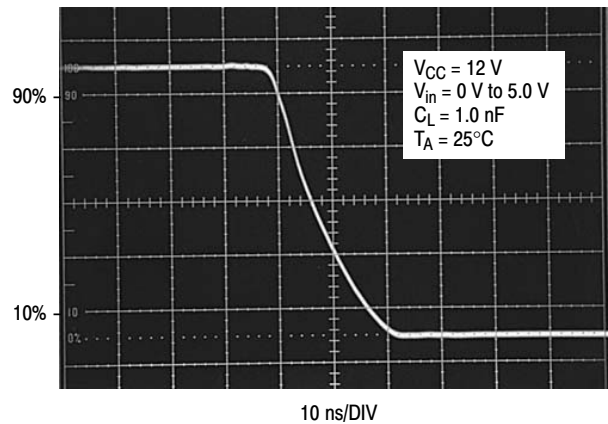
**Figure 9. Drive Output Saturation Voltage versus Load Current**



**Figure 10. Drive Output Saturation Voltage versus Temperature**

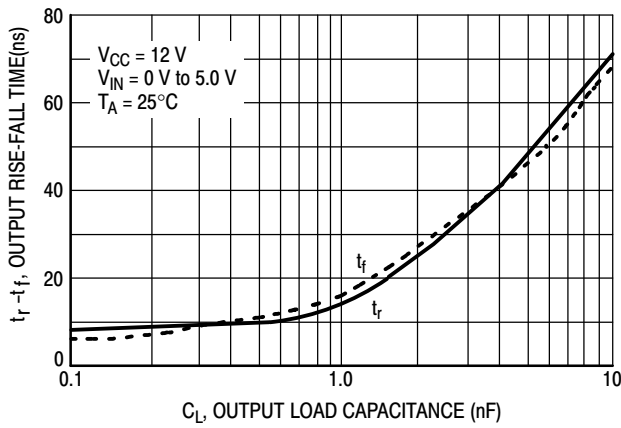


**Figure 11. Drive Output Rise Time**

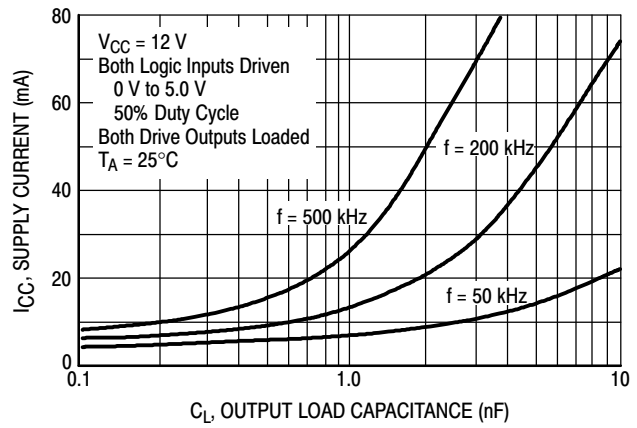


**Figure 12. Drive Output Fall Time**

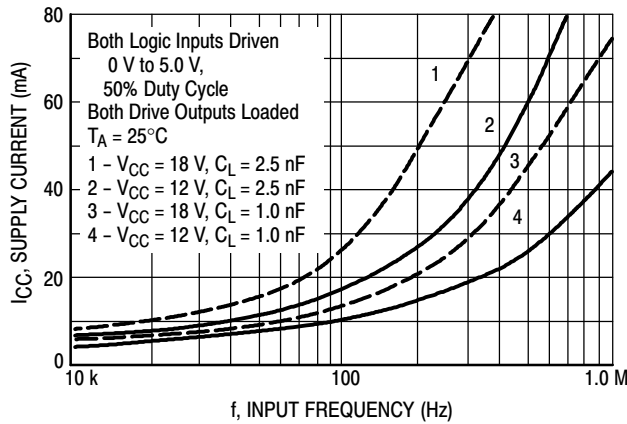
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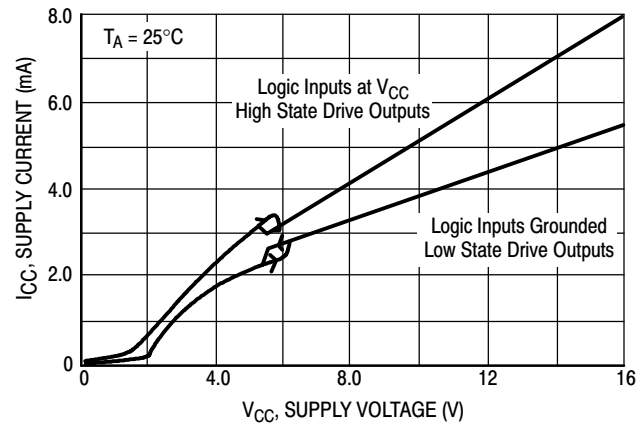
**Figure 13. Drive Output Rise and Fall Time versus Load Capacitance**



**Figure 14. Supply Current versus Drive Output Load Capacitance**



**Figure 15. Supply Current versus Input Frequency**



**Figure 16. Supply Current versus Supply Voltage**

## APPLICATIONS INFORMATION

### Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

### Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to  $V_{CC}$  making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to  $V_{CC}$ . This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a 30 k $\Omega$  pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

### Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4  $\Omega$  at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower  $V_{CC}$  than with comparative CMOS drivers. Each output has a 100 k $\Omega$  pull-down resistor to keep the MOSFET gate low when  $V_{CC}$  is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to  $V_{CC}$  or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above  $V_{CC}$  during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latchup condition. The MC34152 is immune to output latchup. The Drive Outputs contain an internal diode to  $V_{CC}$  for clamping positive voltage transients. When operating with  $V_{CC}$  at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pullup transistor. Since full supply voltage is applied across

the NPN pullup during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

**Undervoltage Lockout**

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as  $V_{CC}$  rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

**Power Dissipation**

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

- where:  $T_J$  = Junction Temperature  
 $T_A$  = Ambient Temperature  
 $P_D$  = Power Dissipation  
 $R_{\theta JA}$  = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

- where:  $P_Q$  = Quiescent Power Dissipation  
 $P_C$  = Capacitive Load Power Dissipation  
 $P_T$  = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} (I_{CCL} [1-D] + I_{CCH} [D])$$

- where:  $I_{CCL}$  = Supply Current with Low State Drive Outputs  
 $I_{CCH}$  = Supply Current with High State Drive Outputs  
 $D$  = Output Duty Cycle

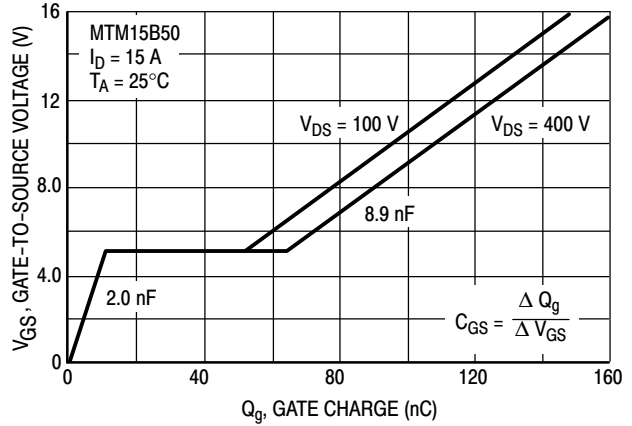
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

- where:  $V_{OH}$  = High State Drive Output Voltage  
 $V_{OL}$  = Low State Drive Output Voltage  
 $C_L$  = Load Capacitance  
 $f$  = Frequency

When driving a MOSFET, the calculation of capacitive load power  $P_C$  is somewhat complicated by the changing gate to source capacitance  $C_{GS}$  as the device switches. To

aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge  $Q_g$  of 110 nC is required when operating the MOSFET with a drain to source voltage  $V_{DS}$  of 400 V.



**Figure 17. Gate-to-Source Voltage versus Gate charge**

The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_{CC} Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34152 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34152 at a higher  $V_{CC}$ , additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08 V_{CC} C_L f - 8 \times 10^{-4})$$

$P_T$  must be greater than zero.

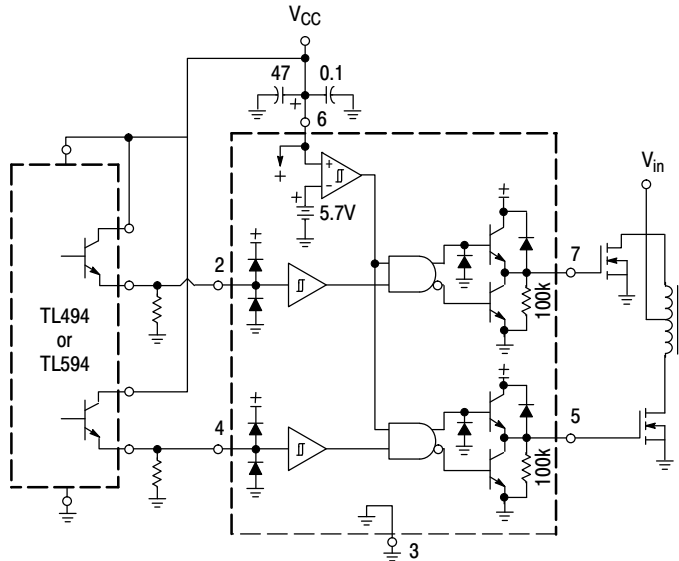
Switching time characterization of the MC34152 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive

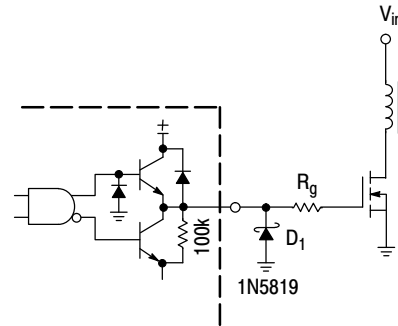
performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the  $V_{CC}$  pin and ground as the layout will permit. Suggested capacitors are a low inductance  $0.1 \mu\text{F}$  ceramic in parallel with a  $4.7 \mu\text{F}$  tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

**Proper printed circuit board layout is extremely critical and cannot be over emphasized.**



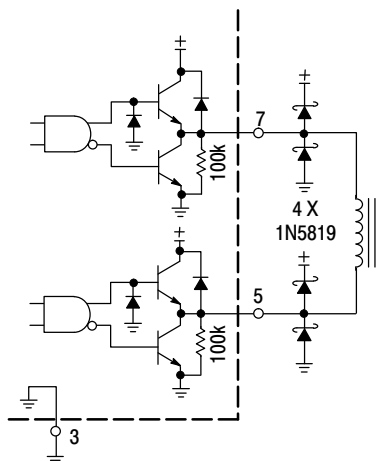
The MC34152 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 18. Enhanced System Performance with Common Switching Regulators



Series gate resistor  $R_g$  may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.  $R_g$  will decrease the MOSFET switching speed. Schottky diode  $D_1$  can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 19. MOSFET Parasitic Oscillations



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above  $V_{CC}$  and below ground.

Figure 20. Direct Transformer Drive

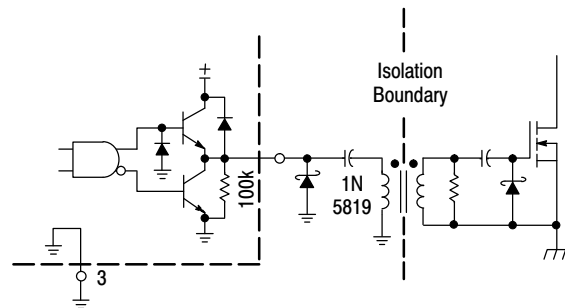
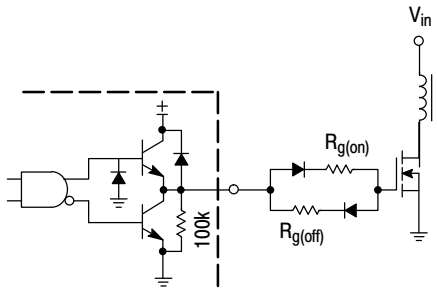


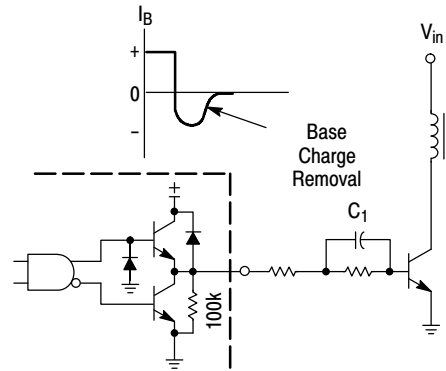
Figure 21. Isolated MOSFET Drive

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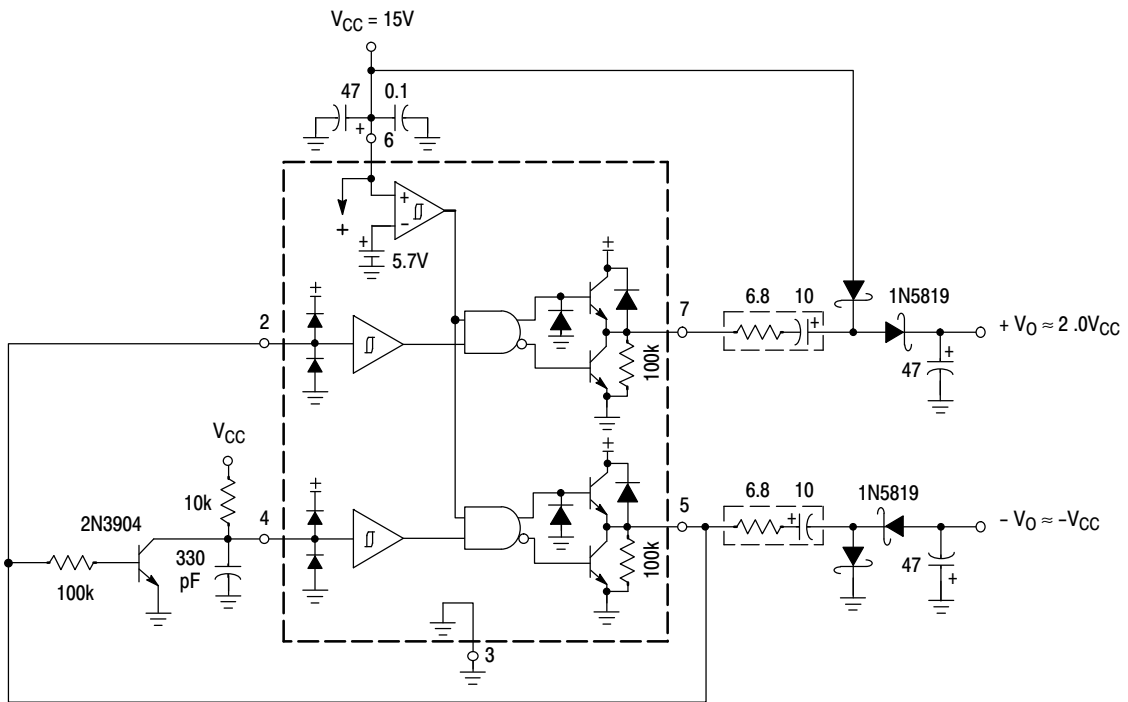
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

**Figure 22. Controlled MOSFET Drive**



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C<sub>1</sub>.

**Figure 23. Bipolar Transistor Drive**



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

**Figure 24. Dual Charge Pump Converter**

Output Load Regulation		
I <sub>O</sub> (mA)	+V <sub>O</sub> (V)	-V <sub>O</sub> (V)
0	27.7	-13.3
1.0	27.4	-12.9
10	26.4	-11.9
20	25.5	-11.2
30	24.6	-10.5
50	22.6	-9.4

## MC34152, MC33152, NCV33152

### ORDERING INFORMATION

Device	Package	Shipping†
MC34152DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC34152DR2G	SOIC-8 (Pb-Free)	2500 Tape & Reel
MC34152PG	PDIP-8 (Pb-Free)	50 Units / Rail
MC33152DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33152DR2G	SOIC-8 (Pb-Free)	2500 Tape & Reel
MC33152PG	PDIP-8 (Pb-Free)	50 Units / Rail
MC33152VDG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33152VDR2G	SOIC-8 (Pb-Free)	2500 Tape & Reel
NCV33152DR2G*	SOIC-8 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV prefix is for automotive and other applications requiring site and change control.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

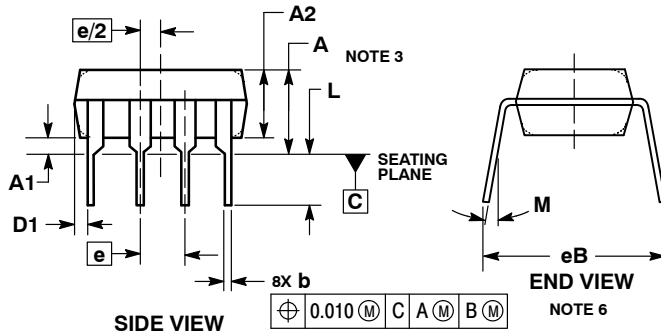
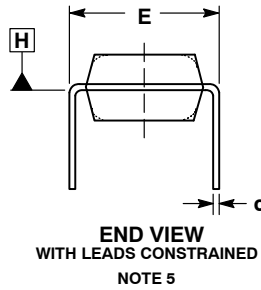
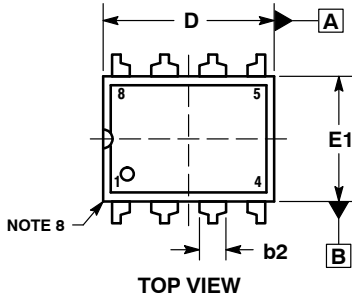
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SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015

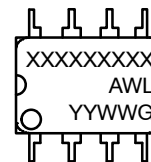


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

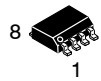
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:  
PIN 1. AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

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DESCRIPTION:	PDIP-8	PAGE 1 OF 1

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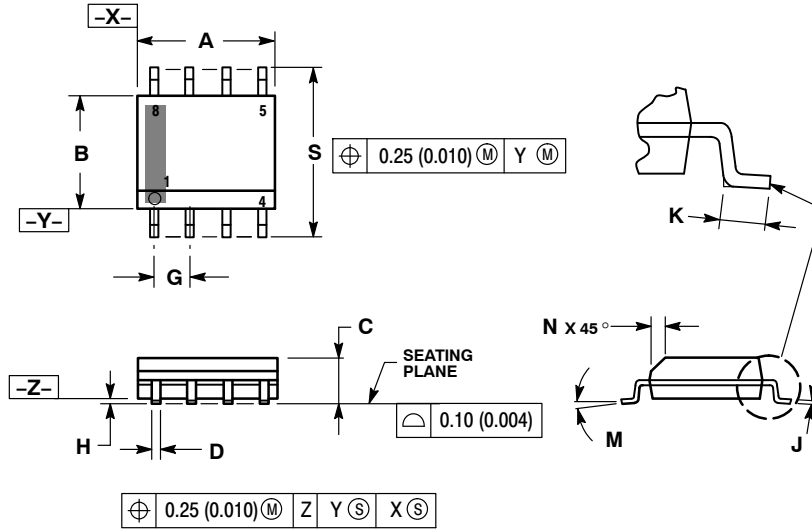
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

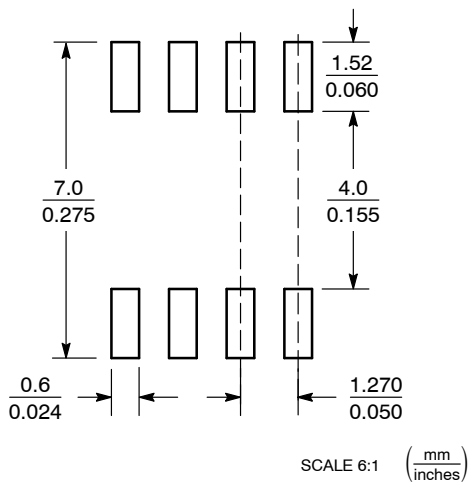
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

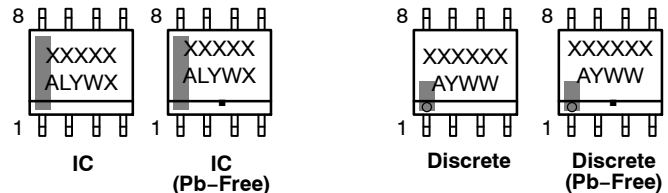
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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