



**THE DATASHEET OF  
PL135-37SC-R**



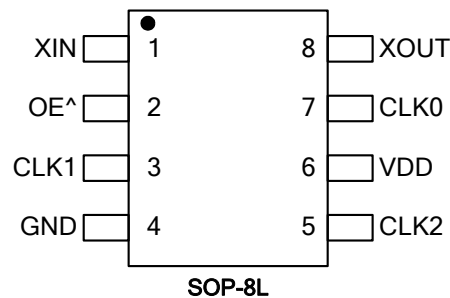
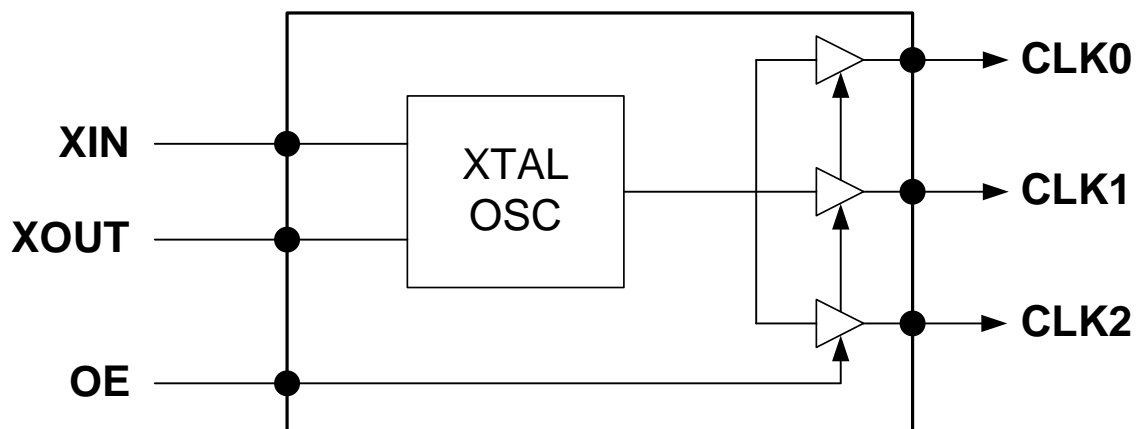
**Low Power, 1.62V to 3.63V, 10MHz to 40MHz, 1:3 Oscillator Fanout Buffer****FEATURES**

- Advanced Oscillator Design for Wide Frequency Coverage
- 3 LVCMOS Outputs
- 12 mA Output Drive Strength
- Input/Output Frequency:
  - Fundamental Crystal: 10MHz to 40MHz
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.62V to 3.63V Power Supply
- Available in SOP-8L GREEN/RoHS Compliant Package

**DESCRIPTION**

The PL135-37 is an advanced oscillator fanout buffer design for high performance, low-power applications. The PL135-37 accepts a fundamental crystal input of 10MHz to 40MHz and produces three LVCMOS outputs of the same frequency. The Output Enable (OE) function can be used to tri-state the outputs.

The PL135-27 offers the best phase noise and jitter performance and lowest power consumption of any comparable IC.

**PACKAGE PIN CONFIGURATION****BLOCK DIAGRAM**

## Low Power, 1.62V to 3.63V, 10MHz to 40MHz, 1:3 Oscillator Fanout Buffer

### PIN DESCRIPTION

Name	SOP-8L	Type	Description
XIN	1	I	Crystal input
OE	2	I	Output enable input. This pin has internal pull-up resistor. All outputs will be tri-stated when pulled low.
CLK1	3	O	Output clock
GND	4	P	Ground connection
CLK2	5	O	Output clock
VDD	6	P	Power supply
CLK0	7	O	Output clock
XOUT	8	I	Crystal output

\* **Note:** This pin includes an internal 60KΩ pull up.

### LAYOUT RECOMMENDATIONS

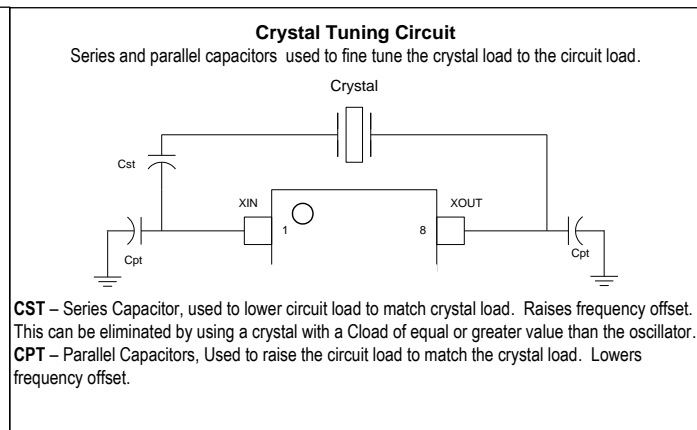
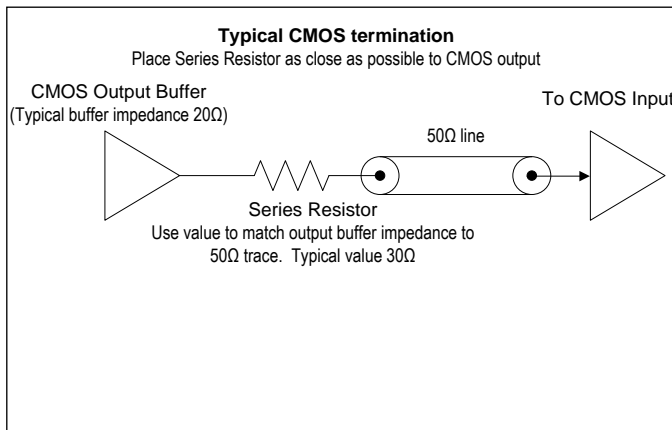
The following guidelines are to assist you with a performance optimized PCB design:

#### Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

#### Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V<sub>DD</sub> pin(s) to limit noise from the power supply
- Multiple V<sub>DD</sub> pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V<sub>DD</sub> can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical value to use is 0.1μF.



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**ELECTRICAL SPECIFICATIONS**
**ABSOLUTE MAXIMUM RATINGS**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	$V_{DD}$	-0.5	4.6	V
Input Voltage Range	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

**AC SPECIFICATIONS**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal	10		40	MHz
Settling Time	At power-up ( $V_{DD} \geq 1.62V$ )			5	ms
Output Enable Time	OE Function; $T_a=25^\circ C$ , 10pF Load			10	ns
$V_{DD}$ Sensitivity	Frequency vs. $V_{DD}$ , $\pm 10\%$	-1		1	ppm
Output Rise Time	15pF Load, 10/90% $V_{DD}$ , 3.3V		2	3	ns
Output Fall Time	15pF Load, 90/10% $V_{DD}$ , 3.3V		2	3	ns
Output to Output Skew	Under all conditions			250	ps
Duty Cycle	Under all conditions	45	50	55	%

**DC SPECIFICATIONS**

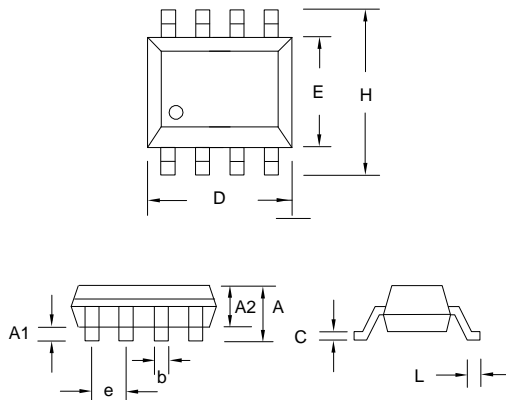
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	$I_{DD}$	$V_{DD} = 3.3V$ , 25MHz, No Load		4		mA
		$V_{DD} = 2.5V$ , 25MHz, No Load		3		mA
		$V_{DD} = 1.8V$ , 25MHz, No Load		2		mA
Supply Current, Standby	$I_{DD\_SB}$	OE Pin Pulled Low, 25MHz, 3.3V			0.6	mA
Operating Voltage	$V_{DD}$		1.62		3.63	V
Output Low Voltage	$V_{OL}$	$I_{OL} = +12mA$ , 3.3V			0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -12mA$ , 3.3V	2.4			V
Output Current	$I_{OSD}$	$V_{OL} = 0.4V$ , $V_{OH} = 2.4V$	12			mA

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**CRYSTAL SPECIFICATIONS**

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	$F_{XIN}$	10		40	MHz
Crystal Loading Rating	$C_{L(xtal)}$		8.5		pF
Maximum Sustainable Drive Level				200	$\mu$ W
Operating Drive Level			50		$\mu$ W
Crystal Shunt Capacitance	$C_0$			3	pF
Effective Series Resistance	ESR			30	$\Omega$

**PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)**
**SOP-8L**

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



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## ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

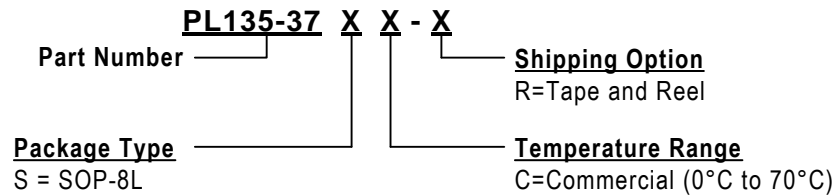
**For part ordering, please contact our Sales Department:**

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

### PART NUMBER

The order number for this device is a combination of the following:  
Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
PL135-37SC-R	P135-37 SC LLLLL	8-Pin SOP-8L (Tape and Reel)

\*Note: LLLLL designates lot number

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