THE DATASHEET OF

ATMEGA88PB-ANR

ATmega48PB/88PB/168PB

AVR Microcontroller with Core Independent Peripherals and PicoPower technology

Introduction

ATmega48PB/88PB/168PB is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48PB/88PB/168PB achieves throughputs approaching 1MIPS/MHz, allowing the system designer to optimize power consumption versus processing speed.

Features

- Advanced RISC architecture
  - 131 instructions – most single clock cycle execution
  - 32 x 8 general purpose working registers
  - Fully static operation
  - Up to 20MIPS throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High endurance non-volatile memory segments
  - 4/8/16KBytes of in-system self-programmable Flash program memory
  - 256/512/512Bytes EEPROM
  - 512/1K/1KBytes internal SRAM
  - Write/Erase cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C
  - Optional boot code section with independent lock bits
    - In-system programming by on-chip boot program
    - True Read-While-Write (RWW) operation
  - Programming lock for software security
- QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix® acquisition
  - Up to 64 sense channels
- Peripheral Features
  - Two 8-bit Timer/Counters (TC) with separate prescaler and compare mode
  - 16-bit Timer/Counter with separate prescaler, compare mode, and capture mode
  - Real Time Counter (RTC) with separate oscillator
  - Six Pulse Width Modulation (PWM) channels
  - 8-channel 10-bit Analog-to-Digital converter (ADC) with temperature measurement
  - Programmable serial USART with start-of-frame detection

  - Master/Slave Serial Interface (SPI)
  - Byte-oriented Two-Wire serial Interface (TWI), Philips I^2C compatible
  - Programmable Watchdog Timer (WDT) with separate on-chip oscillator
  - On-chip Analog Comparator (AC)
  - Interrupt and Wake-up on pin change
    - 256-channel capacitive touch and proximity sensing
- Special microcontroller features
  - Power-On Reset (POR) and programmable brown-out detection (BOD)
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-Save, Power-Down, Standby, and Extended Standby
  - Unique device ID
- I/O
  - 27 programmable I/O pins
- Packages
  - 32-pin TQFP, VFQFN
- Operating voltage
  - 1.8V – 5.5V
- Temperature range
  - -40°C to 105°C
- Speed grades
  - 0 - 4MHz at 1.8-5.5V
  - 0 - 10MHz at 2.7-5.5.V
  - 0 - 20MHz at 4.5-5.5V
- Power consumption at 1MHz, 1.8V, 25°C
  - Active mode: 0.35mA
  - Power-down mode: 0.23µA
  - Power-save mode: <1.4µA (including 32kHz RTC)

Table of Contents

1. Description

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48PB/88PB/168PB provides the following features: 4/8/16Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512 bytes EEPROM, 512/1K/1Kbytes SRAM, 27 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface (I²C), an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and VFQFN packages), a programmable Watchdog Timer with internal Oscillator, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

It offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows programers to explore, develop and debug the their touch applications.

The device is manufactured using high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the ATmega48PB/88PB/168PB is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48PB/88PB/168PB is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and Evaluation kits.

2. Configuration Summary

Table 2-1. Configuration Summary

	ATmega48PB	ATmega88PB	ATmega168PB
Pin count	32	32	32
Flash (KB)	4	8	16
SRAM (Bytes)	512	1024	1024
EEPROM (Bytes)	256	512	512
Max I/O pins	27		
SPI	1		
TWI (I^2C)	1		
USART	1		
ADC	10-bit 15ksps		
ADC channels	8		
AC	1		
8-bit Timer/Counters	2		
16-bit Timer/Counters	1		
PWM channels	6		
Operating voltage	1.8V - 5.5V		
Max operating frequency	20MHz		
Temperature range	-40°C to +105°C		

3. Ordering Information

3.1 ATmega48PB

Speed [MHz](3)	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega48PB-AU ATmega48PB-AUR(4) ATmega48PB-MU ATmega48PB-MUR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +85°C)
		ATmega48PB-AN ATmega48PB-ANR(4) ATmega48PB-MN ATmega48PB-MNR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

Note:

1. This device can also be supplied in wafer form. Contact your local sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. See ”Speed Grades” on page 304.
4. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

3.2 ATmega88PB

Speed [MHz](3)	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega88PB-AU ATmega88PB-AUR(4) ATmega88PB-MU ATmega88PB-MUR(4)	32A 32A 32MS1 32MS	Industrial (-40°C to +85°C)
		ATmega88PB-AN ATmega88PB-ANR(4)ATmega88PB-MN ATmega88PB-MNR(4)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

Note:

1. This device can also be supplied in wafer form. Contact your local sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.
3. See ”Speed Grades” on page 304.
4. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

3.3 ATmega168PB

Speed [MHz]	Power Supply [V]	Ordering Code(2)	Package(1)	Operational Range
20	1.8 - 5.5	ATmega168PB-AU ATmega168PB-AUR(3) ATmega168PB-MU ATmega168PB-MUR(3)	32A 32A 32MS1 32MS1	Industrial (-40°C to +85°C)
		ATmega168PB-AN ATmega168PB-ANR(3) ATmega168PB-MN ATmega168PB-MNR(3)	32A 32A 32MS1 32MS1	Industrial (-40°C to +105°C)

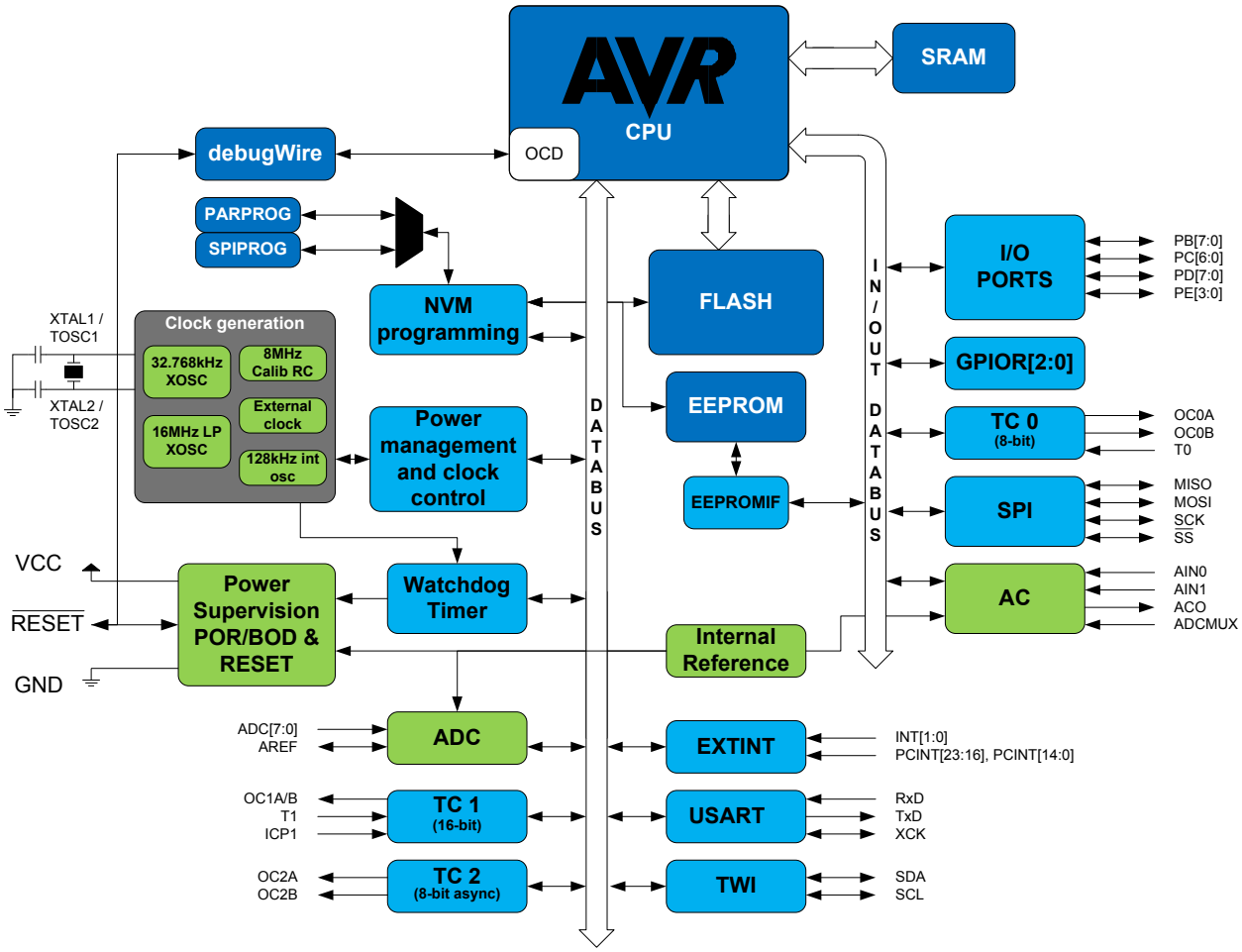
Note:

1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.
3. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VFQFN)

4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Configurations

Figure 5-1. 32 TQFP Pinout ATmega48PB/88PB/168PB

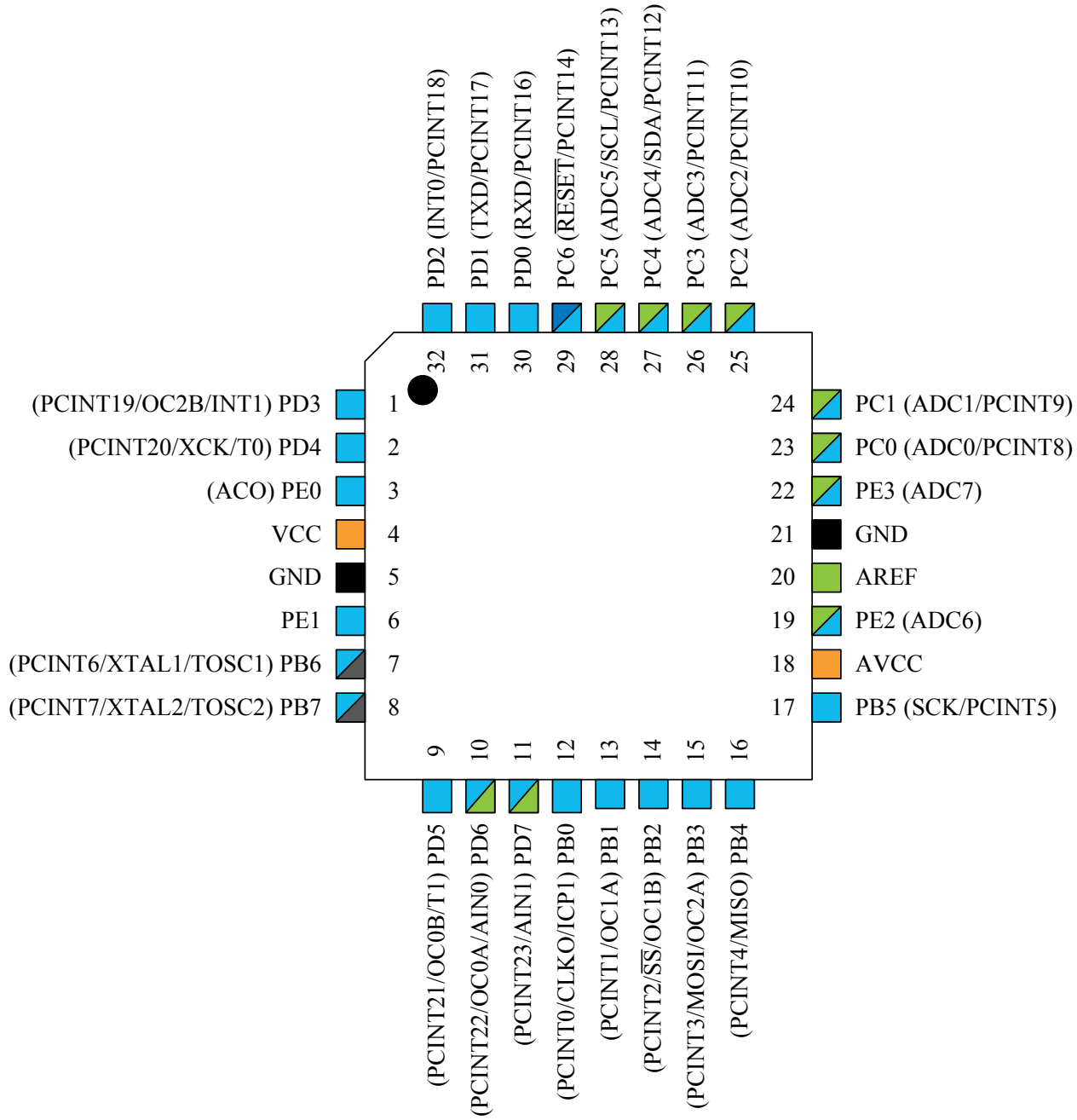
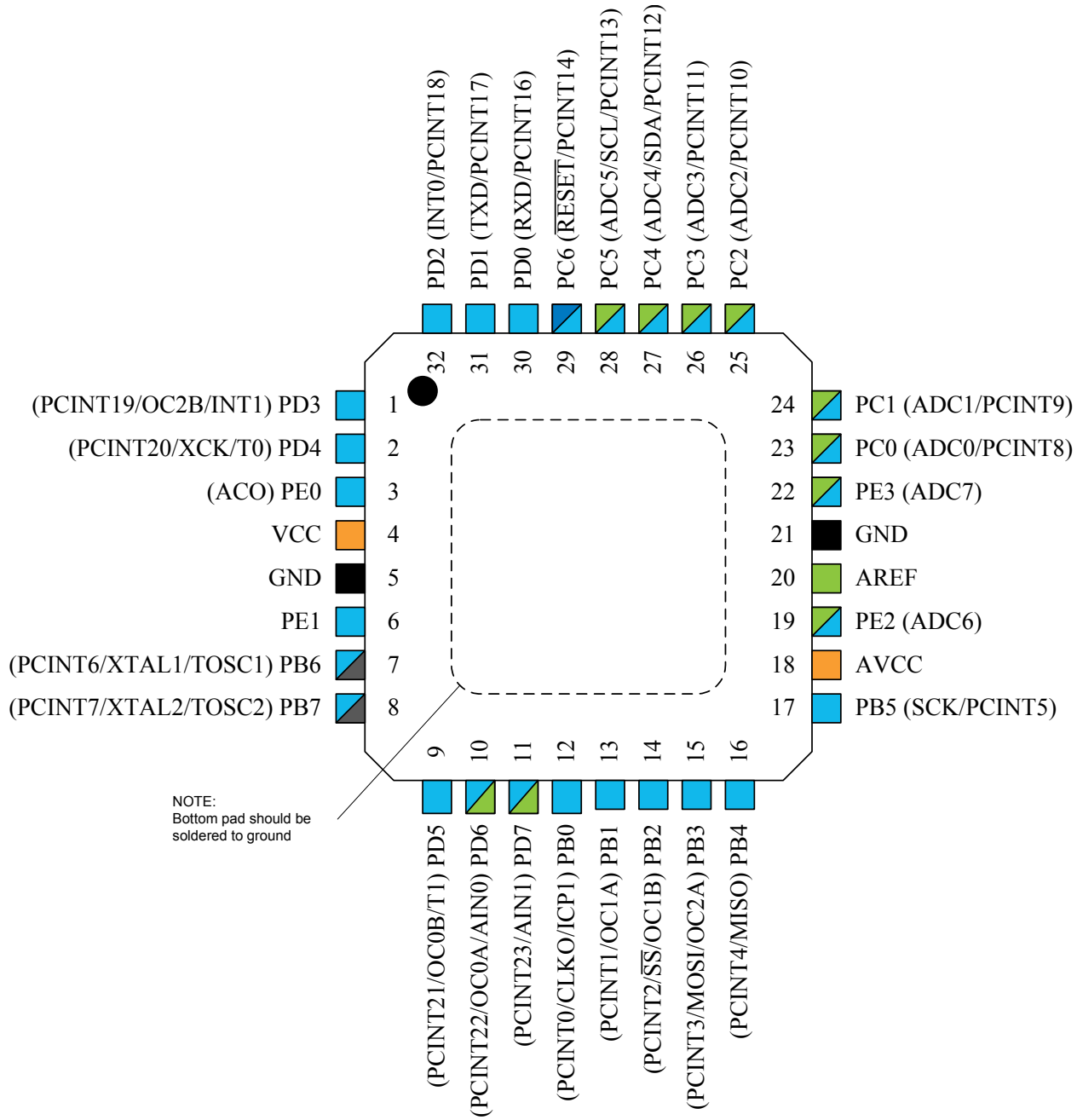


Figure 5-2. 32 VQFN Pinout ATmega48PB/88PB/168PB



5.1 Pin Descriptions

5.1.1 VCC

Digital supply voltage.

5.1.2 GND

Ground.

5.1.3 Port B (PB[7:0]) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each pin). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated during a reset condition even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB[7:6] is used as TOSC[2:1] input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

5.1.4 Port C (PC[5:0])

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each pin). The PC[5:0] output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated during a reset condition even if the clock is not running.

5.1.5 PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in the *Alternate Functions of Port C* section.

5.1.6 Port D (PD[7:0])

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each pin). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated during a reset condition even if the clock is not running.

5.1.7 Port E (PE[3:0])

Port E is an 4-bit bi-directional I/O port with internal pull-up resistors (selected for each pin). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated during a reset condition even if the clock is not running.

5.1.8 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC[3:0], and PE[3:2]. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC[6:4] use digital supply voltage, V_{CC}.

5.1.9 AREF

AREF is the analog reference pin for the A/D Converter.

5.1.10 ADC[7:6] (TQFP and VFQFN Package Only)

In the TQFP and VFQFN package, ADC[7:6] serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

No	PAD	EXTINT	PCINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
1	PD[3]	INT1	PCINT19			OC2B				
2	PD[4]		PCINT20			T0		XCK		
3	PE[0]			ACO						
4	VCC									
5	GND									
6	PE[1]									
7	PB[6]		PCINT6		XTAL1/TOSC1					
8	PB[7]		PCINT7		XTAL2/TOSC2					
9	PD[5]		PCINT21			OC0B	T1			
10	PD[6]		PCINT22	AIN0		OC0A				
11	PD[7]		PCINT23	AIN1						
12	PB[0]		PCINT0		CLKO	ICP1				
13	PB[1]		PCINT1			OC1A				
14	PB[2]		PCINT2			OC1B				$\overline{SS}$
15	PB[3]		PCINT3			OC2A				MOSI
16	PB[4]		PCINT4							MISO
17	PB[5]		PCINT5							SCK
18	AVCC									
19	PE[2]			ADC6						
20	AREF									
21	GND									
22	PE[3]			ADC7						
23	PC[0]		PCINT8	ADC0						
24	PC[1]		PCINT9	ADC1						
25	PC[2]		PCINT10	ADC2						
26	PC[3]		PCINT11	ADC3						
27	PC[4]		PCINT12	ADC4					SDA	
28	PC[5]		PCINT13	ADC5					SCL	
29	PC[6]/$\overline{RESET}$		PCINT14							
30	PD[0]		PCINT16					RXD		
31	PD[1]		PCINT17					TXD		
32	PD[2]	INT0	PCINT18							

7. Comparison Between Processors

The ATmega48PB/88PB/168PB differ only in memory sizes, boot loader support, and interrupt vector sizes. The table below summarizes the different memory and interrupt vector sizes for the devices.

Table 7-1. Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48PB	4KBytes	256Bytes	512Bytes	1 instruction word/vector
ATmega88PB	8KBytes	512Bytes	1KBytes	1 instruction word/vector
ATmega168PB	16KBytes	512Bytes	1KBytes	2 instruction words/vector

ATmega88PB/168PB support a real Read-While-Write Self-Programming Mechanism (SPM). The SPM instruction can only execute from the separate Boot Loader Section. In ATmega48PB there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.

8. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.microchip.com/design-centers/8-bit/microchip-avr-mcus.

9. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

10. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

11. Capacitive Touch Sensing

11.1 QTouch Library

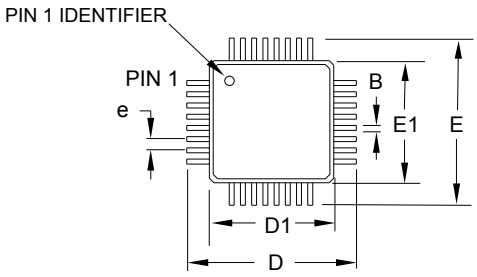
The QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most AVR® microcontrollers. The QTouch Library includes support for the Touch and QMatrix® acquisition methods.

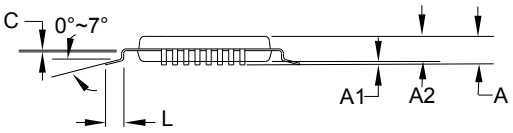
Touch sensing can be added to any application by linking the appropriate QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and down-loadable from QTouch Library . For implementation details and other information, refer to the QTouch Library User Guide - also available for download from the website.

12. Packaging Information

12.1 32-pin 32A





COMMON DIMENSIONS
(Unit of measure = mm)

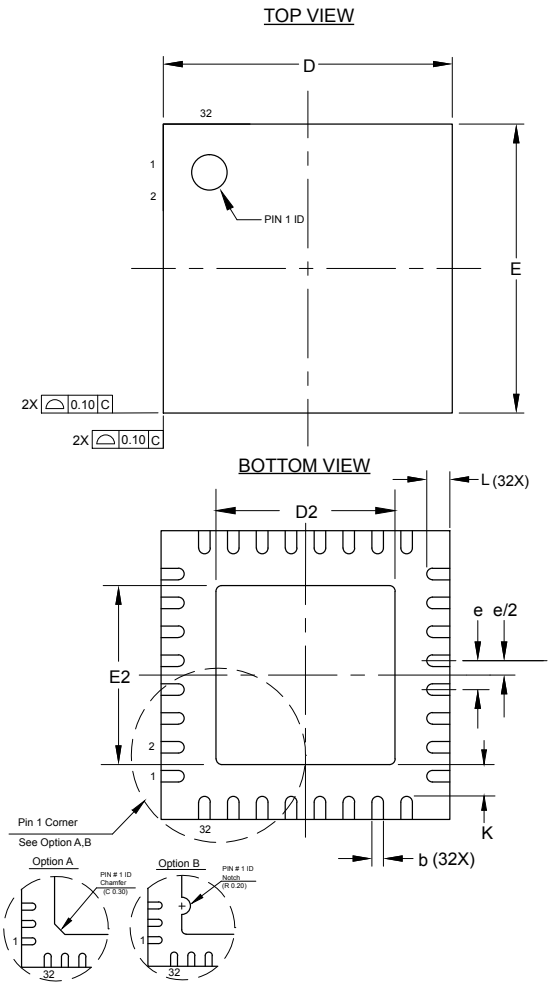
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel	**32A,**32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)	32A	C

12.2 32-pin 32MS1



NOTE:

1. Refer to JEDEC Drawing MO-220, Variation VHHD-2 (Figure 1/Saw Singulation)
2. Dimension “b” applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimensions should not be measured in that radius area.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.80	-	0.90	
A1	0.00	-	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	2
D	4.90	5.00	5.10	
D2	3.00	3.10	3.20	
E	4.90	5.00	5.10	
E2	3.00	3.10	3.20	
e	-	0.50	-	
L	0.30	0.40	0.50	
K	0.20	-	-	

12/4/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 32MS1, 32-pad 5.0x5.0x0.9 mm Body, 0.50mm pitch, 3.1x3.1 mm Exposed pad, Saw Singulated Thermally Enhanced Plastic Very-thin Fine pitch, Quad Flat No Lead package (VFQFN)	**GPC** ZMF	**DRAWING NO.** 32MS1	**REV.** A

13. Errata

13.1 Errata ATmega48PB

The revision letter in this section refers to the revision of the ATmega48PB device.

13.1.1 Rev. A

– Wrong device ID when using debugWire

– Power consumption in power save modes

– USART start-up functionality not working

– External capacitor on AREF pin

– Increased power consumption when using voltage reference other than AVCC

1.) Wrong device ID when using debugWire

The device ID returned using debugWire is incorrect.

Problem Fix/Workaround

None.

2.) Power consumption in power save modes

Power consumption in power save modes will be higher due to improper control of internal power management.

Problem Fix/Workaround

None.

3.) USART start-up functionality not working

While in power save modes, the USART start bit detection logic fails to wake up the device.

Problem Fix/Workaround

None.

4.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

5.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC. The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep. If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.1.2 Rev. B

– External capacitor on AREF pin

– Power consumption in power save modes

– Increased power consumption when using voltage reference other than AVCC

1.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

2.) Power consumption in power save modes

Power consumption in power save modes will be higher due to improper control of internal power management.

Problem Fix/Workaround

None.

3.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC.The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep.If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.1.3 Rev. C

No known errata.

13.1.4 Rev. D to J

Not sampled.

13.1.5 Rev. K

No known errata.

13.2 Errata ATmega88PB

The revision letter in this section refers to the revision of the ATmega88PB device.

13.2.1 Rev. A

– Wrong device ID when using debugWire

– Power consumption in power save modes

– USART start-up functionality not working

– External capacitor on AREF pin

– Increased power consumption when using voltage reference other than AVCC

1.) Wrong device ID when using debugWire

The device ID returned using debugWire is incorrect.

Problem Fix/Workaround

None.

2.) Power consumption in power save modes

Power consumption in power save modes will be higher due to improper control of internal power management.

Problem Fix/Workaround

None.

3.) USART start-up functionality not working

While in power save modes, the USART start bit detection logic fails to wake up the device.

Problem Fix/Workaround

None.

4.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

5.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC. The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep. If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.2.2 Rev. B

– External capacitor on AREF pin

– Increased power consumption when using voltage reference other than AVCC

1.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

2.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC. The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep. If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.2.3 Rev. C

No known errata.

13.2.4 Rev. D to J

Not sampled.

13.2.5 Rev. K

No known errata.

13.3 Errata ATmega168PB

The revision letter in this section refers to the revision of the ATmega168PB device.

13.3.1 Rev. A

– Wrong device ID when using debugWire

– Power consumption in power save modes

– USART start-up functionality not working

– External capacitor on AREF pin

– Increased power consumption when using voltage reference other than AVCC

1.) Wrong device ID when using debugWire

The device ID returned using debugWire is incorrect.

Problem Fix/Workaround

None.

2.) Power consumption in power save modes

Power consumption in power save modes will be higher due to improper control of internal power management.

Problem Fix/Workaround

None

3.) USART start-up functionality not working

While in power save modes, the USART start bit detection logic fails to wakeup the device.

Problem Fix/Workaround

None.

4.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

5.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC. The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep. If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.3.2 Rev. B

– Power consumption in power save modes

– External capacitor on AREF pin

– Increased power consumption when using voltage reference other than AVCC

1.) Power consumption in power save modes

Power consumption in power save modes will be higher due to improper control of internal power management.

Problem Fix/Workaround

None

2.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

3.) Increased power consumption when using voltage reference other than AVCC

Power consumption is higher when using internal or external voltage reference that is not equal to AVCC. The increased current consumption will be the same for active and all sleep modes, but the largest impact will be in low power sleep modes.

Problem Fix/Workaround

Select AVCC as ADC voltage reference before entering sleep mode to avoid extra power consumption during sleep. If no internal or external reference to the ADC is used, an external pull-down resistor should be added to the AREF pin.

13.3.3 Rev. C

– External capacitor on AREF pin

1.) External capacitor on AREF pin

If an external capacitor is used on the analog reference pin (AREF), it should be equal to or larger than 100nF. Smaller capacitor value can make the AREF buffer unstable with large ringing which will reduce the accuracy of the ADC.

Problem Fix/Workaround

None.

13.3.4 Rev. D to M

Not sampled.

13.3.5 Rev. N to O

No known errata.

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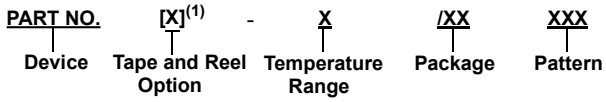

Device:	PIC16F18313, PIC16LF18313, PIC16F18323, PIC16LF18323	
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:(2)	JQ	= UQFN
	P	= PDIP
	ST	= TSSOP
	SL	= SOIC-14
	SN	= SOIC-8
	RF	= UDFN
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

- PIC16LF18313- I/P Industrial temperature, PDIP package
- PIC16F18313- E/SS Extended temperature, SSOP package

Note:

1.

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