



# THE DATASHEET OF DAC8801IDRBT





## 14-Bit, Serial Input Multiplying Digital-to-Analog Converter

### FEATURES

- 14-Bit Monotonic
- $\pm 1$  LSB INL
- $\pm 0.5$  LSB DNL
- Low Noise:  $12 \text{ nV}/\sqrt{\text{Hz}}$
- Low Power:  $I_{DD} = 2 \mu\text{A}$
- +2.7 V to +5.5 V Analog Power Supply
- 2 mA Full-Scale Current  $\pm 20\%$  with  $V_{REF} = 10 \text{ V}$
- 0.5  $\mu\text{s}$  Settling Time
- 4-Quadrant Multiplying Reference-Input
- Reference Bandwidth: 10 MHz
- $\pm 10 \text{ V}$  Reference Input
- Reference Dynamics: -105 THD
- 3-Wire 50-MHz Serial Interface
- Tiny 8-Lead 3 x 3 mm SON and 3 x 5 mm MSOP Packages
- Industry-Standard Pin Configuration

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

### DESCRIPTION

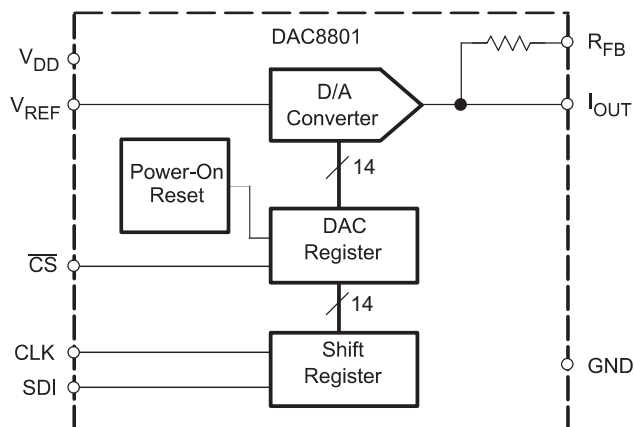
The DAC8801 multiplying digital-to-analog converter is designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage  $V_{REF}$  determines the full-scale output current. An internal feedback resistor ( $R_{FB}$ ) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A serial-data interface offers high-speed, three-wire microcontroller compatible inputs using data-in (SDI), clock (CLK), and chip select ( $\overline{CS}$ ).

On power-up, the DAC register is filled with zeroes, and the DAC output is at zero scale.

The DAC8801 is packaged in space-saving 8-lead SON and MSOP packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION <sup>(1)</sup>

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8801	±1	±0.5	MSOP-8	DGK	-40°C to 85°C	F01	DAC8801DGKT	Tape and Reel, 250
DAC8801	±1	±0.5	MSOP-8	DGK	-40°C to 85°C	F01	DAC8801DGKR	Tape and Reel, 2500
DAC8801	±1	±0.5	SON-8	DRB	-40°C to 85°C	E01	DAC8801DRBT	Tape and Reel, 250
DAC8801	±1	±0.5	SON-8	DRB	-40°C to 85°C	E01	DAC8801DRBR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	DAC8801	UNITS	
$V_{DD}$ to GND	-0.3 to 7	V	
Digital Input voltage to GND	-0.3 to $+V_{DD} + 0.3$	V	
$V_{OUT}$ to GND	-0.3 to $+V_{DD} + 0.3$	V	
Operating temperature range	-40 to 105	°C	
$V_{REF}$ , $R_{FB}$ to GND	-25 to 25	V	
Storage temperature range	-65 to 150	°C	
Junction temperature range ( $T_J$ max)	125	°C	
Power dissipation	$(T_J \text{ max} - T_A) / R_{\theta JA}$	W	
Thermal impedance, $R_{\theta JA}$	55	°C/W	
Lead temperature, soldering	Vapor phase (60s)	215	°C
Lead temperature, soldering	Infrared (15s)	220	°C
ESD rating, HBM	4000	V	
ESD rating, CDM	1000	V	

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ;  $I_{OUT} = \text{Virtual GND}$ ,  $GND = 0\text{ V}$ ;  $V_{REF} = 10\text{ V}$ ;  $T_A = \text{Full Operating Temperature}$ ; all specifications  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  unless otherwise noted.

PARAMETER	CONDITIONS	DAC8801			UNITS
		MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>					
Resolution		14			Bits
Relative accuracy				±1	LSB
Differential nonlinearity				±0.5	LSB
Output leakage current	Data = 0000h, $T_A = 25^\circ\text{C}$			10	nA
Output leakage current	Data = 0000h, $T_A = T_{MAX}$			10	nA
Full-scale gain error	All ones loaded to DAC register		±1	±4	mV
Full-scale tempco			±3		ppm of FSR/ $^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS<sup>(1)</sup></b>					
Output current			2		mA
Output capacitance	Code dependent		50		pF
<b>REFERENCE INPUT<sup>(1)</sup></b>					
$V_{REF}$ Range		-15		15	V
Input resistance			5		k $\Omega$
Input capacitance			5		pF
<b>LOGIC INPUTS AND OUTPUT<sup>(1)</sup></b>					
$V_{IL}$ Input low voltage	$V_{DD} = 2.7\text{V}$			0.6	V
	$V_{DD} = 5\text{V}$			0.8	V
$V_{IH}$ Input high voltage	$V_{DD} = 2.7\text{V}$	2.1			V
	$V_{DD} = 5\text{V}$	2.4			V
$I_{IL}$ Input leakage current				10	$\mu\text{A}$
$C_{IL}$ Input capacitance				10	pF
<b>INTERFACE TIMING</b>					
$f_{CLK}$ Clock input frequency				50	MHz
$t_{(CH)}$ Clock pulse width high		10			ns
$t_{(CL)}$ Clock pulse width low		10			ns
$t_{(CSS)}$ $\overline{CS}$ to Clock setup time		0			ns
$t_{(CSH)}$ Clock to $\overline{CS}$ hold time		10			ns
$t_{(DS)}$ Data setup time		5			ns
$t_{(DH)}$ Data hold time		10			ns
<b>POWER REQUIREMENTS</b>					
$V_{DD}$		2.7		5.5	V
$I_{DD}$ (normal operation)	Logic inputs = 0 V			5	$\mu\text{A}$
$V_{DD} = 4.5\text{ V to }5.5\text{ V}$	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		3	5	$\mu\text{A}$
$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	$V_{IH} = V_{DD}$ and $V_{IL} = GND$		1	2.5	$\mu\text{A}$
<b>AC CHARACTERISTICS<sup>(1)(2)</sup></b>					
$t_s$ Output voltage settling time	To $\pm 0.1\%$ of full-scale, Data = 0000h to 3FFFh to 0000h		0.3		$\mu\text{s}$
	To $\pm 0.006\%$ of full-scale, Data = 0000h to 3FFFh to 0000h		0.5		
Reference multiplying BW	$V_{REF} = 5\text{ V}_{PP}$ , Data = 3FFFh		10		MHz
DAC glitch impulse	$V_{REF} = 0\text{ V}$ , Data = 3FFFh to 2000h		2		nV/s
Feedthrough error	$V_{REF} = 100\text{ mV}_{RMS}$ , 100kHz, Data = 0000h		-70		dB
Digital feedthrough	$\overline{CS} = 1$ and $f_{CLK} = 1\text{MHz}$		2		nV/s

(1) Specified by design and characterization, not production tested.

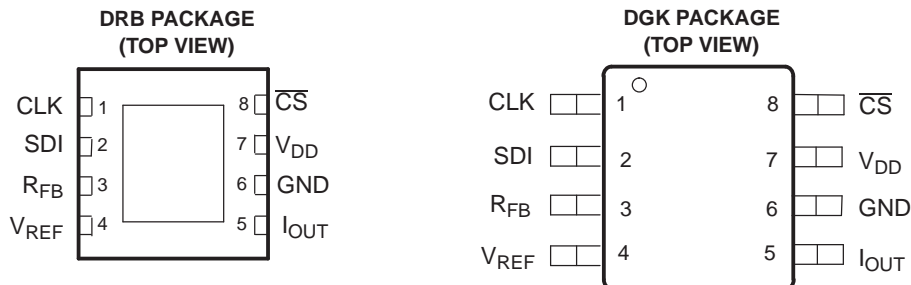
(2) All ac characteristic tests are performed in a closed-loop system using the THS4011 I-to-V converter amplifier.

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ;  $I_{OUT} = \text{Virtual GND}$ ,  $GND = 0\text{ V}$ ;  $V_{REF} = 10\text{ V}$ ;  $T_A = \text{Full Operating Temperature}$ ; all specifications  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  unless otherwise noted.

PARAMETER	CONDITIONS	DAC8801			UNITS
		MIN	TYP	MAX	
Total harmonic distortion	$V_{REF} = 5\text{ V}_{PP}$ , Data = 3FFFh, $f = 1\text{ kHz}$		-105		dB
Output spot noise voltage	$f = 1\text{ kHz}$ , $BW = 1\text{ Hz}$		12		$\text{nV}/\sqrt{\text{Hz}}$

**PIN ASSIGNMENTS**

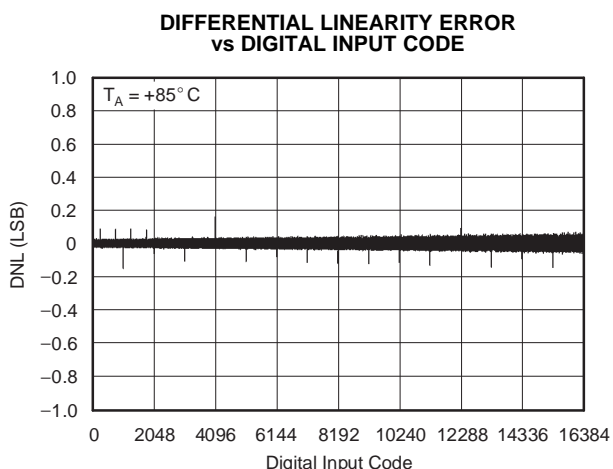
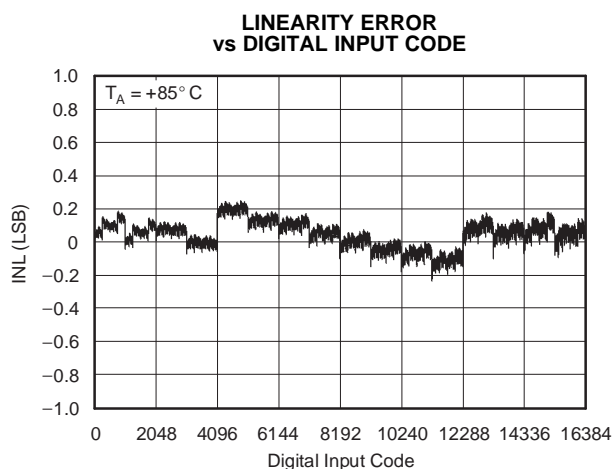
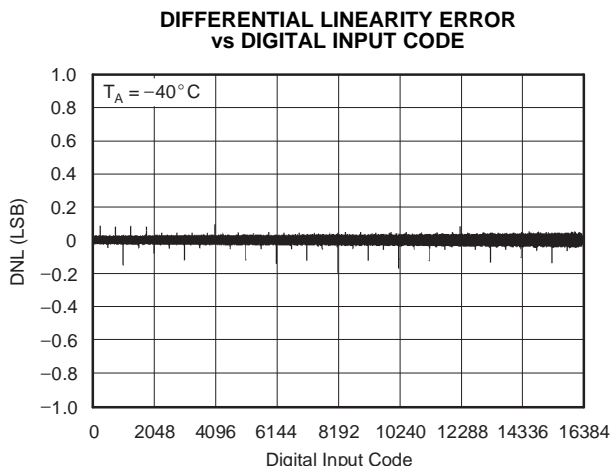
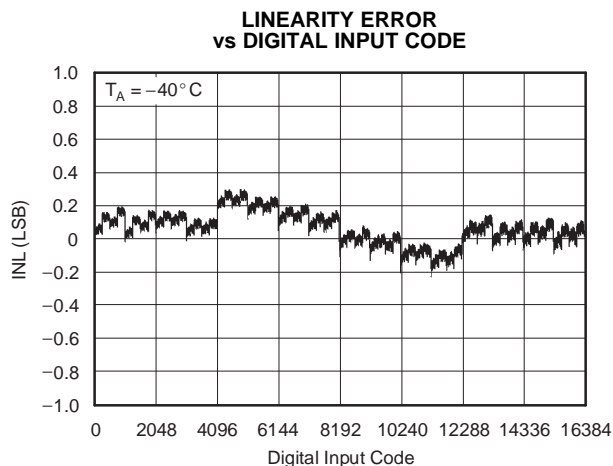
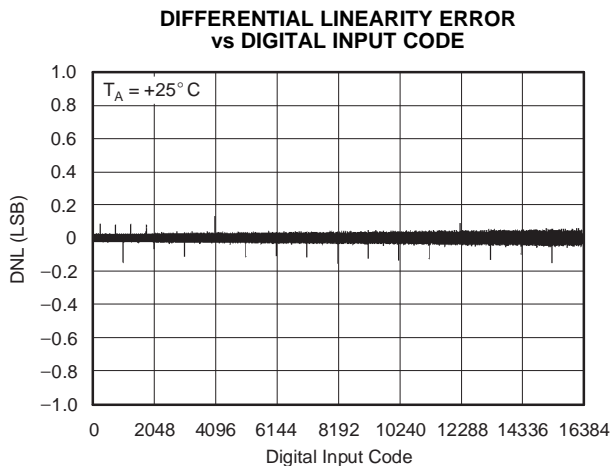
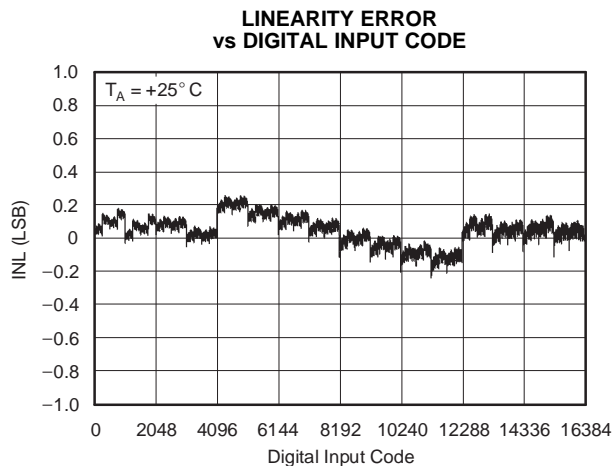


**TERMINAL FUNCTIONS**

PIN	NAME	DESCRIPTION
1	CLK	Clock input, positive edge triggered clocks data into shift register
2	SDI	Serial register input, data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	$R_{FB}$	Internal matching feedback resistor. Connect to external op amp output.
4	$V_{REF}$	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
5	$I_{OUT}$	DAC current output. Connects to inverting terminal of external precision I to V op amp.
6	GND	Analog and digital ground
7	$V_{DD}$	Positive power supply input. Specified range of operation 2.7 V to 5.5 V.
8	$\overline{CS}$	Chip select, active low digital input. Transfers shift register data to DAC register on rising edge. See <a href="#">Table 1</a> for operation.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$**

At  $T_A = 25^\circ\text{C}$ ,  $+V_{DD} = 5\text{ V}$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS:  $V_{DD} = 5\text{ V}$  (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $+V_{DD} = 5\text{ V}$ , unless otherwise noted.

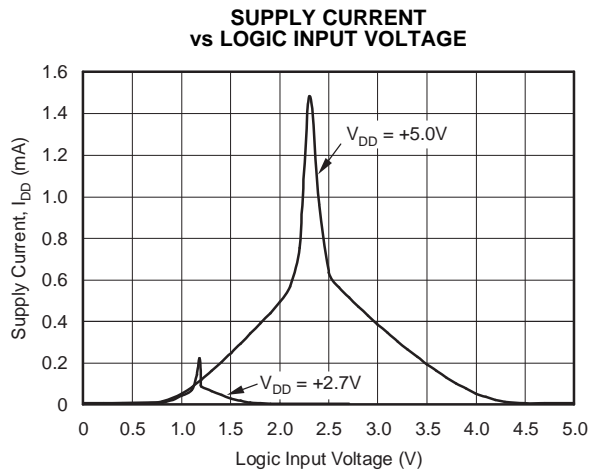


Figure 7.

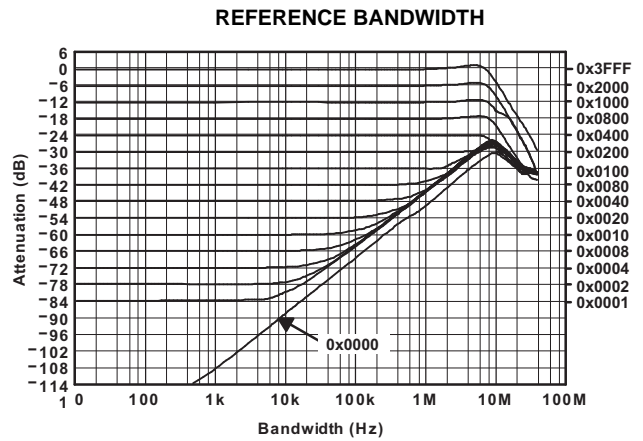


Figure 8.

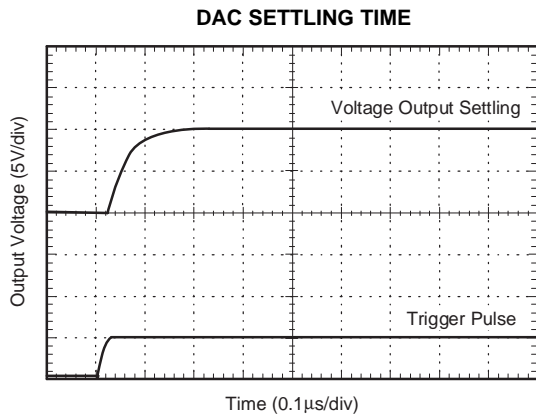


Figure 9.

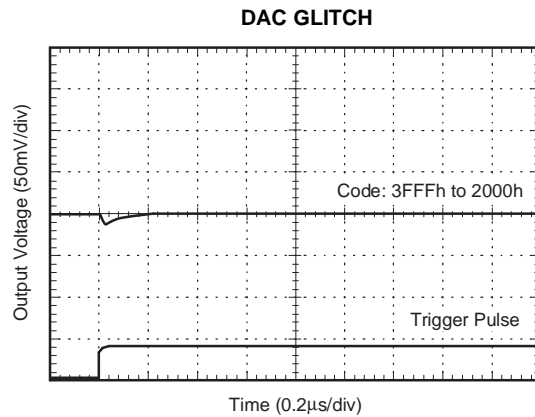


Figure 10.

**TYPICAL CHARACTERISTICS:  $V_{DD} = 2.7\text{ V}$**

At  $T_A = 25^\circ\text{C}$ ,  $+V_{DD} = 2.7\text{ V}$ , unless otherwise noted.

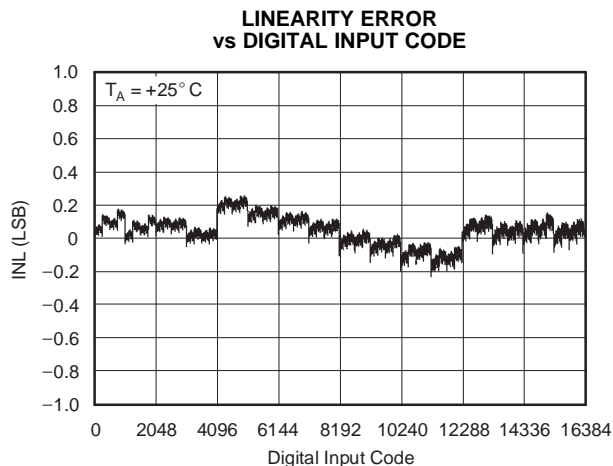


Figure 11.

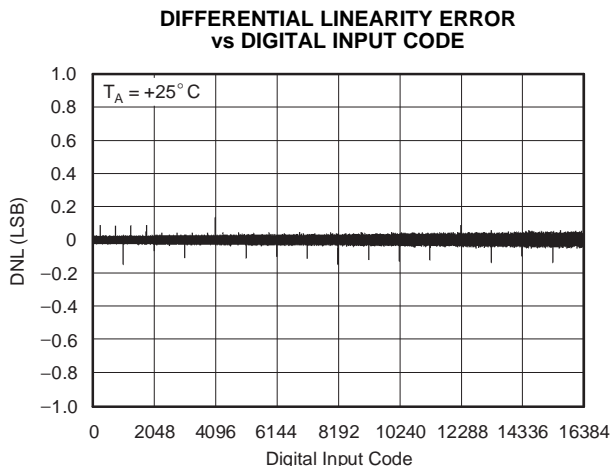


Figure 12.

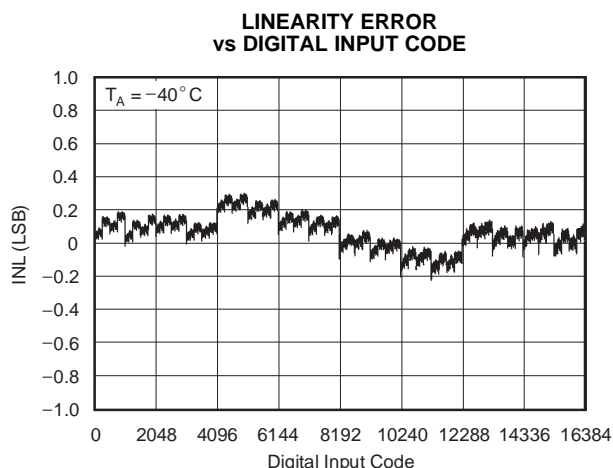


Figure 13.

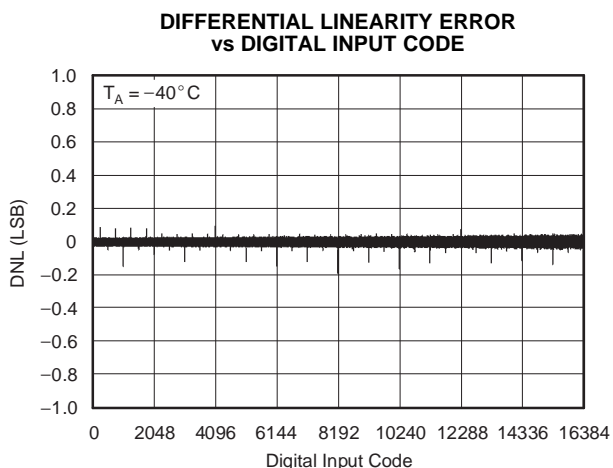


Figure 14.

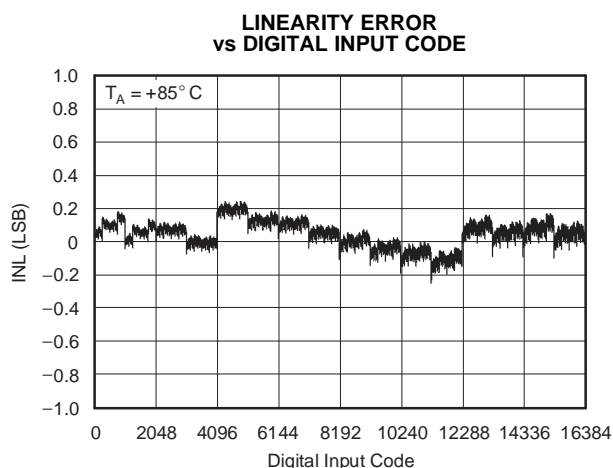


Figure 15.

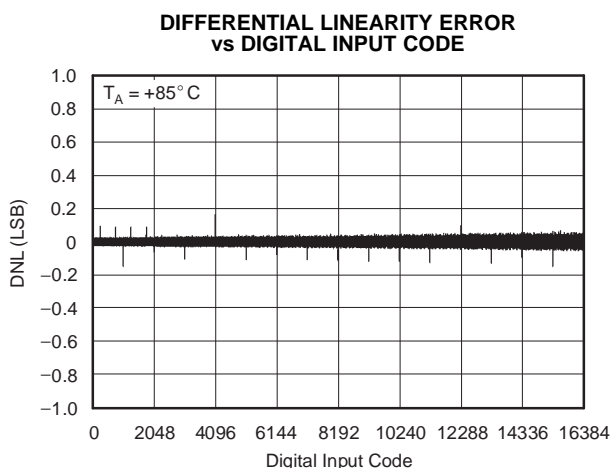


Figure 16.

### THEORY OF OPERATION

The DAC8801 is a single channel current output, 16-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 17, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or the I<sub>OUT</sub> terminal. The I<sub>OUT</sub> terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V<sub>REF</sub> that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 5 kΩ ± 25%. The external reference voltage can vary in a range of -10 V to 10 V, thus providing bipolar I<sub>OUT</sub> current operation. By using an external I/V converter and the DAC8801 R<sub>FB</sub> resistor, output voltage ranges of -V<sub>REF</sub> to V<sub>REF</sub> can be generated.

When using an external I/V converter and the DAC8801 R<sub>FB</sub> resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{16384} \tag{1}$$

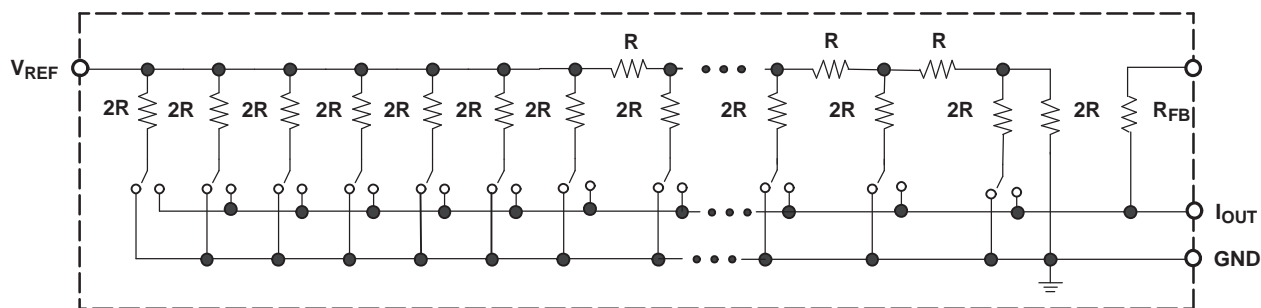


Figure 17. Equivalent R-2R DAC Circuit

Each DAC code determines the 2R leg switch position to either GND or I<sub>OUT</sub>. Because the DAC output impedance as seen looking into the I<sub>OUT</sub> terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I<sub>OUT</sub> terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8801 due to offset modulation versus DAC code. For best linearity performance of the DAC8801, an op amp (OPA277) as shown in Figure 18 is recommended. This circuit allows V<sub>REF</sub> to swing from -10V to +10V.

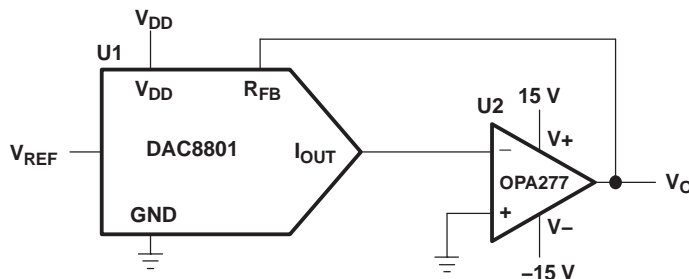


Figure 18. Voltage Output Configuration

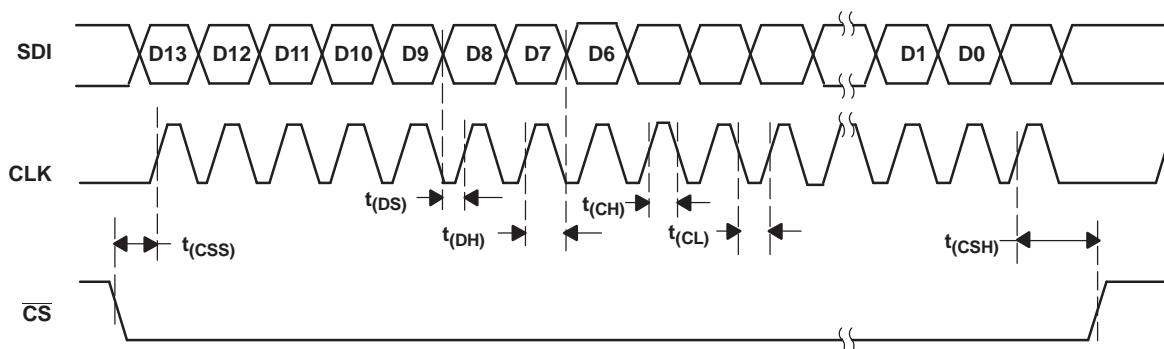


Figure 19. DAC8801 Timing Diagram

Table 1. Control Logic Truth Table<sup>(1)</sup>

CLK	$\overline{CS}$	Serial Shift Register	DAC Register
X	H	No effect	Latched
$\uparrow+$	L	Shift register data advanced one bit	Latched
X	H	No effect	Latched
X	$\uparrow+$	Shift register data transferred to DAC register	New data loaded from serial register

(1)  $\uparrow+$  Positive logic transition; X = Don't care

Table 1. Serial Input Register Data Format, Data Loaded MSB First

Bit	B13 (MSB)	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data <sup>(1)</sup>	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) A full 16-bit data word can be loaded into the serial register, but only the last 14 bits are transferred to the DAC register when  $\overline{CS}$  goes high.

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design as shown in Figure 20, the DAC8801 current output ( $I_{OUT}$ ) and the connection with the inverting node of the op amp should be as short as possible and according to correct PCB layout design. For each code change there is a step function. If the GBP of the op amp is limited and parasitic capacitance is excessive at the inverting node then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C1 (4 pF to 20 pF typ) can be added to the design as shown in Figure 20.

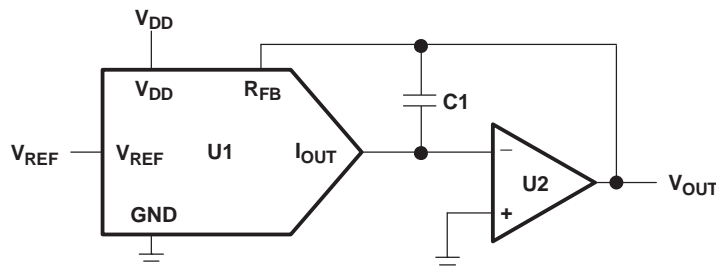


Figure 20. Gain Peaking Prevention Circuit With Compensation Capacitor

Positive Voltage Output Circuit

As shown in Figure 21, in order to generate a positive voltage output, a negative reference is input to the DAC8801. This design is suggested instead of using an inverting amp to invert the output due to tolerance errors of the resistor. For a negative reference,  $V_{OUT}$  and GND of the reference are level-shifted to a virtual ground and a -2.5 V input to the DAC8801 with an op amp.

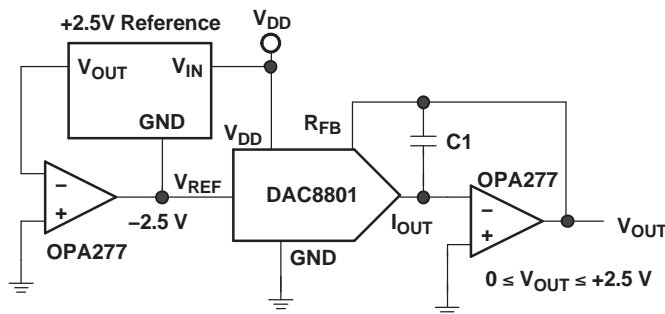


Figure 21. Positive Voltage Output Circuit

## APPLICATION INFORMATION (continued)

### Bipolar Output Circuit

The DAC8801, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output  $I_{OUT}$  is the inverse of the input reference voltage at  $V_{REF}$ .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in [Figure 22](#), external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U4. According to the circuit transfer equation given in [Equation 2](#), input data (D) from code 0 to full scale produces output voltages of  $V_{OUT} = -2.5\text{ V}$  to  $V_{OUT} = 2.5\text{ V}$ .

$$V_{OUT} = \left( \frac{D}{16,384} - 1 \right) \times V_{REF} \quad (2)$$

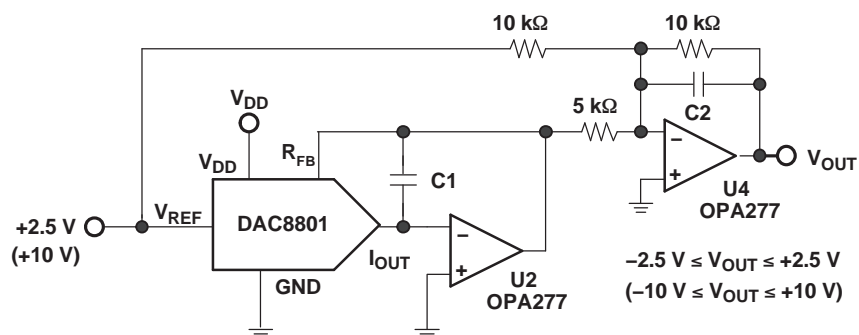


Figure 22. Bipolar Output Circuit

### Programmable Current Source Circuit

A DAC8801 can be integrated into the circuit in [Figure 23](#) to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. A application of this circuit includes a 4-mA to 20-mA current transmitter with up to a 500-Ω load. With a matched resistor network, the load current of the circuit is shown in [Equation 3](#):

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times D \quad (3)$$

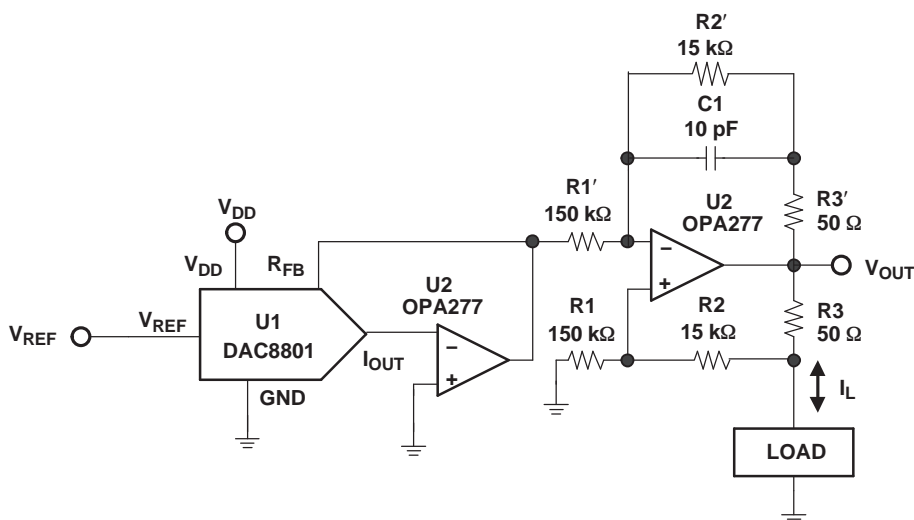


Figure 23. Programmable Bidirectional Current Source Circuit

### APPLICATION INFORMATION (continued)

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive  $\pm 20$  mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested because of the change in the output impedance  $Z_O$ , according to [Equation 4](#):

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (4)$$

As shown in [Equation 4](#), with matched resistors,  $Z_O$  is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used,  $Z_O$  is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; however, for most applications a value of several pF is suggested.

### Cross-Reference

The DAC8801 has an industry-standard pinout. [Table 2](#) provides the cross-reference information.

**Table 2. Cross Reference**

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS REFERENCE
DAC8801IDGK	$\pm 1$	$\pm 1$	-40°C to +85°C	8-Lead MicroSOIC	MSOP-8	ADS5553CRM
DAC8801IDRB	$\pm 1$	$\pm 1$	-40°C to +85°C	8-Lead Small Outline	SON-8	N/A

**Table 3. DAC8801 Revision History**

Revision	Date	Description
A	12/04	Removed the "Product Preview" label.
		Added information to the Features.
		Added Output leakage current Data = 0000h, $T_A = T_{MAX}$ in the Electrical Characteristics table.
		Added Input high voltage for 2.7 V and 5 V in the Electrical Characteristics table.
		Changed the values of the <i>Power Requirements</i> and the <i>AC characteristics</i> in the Electrical Characteristics table.
B	10/06	Changed the ESD rating, HBM from 1500 to 4000 in the Absolute Maximum Ratings.
		Revised <a href="#">Figure 8</a> .

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8801IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	F01	<a href="#">Samples</a>
DAC8801IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	F01	<a href="#">Samples</a>
DAC8801IDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	F01	<a href="#">Samples</a>
DAC8801IDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E01	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8801IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8801IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8801IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

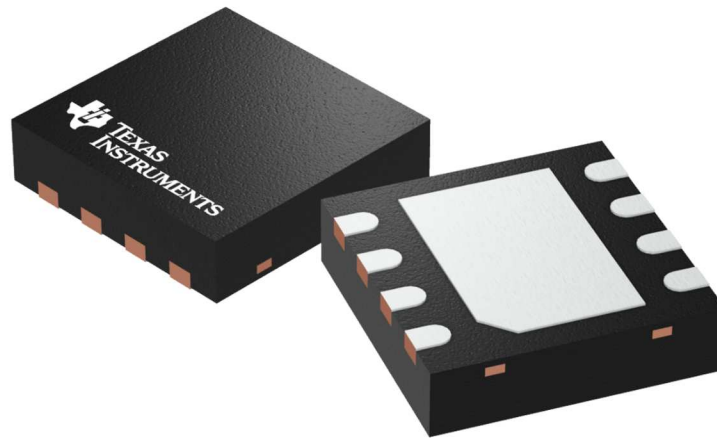
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8801IDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
DAC8801IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8801IDRBT	SON	DRB	8	250	210.0	185.0	35.0

**DRB 8**

**GENERIC PACKAGE VIEW**

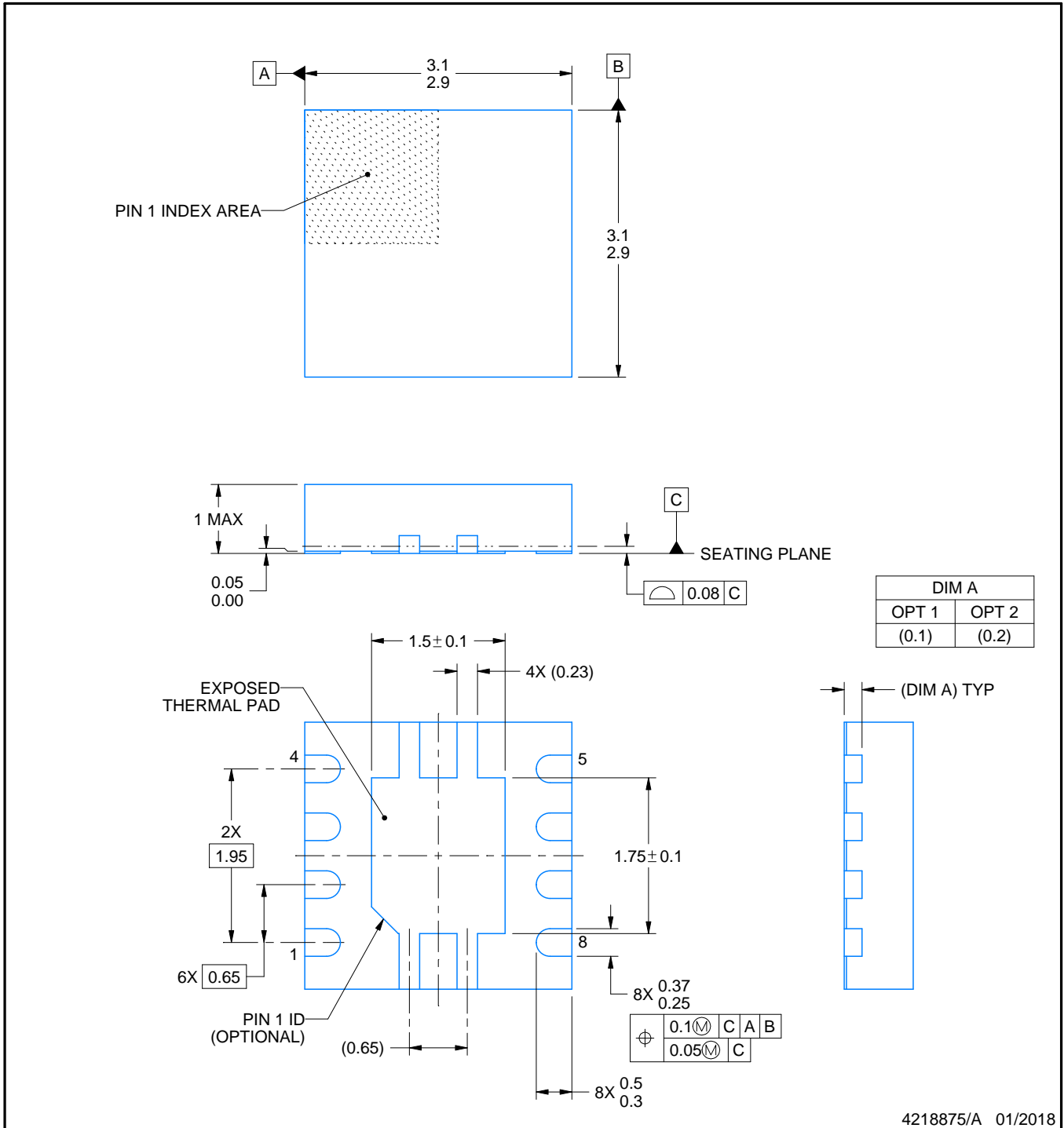
**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L



4218875/A 01/2018

NOTES:

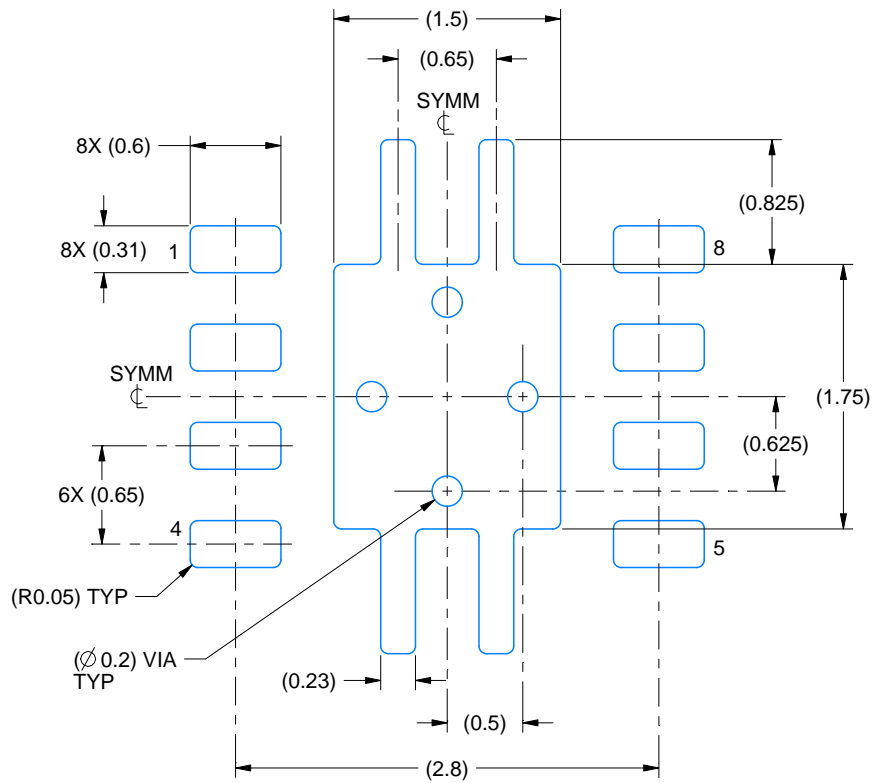
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

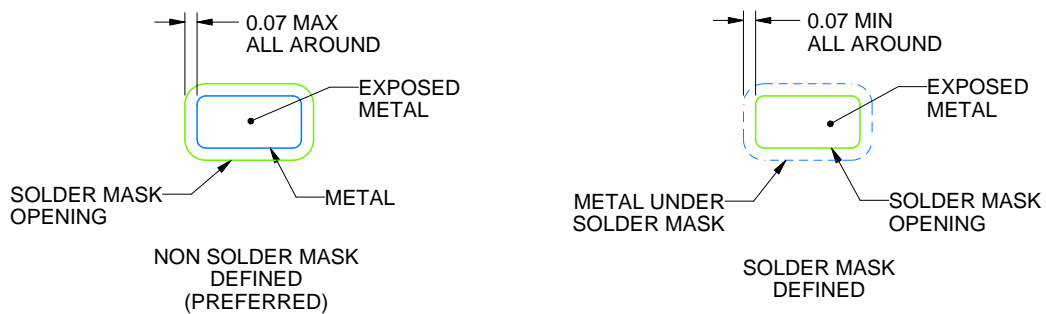
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

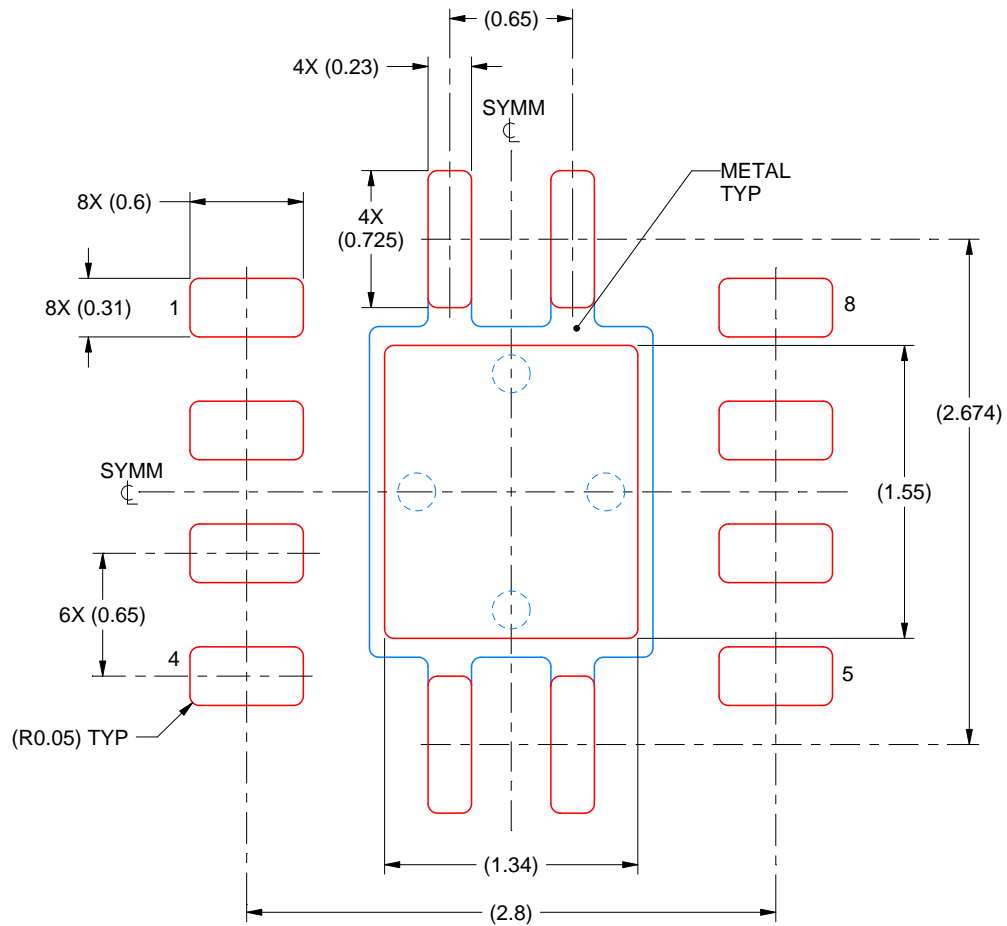
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
84% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

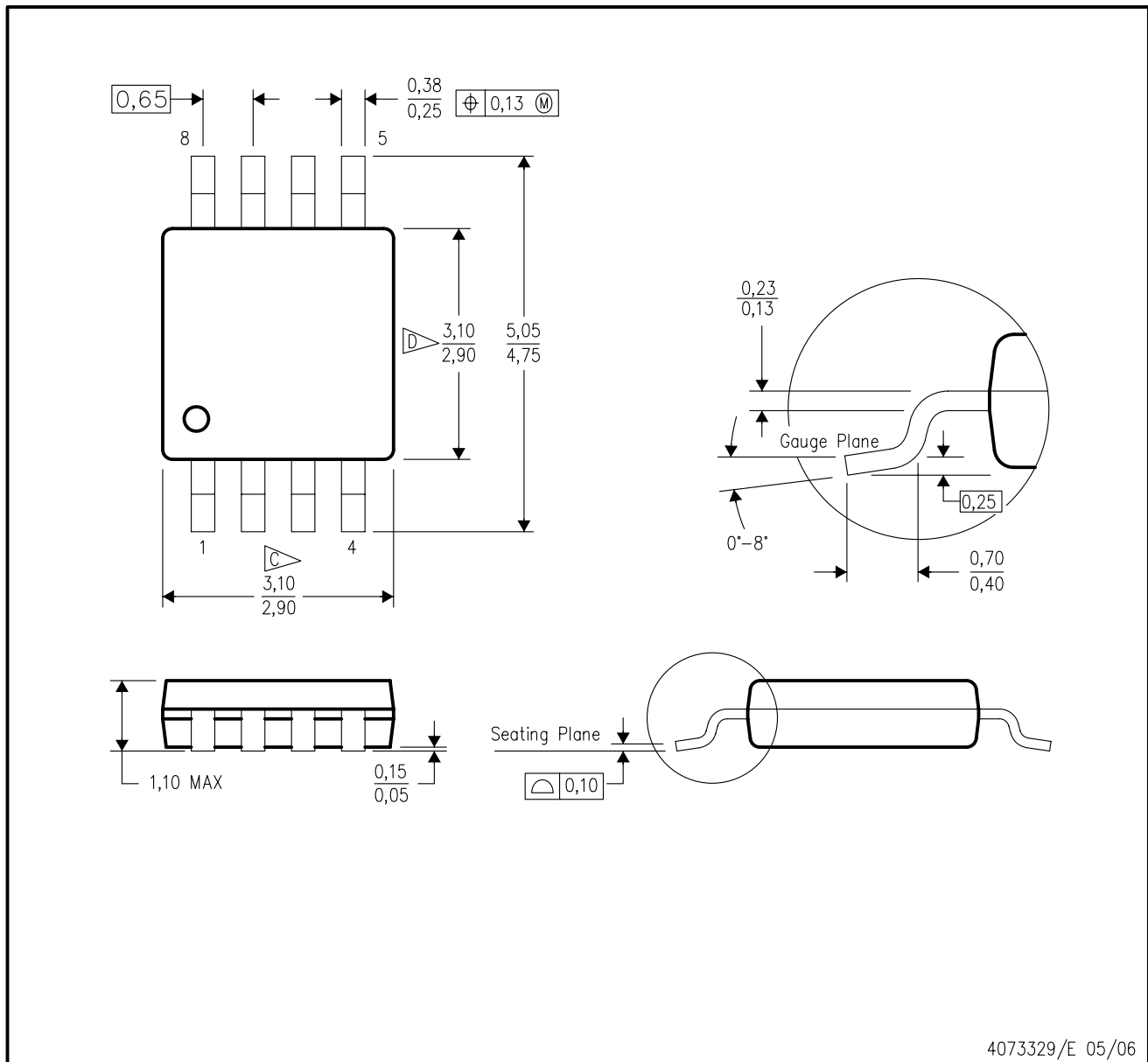
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NOTES: (continued)

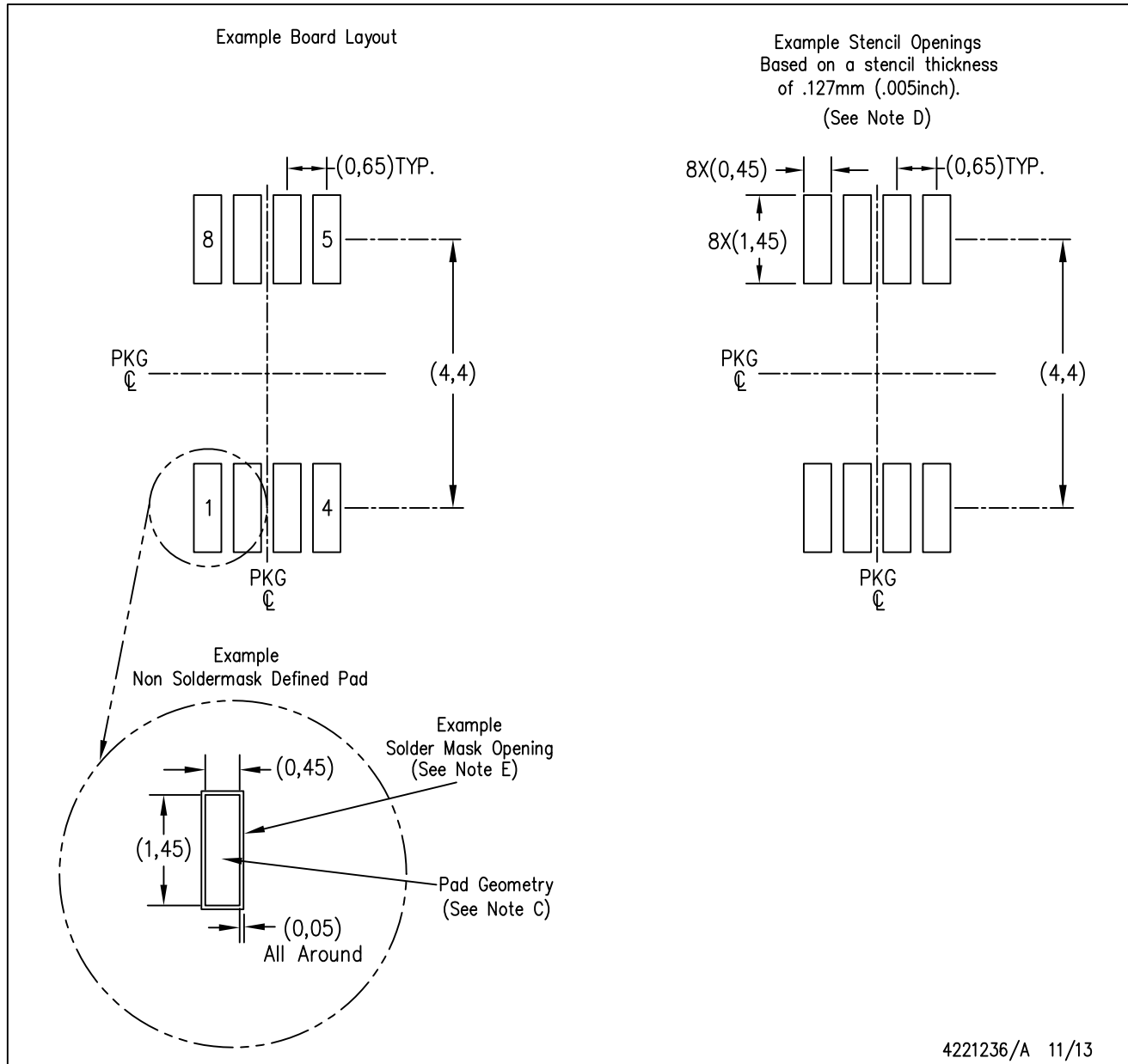
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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