THE DATASHEET OF

AD4115BCPZ

Single-Supply, Multichannel, 125 kSPS, 24-Bit, Sigma-Delta ADC with ±10 V Inputs

Data Sheet **AD4115**

FEATURES

- 24-bit ADC with integrated AFE
  - Fast and flexible output rate: 2.5 SPS to 125 kSPS
  - Channel scan data rate of 24,845 SPS per channel (40.25 µs settling)
  - 85 dB common mode rejection of 50 Hz and 60 Hz at 20 SPS per channel
- ±10 V inputs, either 8 differential or 16 single-ended
  - VIN pin absolute maximum rating ±65 V
  - Absolute input pin voltage up to ±20 V
  - Minimum 1 MΩ impedance
- On-chip 2.5 V reference
  - ±0.12% initial accuracy at 25°C, ±5 ppm/°C (typical) drift
- Internal or external clock
- Power supplies
  - AVDD = 4.5 V to 5.5 V
  - IOVDD = 2 V to 5.5 V
  - Total current consumption AVDD + IOVDD (I_{DD}) = 10.4 mA
- Temperature range: −40°C to +105°C
- 3-wire or 4-wire serial digital interface (Schmitt trigger on SCLK)
  - SPI, QSPI, MICROWIRE, and DSP compatible

APPLICATIONS

- Process control
  - Programmable logic controller (PLC) and distributed control system (DCS) modules
  - Instrumentation and measurement

GENERAL DESCRIPTION

The AD4115 is a low power, low noise, 24-bit, sigma-delta (Σ-Δ) analog-to-digital converter (ADC) that integrates an analog front end (AFE) for eight fully differential or 16 single-ended, high impedance (≥1 MΩ), bipolar, ±10 V voltage inputs.

The AD4115 integrates key analog and digital signal conditioning blocks to configure eight individual setups for each analog input channel in use. The AD4115 features a maximum channel scan rate of 24,845 kSPS (40.25 µs) for fully settled data.

The embedded 2.5 V, low drift (±5 ppm/°C), band gap internal reference (with output reference buffer) reduces the external component count.

The digital filter allows flexible settings, including simultaneous 50 Hz and 60 Hz rejection at a 27.27 SPS output data rate. The user can select different filter settings depending on the requirements of each channel in the application. The automatic channel sequencer enables the ADC to switch through each enabled channel.

The precision performance of the AD4115 is achieved by integrating the proprietary *i*Passives® technology from Analog Devices, Inc. The AD4115 is factory calibrated to achieve a high degree of specified accuracy.

The AD4115 operates with a single power supply that allows simplified use in galvanically isolated applications. The specified operating temperature range is −40°C to +105°C. The AD4115 is housed in a 40-lead, 6 mm × 6 mm LFCSP.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

11/2020—Rev. 0 to Rev. A

Changes to General Description Section 1
Change to Total Unadjusted Error (TUE) Parameter, Table 1 5
Changes to Table 16 and Table 17 21
Changes to Table 30 50

7/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

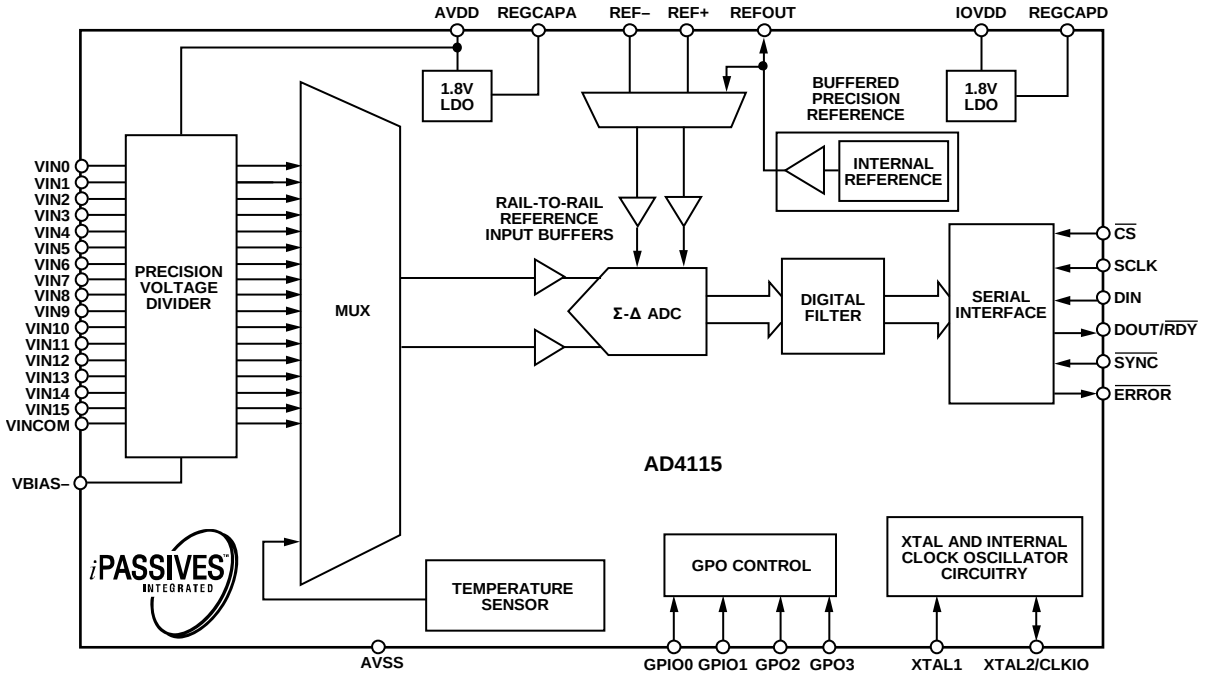


Figure 1.

SPECIFICATIONS

AVDD = 4.5 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = 0 V, DGND = 0 V, VBIAS− = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock (MCLK) = 8 MHz, T_A = T_{MIN} to T_{MAX} (−40°C to +105°C), unless otherwise noted. V_{REF} is the reference voltage, FS is full scale, and FSR is full-scale range.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE INPUTS					
Differential Input Voltage Range[1]	Specified performance	−10		+10	V
	Functional	$-V_{REF} \times 10$		$+V_{REF} \times 10$	V
Absolute Input Pin Voltage		−20		+20	V
Input Impedance		1			MΩ
Offset Error[2]	T_A = 25°C		±1.5		mV
Offset Drift			±8		µV/°C
Gain Error	T_A = 25°C		±0.05		% FS
Gain Drift			±1		ppm/°C
Integral Nonlinearity (INL)			±0.01		% FSR
Total Unadjusted Error (TUE)[3]					
	T_A = 25°C, internal V_{REF}			0.07	% FSR
	0°C to 105°C, internal V_{REF}			0.09	% FSR
	−40°C to +105°C, internal V_{REF}			0.12	% FSR
	25°C, external V_{REF}			0.07	% FSR
	−40°C to +105°C, external V_{REF}			0.08	% FSR
Power Supply Rejection Ratio (PSRR)	AVDD for input voltage (V_{IN}) = 1 V		70		dB
Common-Mode Rejection Ratio (CMRR)	V_{IN} = 1 V				
At DC			85		dB
At 50 Hz and 60 Hz	20 Hz output data rate (postfilter), 50 Hz ± 1 Hz and 60 Hz ± 1 Hz		120		dB
Normal Mode Rejection[3]	50 Hz ± 1 Hz and 60 Hz ± 1 Hz				
	Internal clock, 20 SPS ODR (postfilter)	71	90		dB
	External clock, 20 SPS ODR (postfilter)	85	90		dB
Resolution	See Table 16 and Table 17				
Noise	See Table 16 and Table 17				
ADC SPEED AND PERFORMANCE					
ADC Output Data Rate (ODR)	One channel, see Table 16	2.5		125,000	SPS
No Missing Codes[3]	Excluding sinc3 filter ≥ 62.5 kHz notch	24			Bits
INTERNAL REFERENCE	100 nF external capacitor to AVSS				
Output Voltage	REFOUT with respect to AVSS		2.5		V
Initial Accuracy[3, 4]	REFOUT, T_A = 25°C	−0.12		+0.12	%
Temperature Coefficient			±5	+12	ppm/°C
Reference Load Current (I_{LOAD})		−10		+10	mA
PSRR	AVDD (line regulation)		95		dB
Load Regulation ($\Delta V_{OUT}/\Delta I_{LOAD}$[5])			32		ppm/mA
Voltage Noise (e_N)	0.1 Hz to 10 Hz, 2.5 V reference		4.5		µV rms
Voltage Noise Density	1 kHz, 2.5 V reference		215		nV/√Hz
Turn On Settling Time	100 nF REFOUT capacitor		200		µs
Short-Circuit Current (I_{SC})			25		mA
EXTERNAL REFERENCE INPUTS					
Differential Input Range	V_{REF} = (REF+) − (REF−)	1	2.5	AVDD	V
Absolute Voltage Limits					
Buffers Disabled		AVSS − 0.05		AVDD + 0.05	V
Buffers Enabled		AVSS		AVDD	V
External Reference Input Current					

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Buffers Disabled					
Input Current			±36		µA/V
Input Current Drift	External clock		±1.2		nA/V/°C
	Internal clock		±3		nA/V/°C
Buffers Enabled					
Input Current			±400		nA
Input Current Drift			0.6		nA/°C
Normal Mode Rejection					
CMRR			95		dB
TEMPERATURE SENSOR					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			477		µV/K
GENERAL-PURPOSE OUTPUTS (GPIO0, GPIO1, GPO2, GPO3)	With respect to AVSS				
Floating State Output Capacitance			5		pF
Output Voltage[3]					
High (V_{OH})	Source current (I_{SOURCE}) = 200 µA	AVDD − 1			V
Low (V_{OL})	Sink current (I_{SINK}) = 800 µA			AVSS + 0.4	V
CLOCK					
Internal Clock					
Frequency			8		MHz
Accuracy		−2.5%		+2.5%	%
Duty Cycle			50		%
Output Voltage					
V_{OH}		0.8 × IOVDD			V
V_{OL}				0.4	V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		µs
External Clock (CLKIO)			8	8.192	MHz
Duty Cycle		30	50	70	%
LOGIC INPUTS					
Input Voltage[3]					
High (V_{INH})	2 V ≤ IOVDD < 2.3 V	0.65 × IOVDD			V
	2.3 V ≤ IOVDD ≤ 5.5 V	0.7 × IOVDD			V
Low (V_{INL})	2 V ≤ IOVDD < 2.3 V			0.35 × IOVDD	V
	2.3 V ≤ IOVDD ≤ 5.5 V			0.7	V
Hysteresis	IOVDD ≥ 2.7 V	0.08		0.25	V
	IOVDD < 2.7 V	0.04		0.2	V
Leakage Current		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output Voltage[3]					
V_{OH}	IOVDD ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.7 V ≤ IOVDD < 4.5 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.7 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
V_{OL}	IOVDD ≥ 4.5 V, I_{SINK} = 2 mA			0.4	V
	2.7 V ≤ IOVDD < 4.5 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.7 V, I_{SINK} = 400 µA			0.4	V
Leakage Current[3]	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
POWER REQUIREMENTS					
Power Supply Voltage					

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AVDD to AVSS		4.5		5.5	V
AVSS to DGND		−2.75		0	V
IOVDD to DGND		2		5.5	V
IOVDD to AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS[6]	All outputs unloaded, digital inputs connected to IOVDD or DGND				
Full Operating Mode					
AVDD Current	Including internal reference		9.4	11.5	mA
IOVDD Current	Internal clock		1.4	1.8	mA
Standby Mode	All V_{IN} = 0 V		210		µA
Power-Down Mode	All V_{IN} = 0 V		185		µA
POWER DISSIPATION					
Full Operating Mode			52		mW
Standby Mode			1		mW
Power-Down Mode			925		µW

[1] The full specification is guaranteed for a differential input signal of ±10 V. The device is functional up to a differential input signal of $\pm V_{REF} \times 10$. However, the specified absolute pin voltage must not be exceeded for the proper function.
[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected.
[3] Specification is not production tested but is supported by characterization data at the initial product release.
[4] This specification includes moisture sensitivity level (MSL) preconditioning effects.
[5] V_{OUT} is the output voltage.
[6] This specification is with no load on the REFOUT pin and the digital output pins.

TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, capacitive load (C_{LOAD}) = 20 pF, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN} or T_{MAX}	Unit	Test Conditions/Comments
SCLK			
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.75 V to 5.5 V
	40	ns max	IOVDD = 2 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	12.5	ns max	IOVDD = 4.75 V to 5.5 V
	25	ns max	IOVDD = 2 V to 3.6 V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] This parameter is defined as the time required for the output to cross the V_{OL} or V_{OH} limit.
[4] The SCLK active edge is the falling edge of SCLK.
[5] DOUT/$\overline{RDY}$ returns high after a data register read. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while DOUT/$\overline{RDY}$ is high. Ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

Timing Diagrams

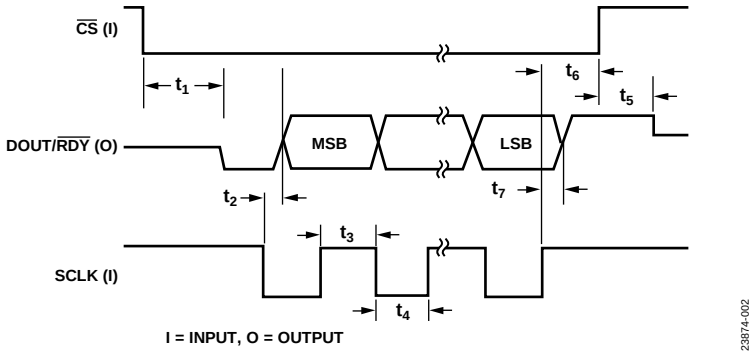


Figure 2. Read Cycle Timing Diagram

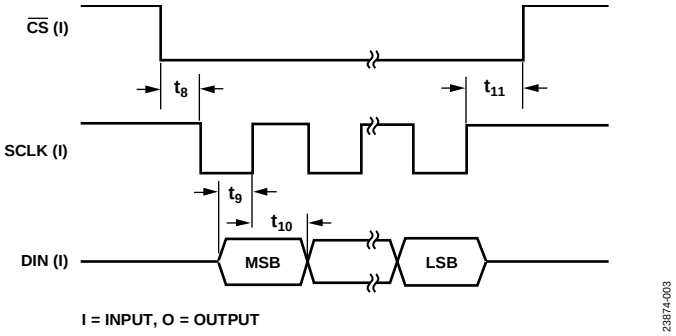


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AVSS	−0.3 V to +6.5 V
AVDD to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
VINx to AVSS	−65 V to +65 V
Reference Input Voltage to AVSS	−0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Soldering, Reflow Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

θ_{JC} is the thermal resistance from the junction to the package case.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-15[1]	34[2]	2.63[3]	°C/W

[1] 4-Layer JEDEC PCB.
[2] Thermal impedance simulated values are based on JEDEC 2S2P thermal test PCB with 16 thermal vias. θ_{JA} is specified for a device soldered on a JEDEC test PCB for surface-mount packages. See JEDEC JESD51.
[3] A cold plate is attached to the PCB bottom and measured at the exposed paddle.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4115

Table 5. AD4115, 40-Lead LFCSP

ESD Model	Withstand Threshold (v)	Class
HBM	±1000	1C
CDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

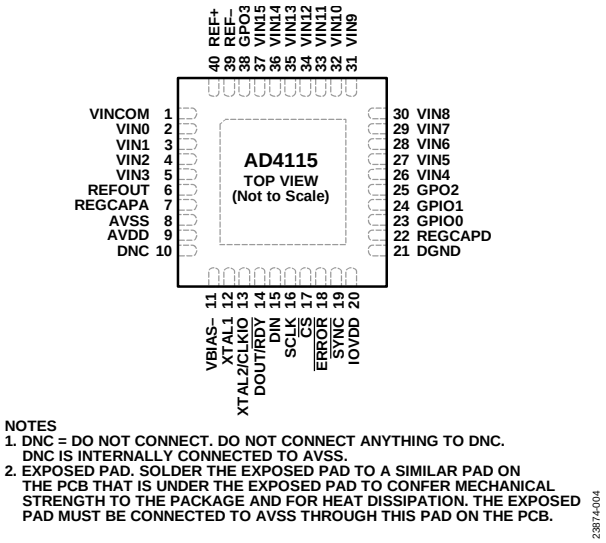


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic[1]	Type[2]	Description
1	VINCOM	AI	Voltage Input Common. Voltage inputs are referenced to VINCOM when the inputs are configured as single-ended. Connect VINCOM to analog ground.
2	VIN0	AI	Voltage Input 0. VIN0 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN1 in differential configuration.
3	VIN1	AI	Voltage Input 1. VIN1 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN0 in differential configuration.
4	VIN2	AI	Voltage Input 2. VIN2 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN3 in differential configuration.
5	VIN3	AI	Voltage Input 3. VIN3 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN2 in differential configuration.
6	REFOUT	AO	Internal Reference Buffered Output. The output is 2.5 V with respect to AVSS. Decouple REFOUT to AVSS using a 0.1 µF capacitor.
7	REGCAPA	AO	Analog Low Dropout (LDO) Regulator Output. Decouple REGCAPA to AVSS using a 1 µF capacitor and a 0.1 µF capacitor.
8	AVSS	P	Negative Analog Supply. AVSS ranges from −2.75 V to 0 V and is nominally set to 0 V.
9	AVDD	P	Analog Supply Voltage. AVDD ranges from 3.0 V to 5.5 V with respect to AVSS.
10	DNC	N/A	Do Not Connect. Do not connect anything to DNC. DNC is internally connected to AVSS.
11	VBIAS−	AI	Voltage Bias Negative. VBIAS− sets the bias voltage for the voltage input AFE. Connect VBIAS− to AVSS.
12	XTAL1	AI	Input 1 for Crystal.
13	XTAL2/CLKIO	AI/DI	Input 2 for Crystal/Clock Input or Output. See the CLOCKSEL bit settings in the ADC Mode Register section for more information.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output/Data Ready Output. The DOUT/$\overline{\text{RDY}}$ dual-purpose pin functions as a serial data output pin to access the output shift register on the ADC. The output shift register can contain data from any on-chip data or control registers. The data-word or control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin and goes low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor that indicates that valid data is available.
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers on the ADC, and the register address (RA) bits of the communications register identify the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. The SCLK serial clock input is used for data transfers to and from the ADC. SCLK has a Schmitt triggered input.
17	$\overline{\text{CS}}$	DI	Chip Select Input. $\overline{\text{CS}}$ is an active low logic input used to select the ADC. Use $\overline{\text{CS}}$ to select the ADC in systems with more than one device on the serial bus. $\overline{\text{CS}}$ can be hardwired low to allow the ADC to

Pin No.	Mnemonic[1]	Type[2]	Description
			operate in 3-wire mode with SCLK, DIN, and DOUT/$\overline{\text{RDY}}$ used to interface with the device. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated.
18	$\overline{\text{ERROR}}$	DI/O	Error Input/Output or General-Purpose Output. $\overline{\text{ERROR}}$ can be used in one of the following three modes: Active low error input mode. This mode sets the ADC_ERROR bit in the status register. Active low, open-drain error output mode. The status register error bits are mapped to the $\overline{\text{ERROR}}$ pin. The $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. $\overline{\text{ERROR}}$ is referenced between IOVDD and DGND.
19	$\overline{\text{SYNC}}$	DI	Synchronization Input. $\overline{\text{SYNC}}$ allows digital filter and analog modulator synchronization when using multiple devices.
20	IOVDD	P	Digital Input/Output Supply Voltage. The IOVDD voltage ranges from 2 V to 5.5 V (nominal). IOVDD is independent of AVDD. For example, IOVDD operates at 3.3 V when AVDD equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V.
21	DGND	P	Digital Ground.
22	REGCAPD	AO	Digital LDO Regulator Output. REGCAPD is for decoupling purposes only. Decouple REGCAPD to DGND using a 1 µF capacitor.
23	GPIO0	DI/O	General-Purpose Input/Output 0. Logic input/output on GPIO0 is referred to the AVDD and AVSS supplies.
24	GPIO1	DI/O	General-Purpose Input/Output 1. Logic input/output on GPIO1 is referred to the AVDD and AVSS supplies.
25	GPO2	DO	General-Purpose Output 2. Logic output on GPO2 is referred to the AVDD and AVSS supplies.
26	VIN4	AI	Voltage Input 4. VIN4 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN5 in differential configuration.
27	VIN5	AI	Voltage Input 5. VIN5 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN4 in differential configuration.
28	VIN6	AI	Voltage Input 6. VIN6 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN7 in differential configuration.
29	VIN7	AI	Voltage Input 7. VIN7 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN6 in differential configuration.
30	VIN8	AI	Voltage Input 8. VIN8 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN9 in differential configuration.
31	VIN9	AI	Voltage Input 9. VIN9 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN8 in differential configuration.
32	VIN10	AI	Voltage Input 10. VIN10 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN11 in differential configuration.
33	VIN11	AI	Voltage Input 11. VIN11 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN10 in differential configuration.
34	VIN12	AI	Voltage Input 12. VIN12 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN13 in differential configuration.
35	VIN13	AI	Voltage Input 13. VIN13 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN12 in differential configuration.
36	VIN14	AI	Voltage Input 14. VIN14 is either referenced to VINCOM in single-ended configuration or referenced to a positive input of an input pair with VIN15 in differential configuration.
37	VIN15	AI	Voltage Input 15. VIN15 is either referenced to VINCOM in single-ended configuration or referenced to a negative input of an input pair with VIN14 in differential configuration.
38	GPO3	DO	General-Purpose Output 3. Logic output on GPO3 is referred to the AVDD and AVSS supplies.
39	REF−	AI	Reference Input Negative Terminal. The REF− voltage can span from AVSS to AVDD − 1 V. The reference can be selected through the REF_SELx bits in the setup configuration registers.
40	REF+	AI	Reference Input Positive Terminal. An external reference can be applied between REF+ and REF−. The REF+ voltage can span from AVDD to AVSS + 1 V. The reference can be selected through the REF_SELx bits in the setup configuration registers.
	EP	P	Exposed Pad. Solder the exposed pad to a similar pad on the PCB that is under the exposed pad to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

[1] The dual function pin mnemonics are referenced by the relevant function only throughout this data sheet.
[2] AI is analog input, AO is analog output, P is power supply, N/A is not applicable, DI is digital input, DO is digital output, and DI/O is bidirectional digital input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

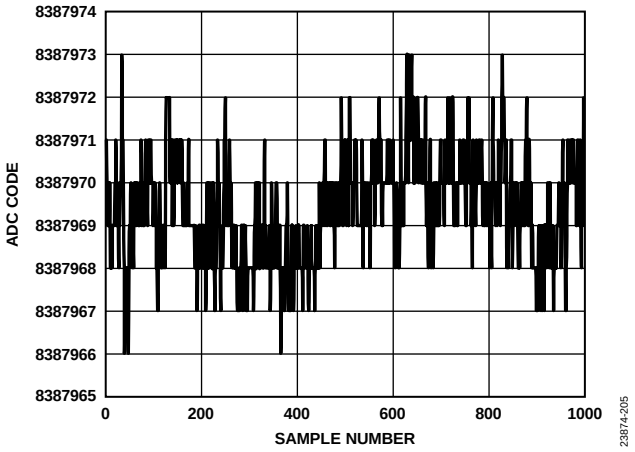


Figure 5. Noise (Output Data Rate = 2.5 SPS)

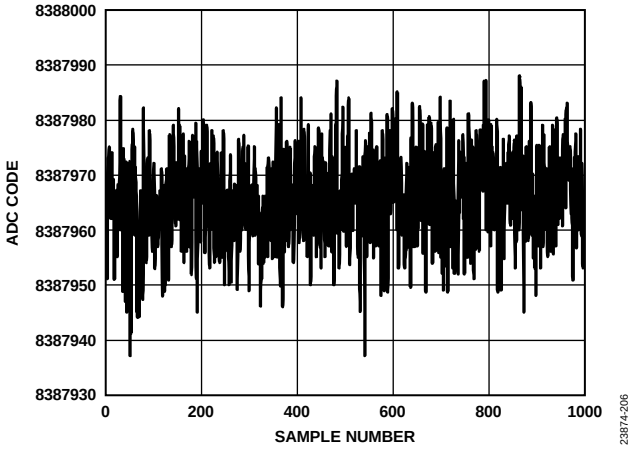


Figure 6. Noise (Output Data Rate = 2.5 kSPS)

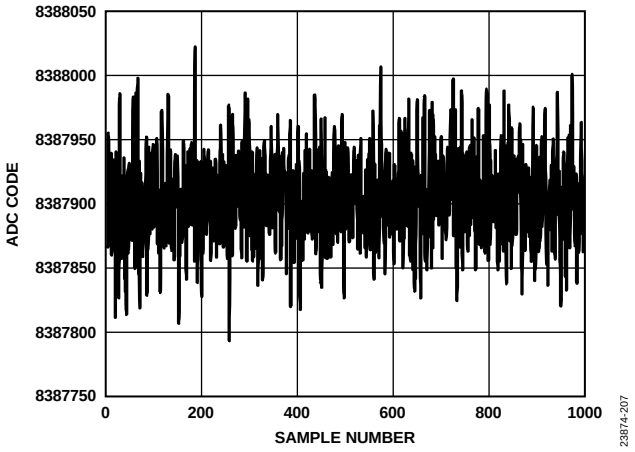


Figure 7. Noise (Output Data Rate = 125 kSPS)

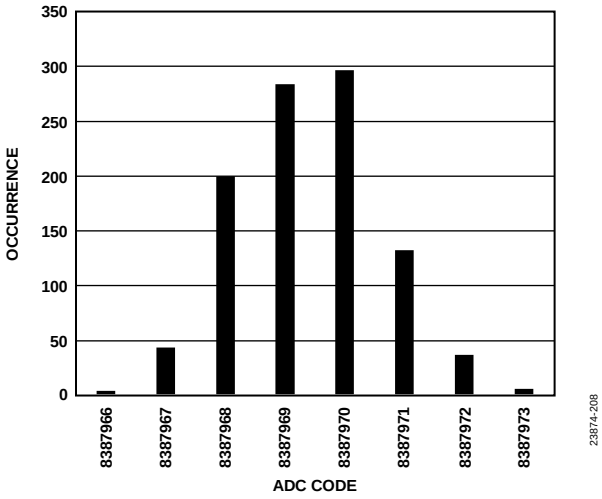


Figure 8. Histogram (Output Data Rate = 2.5 SPS)

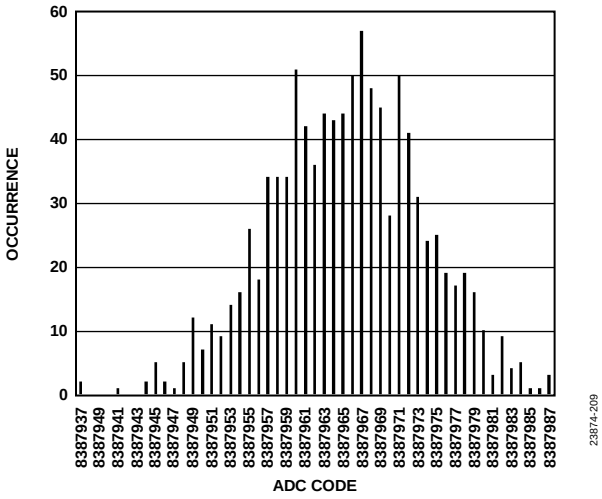


Figure 9. Histogram (Output Data Rate = 2.5 kSPS)

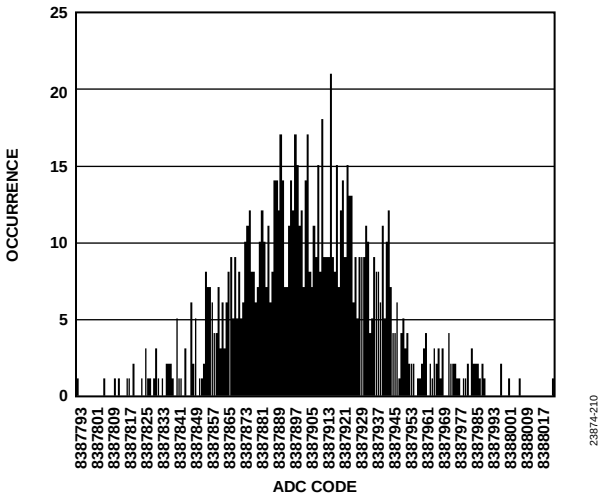


Figure 10. Histogram (Output Data Rate = 125 kSPS

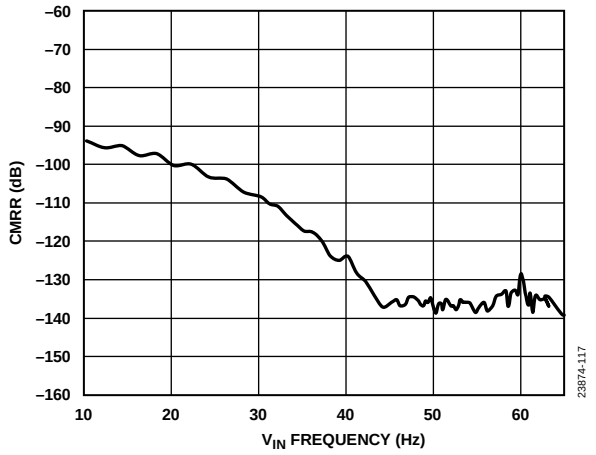


Figure 11. CMRR vs. V_{IN} Frequency (V_{IN} = 0.1 V, Output Data Rate = 20 SPS, Enhanced Filter)

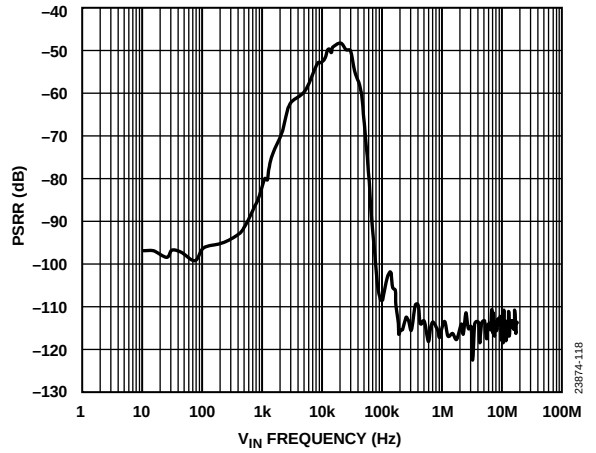


Figure 12. PSRR vs. V_{IN} Frequency

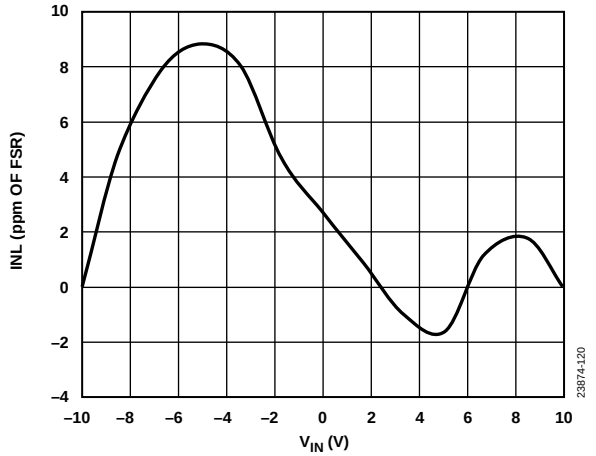


Figure 13. INL vs. V_{IN}

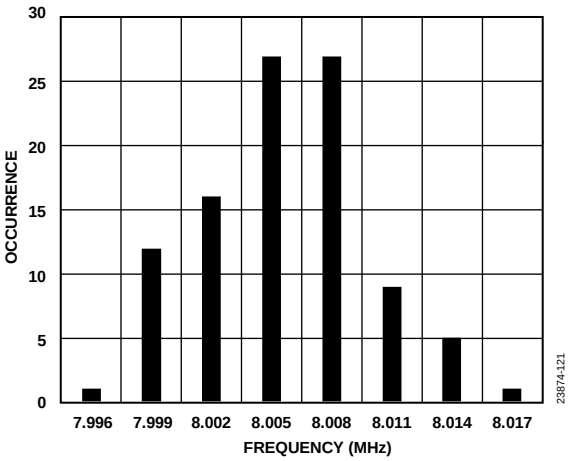


Figure 14. Internal Oscillator Frequency and Accuracy Distribution Histogram

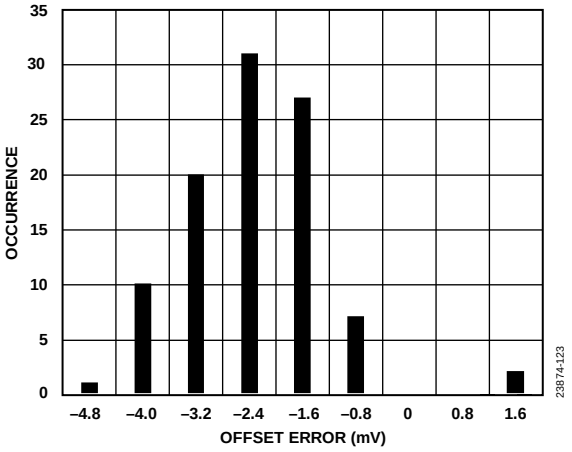


Figure 15. Offset Error Distribution Histogram

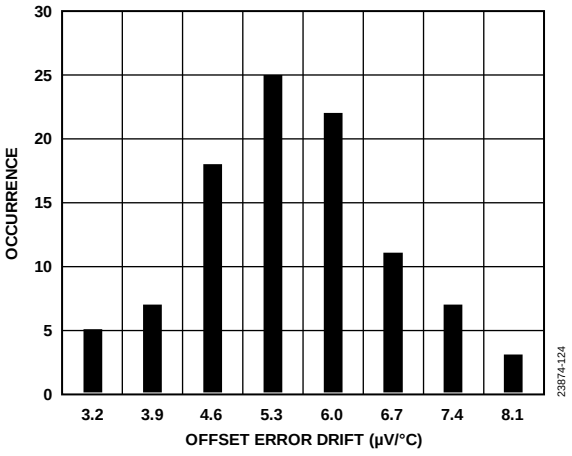


Figure 16. Offset Error Drift Distribution Histogram

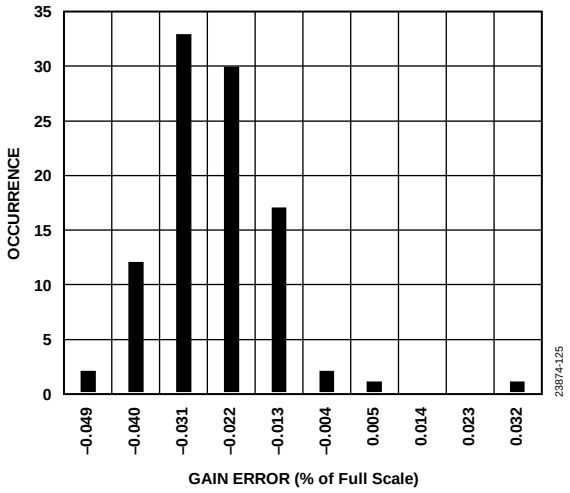


Figure 17. Gain Error Distribution Histogram

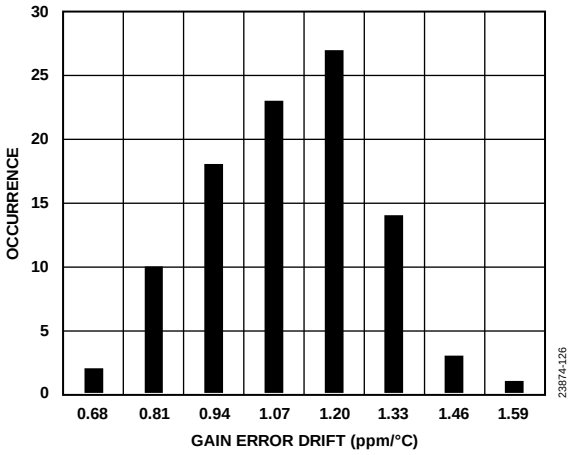


Figure 18. Gain Error Drift Distribution Histogram

THEORY OF OPERATION

The AD4115 offers a fast settling, high resolution, multiplexed ADC with high levels of configurability, including the following features:

- Eight fully differential voltage inputs or 16 single-ended voltage inputs.
- High impedance voltage divider with integrated precision matched resistors
- Embedded proprietary *i*Passives® technology within a small device footprint.
- Per channel configurability where up to eight different setups can be defined. A separate setup can be mapped to each channel. Each setup allows the user to configure whether the buffers are enabled or disabled, gain and offset correction, filter type, ODR, and reference source selection.
- Highly configurable digital filter enabling conversion rates up to 125 kSPS on a single channel and 24.845 kSPS switching.

The AD4115 includes a precision, 2.5 V, low drift (±5 ppm/°C), band gap internal reference. Use this reference in ADC conversions to reduce the external component count. When enabled, the internal reference is output to the REFOUT pin. The internal reference can be used as a low noise biasing voltage for the external circuitry and must be connected to a 0.1 µF decoupling capacitor.

The AD4115 includes two separate linear regulator blocks for the analog and digital circuitry. The analog LDO regulator regulates the AVDD supply to 1.8 V.

The linear regulator for the digital IOVDD supply performs a function similar to the LDO regulator and regulates the input voltage applied at the IOVDD pin to 1.8 V. The serial interface signals always operate from the IOVDD supply seen at the pin. For example, if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD4115 is designed for a multitude of factory automation and process control applications, including PLC and DCS modules. The AD4115 reduces overall system cost and design burden and maintains a high level of accuracy. The AD4115 offers the following system benefits:

- A single 5 V power supply.
- Guaranteed minimum 1 MΩ input impedance.
- Overrange voltage greater than ±10 V.
- Reduced calibration costs.
- High channel count.

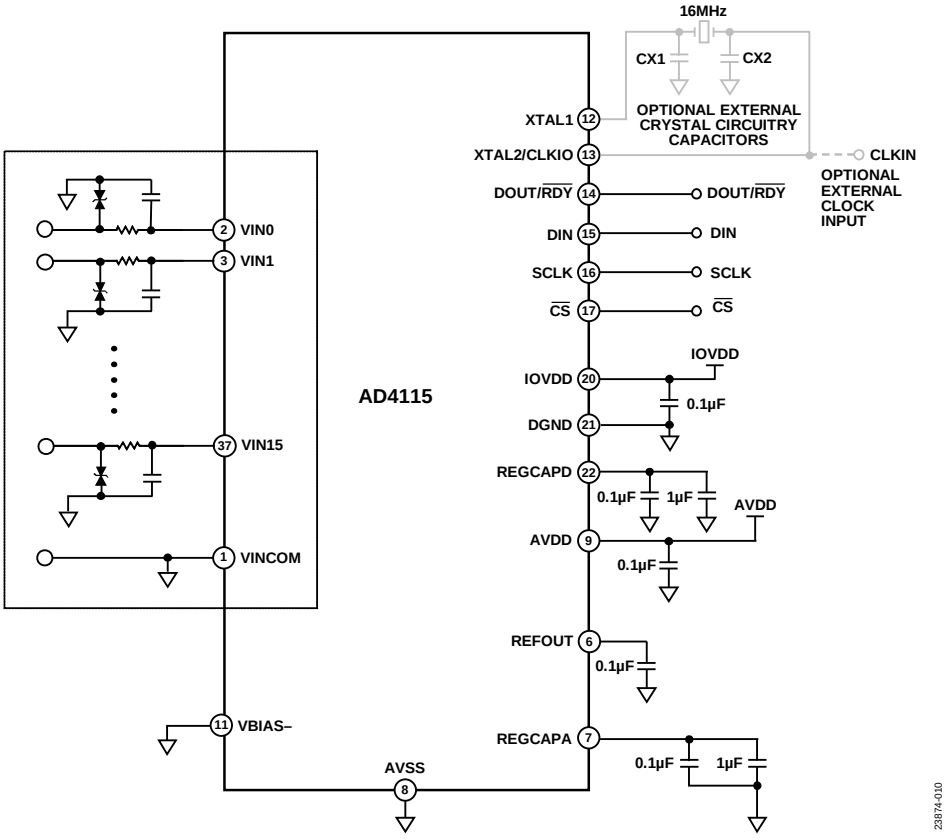


Figure 19. Typical Connection Diagram

POWER SUPPLIES

The AD4115 has two independent power supply pins, AVDD and IOVDD. The AD4115 has no specific requirements for a power supply sequence. However, when all power supplies are stable, a device reset is required. See the AD4115 Reset section for information on how to reset the device.

AVDD powers the internal 1.8 V analog LDO regulator that powers the ADC core. AVDD also powers the crosspoint multiplexer and integrated input buffers. AVDD is referenced to AVSS, and AVDD − AVSS = 5 V. AVDD and AVSS can be a single 5 V supply or ±2.5 V split supplies. Consider the absolute maximum ratings when using split supplies (see the Absolute Maximum Ratings section).

IOVDD powers the internal 1.8 V digital LDO regulator that powers the ADC digital logic. IOVDD sets the voltage levels for the serial peripheral interface (SPI) of the ADC. IOVDD is referenced to DGND, and the voltage from IOVDD to DGND can vary from 2 V (minimum) to 5.5 V (maximum).

Single-Supply Operation (AVSS = DGND)

When the AD4115 is powered from a single supply connected to AVDD, the supply must be 5 V. In this configuration, AVSS and DGND can be shorted together on a single ground plane.

IOVDD can range from 2 V to 5.5 V in this unipolar input configuration.

DIGITAL COMMUNICATION

The AD4115 has either a 3-wire or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and digital signal processors (DSPs). The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. Data is clocked out on the falling (drive) edge and data is clocked in on the rising (sample) edge.

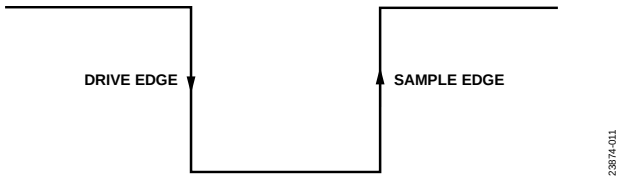


Figure 20. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full ADC register map. This register is an 8-bit, write only register. On power-up or after a reset, the digital interface defaults to a state where the interface expects a write to the communications register. Therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is accessed and if the next operation is a read or write. The RA bits (Bits[5:0] in Register Address 0x00) determine the specific register to which the read or write operation applies (see Table 20).

When the read or write operation to the selected register is complete, the interface returns to the default state to expect a write operation to the communications register.

Figure 21 and Figure 22 show a write to and a read from a register by writing the 8-bit command to the communications register followed by the data for the addressed register.

Figure 21 shows an 8-bit command with the register address followed by 8 bits, 16 bits, or 24 bits of data where the data length on DIN depends on the selected register. Figure 22 shows an 8-bit command with the register address followed by 8 bits, 16 bits, 24 bits, or 32 bits of data where the data length on DOUT depends on the selected register.

To verify correct communication with the device, read the ID register. The ID register is a read only register and contains the value of 0x38DX for the AD4115. The communication register and ID register details are described in Table 7 and Table 8.

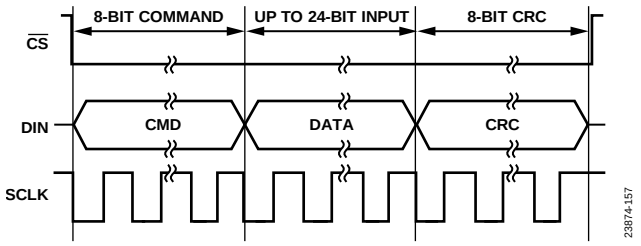


Figure 21. Writing to a Register

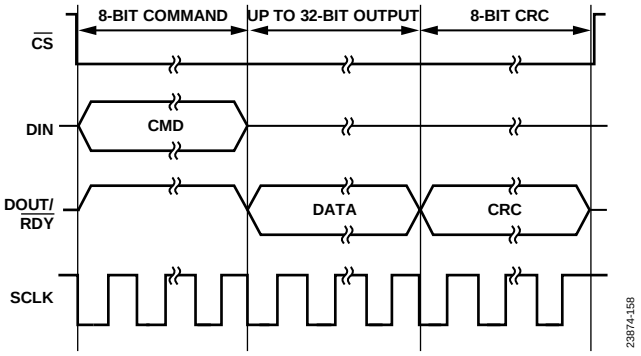


Figure 22. Reading from a Register

AD4115 RESET

When a power-up cycle completes and the power supplies are stable, a device reset is required. If interface synchronization is lost, a device reset is required. A write operation of at least 64 serial clock cycles with DIN high returns the ADC to the default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is used with the digital interface, returning $\overline{CS}$ high sets the digital interface to the default state and halts any serial interface operation.

Table 7. Communications Register Bit Map

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 8. ID Register Bit Map

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x07	ID	[15:0]	ID								0x38DX[1]	R

[1] X means don't care.

CONFIGURATION OVERVIEW

After a power-on or reset, the AD4115 default configuration is as follows:

- Channel configuration: Channel 0 is enabled, the VIN0 and VIN1 pair is selected as the input. Setup 0 is selected (see the Setup Configuration section for more information).
- Setup configuration: the analog input buffers and the reference input buffers are disabled. The REF+ and REF− pins are selected as the reference source. Note that for this setup, the default channel does not operate correctly because the input buffers must be enabled for a VINx input.
- Filter configuration: the sinc5 + sinc1 filter is selected and the maximum output data rate of 125 kSPS is selected.
- ADC mode: continuous conversion mode and the internal oscillator are enabled. The internal reference is disabled.
- Interface mode: cyclic redundancy check (CRC) and the data and status output are disabled.

Note that only a few of the register setting options are shown in this example list. For full register information, see the Register Details section.

Figure 23 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration.
- Setup configuration.
- ADC mode and interface mode configuration.

Channel Configuration

The AD4115 has 16 independent channels and eight independent setups. The user can select any input pair on any channel, as well as any of the eight setups for any channel, which allows full flexibility in the channel configuration. This flexibility allows per channel configuration when using differential inputs and single-ended inputs because each channel can have an individual dedicated setup.

Channel Registers

The channel registers select which voltage input is used for the corresponding channel. Each channel register contains a channel enable/disable bit and the setup selection bits that select from eight available setups to use for the channel.

When the AD4115 operates with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order from Channel 0 to Channel 15. If a channel is disabled, that channel is skipped by the sequencer. Details on the channel register for Channel 0 are shown in Table 9.

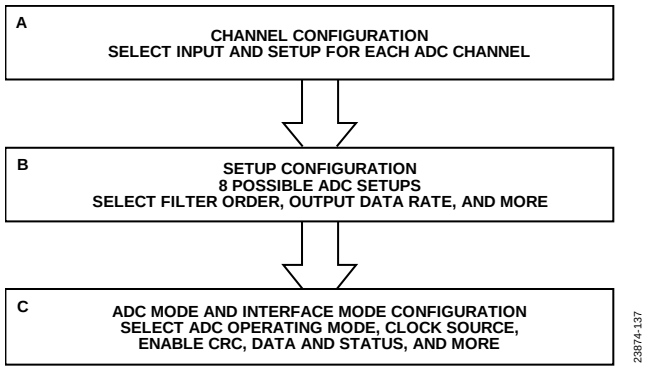


Figure 23. Suggested ADC Configuration Flow

Table 9. Channel Register 0 Bit Map

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			Reserved		INPUT0[9:8]		0x8001	R/W
		[7:0]	INPUT0[7:0]									

Setup Configuration

The AD4115 has eight independent setups. Each setup consists of the following four types of registers:

- Setup configuration register
- Filter configuration register
- Gain register
- Offset register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Gain Register 0, and Offset Register 0. Figure 24 shows the grouping of these registers. The setup is selectable from the channel registers (see the Channel Configuration section), which allows each channel to be assigned to one of the eight separate setups. Table 10 through Table 13 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

Setup Configuration Registers

The setup configuration registers allow the user to select between bipolar mode and unipolar mode to determine the ADC output coding. The user can also select the reference source using these registers. Three reference source options are available: a reference connected between the REF+ and REF− pins, the internal reference, or using AVDD − AVSS as the reference. The input and reference buffers can also be enabled or disabled using these registers.

Filter Configuration Registers

The filter configuration registers select which digital filter is used at the output of the ADC modulator. Set the bits in these registers to select the order of the filter and the output data rate. For more information, see the Digital Filter section.

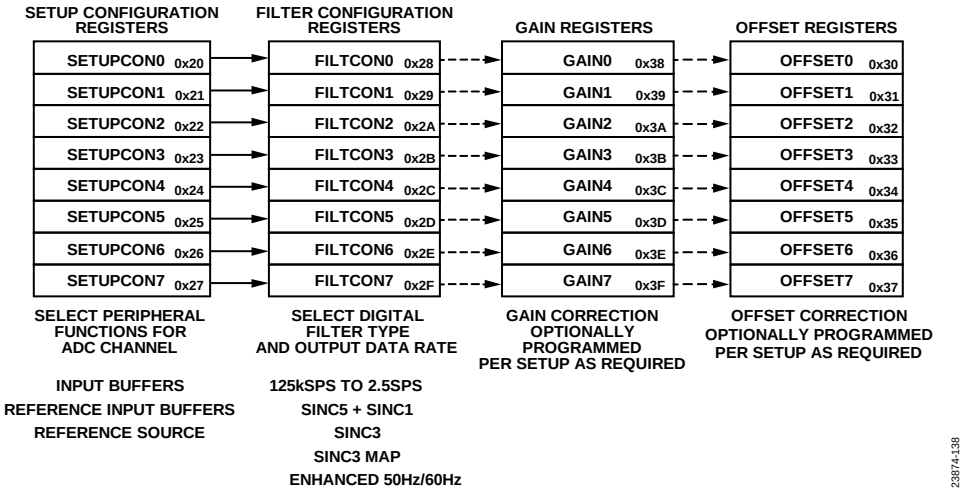


Figure 24. ADC Setup Register Grouping

Table 10. Setup Configuration Register 0

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	INBUF0		0x1000	R/W
		[7:0]	Reserved		REF_SEL0		Reserved					

Table 11. Filter Configuration Register 0

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x28	FILTCON0	[15:8]	SINC3_MAP0	Reserved			ENHFILTEN0	ENHFILT0			0x0500	R/W
		[7:0]	Reserved	ORDER0		ODR0						

Table 12. Gain Register 0

Register	Name	Bits	Bits[23:0]	Reset	R/W
0x38	GAIN0	[23:0]	GAIN0	0x5XXXX0	R/W

Table 13. Offset Register 0

Register	Name	Bits	Bits[23:0]	Reset	R/W
0x30	OFFSET0	[23:0]	OFFSET0	0x800000	R/W

Gain Registers

The gain registers are 24-bit, read and write registers that hold the gain calibration coefficient for the ADC. The power-on reset value of the gain registers is 0x5XXXX0.

Offset Registers

The offset registers are 24-bit, read and write registers that hold the offset calibration coefficient for the ADC. The power-on reset value of the offset registers is 0x800000.

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for the AD4115 to use, as well as the mode for the digital interface.

ADC Mode Register

The ADC mode register primarily sets the ADC conversion mode to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. The ADC mode register also contains the clock source select bits and internal reference enable bit. The reference select bits are contained in the setup configuration registers (see the Setup Configuration section for more information). The details of the ADC mode register are shown in Table 14.

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data plus status read, and continuous read mode. The details of this register are shown in Table 15. For more information, see the Digital Interface section.

Table 14. ADC Mode Register

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x01	ADCMODE	[15:8]	REF_EN	Reserved	SING_CYC	Reserved		Delay			0x2000	R/W
		[7:0]	Reserved	Mode			CLOCKSEL	Reserved				

Table 15. Interface Mode Register

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	IFMODE	[15:8]	Reserved			ALT_ SYNC	IOSTRENGTH	Reserved		DOUT_RESET	0x0000	R/W
		[7:0]	CONTREAD	DATA_ STAT	REG_ CHECK	Reserved	CRC_EN		Reserved	WL16		

NOISE PERFORMANCE AND RESOLUTION

Table 16 to Table 17 show the rms noise, peak-to-peak noise, effective resolution, and noise free (peak-to-peak) resolution of the device for various ODRs. These values are typical and are measured with an external 2.5 V reference and with the ADC continuously converting on multiple channels. The values in Table 16 and Table 17 are generated for the ±10 V voltage input range, with a differential input voltage of 0 V. Note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

Table 16. ±10 V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc5 + Sinc1 Filter

Default Output Data Rate (SPS), SING_CYC = 0 and Single Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
125,000	24,845	40.25 µs	125,000	140.36	17.12	926.38	14.40
62,500	20,725	48.25 µs	62,500	124.42	17.29	821.17	14.57
31,250	15,564	64.25 µs	31,250	99.14	17.62	654.32	14.90
25,000	13,841	72.25 µs	25,000	89.57	17.77	591.16	15.05
15,625	10,390	96.25 µs	15,625	72.94	18.06	481.40	15.34
10,390	10,390	96.25 µs	15,625	71.01	18.10	468.67	15.38
4994	4,994	200.25 µs	5952.4	45.67	18.74	301.42	16.02
2498	2,499	400.25 µs	2717.4	32.42	19.23	213.97	16.51
1000	1,000	1 ms	1033.1	20.24	19.91	133.58	17.19
500	500	2 ms	508.1	13.88	20.46	91.61	17.74
395.5	395.5	2.53 ms	400.6	12.61	20.60	83.23	17.87
200	200	5 ms	201.3	9.702	20.98	64.03	18.25
100	100	10 ms	100.3	7.36	21.37	48.58	18.65
59.87	59.89	16.7 ms	59.98	5.38	21.83	35.51	19.10
49.92	49.92	20.03 ms	50	5.52	21.79	36.43	19.07
20	20.	50 ms	20.01	4.52	22.08	29.83	19.35
16.7	16.66	60.03 ms	16.67	4.07	22.23	26.86	19.51
10	10	100 ms	10	3.15	22.6	16.1	20.2
5	5	200 ms	5	2.92	22.7	12.1	20.7
2.5	2.5	400 ms	2.5	2.49	22.7	12	20.7

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] The noise values are based on 1000 samples for data rates ≥ 395.5 SPS per channel and based on 100 samples for data rates ≤ 200 SPS per channel.

Table 17. ±10 V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc3 Filter

Default Output Data Rate (SPS), SING_CYC = 0 and Single Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
125,000	41,237	24.3 µs	125,000	1008	14.28	6652	11.55
62,500	20,725	48.3 µs	62,500	176.41	16.79	1164	14.07
31,250	10,389.6	96.3 µs	31,250	82.49	17.89	544.43	15.16
25,000	8,316.0	120.3 µs	25,000	73.71	18.05	486.49	15.33
15,625	5,201.6	192.3 µs	15,625	57.99	18.40	382.73	15.67
10,416.7	3,469.2	288.3 µs	10,417	46.93	18.70	309.74	15.98
5000	1,666.0	600.3 µs	5000	31.45	19.28	207.57	16.56
2500	833.2	1.2 ms	2500	22.83	19.74	150.68	17.02
1000	333.33	3 ms	1000	14.35	20.41	94.71	17.69
500	166.67	6 ms	500.0	10.82	20.82	71.41	18.10
400.6	133.51	7.49 ms	400.6	9.66	20.98	63.76	18.26
200	66.67	15 ms	200.0	7.30	21.39	48.18	18.66
100	33.33	30 ms	100.0	5.81	21.71	38.35	18.99
59.98	19.99	50.02 ms	59.98	4.70	22.02	31.02	19.30
50	16.67	60 ms	50.00	4.48	22.09	29.57	19.37

Default Output Data Rate (SPS), SING_CYC = 0 and Single Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
20	6.67	150 ms	20.00	3.30	22.53	21.78	19.81
16.67	5.56	180 ms	16.67	2.78	22.78	18.35	20.06
10	3.33	300 ms	10.00	2.95	22.7	14.9	20.4
5	1.67	600 ms	5.00	2.63	22.7	11.9	20.7
2.5	0.83	1.2 s	2.50	2.43	22.7	11.9	20.7

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.
[2] The noise values are based on 1000 samples for data rates ≥381 SPS per channel and based on 100 samples for data rates ≤200.3 SPS per channel.

CIRCUIT DESCRIPTION

MULIPLEXER

The device has 17 voltage input pins, VIN0 to VIN15 and VINCOM. Each pin connects to the internal multiplexer. The multiplexer enables these inputs to be configured as input pairs. The AD4115 can have up to 16 active channels. When more than one channel is enabled, the channels are automatically sequenced in order from the lowest enabled channel number to the highest enabled channel number. The multiplexer output connects to the input of the integrated true rail-to-rail buffers. These buffers can be bypassed and the multiplexer output can be directly connected to the ADC switched capacitor input. The simplified input circuits are shown in Figure 25.

VOLTAGE INPUTS

The AD4115 can be set up to have either 16 single-ended inputs or eight fully differential inputs. The voltage divider on the AFE has a division ratio of 10 and consists of precision matched resistors that enable an input range of ±20 V from a single 5 V power supply.

Enable the input buffers in the corresponding setup configuration register for the voltage input channels (see Table 29).

Fully Differential Inputs

The differential inputs are paired together in the following pairs: VIN0 and VIN1, VIN2 and VIN3, VIN4 and VIN5, VIN6 and VIN7, VIN8 and VIN9, VIN10 and VIN11, VIN12 and VIN13, and VIN14 and VIN15.

Single-Ended Inputs

The user can measure up to 16 different single-ended voltage inputs. In this case, each voltage input must be paired with the VINCOM pin. Connect the VINCOM pin externally to the AVSS pin.

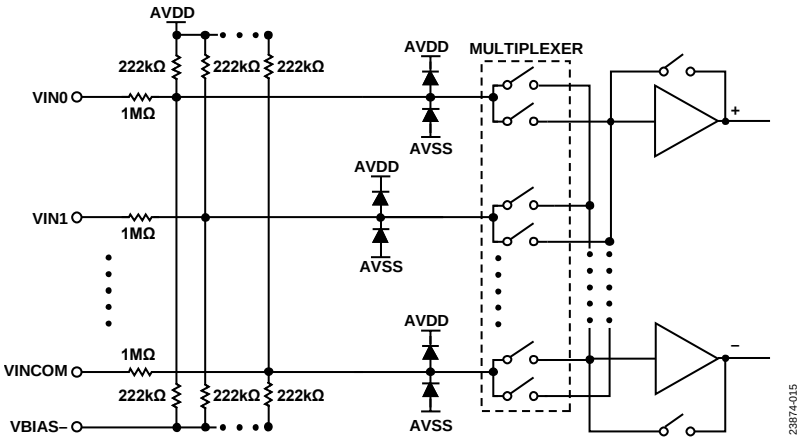


Figure 25. Simplified Voltage Input Circuit

ABSOLUTE INPUT PIN VOLTAGES

The AD4115 voltage input pins are specified for an accuracy of ±10 V, specifically for the differential voltage between any two voltage input pins.

The voltage input pins have separate specifications for the absolute voltage that can be applied, and the unique design of the voltage divider network of the analog front end enables overvoltage robustness on the AD4115, which means the allowed overvoltages vary depending on the AVDD supply. Figure 26 shows the different degrees of robustness that can be achieved for AVDD = 5 V. Figure 26 provides a visual representation and guidance on how an overvoltage on a voltage pin can affect the overall device accuracy.

The guaranteed accuracy section of Figure 26 shows the voltage range that can be applied to a voltage input pin and achieve guaranteed accuracy.

The no loss of accuracy sections show the voltage levels that can be applied without degrading the accuracy of other channels.

The no damage to device sections show the allowable positive and negative voltages that can be applied to a voltage input pin without exceeding the absolute maximum. The performance of other channels is degraded, but the performance recovers when the overvoltage is removed. This voltage range is specified as an absolute maximum rating of ±65 V.

Operation beyond the maximum operating conditions for extended periods can affect product reliability.

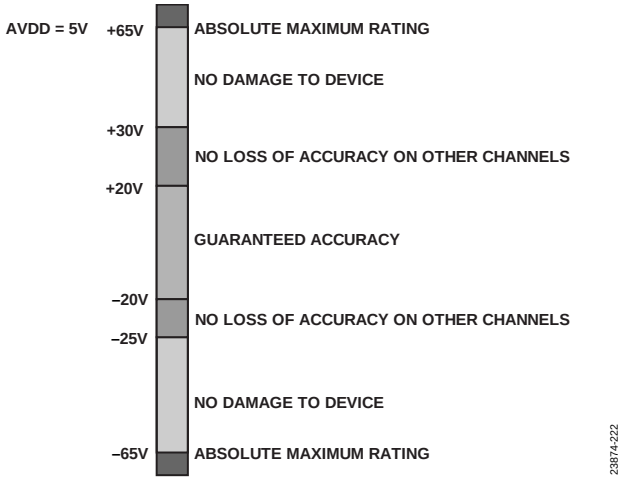


Figure 26. Absolute Input Pin Voltages, AVDD = 5 V

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage that results in a code of 00 … 00, a midscale voltage that results in a code of 100 … 000, and a full-scale input voltage that results in a code of 111 … 111.

The output code for any input voltage is represented with the following equation:

$$Code = (2^N \times V_{IN} \times 0.1)/V_{REF}$$

where:
N = 24 (the number of bits).
V_{IN} is the input voltage.
V_{REF} is the reference voltage.

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage that results in a code of 000 … 000, a zero differential input voltage that results in a code of 100 … 000, and a positive full-scale input voltage that results in a code of 111 … 111. The output code for any analog input voltage is represented with the following equation:

$$Code = 2^{N-1} \times ((V_{IN} \times 0.1/V_{REF}) + 1)$$

AD4115 REFERENCE OPTIONS

The AD4115 provides the reference option of either supplying an external reference to the REF+ and REF− device pins using AVDD − AVSS as the reference, or allowing use of the internal 2.5 V, low noise, low drift reference. To select the reference source to be used by the analog input, set the REF_SELx bits, Bits[5:4], in the corresponding setup configuration register appropriately. The structure of the Setup Configuration Register 0 is shown in Table 10. By default, the AD4115 uses an external reference on power-up.

Internal Reference

The AD4115 includes a low noise, low drift, internal voltage reference that has a 2.5 V output. The internal reference is output on the REFOUT pin after the REF_EN bit in the ADC mode register is set and is decoupled to AVSS with a 0.1 µF capacitor. The AD4115 internal reference is disabled by default on power-up.

External Reference

The AD4115 has a fully differential reference input applied through the REF+ and REF− pins. Standard low noise, low drift voltage references, such as the ADR4525, are recommended for this use. Apply the external reference to the AD4115 reference pins, as shown in Figure 27. Decouple the output of any external reference to AVSS. As shown in Figure 27, the ADR4525 output is decoupled with a 0.1 µF capacitor at the output for stability purposes. The output is connected to a 4.7 µF capacitor that acts as a reservoir for any dynamic charge required by the ADC and is followed by another 0.1 µF decoupling capacitor at the REF+ input. This capacitor is placed as close as possible to the REF+ and REF− pins.

The REF− pin is connected directly to the AVSS potential. When an external reference is used instead of the internal reference to supply the AD4115, ensure that the REFOUT pin is not hardwired to AVSS, which can draw a large current on power-up. The internal reference is controlled by the REF_EN bit (Bit 15) in the ADC mode register, as shown in Table 14. If the internal reference is not used elsewhere in the application, ensure that the REF_EN bit is disabled.

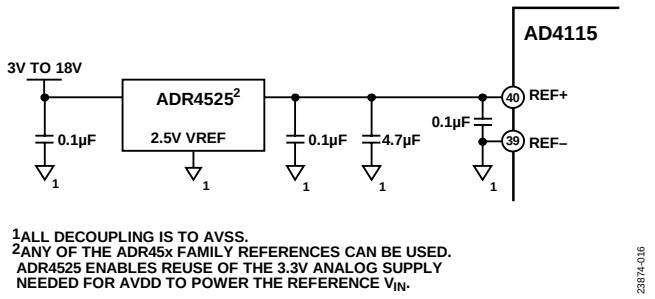


Figure 27. ADR4525 Connected to AD4115 REF+ and REF– Pins

BUFFERED REFERENCE INPUT

The AD4115 has true rail-to-rail, integrated, precision unity-gain buffers on both ADC reference inputs. The buffers provide high input impedance and allow high impedance external sources to be directly connected to the reference inputs. The integrated reference buffers can fully drive the internal reference switch capacitor sampling network to simplify the reference circuit requirements. Each reference input buffer amplifier is fully chopped and minimizes the offset error drift and 1/f noise of the buffer. When using a voltage reference, such as the ADR4525, these buffers are not required because the reference has proper decoupling and can drive the reference inputs directly.

CLOCK SOURCE

The AD4115 uses a nominal master clock of 8 MHz and can source the device sampling clock from one of the following three sources:

- An internal oscillator.
- An external crystal. Use a 16 MHz crystal automatically divided internally to set the 8 MHz clock.
- An external clock source.

All output data rates listed in this data sheet relate to a master clock rate of 8 MHz. Using a lower clock frequency from, for instance, an external source scales any listed data rate proportionally. To achieve the specified data rates, particularly rates for rejection of 50 Hz and 60 Hz, use a 8 MHz clock. To select the master clock source, set the CLOCKSEL bits (Bits[3:2]) in the ADC mode register, as shown in Table 14. The default operation on power-up and reset of the AD4115 is to operate with the internal oscillator. The user can use the SINC3_MAPx bits in the filter configuration registers to fine tune the output data rate and filter notch at low output data rates.

Internal Oscillator

The internal oscillator runs at 16 MHz and is internally divided down to 2 MHz for the modulator. The internal oscillator can be used as the ADC master clock and is the default clock source for the AD4115, which is specified with an accuracy of −2.5% to +2.5%.

The internal clock oscillator can be output on the XTAL2/CLKIO pin. In this case, the clock output is driven to the IOVDD logic level. This option can affect the AD4115 dc performance because of the disturbance introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and affect performance to a greater extent. This effect is further exaggerated if the IOSTRENGTH bit of the interface mode register is set at higher IOVDD levels (see Table 23).

External Crystal

If higher precision, lower jitter clock sources are required, the AD4115 can use an external crystal to generate the master clock. The crystal connects to the XTAL1 and XTAL2/CLKIO pins. The FA-20H, a 16 MHz, 10 ppm, 9 pF crystal from Epson-Toyocom is available in a surface-mount package and is acceptable for this use. As shown in Figure 28, insert two capacitors (CX1 and CX2) from the traces connecting the crystal to the XTAL1 and XTAL2/CLKIO pins. These capacitors allow circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2/CLKIO pins. Therefore, the values of these capacitors differ depending on the PCB layout and the crystal used.

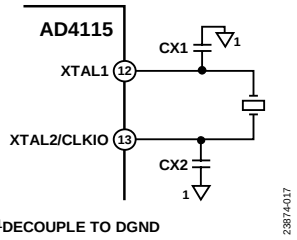


Figure 28. External Crystal Connections

The external crystal circuitry can be sensitive to the SCLK edges depending on the SCLK frequency, IOVDD voltage, crystal circuitry layout, and the crystal used. During crystal startup, any disturbances caused by the SLCK edges can cause double edges on the crystal input, which results in invalid conversions until the crystal voltage reaches a high enough level such that any interference from the SCLK edges is insufficient to cause double clocking. To avoid this double clocking, ensure that the crystal circuitry reaches a sufficient voltage level after startup before applying any serial clocks.

Because of the nature of the crystal circuitry, it is recommended to perform empirical testing of the circuit under the required conditions with the final PCB layout and crystal to ensure correct operation.

External Clock

The AD4115 can also use an externally supplied clock. In systems where an externally supplied clock is used, the external clock is routed to the XTAL2/CLKIO pin. In this configuration, the XTAL2/ CLKIO pin accepts the externally sourced clock and routes the clock input to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

DIGITAL FILTER

The AD4115 has the following three flexible filter options to optimize noise, settling time, and rejection:

- The sinc5 + sinc1 filter.
- The sinc3 filter.
- Enhanced 50 Hz and 60 Hz rejection filters.

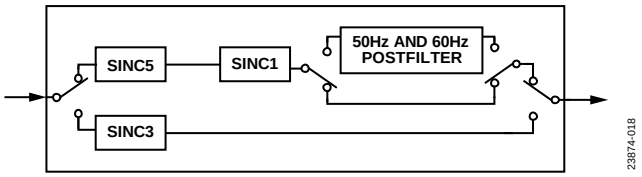


Figure 29. Digital Filter Block Diagram

To configure the filter and output data rate, set the appropriate bits in the filter configuration register for the selected setup. Each channel can use a different setup and, therefore, a different filter and output data rate. See the Register Details section for more information.

SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at multiplexed applications and achieves single-cycle settling at output data rates of ≤10 kSPS. The sinc5 block output is fixed at the maximum rate of 125 kSPS, and the sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 30 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS output data rate. The sinc5 + sinc1 filter has narrow notches and a slow roll-off over frequency.

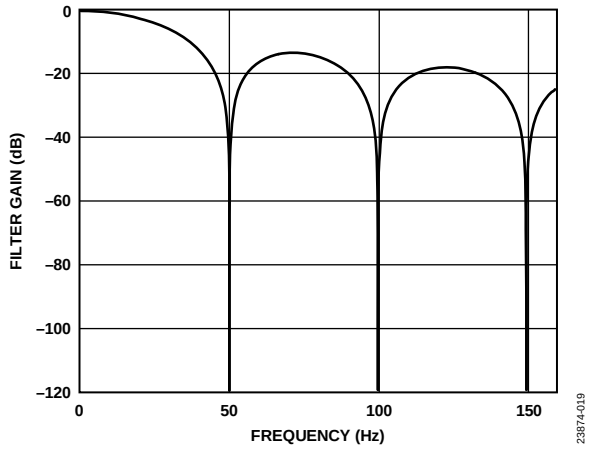


Figure 30. Sinc5 + Sinc1 Filter Response at 50 SPS ODR

The output data rates with the accompanying settling time and rms noise for the sinc5 + sinc1 filter are shown in Table 16.

SINC3 FILTER

The sinc3 filter achieves optimal single-channel noise performance at lower rates and is most suitable for single-channel applications. The sinc3 filter always has a settling time (t_{SETTLE}) equal to the following equation:

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 31 shows the frequency domain filter response for the sinc3 filter. The sinc3 filter has fast roll-off over frequency and has wide notches for optimal notch frequency rejection.

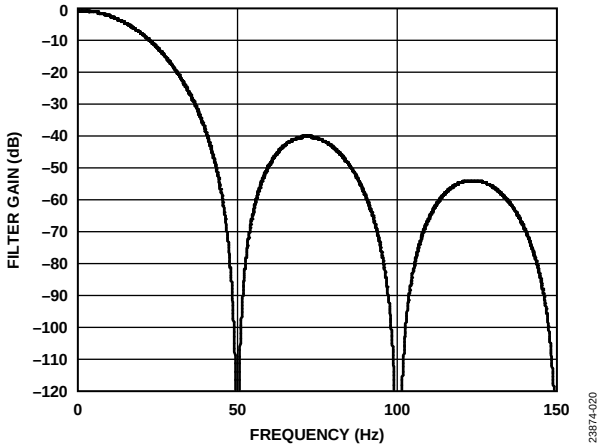


Figure 31. Sinc3 Filter Response

The output data rates with the accompanying settling time and rms noise for the sinc3 filter are shown in Table 17. To fine tune the output data rate for the sinc3 filter, set the SINC3_MAPx bit in the appropriate filter configuration register. If this bit is set, the filter register mapping changes to directly program the sinc3 filter decimation rate. All other options are eliminated. To calculate the data rate when on a single channel, use the following equation:

$$Output\ Data\ Rate = f_{MOD}/(32 \times FILTCONx[14:0])$$

where:
f_{MOD} is the modulator rate (MCLK/2) and is equal to 4 MHz.
FILTCONx[14:0] is the contents of the filter configuration registers with the MSB excluded.

For example, to achieve an output data rate of 50 SPS with the SINC3_MAPx bit enabled, set the FILTCONx register, Bits[14:0], to a value of 2500.

SINGLE-CYCLE SETTLING MODE

To configure the AD4115 to be in a single-cycle settling mode, set the SING_CYC bit in the ADC mode register so that only fully settled data is output. This mode reduces the output data rate to be equal to the ADC settling time for the selected output data rate to achieve single-cycle settling. This bit has no effect on the sinc5 + sinc1 filter at output data rates of ≤10 kSPS or when multiple channels are enabled.

Figure 32 shows a step on the analog input with single-cycle settling mode disabled and the sinc3 filter selected. The analog input requires at least three cycles after the step change for the output to reach the final settled value.

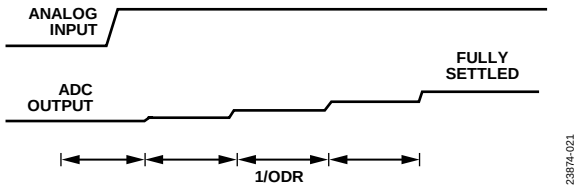


Figure 32. Step Input Without Single-Cycle Settling

Figure 33 shows the same step on the analog input with single-cycle settling enabled. The analog input requires at least a single cycle for the output to be fully settled. The output data rate, as indicated by the $\overline{RDY}$ signal, reduces to equal the settling time of the filter at the selected output data rate.

Figure 33. Step Input with Single Cycle Settling

ENHANCED 50 Hz AND 60 Hz REJECTION FILTERS

The enhanced filters provide rejection of 50 Hz and 60 Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate at up to 27.27 SPS or reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters postfilter the output of the sinc5 + sinc1 filter to operate. For this reason, the user must select the sinc5 + sinc1 filter when using the enhanced filters to achieve the specified settling time and noise performance. Table 18 shows the enhanced filter output data rates with the accompanying settling time, rejection, and voltage input rms noise and resolution. Figure 34 to Figure 41 show the frequency domain plots of the responses from the enhanced filters.

Table 18. Enhanced Filter Output Data Rate, Settling Time, Rejection, and Voltage Input Noise

Output Data Rate (SPS)	Settling Time (ms)	Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (dB)[1]	Noise (µV rms)	Peak-to-Peak Resolution (Bits)	Comments
27.27	36.67	47	6.44	19.1	See Figure 34 and Figure 37
25	40	62	6.09	19.2	See Figure 35 and Figure 38
20	50	85	5.54	19.35	See Figure 36 and Figure 39
16.667	60	90	5.38	19.51	See Figure 40 and Figure 41

[1] Master clock = 2.00 MHz.

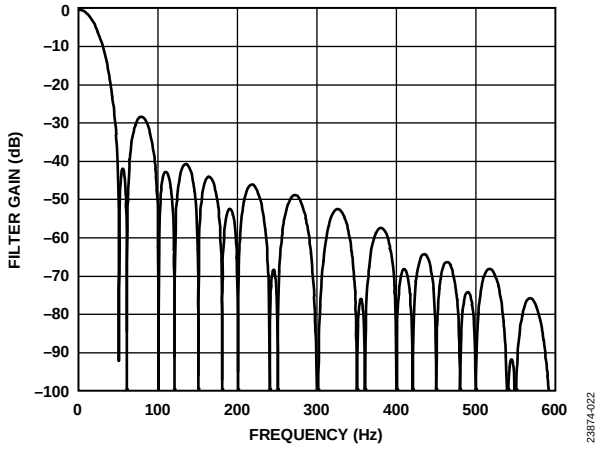


Figure 34. 27.27 SPS ODR, 36.67 ms Settling Time

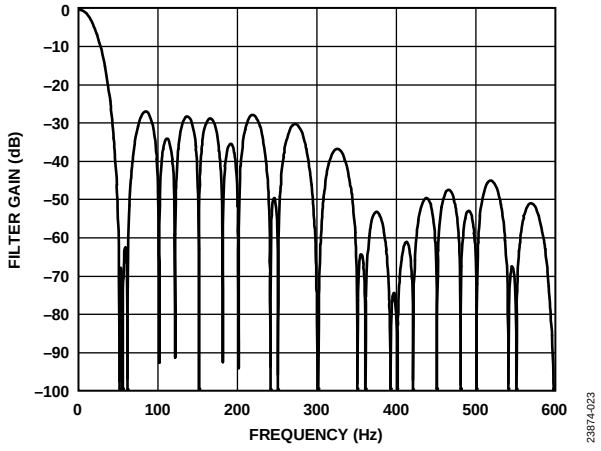


Figure 35. 25 SPS ODR, 40 ms Settling Time

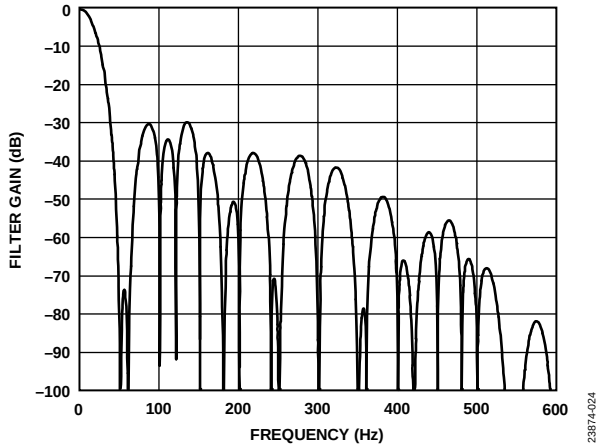


Figure 36. 20 SPS ODR, 50 ms Settling Time

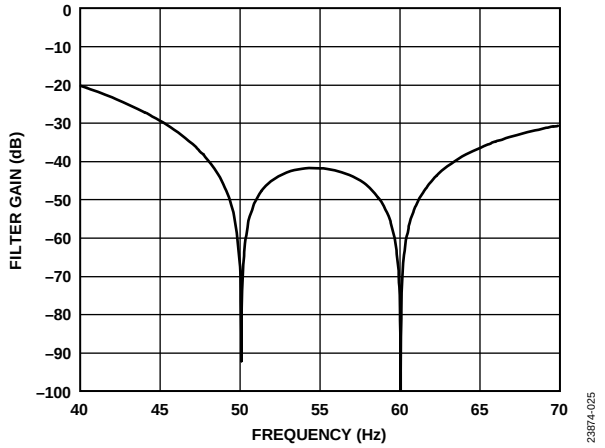


Figure 37. 27.27 SPS ODR, 36.67 ms Settling Time (40 Hz to 70 Hz)

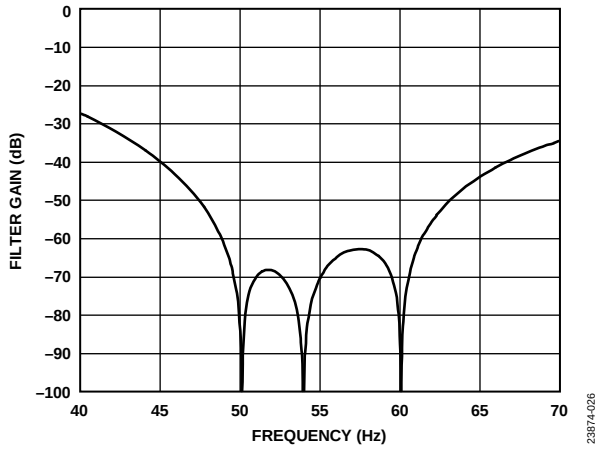


Figure 38. 25 SPS ODR, 40 ms Settling Time (40 Hz to 70 Hz)

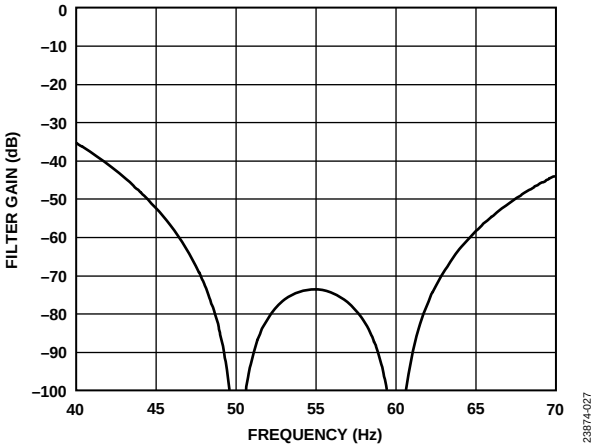


Figure 39. 20 SPS ODR, 50 ms Settling Time (40 Hz to 70 Hz)

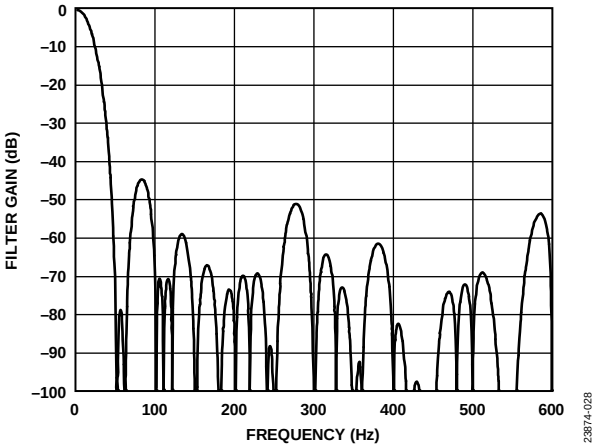


Figure 40. 16.667 SPS ODR, 60 ms Settling Time

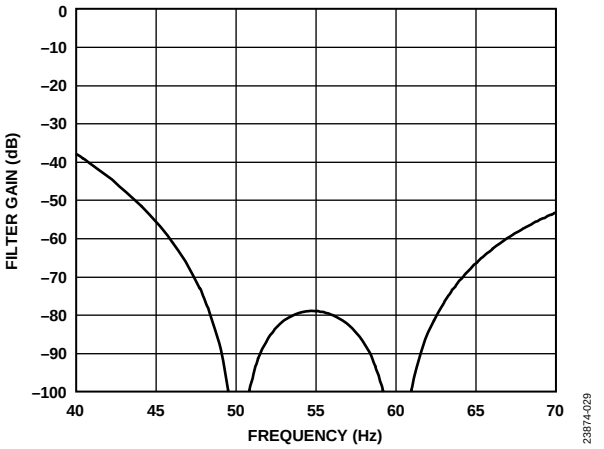


Figure 41. 16.667 SPS ODR, 60 ms Settling Time (40 Hz to 70 Hz)

OPERATING MODES

The AD4115 has nine operating modes that can be set from the ADC mode register and interface mode register (see Table 22 and Table 23). These modes include the following:

- Continuous conversion mode
- Continuous read mode
- Single conversion mode
- Standby mode
- Power-down mode
- Four calibration modes

CONTINUOUS CONVERSION MODE

Continuous conversion mode (see Figure 42) is the default power-up mode. The AD4115 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the $\overline{RDY}$ output also goes low when a conversion is complete. To read a conversion, write to the communications register to indicate that the next operation is a read of the data register. When the data-word is read from the data register, the DOUT/$\overline{RDY}$ pin goes high. The user can read this register additional times, if required. However, ensure that the data register is not accessed at the completion of the next conversion. Otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels and performs one conversion on each channel. When all channels are converted, the sequence starts again with the first channel. The channels are converted in order from the lowest enabled channel to the highest enabled channel. The data register updates as soon as each conversion is available. The $\overline{RDY}$ output pulses low each time a conversion is available and the user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STAT bit in the interface mode register is set to 1, the conversion data and the contents of the status register are output each time the data register is read. The four LSBs of the status register indicate the channel to which the conversion corresponds.

CONTINUOUS READ MODE

In continuous read mode (see Figure 43), it is not required to write to the communications register before reading ADC data. Apply only the required number of serial clocks after the $\overline{RDY}$ output goes low to indicate the end of a conversion. When the conversion is read, the $\overline{RDY}$ output returns high until the next conversion is available. In this mode, the data can be read only once. Ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD4115 to read the data-word, the serial output register resets shortly before the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode. To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while the $\overline{RDY}$ output is low. Alternatively, apply a software reset (64 serial clocks with $\overline{CS}$ = 0 and DIN = 1) to reset the ADC and all register contents. The dummy read and the software reset are the only commands that the interface recognizes after the interface is placed in continuous read mode. Hold DIN low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn with the status bits appended to the data if the DATA_STAT bit is set in the interface mode register. The four LSBs of the status register indicate the channel to which the conversion corresponds.

SINGLE CONVERSION MODE

In single conversion mode (see Figure 44), the AD4115 performs a single conversion and is placed in standby mode when the conversion is complete. The $\overline{RDY}$ output goes low to indicate the completion of a conversion. When the data-word is read from the data register, the $\overline{RDY}$ output goes high. The data register can be read several times, if required, even when the $\overline{RDY}$ output goes high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When the first conversion starts, the $\overline{RDY}$ output goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. When the conversion is available, the $\overline{RDY}$ output goes low and the ADC selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is performed. When the next conversion is complete, the data register updates, which allows the user a limited period in which to read the conversion. When the ADC performs a single conversion on each selected channel, the ADC returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register and the conversion are output each time the data register is read. The four LSBs of the status register indicate the channel to which the conversion corresponds.

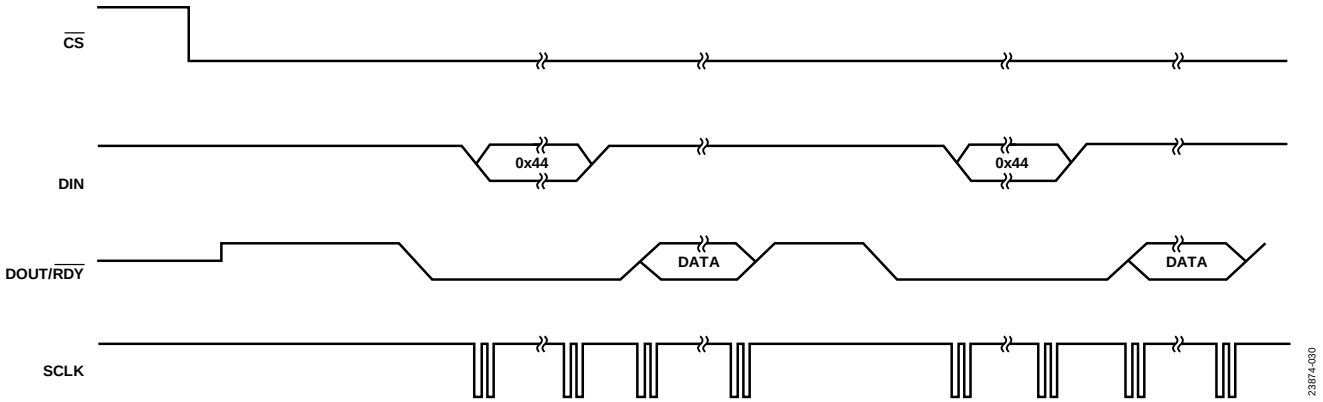


Figure 42. SPI Communication in Continuous Conversion Mode

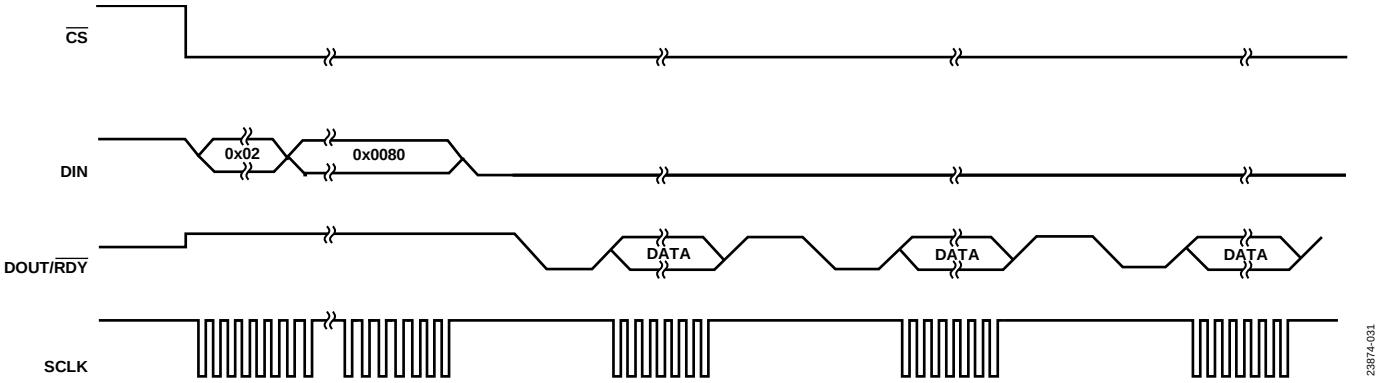


Figure 43. SPI Communication in Continuous Read Mode

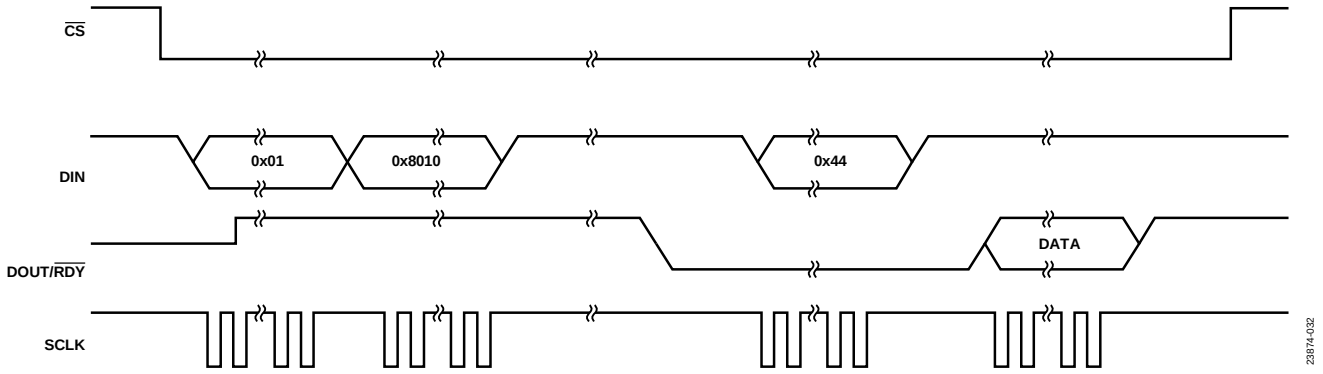


Figure 44. SPI Communication in Single Conversion Mode

STANDBY MODE AND POWER-DOWN MODE

In standby mode, most blocks are powered down. The LDO regulators remain active so that the registers maintain the individual register contents. The crystal oscillator remains active if selected. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator).

In power-down mode, all blocks are powered down, including the LDO regulators. All registers lose the individual register contents and the GPIO outputs are placed in three-state. To prevent accidental entry into power-down mode, place the ADC in standby mode first. Exiting power-down mode requires a serial interface reset (64 serial clocks with $\overline{CS}$ = 0 and DIN = 1). A delay of 500 µs is recommended before issuing a subsequent serial interface command to allow the LDO regulator to power up.

CALIBRATION MODES

The AD4115 allows the user to perform a two-point calibration to eliminate any offset and gain errors. The following four calibration modes are used to eliminate these offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- Internal full-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the default value of the gain register is 0x5XXXX0. The following equations show the calculations used to scale the ADC conversion result. In unipolar mode, the ideal relationship (not considering the ADC gain error and offset error) is calculated as follows:

$$Data = ((0.075 \times V_{IN}/V_{REF}) \times 2^{23} - (Offset - 0x800000)) \times (Gain/0x400000) \times 2$$

In bipolar mode, the ideal relationship (not considering the ADC gain error and offset error) is calculated as follows:

$$Data = ((0.075 \times V_{IN}/V_{REF}) \times 2^{23} - (Offset - 0x800000)) \times (Gain/0x400000) + 0x800000$$

To start a calibration, write the relevant value to the Mode bits in the ADC mode register Bits[6:4]. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register update, the $\overline{RDY}$ bit in the status register resets, the $\overline{RDY}$ output pin returns low (if $\overline{CS}$ is low), and the AD4115 reverts to standby mode.

During an internal offset calibration both modulator inputs are connected internally to the selected negative analog input pin, and the user must ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference. A full-scale input voltage automatically connects to the ADC input to perform an internal full-scale calibration.

For system calibrations, apply the system zero-scale (offset) and system full-scale (gain) voltages to the input pins before initiating the calibration modes. As a result, errors external to the AD4115 are removed. The calibration range of the ADC gain for a system full-scale calibration on a voltage input is from 3.75 × V_{REF} to 10.5 × V_{REF}. If 10.5 × V_{REF} is greater than the absolute input voltage specification for the applied AVDD, use the specification as the upper limit instead of 10.5 × V_{REF} (see the Specifications section).

An internal zero-scale calibration only removes the offset error of the ADC core. This calibration does not remove error from the resistive front end. A system zero-scale calibration reduces the offset error to the order of the noise on that channel.

From an operational point of view, treat a calibration like another ADC conversion. Always perform an offset calibration, if required, before a full-scale calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the $\overline{RDY}$ output to determine the end of a calibration via a polling sequence or an interrupt driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed.

Any calibration can be performed at any output data rate. Lower output data rates result in higher calibration accuracy and the calibration is accurate for all output data rates. A new offset calibration is required for a given channel if the reference source for that channel is changed.

The AD4115 provides access to the on-chip offset and gain calibration registers to allow the microprocessor to read the device calibration coefficients and to write the stored calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal or self calibration.

DIGITAL INTERFACE

The programmable functions of the AD4115 are accessible via the SPI. The serial interface consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line transfers data into the on-chip registers. The DOUT output accesses data from the on-chip registers. SCLK is the serial clock input for the device. All data transfers (either on DIN or on DOUT) occur with respect to the SCLK signal.

The DOUT/$\overline{RDY}$ pin also functions as a data ready signal where the line goes low if $\overline{CS}$ is low when a new data-word is available in the data register. The pin resets high when a read operation from the data register is complete. The $\overline{RDY}$ output also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is updated. Take care to avoid reading from the data register when the $\overline{RDY}$ signal is about to go low. To ensure that no data read occurs, always monitor the $\overline{RDY}$ output. Start reading the data register as soon as $\overline{RDY}$ goes low and ensure a sufficient SCLK rate such that the read is completed before the next conversion result. $\overline{CS}$ is used to select a device and can be used to decode the AD4115 in systems where several components are connected to the serial bus.

The timing diagrams in Figure 2 and Figure 3 show interfacing to the AD4115 using $\overline{CS}$ to decode the device. Figure 2 shows the timing for a read operation from the AD4115, and Figure 3 shows the timing for a write operation to the AD4115. The user can read from the data register several times even though the $\overline{RDY}$ output returns high after the first read operation. Ensure that the read operations are complete before the next output update occurs. In continuous read mode, the data register can be read only once.

To operate the serial interface in 3-wire mode, tie $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD4115. The end of the conversion can also be monitored using the $\overline{RDY}$ bit in the status register.

To reset the serial interface, write 64 serial clocks with $\overline{CS}$ = 0 and DIN = 1. A reset returns the interface to the state in which the interface expects a write to the communications register. This operation resets the contents of all registers to the power-on values. Following a reset, wait 500 µs before addressing the serial interface.

CHECKSUM PROTECTION

The AD4115 has a checksum mode that can be used to improve interface robustness. Use the checksum to ensure that only valid data is written to a register and to allow the data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. To ensure that the register write is complete, read back the register and verify the checksum.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

During read operations, the user can select between this polynomial and a similar exclusive OR (XOR) function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial checksum and the simple XOR checksum.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 32-bit data output. Figure 21 and Figure 22 show SPI write and read transactions, respectively.

If checksum protection is enabled when continuous read mode is active, an implied read data command of 0x44 occurs before each data transmission, which must be accounted for when calculating the checksum value. The checksum protection ensures a nonzero checksum value even if the ADC data equals 0x000000.

CRC CALCULATION

Polynomial

The checksum, which is eight bits wide, is generated using the following polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that the MSB is adjacent to the leftmost Logic 1 of the data. An XOR function is applied to the data to produce a new, shorter number. The polynomial is aligned again so that the MSB is adjacent to the leftmost Logic 1 of the new result and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This value is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value       011001010100001100100001
                    011001010100001100100001000000000       left shifted eight bits
x⁸ + x² + x + 1 =   100000111                                polynomial
   100100100000110010000100000000                           XOR result
   100000111                                                 polynomial
      100011000110010000100000000                            XOR result
      100000111                                              polynomial
         111111100100001000000000                            XOR result
         100000111                                           polynomial value
            111110111000010000000                            XOR result
            100000111                                        polynomial value
               111100000000100000000                         XOR result
               100000111                                     polynomial value
                  111001110000100000000                      XOR result
                  100000111                                  polynomial value
                     110010010010000000                      XOR result
                     100000111                               polynomial value
                        100101010100000000                   XOR result
                        100000111                            polynomial value
                           101101100000000                   XOR result
                           100000111                         polynomial value
                              1101011000000                  XOR result
                              100000111                      polynomial value
                                 101010110000                XOR result
                                 100000111                   polynomial value
                                    1010001000               XOR result
                                    100000111                polynomial value
                                       10000110              checksum = 0x86.
```

XOR Calculation

The checksum, which is eight bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

Example of an XOR Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

Using the previous polynomial example, divide the checksum into three bytes (0x65, 0x43, and 0x21) which results in the following XOR calculation:

```
01100101    0x65
01000011    0x43
00100110    XOR result
00100001    0x21
00000111    CRC
```

INTEGRATED FUNCTIONS

GENERAL-PURPOSE INPUT/OUTPUT

The AD4115 has two general-purpose digital input/output pins (GPIO0 and GPIO1) and two general-purpose digital output pins (GPO2 and GPO3). The GPIO0 and GPIO1 pins can be configured either as inputs or as outputs, but GPO2 and GPO3 are outputs only. To enable the GPIOx and GPOx pins, use the following bits in the GPIOCON register: IP_EN0 and IP_EN1 (or OP_EN0 and OP_EN1) for GPIO0 and GPIO1, and OP_EN2_3 for GPO2 and GPO3.

When the GPIO0 or GPIO1 pin is enabled as an input, the logic level at the pin is contained in the GP_DATA0 bit or GP_DATA1 bit of the GPIOCON register, respectively. When the GPIO0, GPIO1, GPO2, or GPO3 pin is enabled as an output, the GP_DATA0, GP_DATA1, GP_DATA2, or GP_DATA3 bit, respectively, determines the logic level output at the pin. The logic levels for these pins are referenced to AVDD and AVSS and the outputs have an amplitude of either 5 V or 3.3 V, depending on the AVDD − AVSS voltage.

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output if the ERR_EN bits in the GPIOCON register are set to 11. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the $\overline{\text{ERROR}}$ pin. The logic level for the pin is referenced to IOVDD and DGND, and the $\overline{\text{ERROR}}$ pin has an active pull-up.

EXTERNAL MULTIPLEXER CONTROL

If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled using the AD4115 GPIOx and GPOx pins. When the MUX_IO bit is set in the GPIOCON register, the timing of the GPIOx pins is controlled by the ADC and the channel change is synchronized with the ADC, which eliminates any need for external synchronization.

DELAY

The user can insert a programmable delay before the AD4115 starts to take samples. This delay allows an external amplifier or multiplexer to settle and alleviates the specification requirements for the external amplifier or multiplexer. Eight programmable settings, ranging from 0 µs to 8 ms, can be set using the delay bits in the ADC mode register (Register 0x01, Bits[10:8]).

16-BIT AND 24-BIT CONVERSIONS

By default, the AD4115 generates 24-bit conversions. However, the width of the conversions can be reduced to 16 bits. Set Bit WL16 in the interface mode register to 1 to round all data conversions to 16 bits. Clear this bit to set the width of the data conversions to 24 bits.

DOUT_RESET

The serial interface uses a shared DOUT/$\overline{\text{RDY}}$ pin. By default, this pin outputs the signal. During a data read, this pin outputs the data from the register being read. When the read is complete, the pin reverts to output the $\overline{\text{RDY}}$ signal after a short fixed period of time (t_7). Note that this time may be too short for some microcontrollers and can be extended until the $\overline{\text{CS}}$ pin is brought high. Set the DOUT_RESET bit in the interface mode register to 1 to extend the time and require that $\overline{\text{CS}}$ must frame each read operation and complete the serial interface transaction.

SYNCHRONIZATION

Normal Synchronization

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$ pin functions as a synchronization input pin. The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any setup conditions on the device. This reset allows the user to start gathering samples of the analog input from a known point in time, that is, the $\overline{\text{SYNC}}$ rising edge. This pin must be low for at least one master clock cycle to ensure that synchronization occurs. If multiple channels are enabled, the sequencer is reset to the first enabled channel.

If multiple AD4115 devices are operated from a common master clock, the devices can be synchronized so that the corresponding data registers are updated simultaneously. Synchronization is typically completed after each AD4115 performs a calibration or when calibration coefficients are loaded into the device calibration registers. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD4115 into a consistent known state. While the $\overline{\text{SYNC}}$ pin is low, the AD4115 remains in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state and the device starts to gather input samples again on the next master clock edge.

The device exits reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low to high transition. Therefore, when multiple devices are synchronized, take the $\overline{\text{SYNC}}$ pin high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, a difference can occur of one master clock cycle between the devices. That is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

The $\overline{\text{SYNC}}$ input can also be used as a start conversion command for a single channel when in normal synchronization mode. In this mode, the rising edge of the $\overline{\text{SYNC}}$ input starts a conversion, and the falling edge of the $\overline{\text{RDY}}$ output indicates when the conversion is complete. The settling time of the filter is required for each data register update. When the conversion is complete, bring the $\overline{\text{SYNC}}$ input low in preparation for the next conversion start signal.

Alternate Synchronization Mode

In alternate synchronization mode, the $\overline{\text{SYNC}}$ input operates as a start conversion command when several AD4115 channels are enabled. Set the ALT_SYNC bit in the interface mode register to 1 to enable an alternate synchronization scheme. When the $\overline{\text{SYNC}}$ input is taken low, the ADC completes the conversion on the enabled channel, selects the next channel in the sequence, and then waits until the $\overline{\text{SYNC}}$ input is taken high to start the conversion. The $\overline{\text{RDY}}$ output goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. The $\overline{\text{SYNC}}$ input does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

Alternate synchronization mode can only be used when several channels are enabled. Do not use this mode when a single channel is enabled.

ERROR FLAGS

The status register contains three error bits (ADC_ERROR, CRC_ERROR, and REG_ERROR) that flag errors in the ADC conversion, errors in the CRC check, and errors caused by changes in the registers, respectively. The $\overline{\text{ERROR}}$ output can also indicate that an error has occurred.

ADC_ERROR

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an overrange or underrange result is output from the ADC. The ADC also outputs all 0s or all 1s when an undervoltage or overvoltage occurs, respectively. This flag only resets when the overvoltage or undervoltage is removed. This flag is not reset by a read of the data register.

CRC_ERROR

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag resets as soon as the status register is explicitly read.

REG_ERROR

The REG_ERROR flag is used in conjunction with the REG_CHECK bit in the interface mode register. When the REG_CHECK bit is set, the AD4115 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set to 1. For writes to the on-chip registers, set the REG_CHECK bit to 0. When the registers are updated, the REG_CHECK bit can be set to 1. The AD4115 calculates a checksum of the on-chip registers. If one register value has changed, the REG_ERROR bit is set to 1. If an error is flagged, set the REG_CHECK bit to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or interface mode register.

$\overline{\text{ERROR}}$ Input/Output

The $\overline{\text{ERROR}}$ pin functions as an error input/output pin or as a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

When the ERR_EN bits are set to 10, the $\overline{\text{ERROR}}$ pin functions as an open-drain error output. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ output. Therefore, the $\overline{\text{ERROR}}$ output indicates that an error has occurred. Read the status register to identify the error source.

When the ERR_EN bits are set to 01, the $\overline{\text{ERROR}}$ pin functions as an error input. The error output of another component can be connected to the AD4115 $\overline{\text{ERROR}}$ input so that the AD4115 indicates when an error occurs on either the device or the external component. The value on the $\overline{\text{ERROR}}$ input is inverted and OR'ed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the $\overline{\text{ERROR}}$ input is reflected in the ERR_DAT bit in the GPIO configuration register.

The $\overline{\text{ERROR}}$ input/output is disabled when the ERR_EN bits are set to 00. When the ERR_EN bits are set to 11, the $\overline{\text{ERROR}}$ pin operates as a general-purpose output where the ERR_DAT bit determines the logic level of the pin.

DATA_STAT FUNCTION

The contents of the status register can be appended to each conversion on the AD4115 using the DATA_STAT bit in the IFMODE register. This function is useful if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The four LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are flagged by the error bits.

IOSTRENGTH FUNCTION

The serial interface can operate with a power supply as low as 2 V. However, at this low voltage, the DOUT/$\overline{\text{RDY}}$ pin may not have sufficient drive strength if there is moderate parasitic capacitance on the PCB or if the SCLK frequency is high. The IOSTRENGTH bit in the interface mode register increases the drive strength of the DOUT/$\overline{\text{RDY}}$ pin.

INTERNAL TEMPERATURE SENSOR

The AD4115 has an integrated temperature sensor that can be used as a guide for the ambient temperature at which the device is operating. The ambient temperature can be used for diagnostic purposes or as an indicator of when the application circuit must rerun a calibration routine to consider a shift in operating temperature. Select the temperature sensor using the multiplexer in the same way as an input channel.

The temperature sensor requires the input buffers to be enabled on both inputs and for the internal reference to be enabled.

To use the temperature sensor, calibrate the device in a known temperature (25°C) and take a conversion as a reference point. The temperature sensor has a nominal sensitivity of 477 µV/K. The difference in this ideal slope and the slope measured calibrates the temperature sensor. The temperature sensor is specified with a ±2°C typical accuracy after calibration at 25°C. Calculate the temperature with the following equation:

$$Temperature = (Conversion\ Result/477\ \mu V) - 273.15$$

APPLICATIONS INFORMATION

GROUNDING AND LAYOUT

The inputs and reference inputs are differential and most voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD4115 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog inputs and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD4115 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD4115 is high and the noise levels from the converter are low, take care regarding grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the PCB. A minimum etch technique is optimal for ground planes and results in optimal shielding.

In any layout, the user must keep in mind the flow of currents in the system to ensure that the paths for all return currents are as close as possible to the paths that the currents took to reach the corresponding destinations.

Avoid running digital lines under the device. This layout couples noise onto the die and allows the analog ground plane to run under the AD4115 to prevent noise coupling. The power supply lines to the AD4115 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield the fast switching signals, such as clocks, with digital ground to prevent radiating noise to other sections of the PCB and never run clock signals near the inputs. Avoid digital and analog signal crossover. Run traces on opposite sides of the PCB at right angles to each other. This layout reduces the effects of feedthrough on the PCB. A microstrip technique is optimal but is not always possible with a double sided PCB. In this technique, the component side of the PCB is dedicated to ground planes and signals are placed on the solder side.

Ensure that proper decoupling is used when using high resolution ADCs. The AD4115 has two power supply pins, AVDD and IOVDD. The AVDD pin is referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AVSS on each pin. Place the 0.1 µF capacitor as close as possible to the device on each supply, ideally directly against the device. Decouple IOVDD with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to DGND. Decouple all inputs to AVSS. If an external reference is used, decouple the REF+ and REF− pins to AVSS.

The AD4115 has two on-chip LDO regulators. One regulator regulates the AVDD supply and the other regulates the IOVDD supply. For the REGCAPA pin, use 1 µF and 0.1 µF capacitors to decouple to AVSS. Similarly, for the REGCAPD pin, use a 1 µF capacitor to decouple to DGND.

REGISTER SUMMARY

Table 19. Register Summary

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W
0x00	Status	[7:0]	$\overline{RDY}$	ADC_ERROR	CRC_ERROR	REG_ERROR	Channel				0x80	R
0x01	ADCMODE	[15:8]	REF_EN	Reserved	SING_CYC	Reserved		Delay			0x2000	R/W
		[7:0]	Reserved	Mode			CLOCKSEL		Reserved			
0x02	IFMODE	[15:8]	Reserved			ALT_SYNC	IOSTRENGTH	Reserved		DOUT_RESET	0x0000	R/W
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	Reserved	CRC_EN		Reserved	WL16		
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	Data	[23:0]	Data[23:16]								0x000000	R
		[15:8]	Data[15:8]									
		[7:0]	Data[7:0]									
0x06	GPIOCON	[15:8]	Reserved		OP_EN2_3	MUX_IO	SYNC_EN	ERR_EN		ERR_DAT	0x0800	R/W
		[7:0]	GP_DATA3	GP_DATA2	IP_EN1	IP_EN0	OP_EN1	OP_EN0	GP_DATA1	GP_DATA0		
0x07	ID	[15:8]	ID[15:8]								0x38DX	R
		[7:0]	ID[7:0]									
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			Reserved		INPUT0[9:8]		0x8001	R/W
		[7:0]	INPUT0[7:0]									
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			Reserved		INPUT1[9:8]		0x0001	R/W
		[7:0]	INPUT1[7:0]									
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			Reserved		INPUT2[9:8]		0x0001	R/W
		[7:0]	INPUT2[7:0]									
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			Reserved		INPUT3[9:8]		0x0001	R/W
		[7:0]	INPUT3[7:0]									
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			Reserved		INPUT4[9:8]		0x0001	R/W
		[7:0]	INPUT4[7:0]									
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			Reserved		INPUT5[9:8]		0x0001	R/W
		[7:0]	INPUT5[7:0]									
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			Reserved		INPUT6[9:8]		0x0001	R/W
		[7:0]	INPUT6[7:0]									
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			Reserved		INPUT7[9:8]		0x0001	R/W
		[7:0]	INPUT7[7:0]									
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			Reserved		INPUT8[9:8]		0x0001	R/W
		[7:0]	INPUT8[7:0]									
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			Reserved		INPUT9[9:8]		0x0001	R/W
		[7:0]	INPUT9[7:0]									
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			Reserved		INPUT10[9:8]		0x0001	R/W
		[7:0]	Input10[7:0]									
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			Reserved		INPUT11[9:8]		0x0001	R/W
		[7:0]	INPUT11[7:0]									
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			Reserved		INPUT12[9:8]		0x0001	R/W
		[7:0]	INPUT12[7:0]									
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			Reserved		INPUT13[9:8]		0x0001	R/W
		[7:0]	INPUT13[7:0]									
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			Reserved		INPUT14[9:8]		0x0001	R/W
		[7:0]	INPUT14[7:0]									
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			Reserved		INPUT15[9:8]		0x0001	R/W
		[7:0]	INPUT15[7:0]									
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	INBUF0		0x1000	R/W
		[7:0]	Reserved		REF_SEL0		Reserved					
0x21	SETUPCON1	[15:8]	Reserved			BI_UNIPOLAR1	REFBUF1+	REFBUF1−	INBUF1		0x1000	R/W
		[7:0]	Reserved		REF_SEL1		Reserved					

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x22	SETUPCON2	[15:8]	Reserved			BI_UNIPOLAR2	REFBUF2+	REFBUF2−	INBUF2		0x1000	R/W
		[7:0]	Reserved		REF_SEL2		Reserved					
0x23	SETUPCON3	[15:8]	Reserved			BI_UNIPOLAR3	REFBUF3+	REFBUF3−	INBUF3		0x1000	R/W
		[7:0]	Reserved		REF_SEL3		Reserved					
0x24	SETUPCON4	[15:8]	Reserved			BI_UNIPOLAR4	REFBUF4+	REFBUF4−	INBUF4		0x1000	R/W
		[7:0]	Reserved		REF_SEL4		Reserved					
0x25	SETUPCON5	[15:8]	Reserved			BI_UNIPOLAR5	REFBUF5+	REFBUF5−	INBUF5		0x1000	R/W
		[7:0]	Reserved		REF_SEL5		Reserved					
0x26	SETUPCON6	[15:8]	Reserved			BI_UNIPOLAR6	REFBUF6+	REFBUF6−	INBUF6		0x1000	R/W
		[7:0]	Reserved		REF_SEL6		Reserved					
0x27	SETUPCON7	[15:8]	Reserved			BI_UNIPOLAR7	REFBUF7+	REFBUF7−	INBUF7		0x1000	R/W
		[7:0]	Reserved		REF_SEL7		Reserved					
0x28	FILTCON0	[15:8]	SINC3_MAP0	Reserved			ENHFILTEN0	ENHFILT0			0x0500	R/W
		[7:0]	Reserved	ORDER0		ODR0						
0x29	FILTCON1	[15:8]	SINC3_MAP1	Reserved			ENHFILTEN1	ENHFILT1			0x0500	R/W
		[7:0]	Reserved	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	Reserved			ENHFILTEN2	ENHFILT2			0x0500	R/W
		[7:0]	Reserved	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	Reserved			ENHFILTEN3	ENHFILT3			0x0500	R/W
		[7:0]	Reserved	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	Reserved			ENHFILTEN4	ENHFILT4			0x0500	R/W
		[7:0]	Reserved	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	Reserved			ENHFILTEN5	ENHFILT5			0x0500	R/W
		[7:0]	Reserved	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	Reserved			ENHFILTEN6	ENHFILT6			0x0500	R/W
		[7:0]	Reserved	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	Reserved			ENHFILTEN7	ENHFILT7			0x0500	R/W
		[7:0]	Reserved	ORDER7		ODR7						
0x30	OFFSET0	[23:0]	OFFSET0[23:0]								0x800000	R/W
0x31	OFFSET1	[23:0]	OFFSET1[23:0]								0x800000	R/W
0x32	OFFSET2	[23:0]	OFFSET2[23:0]								0x800000	R/W
0x33	OFFSET3	[23:0]	OFFSET3[23:0]								0x800000	R/W
0x34	OFFSET4	[23:0]	OFFSET4[23:0]								0x800000	R/W
0x35	OFFSET5	[23:0]	OFFSET5[23:0]								0x800000	R/W
0x36	OFFSET6	[23:0]	OFFSET6[23:0]								0x800000	R/W
0x37	OFFSET7	[23:0]	OFFSET7[23:0]								0x800000	R/W
0x38	GAIN0	[23:0]	GAIN0[23:0]								0x5XXXX0	R/W
0x39	GAIN1	[23:0]	GAIN1[23:0]								0x5XXXX0	R/W
0x3A	GAIN2	[23:0]	GAIN2[23:0]								0x5XXXX0	R/W
0x3B	GAIN3	[23:0]	GAIN3[23:0]								0x5XXXX0	R/W
0x3C	GAIN4	[23:0]	GAIN4[23:0]								0x5XXXX0	R/W
0x3D	GAIN5	[23:0]	GAIN5[23:0]								0x5XXXX0	R/W
0x3E	GAIN6	[23:0]	GAIN6[23:0]								0x5XXXX0	R/W
0x3F	GAIN7	[23:0]	GAIN7[23:0]								0x5XXXX0	R/W

REGISTER DETAILS

COMMUNICATIONS REGISTER

Address: 0x00, Reset: 0x00, Name: COMMS

All access to the on-chip registers must start with a write to the communications register. This write determines which register is accessed next and whether that operation is a write or a read.

Table 20. Bit Descriptions for COMMS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{WEN}$		This bit must be low to begin communications with the ADC.	0x0	W
6	R/$\overline{W}$		This bit determines if the command is a read or write operation.	0x0	W
		0	Write command.		
		1	Read command.		
[5:0]	RA		The register address bits determine the register to be read from or written to as part of the current communication.	0x00	W
		000000	Status register.		
		000001	ADC mode register.		
		000010	Interface mode register.		
		000011	Register checksum register.		
		000100	Data register.		
		000110	GPIO configuration register.		
		000111	ID register.		
		010000	Channel Register 0.		
		010001	Channel Register 1.		
		010010	Channel Register 2.		
		010011	Channel Register 3.		
		010100	Channel Register 4.		
		010101	Channel Register 5.		
		010110	Channel Register 6.		
		010111	Channel Register 7.		
		011000	Channel Register 8.		
		011001	Channel Register 9.		
		011010	Channel Register 10.		
		011011	Channel Register 11.		
		011100	Channel Register 12.		
		011101	Channel Register 13.		
		011110	Channel Register 14.		
		011111	Channel Register 15.		
		100000	Setup Configuration Register 0.		
		100001	Setup Configuration Register 1.		
		100010	Setup Configuration Register 2.		
		100011	Setup Configuration Register 3.		
		100100	Setup Configuration Register 4.		
		100101	Setup Configuration Register 5.		
		100110	Setup Configuration Register 6.		
		100111	Setup Configuration Register 7.		
		101000	Filter Configuration Register 0.		
		101001	Filter Configuration Register 1.		
		101010	Filter Configuration Register 2.		
		101011	Filter Configuration Register 3.		
		101100	Filter Configuration Register 4.		
		101101	Filter Configuration Register 5.		
		101110	Filter Configuration Register 6.		
		101111	Filter Configuration Register 7.		

Bits	Bit Name	Settings	Description	Reset	Access
		110000	Offset Register 0.		
		110001	Offset Register 1.		
		110010	Offset Register 2.		
		110011	Offset Register 3.		
		110100	Offset Register 4.		
		110101	Offset Register 5.		
		110110	Offset Register 6.		
		110111	Offset Register 7.		
		111000	Gain Register 0.		
		111001	Gain Register 1.		
		111010	Gain Register 2.		
		111011	Gain Register 3.		
		111100	Gain Register 4.		
		111101	Gain Register 5.		
		111110	Gain Register 6.		
		111111	Gain Register 7.		

STATUS REGISTER

Address: 0x00, Reset: 0x80, Name: Status

The status register is an 8-bit register that contains ADC and serial interface status information. The register can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register.

Table 21. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{RDY}$		The status of $\overline{RDY}$ is output to the DOUT/$\overline{RDY}$ pin when $\overline{CS}$ is low and a register is not being read. This bit goes low when the ADC writes a new result to the data register. In ADC calibration modes, this bit goes low when the ADC writes the calibration result. $\overline{RDY}$ is brought high automatically by a read of the data register.	0x1	R
		0	New data result available.		
		1	Awaiting new data result.		
6	ADC_ERROR		By default, this bit indicates if an ADC overrange or underrange occurred. The ADC result is clamped to 0xFFFFFF for overrange errors and 0x000000 for underrange errors. This bit is updated when the ADC result is written and is cleared at the next update after removing the overrange or underrange condition.	0x0	R
		0	No error.		
		1	Error.		
5	CRC_ERROR		This bit indicates if a CRC error occurred during a register write. For register reads, the host microcontroller determines if a CRC error occurred. This bit is cleared by a read of this register.	0x0	R
		0	No error.		
		1	CRC error.		
4	REG_ERROR		This bit indicates if the content of one of the internal registers changes from the value calculated when the register integrity check is activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
		0	No error.		
		1	Error.		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	Channel		These bits indicate which channel was active for the ADC conversion whose result is currently in the data register. This channel may be different from the channel currently being converted. The mapping is a direct map from the channel register. Therefore, Channel 0 results in 0x0 and Channel 15 results in 0xF.	0x0	R
		0000	Channel 0.		
		0001	Channel 1.		
		0010	Channel 2.		
		0011	Channel 3.		
		0100	Channel 4.		
		0101	Channel 5.		
		0110	Channel 6.		
		0111	Channel 7.		
		1000	Channel 8.		
		1001	Channel 9.		
		1010	Channel 10.		
		1011	Channel 11.		
		1100	Channel 12.		
		1101	Channel 13.		
		1110	Channel 14.		
		1111	Channel 15.		

ADC MODE REGISTER

Address: 0x01, Reset: 0x2000, Name: ADCMODE

The ADC mode register controls the operating mode of the ADC and the master clock selection. A write to the ADC mode register resets the filter and the $\overline{\text{RDY}}$ bits and starts a new conversion or calibration.

Table 22. Bit Descriptions for ADCMODE

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
14	Reserved		This bit is reserved. Set this bit to 0.	0x0	R/W
13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to only output at the settled filter data rate.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[12:11]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
[10:8]	Delay		These bits allow a programmable delay to be added after a channel switch to allow the settling of external circuitry before the ADC starts processing its input.	0x0	R/W
		000	0 µs.		
		001	8 µs.		
		010	32 µs.		
		011	80 µs.		
		100	200 µs.		
		101	400 µs.		
		110	1 ms.		
		111	2 ms.		
7	Reserved		This bit is reserved. Set this bit to 0.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	Mode		These bits control the operating mode of the ADC. See the Operating Modes section for more information.	0x0	R/W
		000	Continuous conversion mode.		
		001	Single conversion mode.		
		010	Standby mode.		
		011	Power-down mode.		
		100	Internal offset calibration.		
		101	Internal gain calibration		
		110	System offset calibration.		
		111	System gain calibration.		
[3:2]	CLOCKSEL		These bits select the ADC clock source. Selecting the internal oscillator also enables the internal oscillator.	0x0	R/W
		00	Internal oscillator.		
		01	Internal oscillator output on the XTAL2/CLKIO pin.		
		10	External clock input on the XTAL2/CLKIO pin.		
		11	External crystal on the XTAL1 pin and the XTAL2/CLKIO pin.		
[1:0]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R

INTERFACE MODE REGISTER

Address: 0x02, Reset: 0x0000, Name: IFMODE

The interface mode register configures various serial interface options.

Table 23. Bit Descriptions for IFMODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
12	ALT_SYNC		This bit enables a different behavior of the $\overline{\text{SYNC}}$ pin to allow the use of $\overline{\text{SYNC}}$ as a control for conversions when cycling channels.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
11	IOSTRENGTH		This bit controls the drive strength of the DOUT/$\overline{\text{RDY}}$ pin. Set this bit when reading from the serial interface at high speed with a low IOVDD supply and moderate capacitance.	0x0	R/W
		0	Disabled (default).		
		1	Enabled.		
[10:9]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
8	DOUT_RESET		See the DOUT_RESET section.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
7	CONTREAD		This bit enables the continuous read mode of the ADC data register. The ADC must be configured in continuous conversion mode to use continuous read mode. For more details, see the Operating Modes section.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
6	DATA_STAT		This bit enables the status register to be appended to the data register when read so that channel and status information are transmitted with the data. Appending the status register is the only way to be sure that the channel bits read from the status register correspond to the data in the data register.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
5	REG_CHECK		This bit enables a register integrity checker that can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired with this bit cleared. Then, write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status register is included in the registers that are checked. If a register must have a new value written, this bit must first be cleared. Otherwise, an error is flagged when the new register contents are written.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
4	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
[3:2]	CRC_EN		These bits enable CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one.	0x00	R/W
		00	Disabled.		
		01	XOR checksum enabled for register read transactions. Register writes still use CRC with these bits set.		
		10	CRC checksum enabled for read and write transactions.		
1	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
0	WL16		This bit changes the ADC data register to 16 bits. The ADC is not reset by a write to the interface mode register. Therefore, the ADC result is not rounded to the correct word length immediately after writing to these bits. The first new ADC result is correct.	0x0	R/W
		0	24-bit data.		
		1	16-bit data.		

REGISTER CHECK

Address: 0x03, Reset: 0x000000, Name: REGCHECK

The register check register is a 24-bit checksum calculated by exclusively OR'ing the contents of the user registers. The REG_CHECK bit in the interface mode register must be set for this checksum to operate. Otherwise, the register reads 0.

Table 24. Bit Descriptions for REGCHECK

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register.	0x000000	R

DATA REGISTER

Address: 0x04, Reset: 0x000000, Name: Data

The data register contains the ADC conversion result. The encoding is offset binary, or it can be changed to unipolar by the BI_UNIPOLARx bits in the setup configuration registers. Reading the data register brings the $\overline{\text{RDY}}$ bit and the $\overline{\text{RDY}}$ output high if it is low. The ADC result can be read multiple times. However, because the $\overline{\text{RDY}}$ output is brought high, it is not possible to determine if another ADC result is imminent. After the command to read the ADC register is received, the ADC does not write a new result into the data register.

Table 25. Bit Descriptions for Data

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	Data		This register contains the ADC conversion result. If DATA_STAT is set in the interface mode register, the status register is appended to this register when read, making this a 32-bit register.	0x000000	R

GPIO CONFIGURATION REGISTER

Address: 0x06, Reset: 0x0800, Name: GPIOCON

The GPIO configuration register controls the general-purpose I/O pins of the ADC.

Table 26. Bit Descriptions for GPIOCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	Reserved		Reserved.	0x0	R
13	OP_EN2_3		GPO2/GPO3 output enable. This bit enables the GPO2 and GPO3 pins. The outputs are referenced between AVDD and AVSS.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
12	MUX_IO		This bit allows the ADC to control an external multiplexer, using GPIO0, GPIO1, GPO2, and GPO3 in sync with the internal channel sequencing. The analog input pins used for a channel can still be selected on a per channel basis. Therefore, it is possible to have a 16-channel multiplexer in front of each analog input pair (VIN0/VIN1 to VIN14/VIN15), giving a total of 128 differential channels. However, only 16 channels at a time can be automatically sequenced. Following the sequence of 16 channels, the user changes the analog input to the next pair of input channels, and it sequences through the next 16 channels. There is a delay function that allows extra time for the analog input to settle, in conjunction with any switching of an external multiplexer (see the delay bits in the ADC mode register).	0x0	R
11	SYNC_EN		$\overline{\text{SYNC}}$ input enable. This bit enables the $\overline{\text{SYNC}}$ pin as a sync input. When set low, the $\overline{\text{SYNC}}$ pin holds the ADC and filter in reset until $\overline{\text{SYNC}}$ goes high. An alternative operation of the $\overline{\text{SYNC}}$ pin is available when the ALT_SYNC bit in the interface mode register is set. This mode works only when multiple channels are enabled. In such cases, a low on the $\overline{\text{SYNC}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$ to be used while cycling through channels.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[10:9]	ERR_EN		$\overline{\text{ERROR}}$ pin mode. These bits enable the $\overline{\text{ERROR}}$ pin as an error input/output.	0x0	R/W
		00	Disabled.		
		01	Enable error input (active low). $\overline{\text{ERROR}}$ is an error input. The inverted readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The $\overline{\text{ERROR}}$ pin state can also be read from the ERR_DAT bit in this register.		
		10	Enable open-drain error output (active low). $\overline{\text{ERROR}}$ is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
		11	General-purpose output (active low). $\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This output is referenced between IOVDD and DGND, as opposed to the AVDD and AVSS levels used by the GPIOx and GPOx pins. The output has an active pull-up resistor in this case.		
8	ERR_DAT		$\overline{\text{ERROR}}$ pin data. This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. This bit reflects the readback status of the pin if the pin is enabled as an input.	0x0	R/W
		0	Logic 0.		
		1	Logic 1.		
7	GP_DATA3		GPIO1 data. This bit is the write data for GPIO1.	0x0	R/W
		0	GPIO1 = 0.		
		1	GPIO1 = 1.		
6	GP_DATA2		GPIO0 data. This bit is the write data for GPIO0.	0x0	R/W
		0	GPIO0 = 0.		
		1	GPIO0 = 1.		

Bits	Bit Name	Settings	Description	Reset	Access
5	IP_EN1		This bit runs GPIO1 into an input. Input is equal to AVDD and AVSS.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
4	IP_EN0		This bit runs GPIO0 into an input. Input is equal to AVDD and AVSS.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
3	OP_EN1		This bit runs GPIO1 into an output. Outputs are referenced between AVDD and AVSS.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
2	OP_EN0		This bit runs GPIO0 into an output. Outputs are referenced between AVDD and AVSS.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
1	GP_DATA1		This bit is the readback or write data for GPIO1.	0x0	R/W
0	GP_DATA0		This bit is the readback or write data for GPIO0.	0x0	R/W

ID REGISTER

Address: 0x07, Reset: 0x38DX, Name: ID

The ID register returns a 16-bit ID. For the AD4115, this value is 0x38DX, where x is don't care.

Table 27. Bit Descriptions for ID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		Product ID. The ID register returns a 16-bit ID code that is specific to the ADC.	0x38DX	R

CHANNEL REGISTER 0 TO CHANNEL REGISTER 15

Address: 0x10 to 0x1F, Reset: 0x8001, Name: CH0 to CH15

The channel registers are 16-bit registers that select the currently active channels, the selected inputs for each channel, and the setup to be used to configure the ADC for that channel. The layout for CH0 to CH15 is identical.

Table 28. Bit Descriptions for CH0 to CH15

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_ENx		This bit enables Channel x. If more than one channel is enabled, the ADC automatically sequences between them.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[14:12]	SETUP_SELx		These bits identify which of the eight setups is used to configure the ADC for this channel. A setup comprises a set of four registers: a setup configuration register, a filter configuration register, an offset register, and a gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels, or up to eight channels can be configured differently.	0x0	R/W
		000	Setup 0.		
		001	Setup 1.		
		010	Setup 2.		
		011	Setup 3.		
		100	Setup 4.		
		101	Setup 5.		
		110	Setup 6.		
		111	Setup 7.		
[11:10]	Reserved		Reserved.	0x0	R
[9:0]	INPUTx		These bits select which input pair is connected to the input of the ADC for this channel.	0x1	R/W
		0000000001	VIN0, VIN1.		
		0000010000	VIN0, VINCOM.		

Bits	Bit Name	Settings	Description	Reset	Access
		0000100000	VIN1, VIN0.		
		0000110000	VIN1, VINCOM.		
		0001000011	VIN2, VIN3.		
		0001010000	VIN2, VINCOM.		
		0001100010	VIN3, VIN2.		
		0001110000	VIN3, VINCOM.		
		0010000101	VIN4, VIN5.		
		0010010000	VIN4, VINCOM.		
		0010100100	VIN5, VIN4.		
		0010110000	VIN5, VINCOM.		
		0011000111	VIN6, VIN7.		
		0011010000	VIN6, VINCOM.		
		0011100110	VIN7, VIN6.		
		0011110000	VIN7, VINCOM.		
		0100001001	VIN8, VIN9.		
		0100010000	VIN8, VINCOM.		
		0100101000	VIN9, VIN8.		
		0100110000	VIN9, VINCOM.		
		0101001011	VIN10, VIN11.		
		0101010000	VIN10, VINCOM.		
		0101101010	VIN11, VIN10.		
		0101110000	VIN11, VINCOM.		
		0110001101	VIN12, VIN13.		
		0110010000	VIN12, VINCOM.		
		0110101100	VIN13, VIN12.		
		0110110000	VIN13, VINCOM.		
		0111001111	VIN14, VIN15.		
		0111010000	VIN14, VINCOM.		
		0111101110	VIN15, VIN14.		
		0111110000	VIN15, VINCOM.		
		1000110010	Temperature sensor.		
		1010110110	Reference.		

SETUP CONFIGURATION REGISTER 0 TO SETUP CONFIGURATION REGISTER 7

Address: 0x20 to 0x27, Reset: 0x1000 Name: SETUPCON0 to SETUPCON7

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, and output coding of the ADC. The layout for SETUPCON0 to SETUPCON7 is identical.

Table 29. Bit Descriptions for SETUPCON0 to SETUPCON7

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
12	BI_UNIPOLARx		Bipolar/unipolar. This bit sets the output coding of the ADC for Setup x.	0x1	R/W
		0	Unipolar coded output.		
		1	Bipolar coded output.		
11	REFBUFx+		REF+ buffer. This bit enables or disables the REF+ input buffer.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
10	REFBUFx−		REF− buffer. This bit enables or disables the REF− input buffer.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
[9:8]	INBUFx		Input buffer. This bit enables or disables input buffers.	0x0	R/W
		00	Disabled.		
		01	Reserved.		
		10	Reserved.		
		11	Enabled.		
[7:6]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
[5:4]	REF_SELx		These bits allow the user to select the reference source for ADC conversion on Setup 0.	0x0	R/W
		00	External reference, REF±.		
		10	Internal 2.5 V reference, must be enabled via ADCMODE (see Table 22).		
		11	AVDD − AVSS.		
[3:0]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R

FILTER CONFIGURATION REGISTER 0 TO FILTER CONFIGURATION REGISTER 7

Address: 0x28 to 0x2F, Reset: 0x0500, Name: FILTCON0 to FILTCON7

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence. The layout for FILTCON0 to FILTCON7 is identical.

Table 30. Bit Descriptions for FILTCON0 to FILTCON7

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAPx		If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter for Setup x. All other options are eliminated. This bit allows fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals $f_{MOD}/(32 \times FILTCON0[14:0])$.	0x0	R/W
[14:12]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
11	ENHFILTENx		This bit enables various postfilters for enhanced 50 Hz/60 Hz rejection for Setup x. The ORDERx bits must be set to 00 to select the sinc5 + sinc1 filter for this function to work.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
[10:8]	ENHFILTx		These bits select between various postfilters for enhanced 50 Hz/60 Hz rejection for Setup x.	0x5	R/W
		010	27 SPS, 47 dB rejection, 36.7 ms settling.		
		011	25 SPS, 62 dB rejection, 40 ms settling.		
		101	20 SPS, 86 dB rejection, 50 ms settling.		
		110	16.67 SPS, 92 dB rejection, 60 ms settling.		
7	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
[6:5]	ORDERx		These bits control the order of the digital filter that processes the modulator data for Setup x.	0x0	R/W
		00	Sinc5 + sinc1 (default).		
		11	Sinc3.		
[4:0]	ODRx		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup x. Rates shown are for a single-channel enabled sinc5 + sinc 1 filter. See Table 16 for multiple channels enabled.	0x0	R/W
		00000	125,000 SPS.		
		00001	125,000 SPS.		
		00010	62,500 SPS.		
		00011	62,500 SPS.		
		00100	31,250 SPS.		
		00101	25,000 SPS.		
		00110	15,625 SPS.		
		00111	10390 (10416.7 SPS for sinc3).		

Bits	Bit Name	Settings	Description	Reset	Access
		01000	4994 (5000 SPS for sinc3).		
		01001	2498 (2500 SPS for sinc3).		
		01010	1000.00 SPS.		
		01011	500.00 SPS.		
		01100	395.5 (400.6 SPS for sinc3).		
		01101	200.00 SPS.		
		01110	100.00 SPS.		
		01111	59.87 SPS.		
		10000	49.92 SPS (50 SPS for sinc3).		
		10001	20 SPS.		
		10010	16.67 SPS.		
		10011	10 SPS.		
		10100	5 SPS.		
		10101	2.5 SPS.		
		10110	2.5 SPS.		

OFFSET REGISTER 0 TO OFFSET REGISTER 7

Address: 0x30 to 0x37, Reset: 0x800000, Name: OFFSET0 to OFFSET7

The offset (zero-scale) registers are 16-bit registers that can be used to compensate for any offset error in the ADC or in the system. The layout for OFFSET0 to OFFSET7 is identical.

Table 31. Bit Descriptions for OFFSET0 to OFFSET7

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSETx		Offset calibration coefficient for Setup x.	0x800000	R/W

GAIN REGISTER 0 TO GAIN REGISTER 7

Address: 0x38 to0x3F, Reset: 0x5XXXX0, Name: GAIN0 to GAIN7

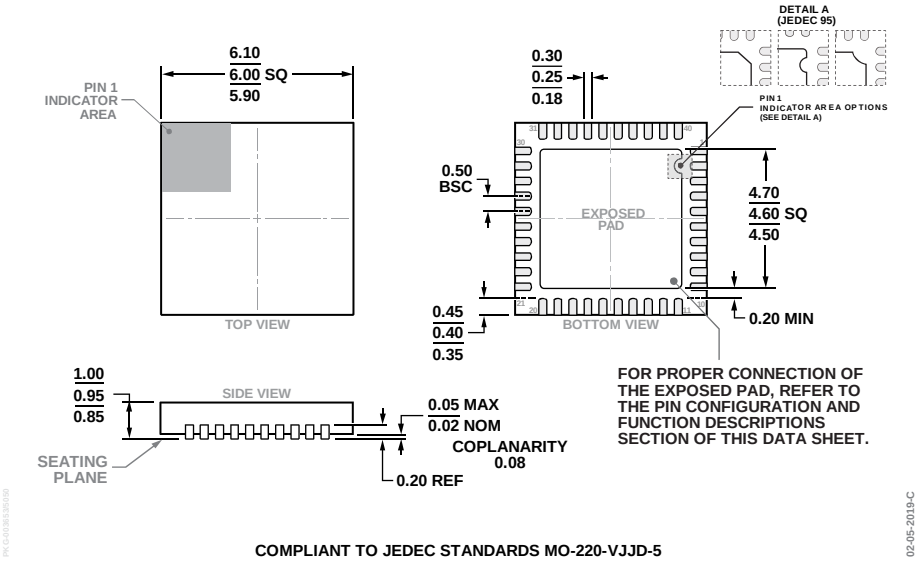
The full-scale gain registers are 16-bit registers that can be used to compensate for any gain error in the ADC or in the system. The layout for GAIN0 to GAIN7 is identical.

Table 32. Bit Descriptions for GAIN0 to GAIN7

Bits	Bit Name	Settings	Description	Reset[1]	Access
[23:0]	GAINx		Gain calibration coefficient for Setup x.	0x5XXXX0	R/W

[1] X means don't care.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD4115BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
AD4115BCPZ-RL7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
EVAL-AD4115SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation Controller Board	

[1] Z = RoHS Compliant Part.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AD4115BCPZ on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management