



**THE DATASHEET OF  
LTC2640CTS8-LZ12#TRMPBF**



## Single 12-/10-/8-Bit SPI $V_{OUT}$ DACs with 10ppm/°C Reference

### FEATURES

- **Integrated Precision Reference**  
 2.5V Full-Scale 10ppm/°C (LTC2640-L)  
 4.096V Full-Scale 10ppm/°C (LTC2640-H)
- **Maximum INL Error: 1LSB (LTC2640A-12)**
- **Bidirectional Reference: Input or 10ppm/°C Output**
- **Low Noise (0.7mVpp, 0.1Hz to 200kHz)**
- **Guaranteed Monotonic Over Temperature**
- **2.7V to 5.5V Supply Range (LTC2640-L)**
- **Low Power Operation: 180µA at 3V**
- **Power Down to 1.8µA Maximum (C and I Grades)**
- **Asynchronous DAC Clear Pin (LTC2640-Z)**
- **Power-On Reset to Zero or Mid-Scale options**
- **Double-Buffered Data Latches**
- **Guaranteed Operation from -40°C to 125°C (H-Grade)**
- **8-Lead TSOT-23 (ThinSOT™) Package**

### APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Automatic Test Equipment
- Portable Equipment
- Automotive
- Optical Networking

### DESCRIPTION

The LTC®2640 is a family of 12-, 10-, and 8-bit voltage-output DACs with an integrated, high-accuracy, low-drift reference in an 8-lead TSOT-23 package. It has a rail-to-rail output buffer that is guaranteed monotonic.

The LTC2640-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2640-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. A 10ppm/°C reference output is available at the REF pin.

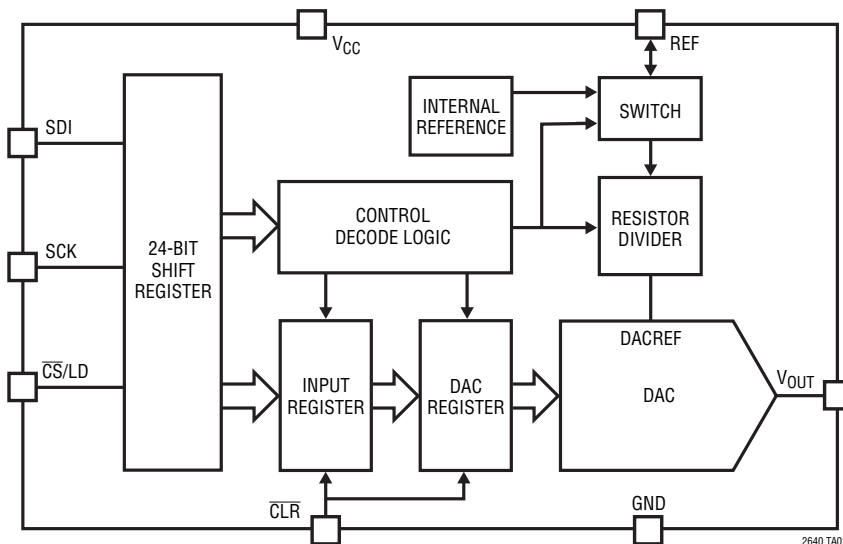
Each DAC can also operate in External Reference mode, in which a voltage supplied to the REF pin sets the full-scale output.

The LTC2640 DACs use a SPI/MICROWIRE™ compatible 3-wire serial interface which operates at clock rates up to 50MHz.

The LTC2640 incorporates a power-on reset circuit. Options are available for Reset to Zero-Scale or Reset to Mid-Scale after power-up.

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### BLOCK DIAGRAM (LTC2640-Z)



**Integral Nonlinearity (LTC2640A-LZ12)**



2640 TA01b

2640fd

# LTC2640

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{CC}$ ) ..... -0.3V to 6V  
CLR,  $\overline{CS/LD}$ , REF\_SEL, SCK, SDI ..... -0.3V to 6V  
 $V_{OUT}$ , REF ..... -0.3V to Min( $V_{CC} + 0.3V$ , 6V)  
Operating Temperature Range  
LTC2640C ..... 0°C to 70°C  
LTC2640I ..... -40°C to 85°C  
LTC2640H ..... -40°C to 125°C

Maximum Junction Temperature ..... 150°C  
Storage Temperature Range ..... -65°C to 150°C  
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LTC2640#orderinfo>

LTC2640	A	C	TS8	-L	M	12	#TRM	PBF	
									<b>LEAD FREE DESIGNATOR</b>
									<b>TAPE AND REEL</b> TR = 2,500-Piece Tape and Reel TRM = 500-Piece Tape and Reel
									<b>RESOLUTION</b> 12 = 12-Bit 10 = 10-Bit 8 = 8-Bit
									<b>POWER-ON RESET</b> M = Reset to Mid-Scale Z = Reset to Zero-Scale
									<b>FULL-SCALE VOLTAGE, INTERNAL REFERENCE MODE</b> L = 2.5V H = 4.096V
									<b>PACKAGE TYPE</b> TS8 = 8-Lead Plastic TSOT-23
									<b>TEMPERATURE GRADE</b> C = Commercial Temperature Range (0°C to 70°C) I = Industrial Temperature Range (-40°C to 85°C) H = Automotive Temperature Range (-40°C to 125°C)
									<b>ELECTRICAL GRADE (OPTIONAL)</b> A = ±1LSB Maximum INL (12-Bit)
									<b>PRODUCT PART NUMBER</b>

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING*	V <sub>FS</sub> WITH INTERNAL REFERENCE	POWER-ON RESET TO CODE	PIN 8	RESOLUTION	V <sub>CC</sub>	MAXIMUM INL
LTC2640A-LM12	LTDHV	2.5V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	2.7V – 5.5V	±1LSB
LTC2640A-LZ12	LTDHW	2.5V • (4095/4096)	Zero	$\overline{\text{CLR}}$	12-Bit	2.7V – 5.5V	±1LSB
LTC2640A-HM12	LTDHX	4.096V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	4.5V – 5.5V	±1LSB
LTC2640A-HZ12	LTDHY	4.096V • (4095/4096)	Zero	$\overline{\text{CLR}}$	12-Bit	4.5V – 5.5V	±1LSB
LTC2640-LM12	LTDHV	2.5V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	2.7V – 5.5V	±2.5LSB
LTC2640-LM10	LTDHZ	2.5V • (1023/1024)	Mid-Scale	REF_SEL	10-Bit	2.7V – 5.5V	±1LSB
LTC2640-LM8	LTDJF	2.5V • (255/256)	Mid-Scale	REF_SEL	8-Bit	2.7V – 5.5V	±0.5LSB
LTC2640-LZ12	LTDHW	2.5V • (4095/4096)	Zero	$\overline{\text{CLR}}$	12-Bit	2.7V – 5.5V	±2.5LSB
LTC2640-LZ10	LTDJB	2.5V • (1023/1024)	Zero	$\overline{\text{CLR}}$	10-Bit	2.7V – 5.5V	±1LSB
LTC2640-LZ8	LTDJG	2.5V • (255/256)	Zero	$\overline{\text{CLR}}$	8-Bit	2.7V – 5.5V	±0.5LSB
LTC2640-HM12	LTDHX	4.096V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	4.5V – 5.5V	±2.5LSB
LTC2640-HM10	LTDJC	4.096V • (1023/1024)	Mid-Scale	REF_SEL	10-Bit	4.5V – 5.5V	±1LSB
LTC2640-HM8	LTDJH	4.096V • (255/256)	Mid-Scale	REF_SEL	8-Bit	4.5V – 5.5V	±0.5LSB
LTC2640-HZ12	LTDHY	4.096V • (4095/4096)	Zero	$\overline{\text{CLR}}$	12-Bit	4.5V – 5.5V	±2.5LSB
LTC2640-HZ10	LTDJD	4.096V • (1023/1024)	Zero	$\overline{\text{CLR}}$	10-Bit	4.5V – 5.5V	±1LSB
LTC2640-HZ8	LTDJJ	4.096V • (255/256)	Zero	$\overline{\text{CLR}}$	8-Bit	4.5V – 5.5V	±0.5LSB

\*The temperature grade is identified by a label on the shipping container.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{OUT}$  unloaded unless otherwise specified.

LTC2640-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2640A-LM12/-LZ12 ( $V_{FS} = 2.5\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	LTC2640-8			LTC2640-10			LTC2640-12			LTC2640A-12			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DC Performance</b>															
	Resolution		●	8		10		12		12				Bits	
	Monotonicity	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 3)	●	8		10		12		12				Bits	
DNL	Differential Nonlinearity	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 3)	●		$\pm 0.5$		$\pm 0.5$		$\pm 1$		$\pm 1$			LSB	
INL	Integral Nonlinearity	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 3)	●	$\pm 0.05$	$\pm 0.5$	$\pm 0.2$	$\pm 1$	$\pm 1$	$\pm 2.5$	$\pm 0.5$	$\pm 1$			LSB	
ZSE	Zero-Scale Error	$V_{CC} = 3\text{V}$ , Internal Ref., Code = 0	●	0.5	5	0.5	5	0.5	5	0.5	5			mV	
$V_{OS}$	Offset Error	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 4)	●	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$			mV	
$V_{OSTC}$	$V_{OS}$ Temperature Coefficient	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 4)		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$				$\mu\text{V}/^\circ\text{C}$	
FSE	Full-Scale Error	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 10)	●	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$			%FSR	
$V_{FSTC}$	Full-Scale Voltage Temperature Coefficient	$V_{CC} = 3\text{V}$ , Internal Ref. (Note 9)		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$				ppm/ $^\circ\text{C}$	
		C-Grade		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$				ppm/ $^\circ\text{C}$	
		I-Grade		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$				ppm/ $^\circ\text{C}$	
		H-Grade		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$				ppm/ $^\circ\text{C}$	
	Load Regulation	Internal Ref., Mid-Scale, $V_{CC} = 3\text{V} \pm 10\%$ , $-5\text{mA} \leq I_{OUT} \leq 5\text{mA}$ , $V_{CC} = 5\text{V} \pm 10\%$ , $-10\text{mA} \leq I_{OUT} \leq 10\text{mA}$	●	0.009	0.016	0.035	0.064	0.14	0.256	0.14	0.256			LSB/mA	
			●	0.009	0.016	0.035	0.064	0.14	0.256	0.14	0.256			LSB/mA	
$R_{OUT}$	DC Output Impedance	Internal Ref., Mid-Scale, $V_{CC} = 3\text{V} \pm 10\%$ , $-5\text{mA} \leq I_{OUT} \leq 5\text{mA}$ , $V_{CC} = 5\text{V} \pm 10\%$ , $-10\text{mA} \leq I_{OUT} \leq 10\text{mA}$	●	0.09	0.156	0.09	0.156	0.09	0.156	0.09	0.156			$\Omega$	
			●	0.09	0.156	0.09	0.156	0.09	0.156	0.09	0.156			$\Omega$	

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OUT}$	DAC Output Span	External Reference Internal Reference		0 to $V_{REF}$ 0 to 2.5		V V
PSR	Power Supply Rejection	$V_{CC} = 3\text{V} \pm 10\%$ or $5\text{V} \pm 10\%$		-80		dB
$I_{SC}$	Short-Circuit Output Current (Note 5) Sinking Sourcing	$V_{FS} = V_{CC} = 5.5\text{V}$ Zero-Scale; $V_{OUT}$ shorted to $V_{CC}$ Full-Scale; $V_{OUT}$ shorted to GND	●	27 -28	48 -48	mA mA

**Power Supply**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Positive Supply Voltage	For Specified Performance	●	2.7	5.5	V
$I_{CC}$	Supply Current (Note 6)	$V_{CC} = 3\text{V}$ , $V_{REF} = 2.5\text{V}$ , External Reference	●	150	200	$\mu\text{A}$
		$V_{CC} = 3\text{V}$ , Internal Reference	●	180	240	$\mu\text{A}$
		$V_{CC} = 5\text{V}$ , $V_{REF} = 2.5\text{V}$ , External Reference	●	160	210	$\mu\text{A}$
		$V_{CC} = 5\text{V}$ , Internal Reference	●	190	260	$\mu\text{A}$
$I_{SD}$	Supply Current in Power-Down Mode (Note 6)	$V_{CC} = 5\text{V}$ , C-Grade, I-Grade	●	0.6	1.8	$\mu\text{A}$
		$V_{CC} = 5\text{V}$ , H-Grade	●	0.6	4	$\mu\text{A}$

# LTC2640

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LTC2640-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2640A-LM12/-LZ12 ( $V_{FS} = 2.5\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Reference Input</b>							
	Input Voltage Range		●	0	$V_{CC}$	V	
	Resistance		●	160	190	220	$k\Omega$
	Capacitance			7.5		pF	
$I_{REF}$	Reference Current, Power-Down Mode	DAC Powered Down	●	0.005	0.1	$\mu\text{A}$	
<b>Reference Output</b>							
	Output Voltage		●	1.240	1.250	1.260	V
	Reference Temperature Coefficient			$\pm 10$		ppm/ $^\circ\text{C}$	
	Output Impedance			0.5		$k\Omega$	
	Capacitive Load Driving			10		$\mu\text{F}$	
	Short-Circuit Current	$V_{CC} = 5.5\text{V}$ ; REF Shorted to GND		2.5		mA	
<b>Digital I/O</b>							
$V_{IH}$	Digital Input High Voltage	$V_{CC} = 3.6\text{V}$ to $5.5\text{V}$ $V_{CC} = 2.7\text{V}$ to $3.6\text{V}$	● ●	2.4 2		V V	
$V_{IL}$	Digital Input Low Voltage	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ $V_{CC} = 2.7\text{V}$ to $4.5\text{V}$	● ●		0.8 0.6	V V	
$I_{LK}$	Digital Input Leakage	$V_{IN} = \text{GND}$ to $V_{CC}$	●		$\pm 1$	$\mu\text{A}$	
$C_{IN}$	Digital Input Capacitance	(Note 7)	●		2.5	pF	
<b>AC Performance</b>							
$t_S$	Settling Time	$V_{CC} = 3\text{V}$ (Note 8) $\pm 0.39\%$ ( $\pm 1\text{LSB}$ at 8-Bits) $\pm 0.098\%$ ( $\pm 1\text{LSB}$ at 10-Bits) $\pm 0.024\%$ ( $\pm 1\text{LSB}$ at 12-Bits)			3.2 3.8 4.1	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$	
	Voltage Output Slew Rate			1		V/ $\mu\text{s}$	
	Capacitance Load Driving			500		pF	
	Glitch Impulse	At Mid-Scale Transition		2.1		nV•s	
	Multiplying Bandwidth	External Reference		300		kHz	
$e_n$	Output Voltage Noise Density	At $f = 1\text{kHz}$ , External Reference At $f = 10\text{kHz}$ , External Reference At $f = 1\text{kHz}$ , Internal Reference At $f = 10\text{kHz}$ , Internal Reference		140 130 160 150		nV $\sqrt{\text{Hz}}$ nV $\sqrt{\text{Hz}}$ nV $\sqrt{\text{Hz}}$ nV $\sqrt{\text{Hz}}$	
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference, $C_{REF} = 0.33\mu\text{F}$		20 20 650 670		$\mu\text{V}_{P-P}$ $\mu\text{V}_{P-P}$ $\mu\text{V}_{P-P}$ $\mu\text{V}_{P-P}$	

**TIMING CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ . (See Figure 1) (Note 7).

LTC2640-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2640A-LM12/-LZ12 ( $V_{FS} = 2.5\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_1$	SDI Valid to SCK Setup	●	4			ns
$t_2$	SDI Valid to SCK Hold	●	4			ns
$t_3$	SCK High Time	●	9			ns
$t_4$	SCK Low Time	●	9			ns
$t_5$	$\overline{\text{CS}}/\text{LD}$ Pulse Width	●	10			ns
$t_6$	LSB SCK High to $\overline{\text{CS}}/\text{LD}$ High	●	7			ns
$t_7$	$\overline{\text{CS}}/\text{LD}$ Low to SCK High	●	7			ns
$t_9$	CLR Pulse Width	●	20			ns
$t_{10}$	$\overline{\text{CS}}/\text{LD}$ High to SCK Pos. Edge	●	7			ns
	SCK Frequency	50% Duty Cycle	●		50	MHz

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $V_{OUT}$  unloaded unless otherwise specified.

LTC2640-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2640A-HM12/-HZ12 ( $V_{FS} = 4.096\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	LTC2640-8			LTC2640-10			LTC2640-12			LTC2640A-12			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DC Performance</b>															
	Resolution	●	8			10			12			12			Bits
	Monotonicity	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 3)	●	8			10			12			12		Bits
DNL	Differential Nonlinearity	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 3)	●		$\pm 0.5$		$\pm 0.5$		$\pm 1$		$\pm 1$		$\pm 1$		LSB
INL	Integral Nonlinearity	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 3)	●	$\pm 0.05$	$\pm 0.5$	$\pm 0.2$	$\pm 1$	$\pm 1$	$\pm 2.5$	$\pm 0.5$	$\pm 1$	$\pm 0.5$	$\pm 1$		LSB
ZSE	Zero-Scale Error	$V_{CC} = 5\text{V}$ , Internal Ref., Code = 0	●	0.5	5	0.5	5	0.5	5	0.5	5	0.5	5		mV
$V_{OS}$	Offset Error	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 4)	●	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$	$\pm 0.5$	$\pm 5$		mV
$V_{OSTC}$	$V_{OS}$ Temperature Coefficient	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 4)		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$			$\mu\text{V}/^\circ\text{C}$
FSE	Full-Scale Error	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 10)	●	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$	$\pm 0.08$	$\pm 0.4$		%FSR
$V_{FSTC}$	Full-Scale Voltage Temperature Coefficient	$V_{CC} = 5\text{V}$ , Internal Ref. (Note 9) C-Grade I-Grade H-Grade		$\pm 10$ $\pm 10$ $\pm 10$		$\pm 10$ $\pm 10$ $\pm 10$		$\pm 10$ $\pm 10$ $\pm 10$		$\pm 10$ $\pm 10$ $\pm 10$		$\pm 10$ $\pm 10$ $\pm 10$			ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$
	Load Regulation	$V_{CC} = 5\text{V} \pm 10\%$ , Internal Ref. Mid-Scale, $-10\text{mA} \leq I_{OUT} \leq 10\text{mA}$	●	0.006	0.01	0.022	0.04	0.09	0.16	0.09	0.16	0.09	0.16		LSB/mA
$R_{OUT}$	DC Output Impedance	$V_{CC} = 5\text{V} \pm 10\%$ , Internal Ref. Mid-Scale, $-10\text{mA} \leq I_{OUT} \leq 10\text{mA}$	●	0.09	0.156	0.09	0.156	0.09	0.156	0.09	0.156	0.09	0.156		$\Omega$

# LTC2640

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LTC2640-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2640A-HM12/-HZ12 ( $V_{FS} = 4.096\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{OUT}$	DAC Output Span	External Reference		0 to $V_{REF}$		V	
		Internal Reference		0 to 4.096		V	
PSR	Power Supply Rejection	$V_{CC} = 5\text{V} \pm 10\%$		-80		dB	
$I_{SC}$	Short-Circuit Output Current (Note 5) Sinking Sourcing	$V_{FS} = V_{CC} = 5.5\text{V}$ Zero-Scale; $V_{OUT}$ shorted to $V_{CC}$	●	27	48	mA	
		Full-Scale; $V_{OUT}$ shorted to GND	●	-28	-48	mA	
<b>Power Supply</b>							
$V_{CC}$	Positive Supply Voltage	For Specified Performance	●	4.5	5.5	V	
$I_{CC}$	Supply Current (Note 6)	$V_{CC} = 5\text{V}$ , $V_{REF} = 4.096\text{V}$ , External Reference	●	160	220	$\mu\text{A}$	
		$V_{CC} = 5\text{V}$ , Internal Reference	●	200	270	$\mu\text{A}$	
$I_{SD}$	Supply Current in Power-Down Mode (Note 6)	$V_{CC} = 5\text{V}$ , C-Grade, I-Grade	●	0.6	1.8	$\mu\text{A}$	
		$V_{CC} = 5\text{V}$ , H-Grade	●	0.6	4	$\mu\text{A}$	
<b>Reference Input</b>							
	Input Voltage Range		●	0	$V_{CC}$	V	
	Resistance		●	160	190	$\text{k}\Omega$	
	Capacitance			7.5		pF	
$I_{REF}$	Reference Current, Power-Down Mode	DAC Powered Down	●	0.005	0.1	$\mu\text{A}$	
<b>Reference Output</b>							
	Output Voltage		●	2.032	2.048	2.064	V
	Reference Temperature Coefficient				$\pm 10$	ppm/ $^\circ\text{C}$	
	Output Impedance			0.5		$\text{k}\Omega$	
	Capacitive Load Driving			10		$\mu\text{F}$	
	Short-Circuit Current	$V_{CC} = 5.5\text{V}$ ; REF Shorted to GND		4.3		mA	
<b>Digital I/O</b>							
$V_{IH}$	Digital Input High Voltage		●	2.4		V	
$V_{IL}$	Digital Input Low Voltage		●		0.8	V	
$I_{LK}$	Digital Input Leakage	$V_{IN} = \text{GND}$ to $V_{CC}$	●		$\pm 1$	$\mu\text{A}$	
$C_{IN}$	Digital Input Capacitance	(Note 7)	●		2.5	pF	
<b>AC Performance</b>							
$t_S$	Settling Time	$V_{CC} = 5\text{V}$ (Note 8) $\pm 0.39\%$ ( $\pm 1\text{LSB}$ at 8 Bits)		3.7		$\mu\text{s}$	
		$\pm 0.098\%$ ( $\pm 1\text{LSB}$ at 10 Bits)		4.2		$\mu\text{s}$	
		$\pm 0.024\%$ ( $\pm 1\text{LSB}$ at 12 Bits)		4.6		$\mu\text{s}$	
		Voltage Output Slew Rate		1		V/ $\mu\text{s}$	
	Capacitance Load Driving			500		pF	
	Glitch Impulse	At Mid-Scale Transition		3.0		nV•s	
	Multiplying Bandwidth	External Reference		300		kHz	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $V_{OUT}$  unloaded unless otherwise specified.

LTC2640-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2640A-HM12/-HZ12 ( $V_{FS} = 4.096\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$e_n$	Output Voltage Noise Density	At $f = 1\text{kHz}$ , External Reference		140		$\text{nV}\sqrt{\text{Hz}}$
		At $f = 10\text{kHz}$ , External Reference		130		$\text{nV}\sqrt{\text{Hz}}$
		At $f = 1\text{kHz}$ , Internal Reference		210		$\text{nV}\sqrt{\text{Hz}}$
		At $f = 10\text{kHz}$ , Internal Reference		200		$\text{nV}\sqrt{\text{Hz}}$
	Output Voltage Noise	0.1Hz to 10Hz, External Reference		20		$\mu\text{V}_{\text{P-P}}$
		0.1Hz to 10Hz, Internal Reference		20		$\mu\text{V}_{\text{P-P}}$
		0.1Hz to 200kHz, External Reference		650		$\mu\text{V}_{\text{P-P}}$
		0.1Hz to 200kHz, Internal Reference,		670		$\mu\text{V}_{\text{P-P}}$
		$C_{\text{REF}} = 0.33\mu\text{F}$				

**TIMING CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ . (See Figure 1) (Note 7).

LTC2640-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2640A-HM12/-HZ12 ( $V_{FS} = 4.096\text{V}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_1$	SDI Valid to SCK Setup		●	4		ns
$t_2$	SDI Valid to SCK Hold		●	4		ns
$t_3$	SCK High Time		●	9		ns
$t_4$	SCK Low Time		●	9		ns
$t_5$	$\overline{\text{CS}}/\text{LD}$ Pulse Width		●	10		ns
$t_6$	LSB SCK High to $\overline{\text{CS}}/\text{LD}$ High		●	7		ns
$t_7$	$\overline{\text{CS}}/\text{LD}$ Low to SCK High		●	7		ns
$t_9$	CLR Pulse Width		●	20		ns
$t_{10}$	$\overline{\text{CS}}/\text{LD}$ High to SCK Pos. Edge		●	7		ns
	SCK Frequency	50% Duty Cycle	●		50	MHz

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltages are with respect to GND.

**Note 3:** Linearity and monotonicity are defined from code  $k_L$  to code  $2^N - 1$ , where  $N$  is the resolution and  $k_L$  is given by  $k_L = 0.016 \cdot (2^N / V_{FS})$ , rounded to the nearest whole code. For  $V_{FS} = 2.5\text{V}$  and  $N = 12$ ,  $k_L = 26$  and linearity is defined from code 26 to code 4,095. For  $V_{FS} = 4.096\text{V}$  and  $N = 12$ ,  $k_L = 16$  and linearity is defined from code 16 to code 4,095.

**Note 4:** Inferred from measurement at code 16 (LTC2640-12), code 4 (LTC2640-10) or code 1 (LTC2640-8), and at full-scale.

**Note 5:** This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 6:** Digital inputs at 0V or  $V_{CC}$ .

**Note 7:** Guaranteed by design and not production tested.

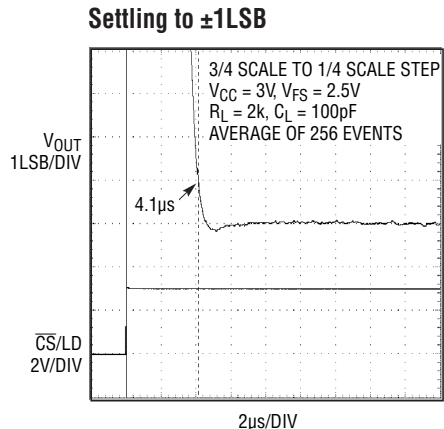
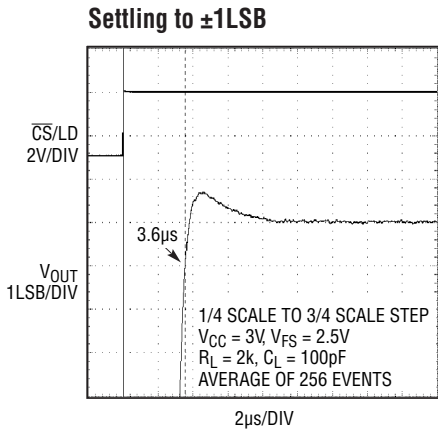
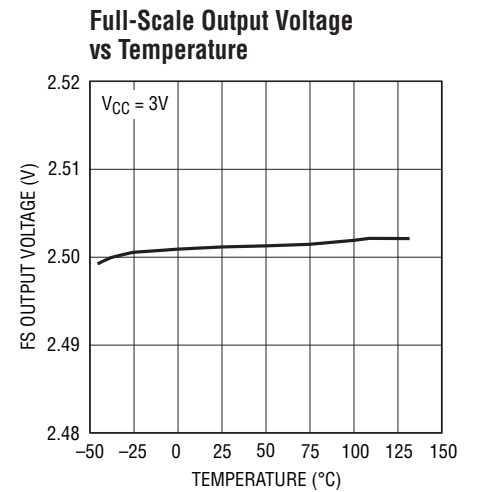
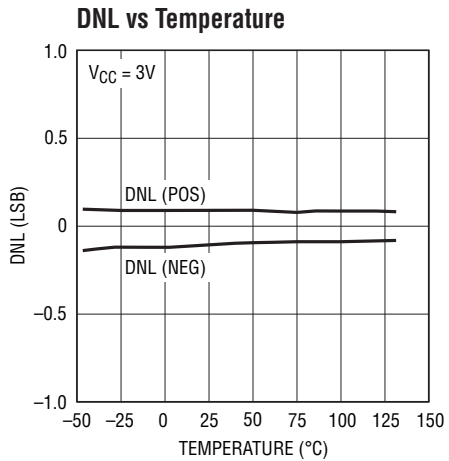
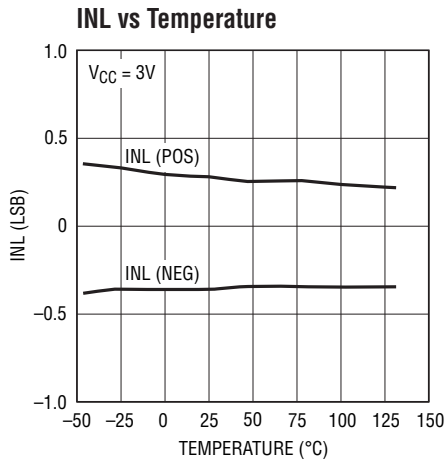
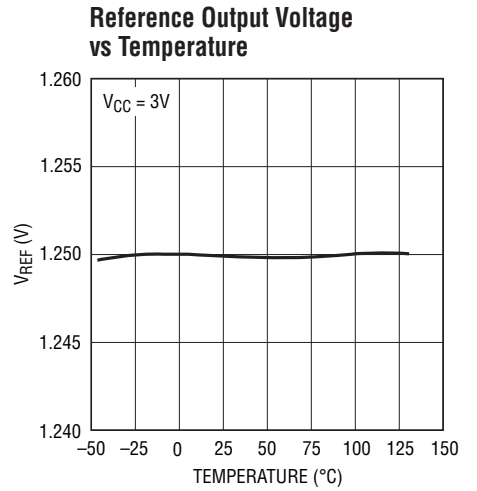
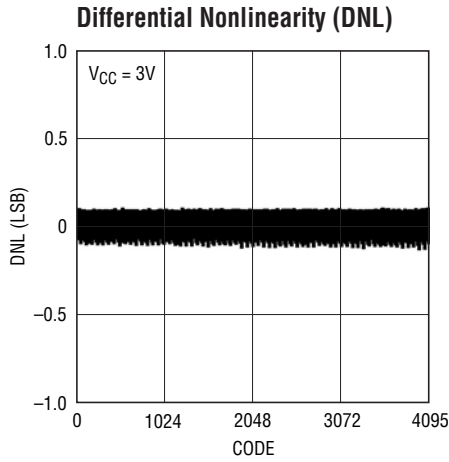
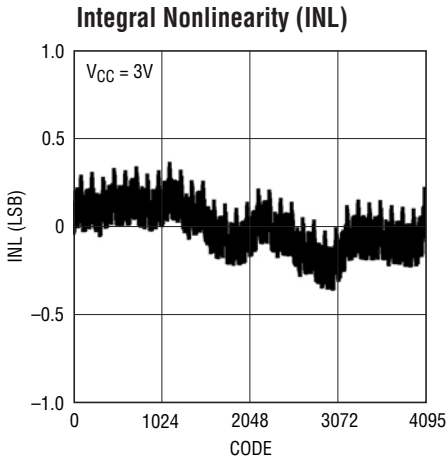
**Note 8:** Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2k in parallel with 100pF to GND.

**Note 9:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

**Note 10:** Full-scale error is determined using the reference voltage measured at the REF pin.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

LTC2640-L12 (Internal Reference,  $V_{FS} = 2.5\text{V}$ )



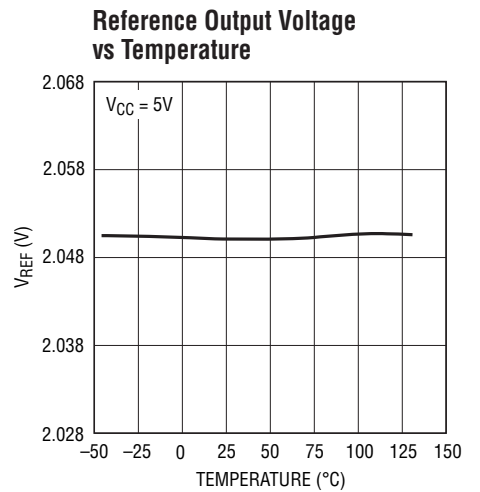
**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.  
 LTC2640-H12 (Internal Reference,  $V_{FS} = 4.096\text{V}$ )



2640 G09



2640 G10



2640 G11



2640 G12

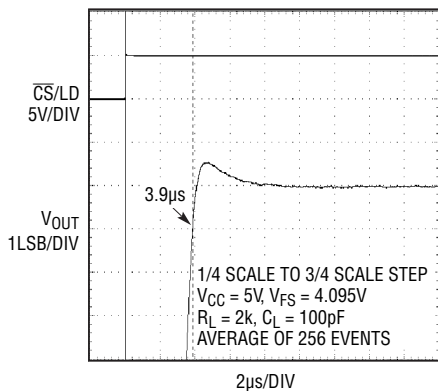


2640 G13



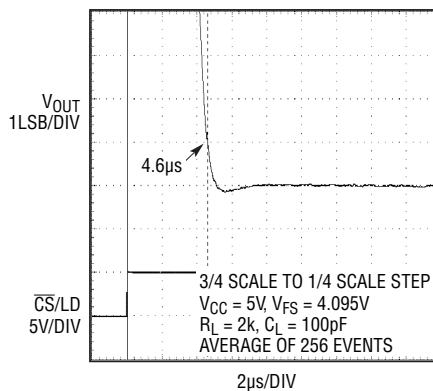
2640 G14

**Settling to  $\pm 1\text{LSB}$**



2640 G15

**Settling to  $\pm 1\text{LSB}$**



2640 G16

# LTC2640

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

LTC2640-10



2640 G17



2640 G18

### LTC2640-8

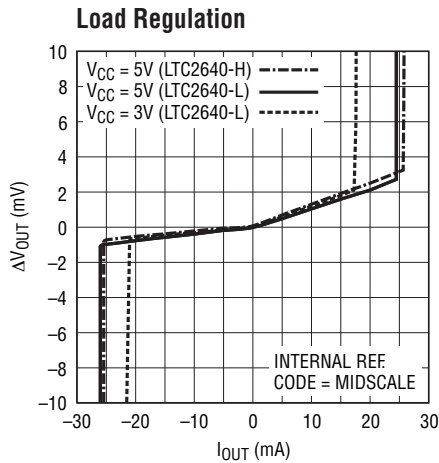


2640 G19



2640 G20

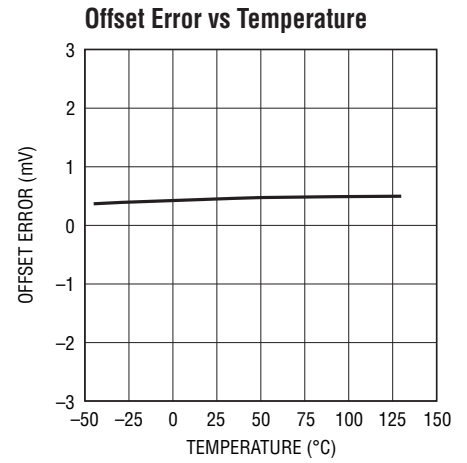
### LTC2640



2630 G21



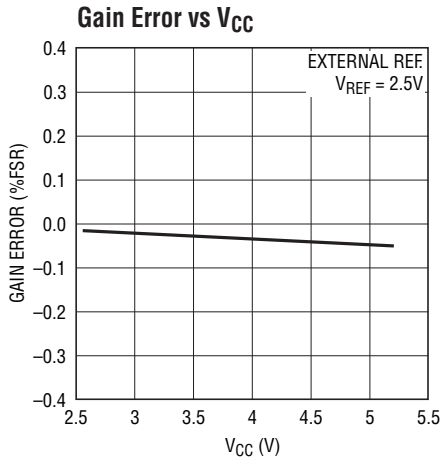
2630 G22



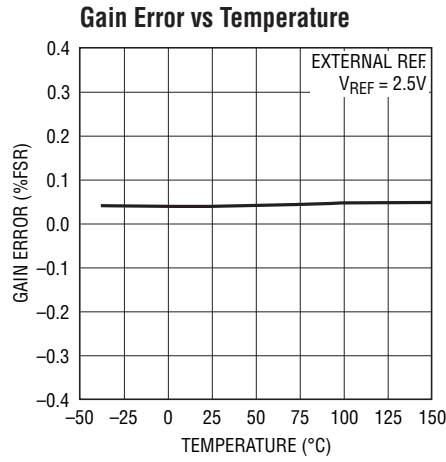
2640 G23

2640fd

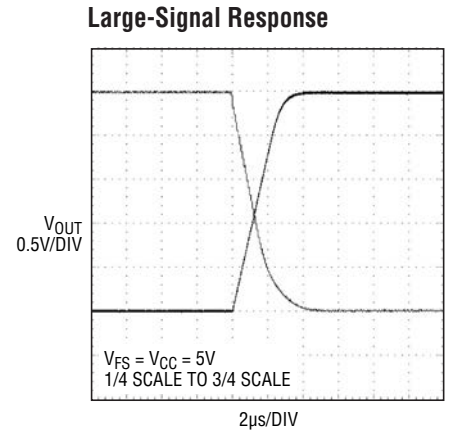
**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.  
LTC2640



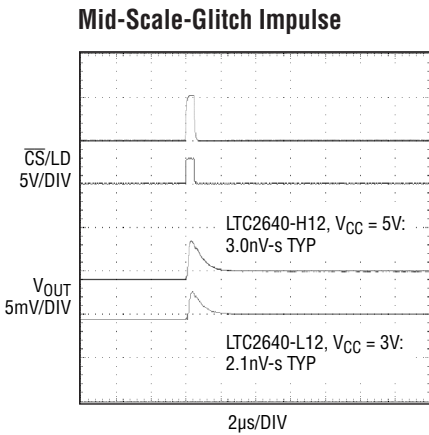
2640 G24



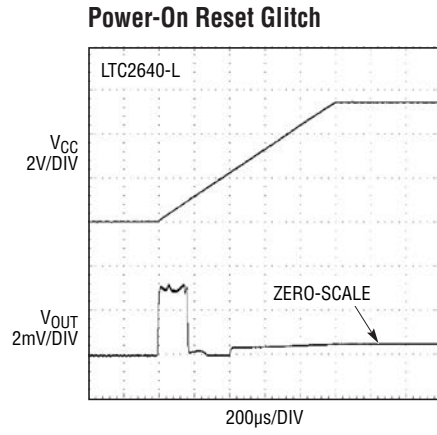
2640 G25



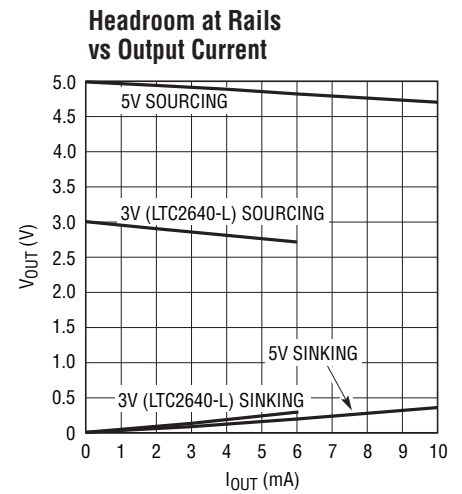
2640 G26



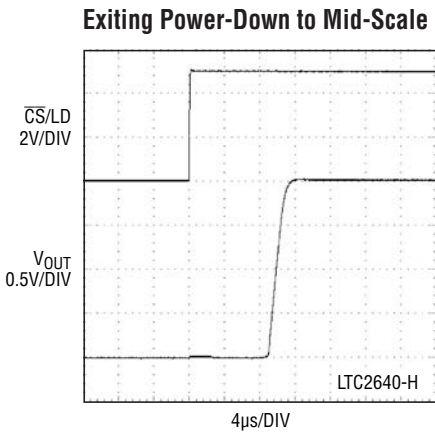
2640 G27



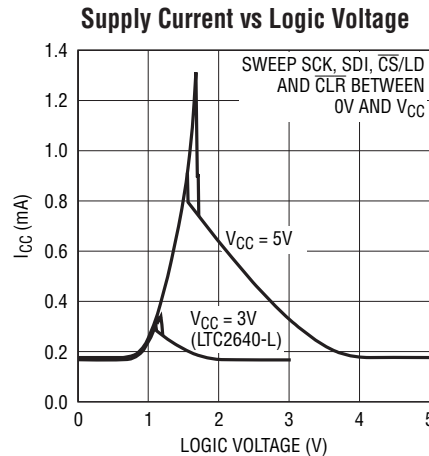
2640 G28



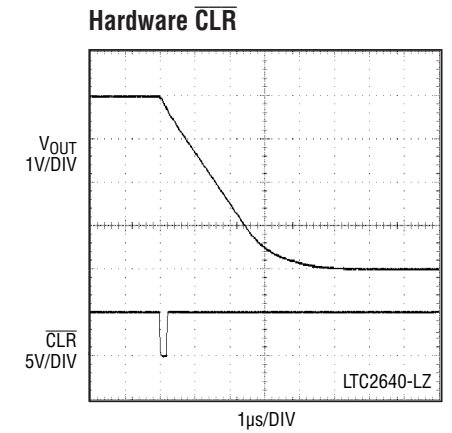
2640 G29



2640 G30



2640 G31



2640 G32

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

LTC2640



## PIN FUNCTIONS

**$\overline{CS/LD}$  (Pin 1):** Serial Interface Chip Select/Load Input. When  $\overline{CS/LD}$  is low, SCK is enabled for shifting data on SDI into the register. When  $\overline{CS/LD}$  is taken high, SCK is disabled and the specified command (see Table 1) is executed.

**SCK (Pin 2):** Serial Interface Clock Input. CMOS and TTL compatible.

**SDI (Pin 3):** Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2640 accepts input word lengths of either 24- or 32-bits.

**GND (Pin 4):** Ground.

**$V_{CC}$  (Pin 5):** Supply Voltage Input.  $2.7V \leq V_{CC} \leq 5.5V$  (LTC2640-L) or  $4.5V \leq V_{CC} \leq 5.5V$  (LTC2640-H). Bypass to GND with a  $0.1\mu F$  capacitor.

**REF (Pin 6):** Reference Voltage Input or Output. When External Reference mode is selected, REF is an input ( $0V \leq V_{REF} \leq V_{CC}$ ) where the voltage supplied sets the

full-scale voltage. When Internal Reference is selected, the  $10\text{ppm}/^\circ\text{C}$   $1.25V$  (LTC2640-L) or  $2.048V$  (LTC2640-H) internal reference is available at the pin. This output may be bypassed to GND with up to  $10\mu F$  ( $0.33\mu F$  is recommended), and must be buffered when driving external DC load current.

**$V_{OUT}$  (Pin 7):** DAC Analog Voltage Output.

**$\overline{CLR}$  (Pin 8, LTC2640-Z):** Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage output to reset to Zero. CMOS and TTL compatible.

**REF\_SEL (Pin 8, LTC2640-M):** Selects default Reference at power-up. Tie to  $V_{CC}$  to select the Internal Reference, or GND to select an External Reference. After power-up, the logic state at this pin is ignored and the reference may be changed only by software command.

**BLOCK DIAGRAMS**

**LTC2640-Z**



**LTC2640-M**



2640 BD

# TIMING DIAGRAM



Figure 1. Serial Interface Timing

2640 F01

## OPERATION

The LTC2640 is a family of single voltage-output DACs in 8-lead ThinSOT packages. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. 12 combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero or mid-scale), and full-scale voltage (2.5V or 4.096V) are available. The LTC2640 is controlled using a 3-wire SPI/MICROWIRE compatible interface.

### Power-On Reset

The LTC2640-HZ/LTC2640-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2640 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 5mV above zero-scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See “Power-On Reset Glitch” in the Typical Performance Characteristics section.

The LTC2640-HM/LTC2640-LM provide an alternative reset, setting the output to mid-scale when power is first applied.

Default reference mode selection is described in the Reference Modes section.

### Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range  $-0.3V \leq V_{REF} \leq V_{CC} + 0.3V$  (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at  $V_{CC}$  (Pin 5) is in transition.

### Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left( \frac{k}{2^N} \right) V_{REF}$$

where  $k$  is the decimal equivalent of the binary DAC input code,  $N$  is the resolution, and  $V_{REF}$  is either 2.5V (LTC2640-LM/LTC2640-LZ) or 4.096V (LTC2640-HM/LTC2640-HZ) when in Internal Reference mode, and the voltage at REF (Pin 6) when in External Reference mode.



Figure 2. Command and Data Input Format

## OPERATION

### Serial Interface

The  $\overline{CS}/LD$  input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first, followed by 4 don't-cares bits, and finally the 16-bit data word. The data word comprises the 12-, 10- or 8-bit input code, ordered MSB-to-LSB, followed by 4, 6 or 8 don't-cares bits (LTC2640-12, LTC2640-10 and LTC2640-8 respectively; see Figure 2). Data can only be transferred to the device when the  $\overline{CS}/LD$  signal is low, beginning on the first rising edge of SCK. SCK may be high or low at the falling edge of  $\overline{CS}/LD$ . The rising edge of  $\overline{CS}/LD$  ends the data transfer and causes the device to execute the command specified in the 24-bit input sequence. The complete sequence is shown in Figure 3a.

The command (C3-C0) assignments are shown in Table 1. The first three commands in the table consist of write and update operations. A Write operation loads a 16-bit data word from the 24-bit shift register into the input register. In an Update operation, the input register is copied to the DAC register and converted to an analog voltage at the DAC output. Write to and Update combines the first two commands. The Update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

**Table 1. Command Codes**

COMMAND*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power-Up) DAC Register
0	0	1	1	Write to and Update (Power-Up) DAC Register
0	1	0	0	Power Down
0	1	1	0	Select Internal Reference
0	1	1	1	Select External Reference

\*Command codes not shown are reserved and should not be used

While the minimum input sequence is 24-bits, it may optionally be extended to 32-bits to accommodate micro-processors that have a minimum word width of 16-bits (2-bytes). To use the 32-bit width, 8 don't-cares bits are

transferred to the device first, followed by the 24-bit sequence described. Figure 3b shows the 32-bit sequence.

The 16-bit data word is ignored for all commands that do not include a Write operation.

### Reference Modes

For applications where an accurate external reference is not available, the LTC2640 has a user-selectable, integrated reference. The LTC2640-LM/LTC2640-LZ provide a full-scale output of 2.5V. The LTC2640-HM/LTC2640-HZ provide a full-scale output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal Reference mode can be selected by using command 0110, and is the power-on default for LTC2640-HZ/LTC2640-LZ, as well as for LTC2640-HM/LTC2640-LM when REF\_SEL is tied high.

The 10ppm/°C, 1.25V (LTC2640-LM/LTC2640-LZ) or 2.048V (LTC2640-HM/LTC2640-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; 0.33μF is recommended, and up to 10μF can be driven without oscillation. This output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in External Reference mode using command 0111. In this mode, an input voltage supplied externally to the REF pin provides the reference ( $0V \leq V_{REF} \leq V_{CC}$ ) and the supply current is reduced. External Reference mode is the power-on default for LTC2640-HM/LTC2640-LM when REF\_SEL is tied low.

The reference mode of LTC2640-HZ/LTC2640-LZ can be changed only by software command. The same is true for LTC2640-HM/LTC2640-LM after power-on, after which the logic state on REF\_SEL is ignored.

### Power-Down Mode

For power-constrained applications, the LTC2640's power-down mode can be used to reduce the supply current whenever the DAC output is not needed. When in power-down, the buffer amplifier, bias circuit, and reference circuit are disabled and draw essentially zero current. The DAC output is put into a HIGH-impedance state, and the output pin is passively pulled to ground through a 200k

## OPERATION

resistor. Input and DAC register contents are not disturbed during power-down.

The DAC can be put into power-down mode by using command 0100. The supply current is reduced to 1.8 $\mu$ A maximum (C and I grades) and the REF pin becomes HIGH impedance (typically > 1G $\Omega$ ).

Normal operation resumes after executing any command that includes a DAC update, as shown in Table 1. The DAC is powered up and its voltage output is updated. Normal settling is delayed while the bias, reference, and amplifier circuits are re-enabled. When the REF pin output is bypassed to GND with 1nF or less, the power-up delay time is 20 $\mu$ s for settling to 12-bits. This delay increases to 200 $\mu$ s for 0.33 $\mu$ F, and 10ms for 10 $\mu$ F.

### Voltage Output

The LTC2640's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1 $\Omega$  when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50 $\Omega$  typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50 $\Omega$  • 1mA, or 50mV). See the graph "Headroom at Rails vs. Output Current" in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

### Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit the lowest codes, as shown in Figure 4b. Similarly, limiting can occur near full-scale when the REF pin is tied to  $V_{CC}$ . If  $V_{REF} = V_{CC}$  and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at  $V_{CC}$ , as shown in Figure 4c. No full-scale limiting can occur if  $V_{REF}$  is less than  $V_{CC} - FSE$ .

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

### Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2640 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1 $\Omega$ ). Note that the LTC2640 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2640 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

OPERATION



Figure 3a. LTC2640-12 24-Bit Load Sequence (Minimum Input Word).  
 LTC2640-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Cares Bits;  
 LTC2640-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Cares Bits



Figure 3b. LTC2640-12 32-Bit Load Sequence  
 LTC2640-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Cares Bits;  
 LTC2640-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Cares Bits

## OPERATION



**Figure 4. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown for 12-Bits)**

**(a) Overall Transfer Function**

**(b) Effect of Negative Offset for Codes Near Zero**

**(c) Effect of Positive Full-Scale Error for Codes Near Full-Scale**

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2640#packaging> for the most recent package drawings.

**TS8 Package**  
**8-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1637 Rev A)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	10/13	Updated TS8 package drawing to Rev A.	22
D	06/17	Removed Note 3.	9

## TYPICAL APPLICATION

Programmable  $\pm 5V$  Output



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC1663</a>	Single 10-Bit $V_{OUT}$ DAC in SOT-23	$V_{CC} = 2.7V$ to $5.5V$ , $60\mu A$ , Internal Reference, SMBus Interface
<a href="#">LTC1669</a>	Single 10-Bit $V_{OUT}$ DAC in SOT-23	$V_{CC} = 2.7V$ to $5.5V$ , $60\mu A$ , Internal Reference, I <sup>2</sup> C Interface
<a href="#">LTC2360/LTC2362/LTC2365/LTC2366</a>	12-Bit SAR ADCs in TSOT23-6/TSOT23-8 Packages	100ksps/250ksps/500ksps/1Msps/3Msps Output Rates
<a href="#">LTC2450/LTC2452</a>	16-Bit Single-Ended/Differential Delta Sigma ADCs	SPI Interface, Tiny DFN Packages, 60Hz Output Rate
<a href="#">LTC2451/LTC2453</a>	16-Bit Single-Ended/Differential Delta Sigma ADCs	I <sup>2</sup> C Interface, Tiny DFN and TSOT23-8 Packages, 60Hz Output Rate
<a href="#">LTC2600/LTC2610/LTC2620</a>	Octal 16-/14-/12-Bit $V_{OUT}$ DACs in 16-Lead SSOP	$250\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, SPI Serial Interface
<a href="#">LTC2601/LTC2611/LTC2621</a>	Single 16-/14-/12-Bit $V_{OUT}$ DACs in 10-Lead DFN	$300\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, SPI Serial Interface
<a href="#">LTC2602/LTC2612/LTC2622</a>	Dual 16-/14-/12-Bit $V_{OUT}$ DACs in 8-Lead MSOP	$300\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, SPI Serial Interface
<a href="#">LTC2604/LTC2614/LTC2624</a>	Quad 16-/14-/12-Bit $V_{OUT}$ DACs in 16-Lead SSOP	$250\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, SPI Serial Interface
<a href="#">LTC2605/LTC2615/LTC2625</a>	Octal 16-/14-/12-Bit $V_{OUT}$ DACs with I <sup>2</sup> C Interface	$250\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, I <sup>2</sup> C Interface
<a href="#">LTC2606/LTC2616/LTC2626</a>	Single 16-/14-/12-Bit $V_{OUT}$ DACs with I <sup>2</sup> C Interface	$270\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output, I <sup>2</sup> C Interface
<a href="#">LTC2609/LTC2619/LTC2629</a>	Quad 16-/14-/12-Bit $V_{OUT}$ DACs with I <sup>2</sup> C Interface	$250\mu A$ per DAC, $2.5V$ to $5.5V$ Supply Range, Rail-to-Rail Output with Separate $V_{REF}$ Pins for Each DAC
<a href="#">LTC2630</a>	Single 12-/10-/8-Bit $V_{OUT}$ DACs with 10ppm/°C Reference in SC70	$180\mu A$ per DAC, $2.7V$ to $5.5V$ Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, SPI Interface
<a href="#">LTC2631</a>	Single 12-/10-/8-Bit I <sup>2</sup> C $V_{OUT}$ DACs with 10ppm/°C Reference in ThinSOT	$180\mu A$ per DAC, $2.7V$ to $5.5V$ Supply Range, 10ppm/°C Reference, Selectable External Ref. Mode, Rail-to-Rail Output, I <sup>2</sup> C Interface

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