THE DATASHEET OF

NCP1239AD100R2G

www.win-source.net 0086-755-83957316

Fixed Frequency Current-Mode Controller for Flyback Converter

NCP1239

SOIC−7
CASE 751U

The NCP1239 is a fixed-frequency current-mode controller featuring a high-voltage start-up current source to provide a quick and lossless power-on sequence. This function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal start-up current source to supply the controller during start-up, transients, latch, stand-by etc.

With a supply range up to 35 V, the controller hosts a jittered 65 or 100-kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current that insures excellent efficiency in light load condition.

NCP1239 features a timer-based fault detection circuitry that ensures a quasi-flat overload detection, independent of the input voltage.

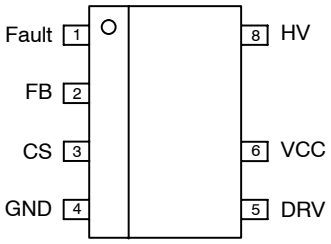
Features

- Fixed-Frequency 65-kHz or 100-kHz Current-Mode Control Operation
- Frequency Foldback Down to 26 kHz and Skip Mode to Maximize Performance in Light Load Conditions
- Adjustable Over Power Protection (OPP) Circuit
- High-Voltage Current Source with Brown-Out (BO) Detection
- Internal Slope Compensation
- Internal Fixed Soft-Start
- Frequency Jittering in Normal and Frequency Foldback Modes
- 64-ms Timer-Based Short-Circuit Protection with Auto-Recovery or Latched Operation
- Pre-Short Ready for Latched OCP Versions
- Latched OVP on VCC – Autorecovery for C and E Versions
- Latched OVP/OTP Input for Improved Robustness
- 35-V V_{CC} Operation
- ±500 mA Peak Source/Sink Drive Capability
- Internal Thermal Shutdown
- Extremely Low No-Load Standby Power
- Pin-to-Pin Compatible with the Existing NCP1236/1247 Series
- These Devices are Pb-Free and are RoHS Compliant

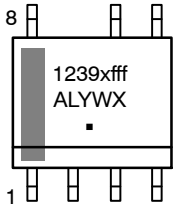
Typical Applications

- AC-DC Converters for TVs, Set-Top Boxes and Printers
- Offline Adapters for Notebooks and Netbooks

PIN CONNECTIONS



MARKING DIAGRAM



1239xfff	= Specific Device Code
x	= A, B, C, D, E, F, G, H, I, J, K, L, M, N, P, Q or R
	fff = 065 or 100
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 26 of this data sheet.

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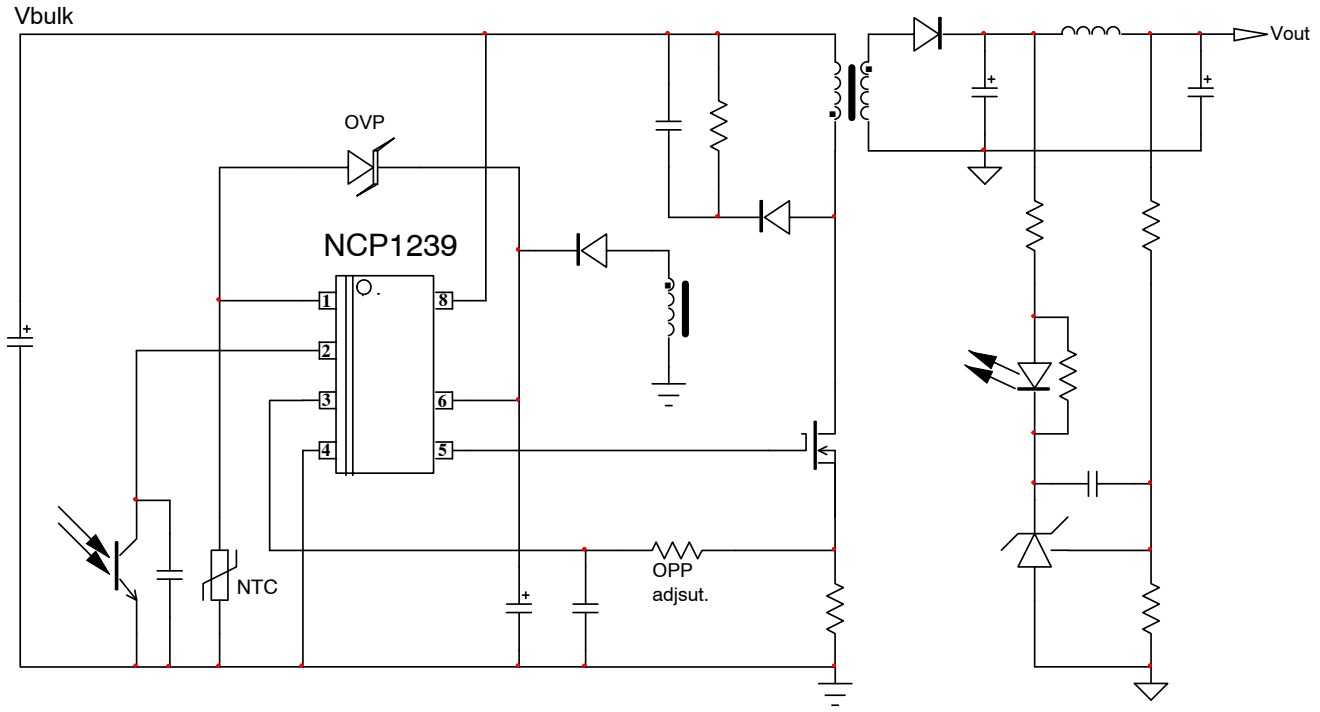

Figure 1. Application Schematic (OPP Adjustment)

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch.
2	FB	Hooking an optocoupler collector to this pin will allow regulation.
3	CS	This pin monitors the primary peak current but also offers an overpower compensation adjustment. When the CS pin is brought above 1.2 V, the part is permanently latched off.
4	GND	The controller ground.
5	DRV	The driver's output to an external MOSFET gate.
6	VCC	This pin is connected to an external auxiliary voltage. An OVP comparator monitors this pin and offers a means to latch the converter in fault conditions.
7	NC	Non-connected for improved creepage distance.
8	HV	Connected to the bulk capacitor or rectified ac line, this pin powers the internal current source to deliver a start-up current. It is also used to provide the brown-out detection and the HV sensing for the Overpower protection.

Table 2. DEVICE OPTION AND DESIGNATIONS

Device	Fre-quency	OCP Protection	OCP Timer	V_{cc} OVP Threshold	V_{cc} OVP Protection	Fault pin Protection	BO Levels	BO Timer	Soft–start Timer	DSS Func-tion
NCP1239AD65R2G	65 kHz	Latch	64 ms	25.5 V	Latch	Latch	110 / 101	68 ms	8 ms	Disable
NCP1239BD65R2G	65 kHz	Auto–Recovery	64 ms	25.5 V	Latch	Latch	110 / 101	68 ms	8 ms	Disable
NCP1239CD65R2G	65 kHz	Auto–Recovery	64 ms	25.5 V	Auto–Recovery	Latch	110 / 101	68 ms	8 ms	Disable
NCP1239DD65R2G	65 kHz	Auto–Recovery	64 ms	25.5 V	Latch	Latch	101 / 95	68 ms	8 ms	Disable
NCP1239ED65R2G	65 kHz	Auto–Recovery	64 ms	25.5 V	Auto–Recovery	Auto–Recovery	110 / 101	68 ms	8 ms	Disable
NCP1239FD65R2G	65 kHz	Latch	64 ms	32 V	Latch	Latch	229 / 176	68 ms	4 ms	Disable
NCP1239HD65R2G	65 kHz	Latch	64 ms	25.5 V	Latch	Latch	229 / 224	68 ms	8 ms	Disable
NCP1239ID65R2G	65 kHz	Latch	128 ms	25.5 V	Latch	Latch	101 / 95	68 ms	4 ms	Disable
NCP1239JD65R2G	65 kHz	Latch	128 ms	32 V	Latch	Latch	101 / 95	68 ms	8 ms	Enable
NCP1239KD65R2G	65 kHz	Auto–Recovery	128 ms	25.5 V	Auto–Recovery	Auto–Recovery	110 / 101	68 ms	8 ms	Disable
NCP1239LD65R2G	65 kHz	Auto–Recovery	128 ms	25.5 V	Latch	Latch	82 / 77	68 ms	4 ms	Disable
NCP1239MD65R2G	65 kHz	Auto–Recovery	128 ms	32 V	Auto–Recovery	Auto–Recovery	229 / 224	68 ms	4 ms	Enable
NCP1239ND65R2G	65 kHz	Auto–Recovery	128 ms	32 V	Auto–Recovery	Latch	229 / 224	68 ms	4 ms	Enable
NCP1239PD65R2G	65 kHz	Auto–Recovery	64 ms	25.5 V	Auto–Recovery	Auto–Recovery	82 / 79	68 ms	8 ms	Disable
NCP1239QD65R2G	65 kHz	Auto–Recovery	128 ms	25.5 V	Auto–Recovery	Auto–Recovery	82 / 79	68 ms	8 ms	Disable
NCP1239RD65R2G	65 kHz	Auto–Recovery	128 ms	25.5 V	Latch	Latch	101 / 95	272 ms	4 ms	Disable
NCP1239AD100R2G	100 kHz	Latch	64 ms	25.5 V	Latch	Latch	110 / 101	68 ms	8 ms	Disable
NCP1239BD100R2G	100 kHz	Auto–Recovery	64 ms	25.5 V	Latch	Latch	110 / 101	68 ms	8 ms	Disable
NCP1239DD100R2G	100 kHz	Auto–Recovery	64 ms	25.5 V	Latch	Latch	101 / 95	68 ms	8 ms	Disable
NCP1239ED100R2G	100 kHz	Auto–Recovery	64 ms	25.5 V	Auto–Recovery	Auto–Recovery	110 / 101	68 ms	8 ms	Disable
NCP1239GD100R2G	100 kHz	Latch	64 ms	25.5 V	Latch	Latch	95 / 86	136 ms	8 ms	Disable
NCP1239LD100R2G	100 kHz	Auto–Recovery	128 ms	25.5 V	Latch	Latch	82 / 77	68 ms	4 ms	Disable

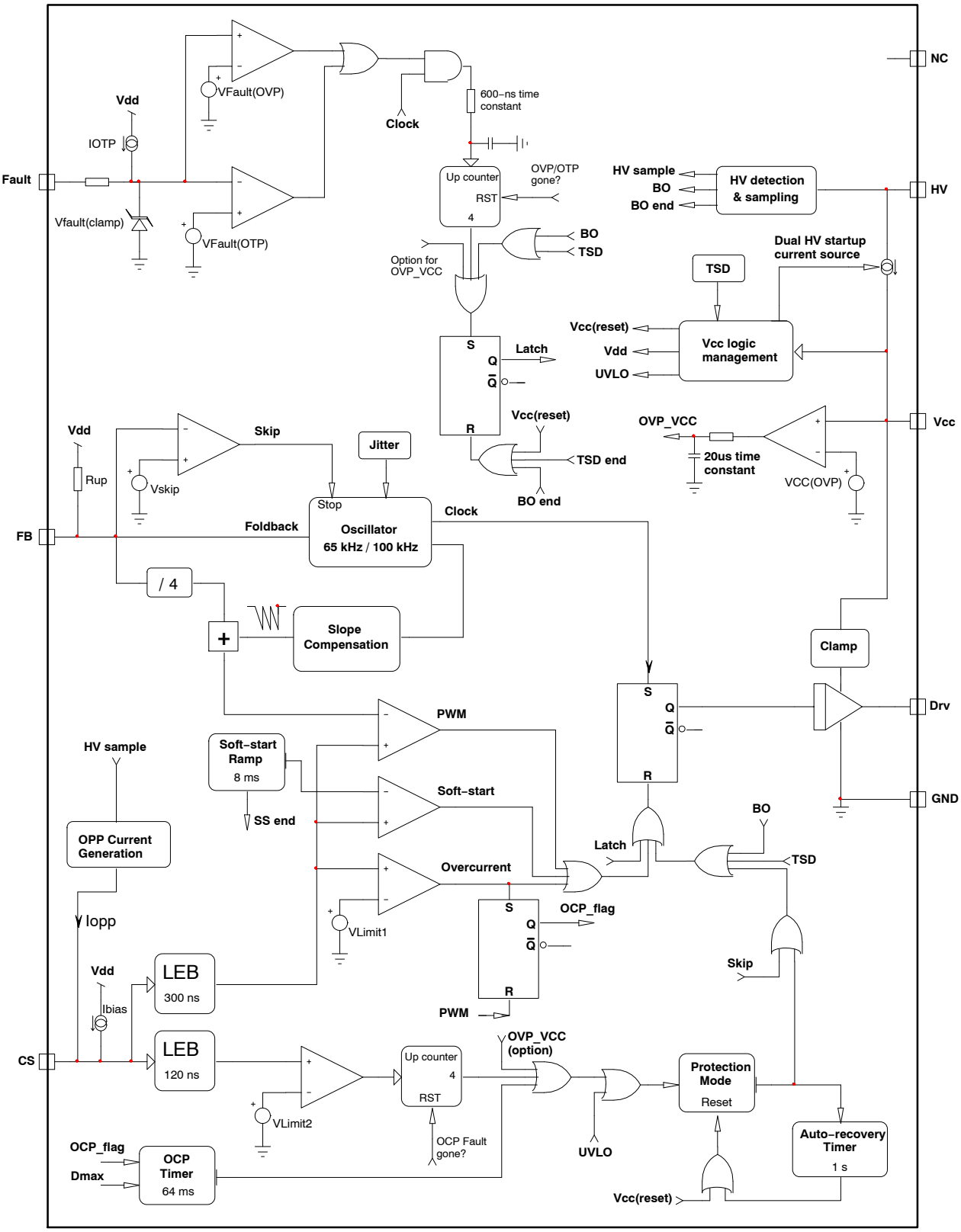

Figure 2. Simplified Block Diagram

Table 3. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, V_{CC} Pin, Continuous Voltage	V_{CC}	−0.3 to 35	V
Maximum Voltage on Low Power Pins CS, FB and Fault		−0.3 to 5.5	V
Maximum Voltage on DRV Pin	V_{DRV}	−0.3 to 20	V
High Voltage Pin	HV	−0.3 to 650	V
Thermal Resistance Junction-to-Air Single Layer PCB 25 mm², 2 Oz Cu Printed Circuit Copper Clad	$R_{\theta J-A}$	250	°C/W
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	−60 to 150	°C
ESD Capability (Note 2) Human Body Model − All Pins Except HV Machine Model	ESD_{HBM} ESD_{MM}	4 200	kV V
Charged-Device Model ESD Capability per JEDEC JESD22−C101E		1	kV
Moisture Sensitivity Level	MSL	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC JESD22−A114F
   ESD Machine Model tested per JEDEC JESD22−A115C
   Charged-Device Model ESD Capability tested per JEDEC JESD22−C101E
   Latch-up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78

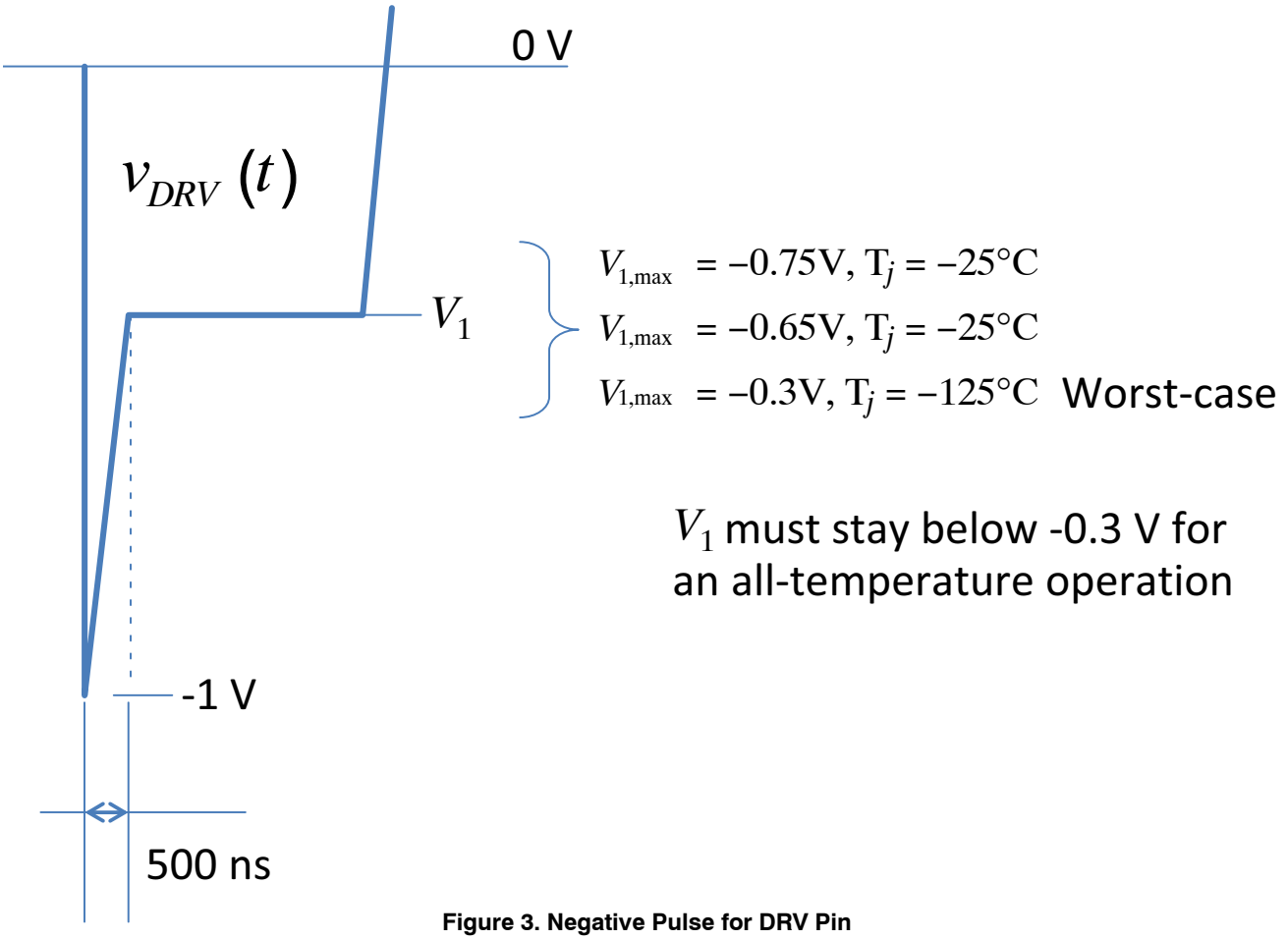

Figure 3. Negative Pulse for DRV Pin

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max Values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
START-UP SECTION						
Minimum Voltage for Current Source Operation	I_{HV} = 90% I_{START2}, V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{HV(min)}$	–	25	60	V
Current Flowing Out of V_{CC} Pin	V_{CC} = 0 V	I_{START1}	0.2	0.5	0.8	mA
Current Flowing Out of V_{CC} Pin	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{START2}	1.5	3	4.5	mA
HV Pin Leakage Current	V_{HV} = 325 V	I_{LEAK1}	–	8	20	μA
SUPPLY SECTION						
Start-Up Threshold HV Current Source Stop Threshold	V_{CC} Increasing	$V_{CC(on)}$	11.0	12.0	13.0	V
HV Current Source Restart Threshold	V_{CC} Decreasing	$V_{CC(min)}$	9.0	10.0	11.0	V
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.0	8.8	9.4	V
Operating Hysteresis	$V_{CC(on)}$ = $V_{CC(off)}$	$V_{CC(hys)}$	3.0	–	–	V
V_{CC} Level for I_{START1} to I_{START2} Transition		$V_{CC(inhibit)}$	0.7	1.2	1.7	V
V_{CC} Level where Logic Functions are Reset	V_{CC} Decreasing	$V_{CC(reset)}$	6.5	7	7.5	V
Internal IC Consumption	V_{FB} = 3.2 V, F_{SW} = 65 kHz and C_L = 0	ICC1	–	1.4	2.2	mA
Internal IC Consumption	V_{FB} = 3.2 V, F_{SW} = 65 kHz and C_L = 1 nF	ICC2	–	2.1	3.0	mA
Internal IC Consumption	V_{FB} = 3.2 V, F_{SW} = 100 kHz and C_L = 0	ICC1	–	1.7	2.5	mA
Internal IC Consumption	V_{FB} = 3.2 V, F_{SW} = 100 kHz and C_L = 1 nF	ICC2	–	3.1	4.0	mA
Internal IC Consumption in Skip Cycle	V_{CC} = 12 V, V_{FB} = 0.775 V Driving 8 A/600 V MOSFET	ICC(stb)	–	500	–	μA
Internal IC Consumption in Skip Cycle L, P and Q versions	V_{CC} = 12 V, V_{FB} = 0.775 V Driving 8 A/600 V MOSFET	ICC(stb)	–	565	–	μA
Internal IC Consumption in Fault Mode	Fault or Latch	ICC3	–	400	–	μA
Internal IC Consumption in Fault Mode L, P and Q versions	Fault or Latch	ICC3	–	480	–	μA
Internal IC Consumption before Start-Up	$V_{CC(min)}$ < V_{CC} < $V_{CC(on)}$	ICC4	–	310	–	μA
Internal IC Consumption before Start-Up	V_{CC} < $V_{CC(min)}$	ICC5	–	20	–	μA
DRIVE OUTPUT						
Rise Time (10−90%)	V_{DRV} from 10 to 90% V_{CC} = $V_{CC(off)}$ + 0.2 V, C_L = 1 nF	t_R	–	40	–	ns
Fall Time (90−10%)	V_{DRV} from 90 to 10% V_{CC} = $V_{CC(off)}$ + 0.2 V, C_L = 1 nF	t_F	–	30	–	ns
Source Resistance		R_{OH}	–	6	–	Ω
Sink Resistance		R_{OL}	–	6	–	Ω
Peak Source Current	DRV High State, V_{DRV} = 0 V (Note 1) V_{CC} = $V_{CC(off)}$ + 0.2 V, C_L = 1 nF	I_{SOURCE}	–	500	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Guaranteed by design
2. CS pin source current is a sum of I_{BIAS} and I_{OPP}, thus at V_{HV} = 125 V is observed the I_{BIAS} only, because I_{OPC} is switched off.

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max Values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT						
Peak Sink Current	DRV Low State, $V_{DRV} = V_{CC}$ (Note 1) $V_{CC} = V_{CC(off)} + 0.2$ V, C_L = 1 nF	I_{SINK}	–	500	–	mA
High State Voltage (Low V_{CC} Level)	V_{CC} = 9 V, R_{DRV} = 33 kΩ DRV High State	$V_{DRV(low)}$	8.8	–	–	V
High State Voltage (High V_{CC} Level)	$V_{CC} = V_{CC(OVP)} - 0.2$ V, DRV High State and Unloaded	$V_{DRV(clamp)}$	11.0	13.5	16.0	V
CURRENT COMPARATOR						
Input Pull-Up Current	V_{CS} = 0.7 V	I_{BIAS}	–	1	–	μA
Maximum Internal Current Setpoint	T_J from −40°C to +125°C (No OPP)	V_{LIMIT1}	0.752	0.800	0.848	V
Abnormal Over-Current Fault Threshold	T_J = +25°C (No OPP)	V_{LIMIT2}	1.10	1.20	1.30	V
Default Internal Voltage Set Point for Frequency Foldback Trip Point	~59% of V_{LIMIT}	$V_{FOLD(CS)}$	–	475	–	mV
Internal Peak Current Setpoint Freeze	~31% of V_{LIMIT}	$V_{FREEZE(CS)}$	–	250	–	mV
Propagation Delay from V_{LIMIT} Detection to Gate Off-State	DRV Output Unloaded	t_{DEL}	–	50	100	ns
Leading Edge Blanking Duration		t_{LEB1}	–	300	–	ns
Abnormal Over-Current Fault Blanking Duration for V_{LIMIT3}		t_{LEB2}	–	120	–	ns
Number of Clock Cycles before Fault Confirmation		t_{COUNT}	–	4	–	
Internal Soft-Start Duration	Activated upon startup or auto−recovery A, B, C, D, E, G, H, J, K, P or Q versions F, I, L, M, N or R versions	t_{SS}	 – –	 8 4	 – –	ms
INTERNAL OSCILLATOR						
Oscillation Frequency (65-kHz Version)		f_{OSC}	60	65	70	kHz
Oscillation Frequency (100-kHz Version)		f_{OSC}	92	100	108	kHz
Maximum Duty-Cycle		D_{MAX}	76	80	84	%
Frequency Jittering	In Percentage of f_{OSC} − Jitter is Kept even in Foldback Mode	f_{JITTER}	–	±5	–	%
Swing Frequency		f_{SWING}	–	240	–	Hz
FEEDBACK SECTION						
Equivalent AC Resistor from FB to GND	(Note 1)	R_{EQ}	–	25	–	kΩ
Internal Pull-Up Voltage on FB Pin	FB open	$V_{FB(ref)}$	4.1	4.3	–	V
V_{FB} to Current Setpoint Division Ratio		K_{FB}	–	4	–	
Feedback Voltage below which the Peak Current is Frozen		V_{FREEZE}	–	1.0	–	V
FREQUENCY FOLDBACK						
Frequency Foldback Level on FB Pin	≈ 59% of Maximum Peak Current	V_{FOLD}	–	1.90	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design
2. CS pin source current is a sum of I_{BIAS} and I_{OPP}, thus at V_{HV} = 125 V is observed the I_{BIAS} only, because I_{OPC} is switched off.

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max Values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FREQUENCY FOLDBACK						
Transition Frequency below which Skip-Cycle Occurs	$V_{FB} = V_{SKIP}$ + 0.5 V	f_{TRANS}	22	26	30	kHz
End of Frequency Foldback Feedback Level	$f_{SW} = f_{MIN}$	$V_{FOLD(end)}$	–	1.50	–	V
Skip-Cycle Level Voltage on FB Pin		V_{SKIP}	–	0.80	–	V
Hysteresis on the Skip Comparator	(Note 1)	$V_{SKIP(hyst)}$	–	30	–	mV
INTERNAL RAMP COMPENSATION						
Compensation Ramp Slope	F_{SW} = 65 kHz, R_{UP} = 30 kΩ F_{SW} = 100 kHz, R_{UP} = 30 kΩ	S_{65} S_{100}	– –	–29 –45	– –	mV/μs
OVERPOWER COMPENSATION (OPP)						
V_{HV} to I_{OPP} Conversion Ratio		K_{OPP}	–	0.54	–	μA/V
Current Flowing Out of CS Pin (Note 2)	V_{HV} = 125 V V_{HV} = 162 V V_{HV} = 328 V V_{HV} = 365 V	$I_{OPP(125)}$ $I_{OPP(162)}$ $I_{OPP(328)}$ $I_{OPP(365)}$	– – – 105	0 20 110 130	– – – 150	μA
Current Flowing Out of CS Pin for L version (Note 2)	V_{HV} = 108 V V_{HV} = 145 V V_{HV} = 294 V V_{HV} = 327 V	$I_{OPP(108)}$ $I_{OPP(145)}$ $I_{OPP(294)}$ $I_{OPP(327)}$	– – – 105	0 20 110 130	– – – 150	μA
Percentage of Applied OPP Current	$V_{FB} < V_{FOLD}$	I_{OPP1}	–	0	–	%
Percentage of Applied OPP Current	$V_{FB} > V_{FOLD}$ + 0.7 V (V_{OPP})	I_{OPP2}	–	100	–	%
Clamped OPP Current	V_{HV} > 365 V	I_{OPP3}	105	130	150	μA
Watchdog Timer for DC Operation		$t_{WD(OPP)}$	–	32	–	ms
BROWN-OUT (BO)						
Brown-Out Thresholds (A,B,C,E & K versions)	V_{HV} Increasing	$V_{BO(on)}$	100	110	120	V
Brown-Out Thresholds (A,B,C,E & K versions)	V_{HV} Decreasing	$V_{BO(off)}$	93	101	109	V
Brown-Out Thresholds (D, I, J and R versions)	V_{HV} Increasing	$V_{BO(on)}$	92	101	110	V
Brown-Out Thresholds (D, I, J and R versions)	V_{HV} Decreasing	$V_{BO(off)}$	87	95	103	V
Brown-Out Thresholds (F version only)	V_{HV} Increasing	$V_{BO(on)}$	211	229	247	V
Brown-Out Thresholds (F version only)	V_{HV} Decreasing	$V_{BO(off)}$	164	176	188	V
Brown-Out Thresholds (G version only)	V_{HV} Increasing	$V_{BO(on)}$	86	95	104	V
Brown-Out Thresholds (G version only)	V_{HV} Decreasing	$V_{BO(off)}$	79	86	93	V
Brown-Out Thresholds (H, M and N versions)	V_{HV} Increasing	$V_{BO(on)}$	211	229	247	V
Brown-Out Thresholds (H, M and N versions)	V_{HV} Decreasing	$V_{BO(off)}$	208	224	240	V
Brown-Out Thresholds (L version only)	V_{HV} Increasing	$V_{BO(on)}$	74	82	90	V
Brown-Out Thresholds (L version only)	V_{HV} Decreasing	$V_{BO(off)}$	70	77	84	V
Brown−out thresholds (P and Q versions)	V_{HV} increasing	$V_{BO(on)}$	74	82	90	V
Brown−out thresholds (P and Q versions)	V_{HV} decreasing	$V_{BO(off)}$	72	79	86	V
Brown-Out Timer Duration (A, B, C, D, E, F, H, I, J, K, L, M, N, P and Q versions)	V_{HV} Decreasing	t_{BO}	54	68	82	ms
Brown-Out Timer Duration (G version only)	V_{HV} Decreasing	t_{BO}	110	136	162	ms
Brown-Out Timer Duration (R version only)	V_{HV} Decreasing	t_{BO}	216	272	324	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design
2. CS pin source current is a sum of I_{BIAS} and I_{OPP}, thus at V_{HV} = 125 V is observed the I_{BIAS} only, because I_{OPC} is switched off.

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max Values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FAULT INPUT (OTP/OVP)						
Over-Voltage Protection Threshold	V_{FAULT} Increasing	$V_{FAULT(OVP)}$	2.8	3.0	3.2	V
Over-Temperature Protection Threshold	V_{FAULT} Decreasing	$V_{FAULT(OTP)}$	0.37	0.40	0.43	V
NTC Biasing Current	V_{FAULT} = 0 V	I_{OTP}	39	45	51	μA
Additional NTC Biasing Current during Soft-Start Only	V_{FAULT} = 0 V − During Soft-Start Only	I_{OTP_boost}	38	44	50	μA
Latch Clamping Voltage	I_{FAULT} = 0 mA	$V_{FAULT(clamp)0}$	1.1	1.35	1.6	V
Latch Clamping Voltage	I_{FAULT} = 1 mA	$V_{FAULT(clamp)1}$	2.2	2.7	3.2	V
Blanking Time after Drive Turn Off		$t_{LATCH(blank)}$	–	1	–	μs
Number of Clock Cycles before Latch Confirmation		$t_{LATCH(count)}$	–	4	–	
OVER-CURRENT PROTECTION (OCP)						
Internal OCP Timer Duration	A, B, C, D, E, F, G, H and P versions	t_{OCP}	51	64	77	ms
Internal OCP Timer Duration	I, J, K, L, M, N, Q and R versions	t_{OCP}	102	128	154	ms
Auto-Recovery Timer		$t_{AUTOREC}$	0.85	1	1.35	s
V_{CC} OVER-VOLTAGE (V_{CC} OVP)						
Latched Over Voltage Protection on V_{CC} Pin	A, B, C, D, E, G, H, I, K, L, P, Q or R versions	$V_{CC(OVP)}$	24.0	25.5	27.0	V
Latched Over Voltage Protection on V_{CC} Pin	F, J, M and N versions	$V_{CC(OVP)}$	30.0	32.0	34.0	V
Delay before OVP on V_{CC} Confirmation		$t_{OVP(delay)}$	–	20	–	μs
THERMAL SHUTDOWN (TSD)						
Temperature Shutdown	T_J Increasing (Note 1)	T_{SHDN}	135	150	165	°C
Temperature Shutdown Hysteresis	T_J Decreasing (Note 1)	$T_{SHDN(hys)}$	–	20	–	°C

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1. Guaranteed by design
2. CS pin source current is a sum of I_{BIAS} and I_{OPP}, thus at V_{HV} = 125 V is observed the I_{BIAS} only, because I_{OPC} is switched off.

TYPICAL PERFORMANCE CHARACTERISTICS

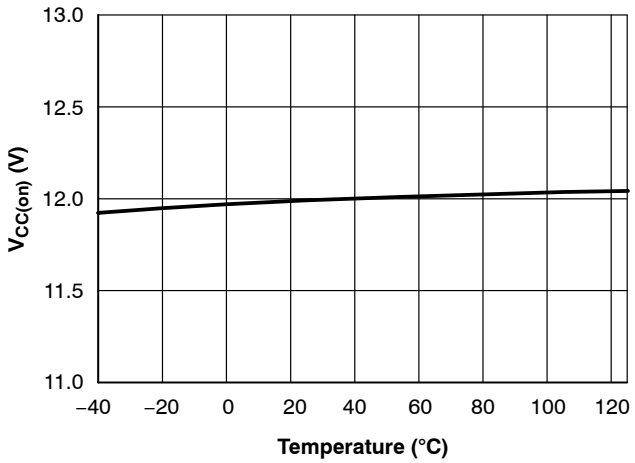


Figure 4. $V_{CC(on)}$ vs. Junction Temperature

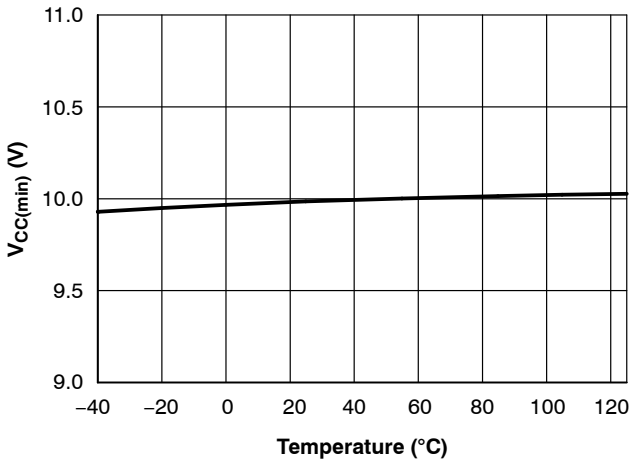


Figure 5. $V_{CC(min)}$ vs. Junction Temperature

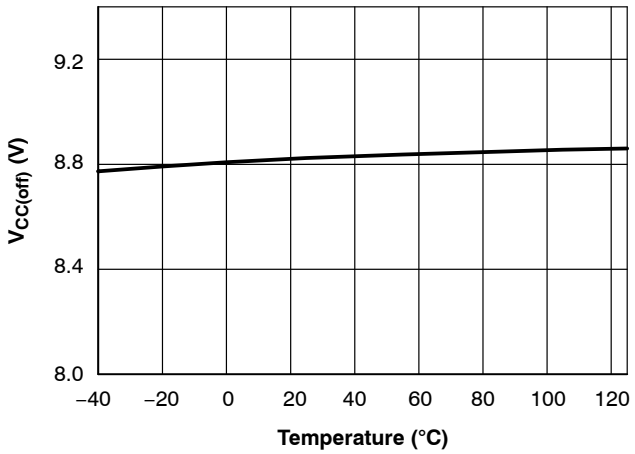


Figure 6. $V_{CC(off)}$ vs. Junction Temperature

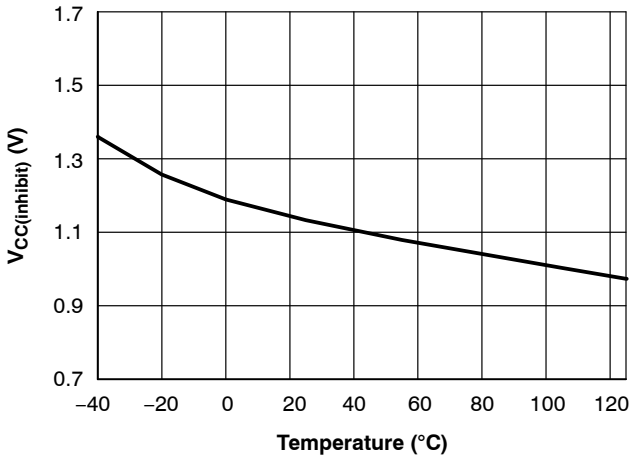


Figure 7. $V_{CC(inhibit)}$ vs. Junction Temperature

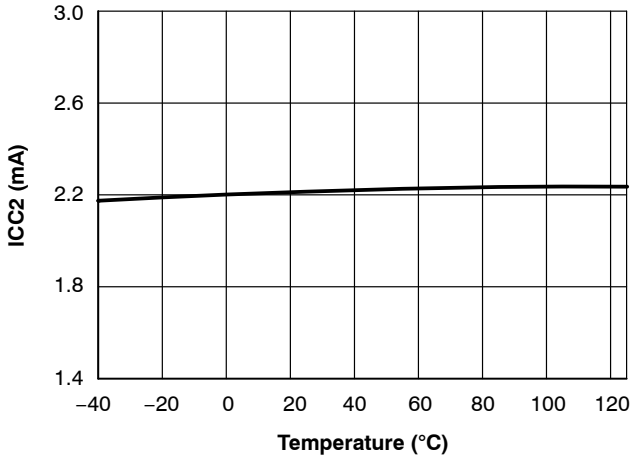


Figure 8. ICC2 (65-kHz Version) vs. Junction Temperature

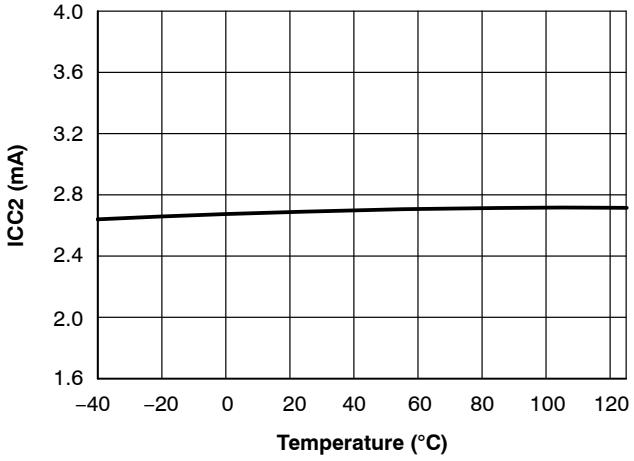


Figure 9. ICC2 (100-kHz Version) vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

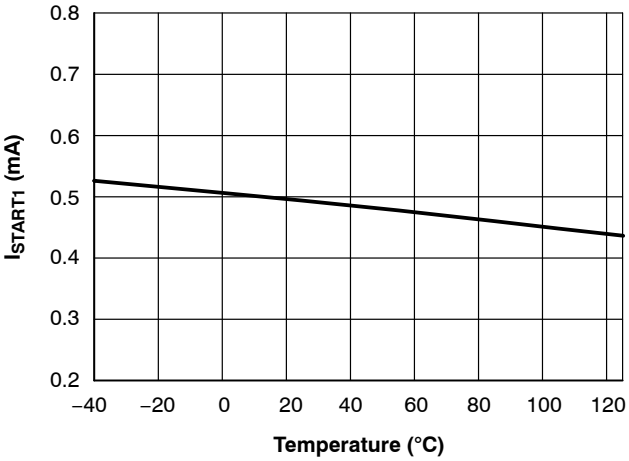


Figure 10. I_{START1} vs. Junction Temperature

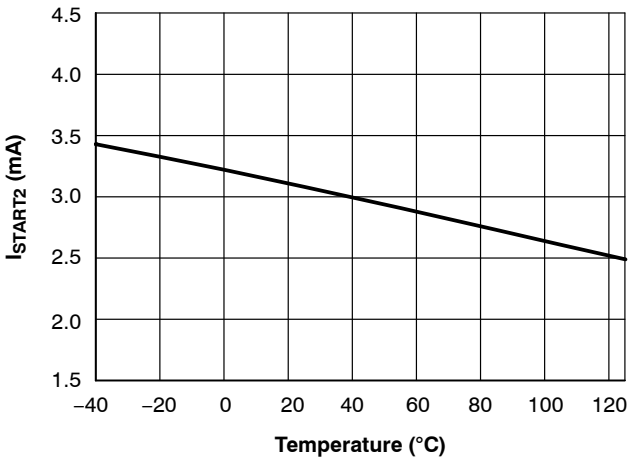


Figure 11. I_{START2} vs. Junction Temperature

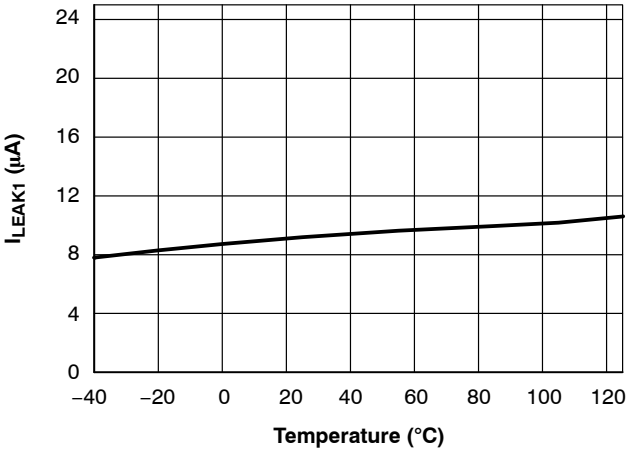


Figure 12. I_{LEAK1} vs. Junction Temperature

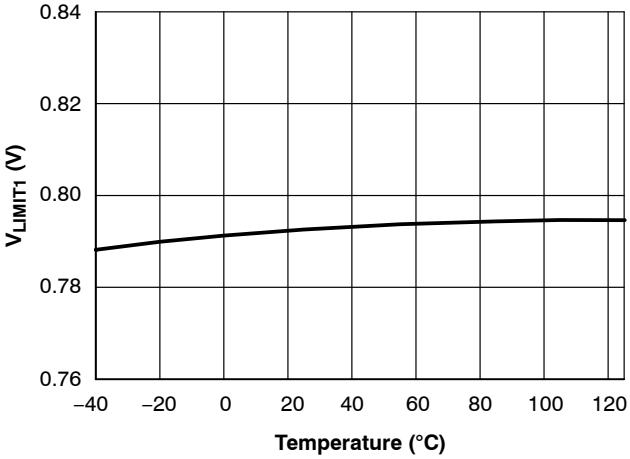


Figure 13. V_{LIMIT1} vs. Junction Temperature

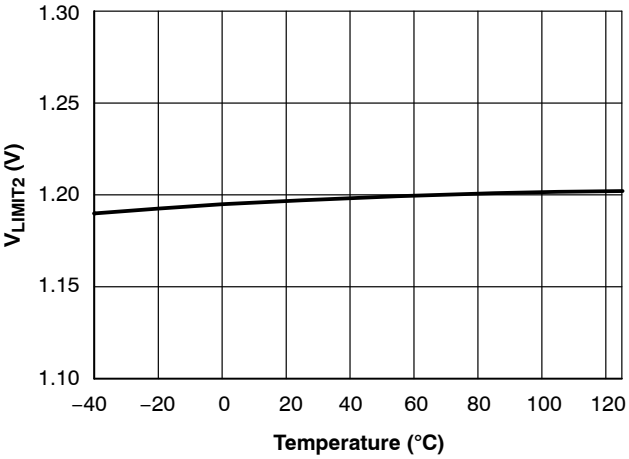


Figure 14. V_{LIMIT2} vs. Junction Temperature

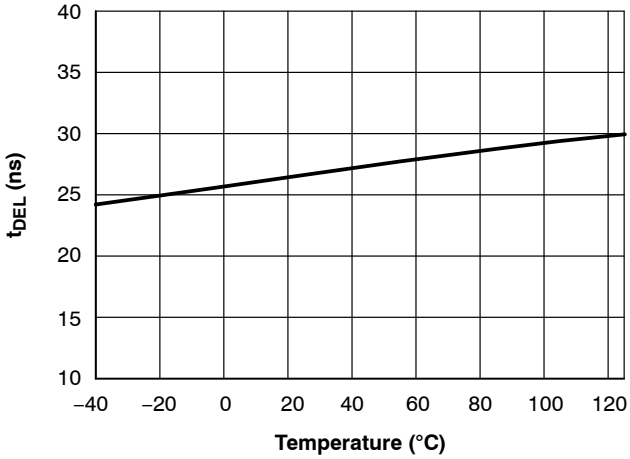


Figure 15. t_{DEL} vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

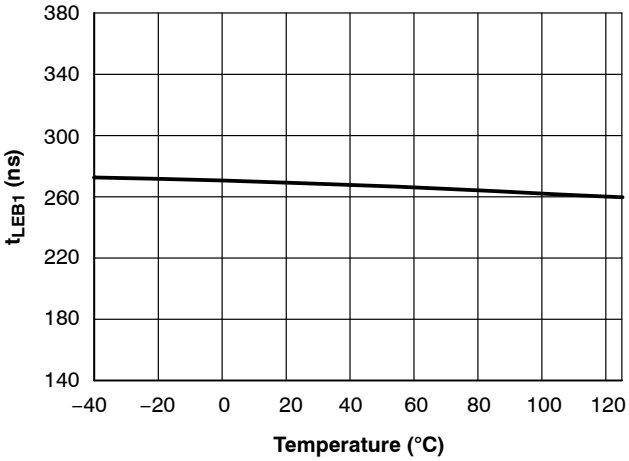


Figure 16. t_{LEB1} vs. Junction Temperature

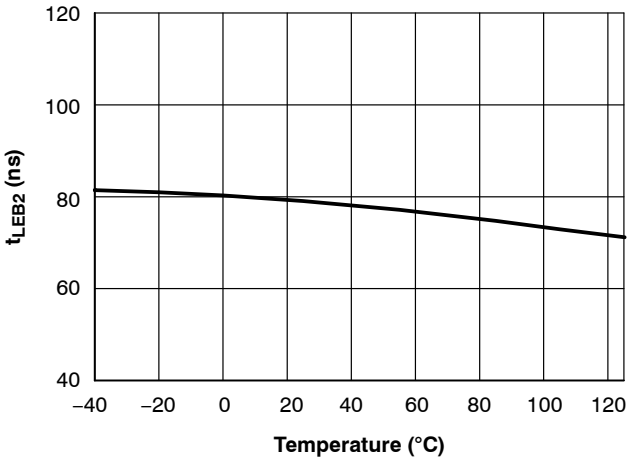


Figure 17. t_{LEB2} vs. Junction Temperature

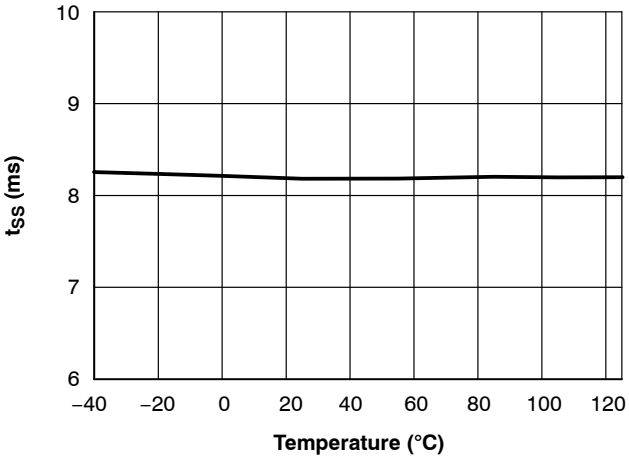


Figure 18. t_{SS} vs. Junction Temperature

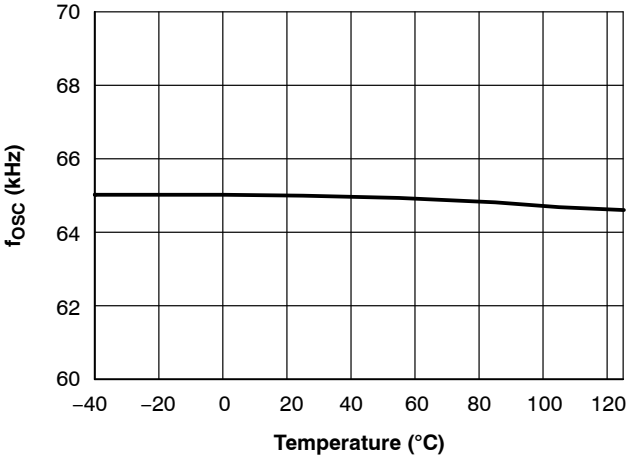


Figure 19. f_{OSC} (65-kHz Version) vs. Junction Temperature

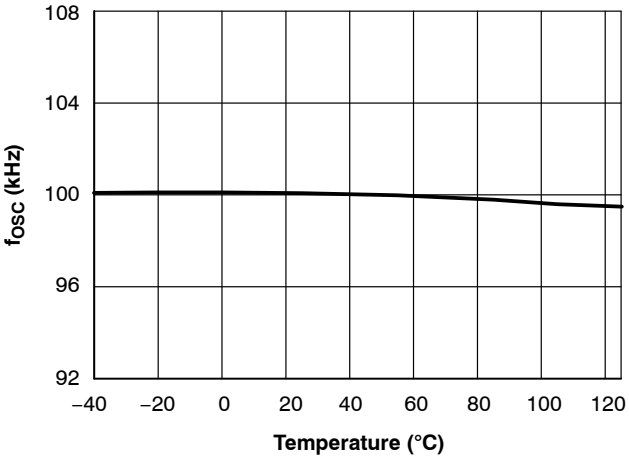


Figure 20. f_{OSC} (100-kHz Version) vs. Junction Temperature

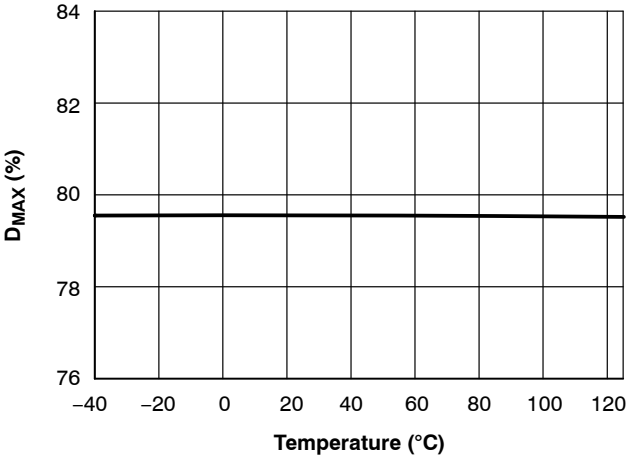


Figure 21. D_{MAX} vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

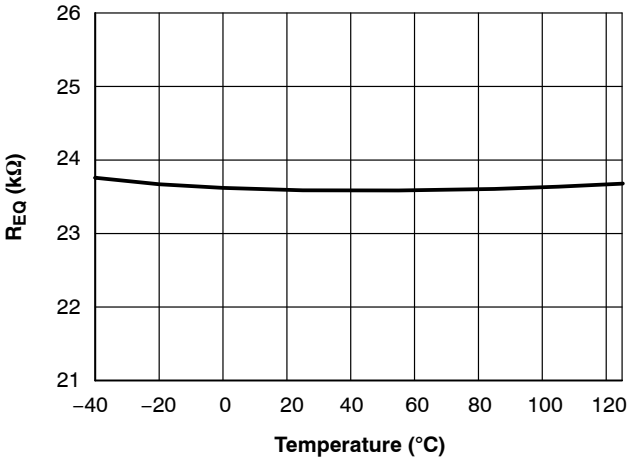


Figure 22. R_{EQ} vs. Junction Temperature

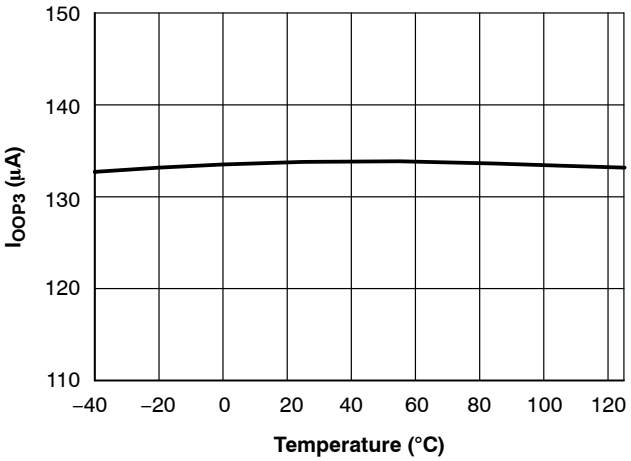


Figure 23. I_{OOP3} vs. Junction Temperature

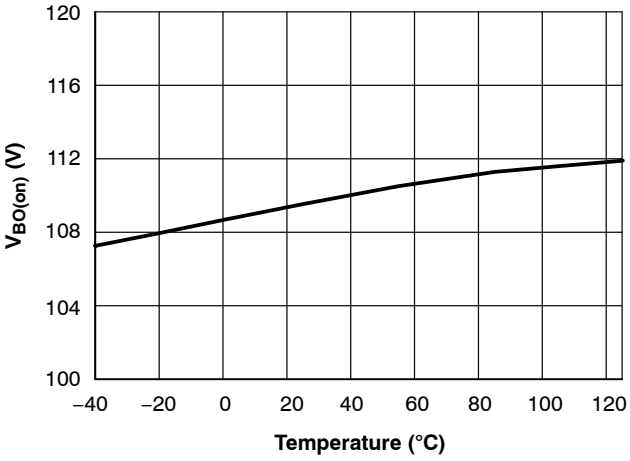


Figure 24. $V_{BO(on)}$ vs. Junction Temperature

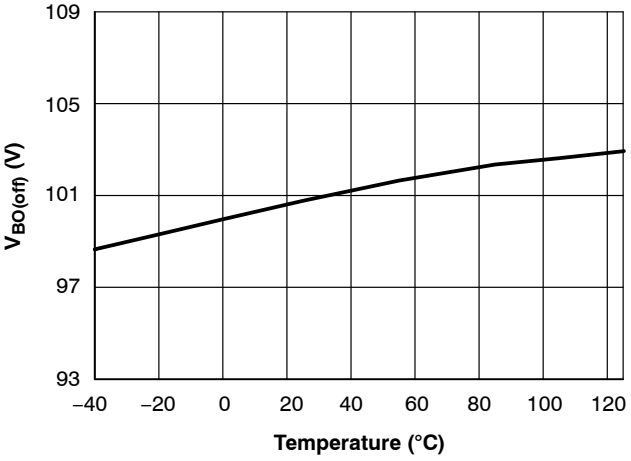


Figure 25. $V_{BO(off)}$ vs. Junction Temperature

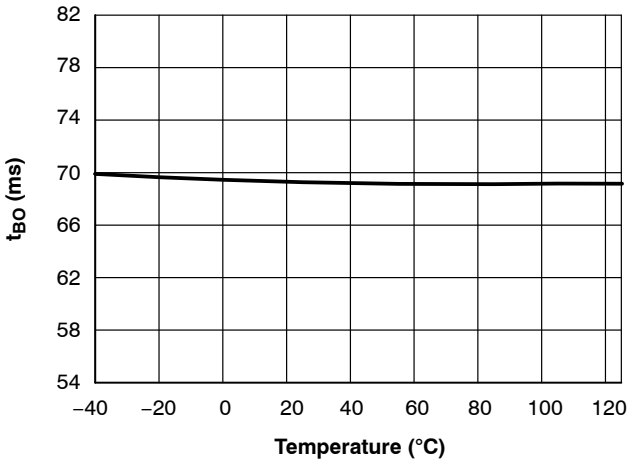


Figure 26. t_{BO} vs. Junction Temperature

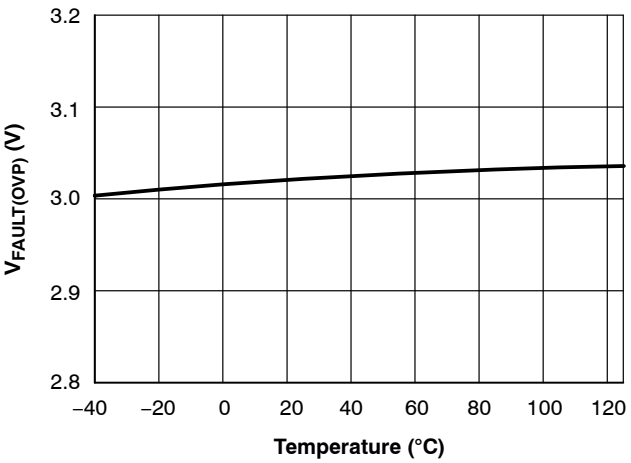


Figure 27. $V_{FAULT(OVP)}$ vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

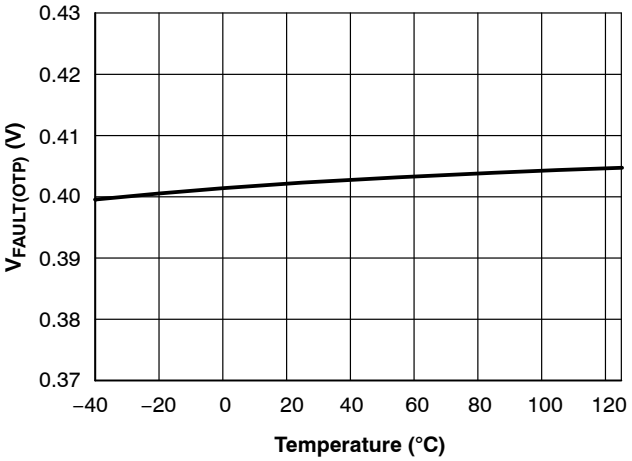


Figure 28. $V_{FAULT(OTP)}$ vs. Junction Temperature

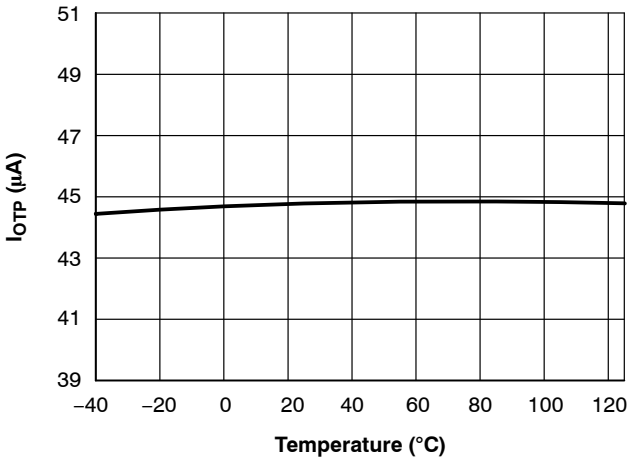


Figure 29. I_{OTP} vs. Junction Temperature

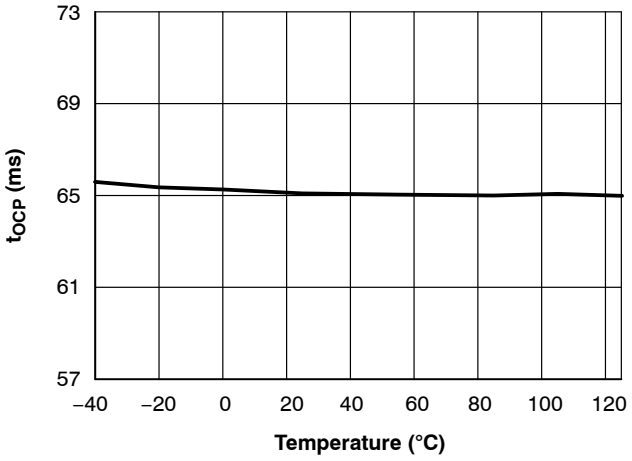


Figure 30. t_{OCP} vs. Junction Temperature

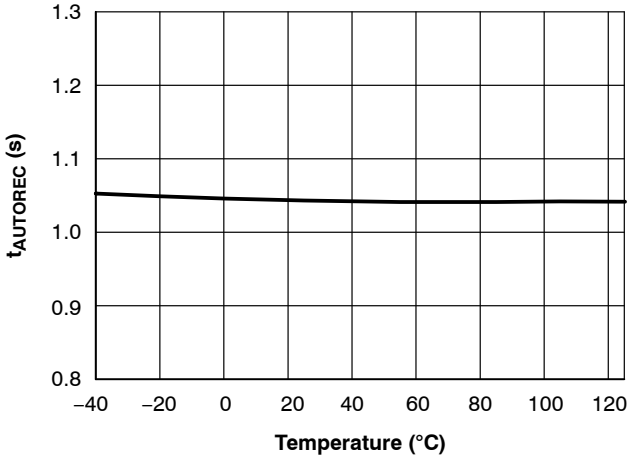


Figure 31. $t_{AUTOREC}$ vs. Junction Temperature

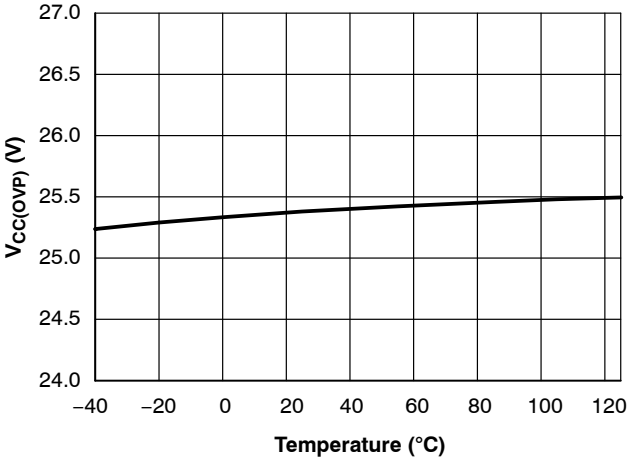


Figure 32. $V_{CC(OVP)}$ vs. Junction Temperature

DEFINITION

General

The NCP1239 implements a standard current mode architecture where the switch-off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count and cost effectiveness are the key parameters, particularly in low-cost ac-dc adapters, open-frame power supplies etc. The NCP1239 packs all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non-dissipative over power protection (OPP), a brown-out protection or HV start-up current source.

Current-Mode Operation with Internal Ramp Compensation

Implementing peak current mode control operating at a 65 or 100-kHz switching frequency, the NCP1239 offers a fixed internal compensation ramp that can easily by summed up to the sensed current. The controller can be used in CCM applications with wide input voltage range thanks to its fixed ramp compensation that prevents the appearance of sub-harmonic oscillations

Internal Brown-Out Protection

A portion of the bulk voltage is internally sensed via the high-voltage pin monitoring (pin 8). When the voltage on this pin is too low, the part stops pulsing. No re-start attempt is made until the controller senses that the voltage is back within its normal range. When the brown-out comparator senses the voltage is acceptable, de-latch occurs and the controller authorizes a re-start synchronized with $V_{CC(on)}$.

Adjustable Overpower Compensation

The high input voltage sensed on the HV pin is converted into a current. This current builds an offset superimposed on the current sense voltage which is proportional to the input voltage. By choosing the resistance value in series with the CS pin, the amount of compensation can be adjusted to the application.

High-Voltage Start-Up

Low standby power results cannot be obtained with the classical resistive start-up network. In this part, a high-voltage current-source provides the necessary current at start-up and turns off afterwards. An option is available to activate the Dynamic Self−Supply (DSS). The start−up current source is turned on to supply the controller if the Vcc voltage drops below a certain level in light load.

EMI Jittering

An internal low-frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).

Frequency Foldback Capability

A continuous flow of pulses is not compatible with no-load/light-load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.9 V, the oscillator starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback level reaches 1.5 V, the frequency hits its lower stop at 26 kHz. When the feedback pin goes further down and reaches 1.0 V, the peak current setpoint is internally frozen. Below this point, if the power continues to drop, the controller enters classical skip-cycle mode at a 31% frozen peak current.

Internal Soft-Start

A soft-start precludes the main power switch from being stressed upon start-up. In this controller, the soft-start is internally fixed to 8 ms. Soft-start is activated when a new start-up sequence occurs or during an auto-recovery hiccup.

Fault Input

The NCP1239 includes a dedicated fault input accessible via its fault pin (pin 1). It can be used to sense an over-voltage condition on the adapter. The circuit can be latched off by pulling the pin above the upper fault threshold, $V_{FAULT(OVP)}$, typically 3.0 V. The controller is also disabled if the fault pin voltage, V_{FAULT}, is pulled below the lower fault threshold, $V_{FAULT(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an over-temperature fault (by the means of an NTC).

OVP Protection on V_{CC}

It is sometimes interesting to implement a circuit protection by sensing the V_{CC} level. This is what this controller does by monitoring its V_{CC} pin. When the voltage on this pin exceeds $V_{cc(ovp)}$ threshold, the pulses are immediately stopped and the part enters in an endless hiccup or auto-recovery mode depending on controller options.

Short-Circuit/Overload Protection

Short-circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8-V maximum peak current limit is activated, an error flag is asserted and a time period starts, thanks to the 64-ms timer. When the fault is validated, all pulses are stopped and the controller enters an auto-recovery burst mode, with a soft-start sequence at the beginning of each cycle. An internal timer keeps the pulses off for 1 s typically which, associated to the 64-ms pulsing re-try period, ensures a duty-cycle in fault mode less than 10%, independent from the line level. As soon as the fault disappears, the SMPS resumes operation. Please note that some version offers an auto-recovery mode as we just described, some do not and latch off in case of a short-circuit.

HV CURRENT SOURCE PIN

The NCP1239 HV circuitry provides three features:

- Start-Up Current Source to Charge the V_{CC} Capacitor at Power On
- Brown-Out Protection: when the HV Pin Voltage is below $V_{BO(off)}$ for the 68-ms Blanking Time (136 ms for G version), the NCP1239 Stops Operating and Recovers whenthe HV Pin Voltage Exceeds $V_{BO(on)}$
- Over Power Protection: HV Pin Voltage is Sensed to Determine the Amount of OPP Current Flowing Out the CS Pin

The HV pin can be connected either to the bulk capacitor or to the input line terminals through a diode. It is further recommended to implement one or two resistors (in the range of 2.2 kΩ) to reduce the noise that can be picked-up by the HV pin.

START-UP SEQUENCE

The start-up time of a power supply largely depends on the time necessary to charge the V_{CC} capacitor to the controller start-up threshold ($V_{CC(on)}$ which is 12 V typically). The NCP1239 high-voltage current-source provides the necessary current for a prompt start-up and turns off afterwards. The delivered current (I_{START1}) is reduced to less than 0.5 mA when the V_{CC} voltage is below $V_{CC(inhibit)}$ (1.2 V typically). This feature reduces the die stress if the V_{CC} pin happens to be accidentally grounded. When V_{CC} exceeds $V_{CC(inhibit)}$, a 3-mA current (I_{START2}) is provided and charges the V_{CC} capacitor. Please note that the internal IC consumption is increased from few μA to 310 μA (ICC4) when V_{CC} crosses $V_{CC(min)}$ in order to have internal logic wake-up when V_{CC} reaches $V_{CC(on)}$.

The V_{CC} charging time is then the total of the three following durations:

- Charge from 0 V to $V_{CC(inhibit)}$:

$$t_{START1} = \frac{V_{CC(inhibit)} \cdot C_{V_{CC}}}{I_{START1} - ICC5} \quad \text{(eq. 1)}$$

- Charge from $V_{CC(inhibit)}$ to $V_{CC(min)}$:

$$t_{START2} = \frac{\left(V_{CC(min)} - V_{CC(inhibit)}\right) \cdot C_{V_{CC}}}{I_{START2} - ICC5} \quad \text{(eq. 2)}$$

- Charge from $V_{CC(min)}$ to $V_{CC(on)}$:

$$t_{START3} = \frac{\left(V_{CC(on)} - V_{CC(min)}\right) \cdot C_{V_{CC}}}{I_{START2} - ICC4} \quad \text{(eq. 3)}$$

Assuming a 22-μF V_{CC} capacitor is selected and replacing I_{START1}, I_{START2}, ICC4, ICC5, $V_{CC(inhibit)}$ and $V_{CC(on)}$ by their typical values, it comes:

$$t_{START1} = \frac{12 \cdot 22\,u}{500\,u - 20\,u} = 55\ ms \quad \text{(eq. 4)}$$

$$t_{START2} = \frac{(10 - 1.2) \cdot 22\,u}{3\,m - 20\,u} = 65\ ms \quad \text{(eq. 5)}$$

$$t_{START3} = \frac{(12 - 10) \cdot 22\,u}{3\,m - 310\,u} = 16\ ms \quad \text{(eq. 6)}$$

$$t_{START} = t_{START1} + t_{START2} + t_{START3} = 136\ ms \quad \text{(eq. 7)}$$

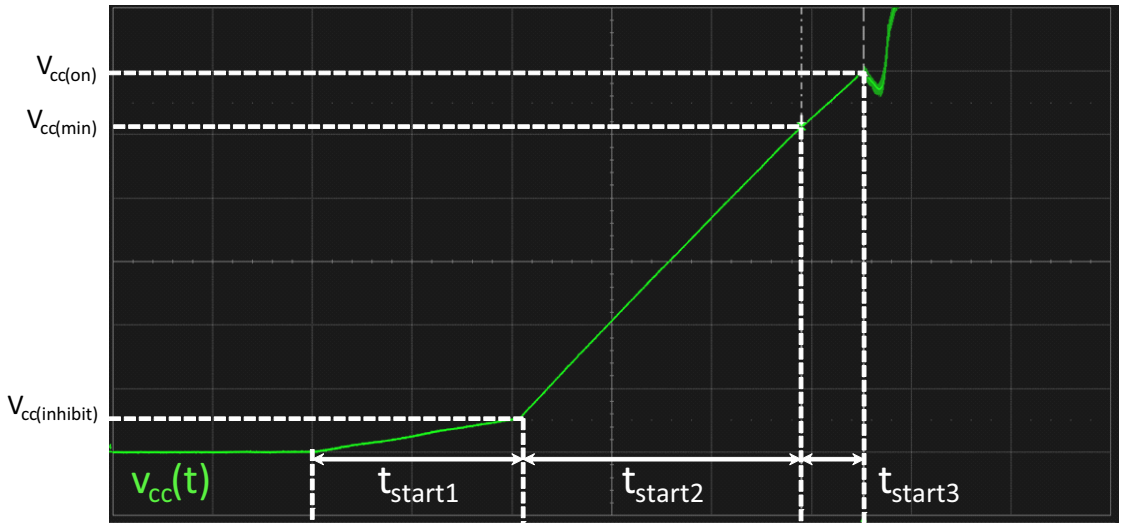


Figure 33. The V_{CC} at Start-Up is Made of Two Segments Given the Short-Circuit Protection Implemented on the HV Source

If the V_{CC} capacitor is first dimensioned to supply the controller for the traditional 5 to 50 ms until the auxiliary winding takes over, no-load standby requirements usually cause it to be larger. The HV start-up current source is then a key feature since it allows keeping short start-up times with large V_{CC} capacitors (the total start-up sequence duration is often required to be less than 1 s).

When the DSS mode is enable (NCP1239JD65), the V_{CC} voltage is maintained between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start−up current source on and off. This function can be used only during transient load or in light load condition. The HV current source cannot supply the controller in Fixed−frequency operation otherwise the die will overheat. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

BROWN-OUT CIRCUITRY

For the vast majority of controllers, input line sensing is performed via a resistive network monitoring the bulk voltage or the incoming ac signal. When in the quest of low standby power, the external network adds a consumption burden and deteriorates the power supply standby power performance. Owing to its proprietary high-voltage technology, ON Semiconductor now offers onboard line sensing without using an external network. The system includes a 90-MΩ resistive network that brings a minimum start-up threshold and an auto-recovery brown-out protection. Both levels are independent from the input voltage ripple. The brown-out thresholds are fixed (see levels in the electrical characteristics table), but they are designed to fit most of standard ac-dc converter applications. The simplified internal schematic appears in Figure 34 while typical operating waveforms are drawn in Figure 35 and Figure 36.

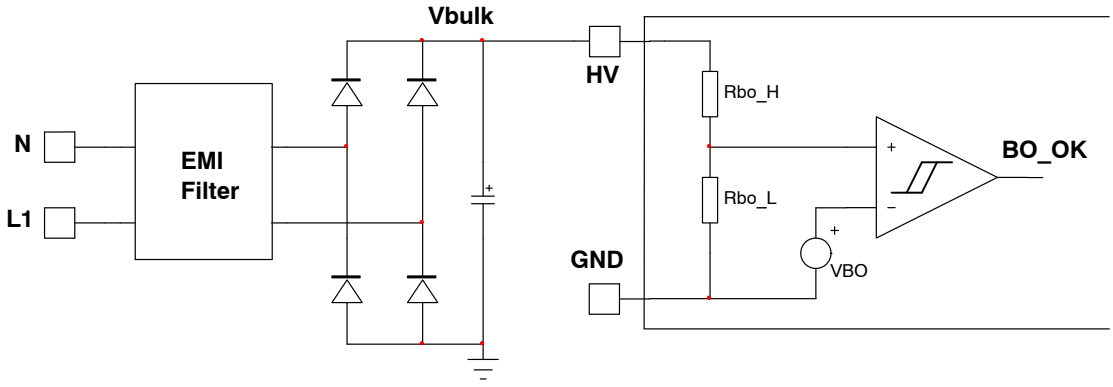


Figure 34. A Simplified View of the Brown-Out Circuitry

When the HV pin voltage drops below the $V_{BO(off)}$ threshold, the brown-out protection trips: the controller stops generating DRV pulses once the BO timer elapses. V_{CC} is discharged to $V_{CC(min)}$ by the controller consumption itself. When this level is reached, the HV current source is activated to lifts V_{CC} up again. At new $V_{CC(on)}$, BO signal is again sensed. If $V_{HV} > V_{BO(on)}$, the parts restarts. If the condition is not met, no drive pulse is delivered and internal IC consumption brings V_{CC} down again. As a result, V_{CC} operates in hiccup mode during a BO event.

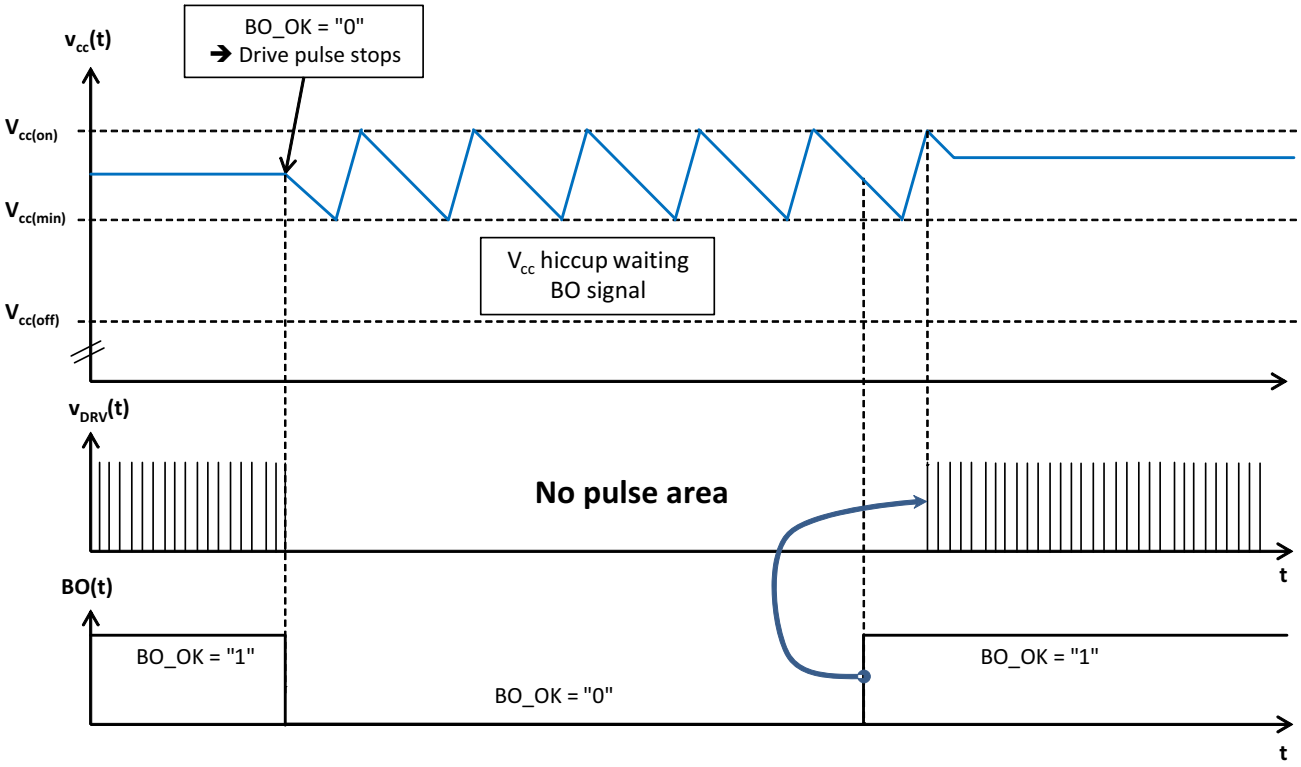


Figure 35. BO Event during Normal Operation

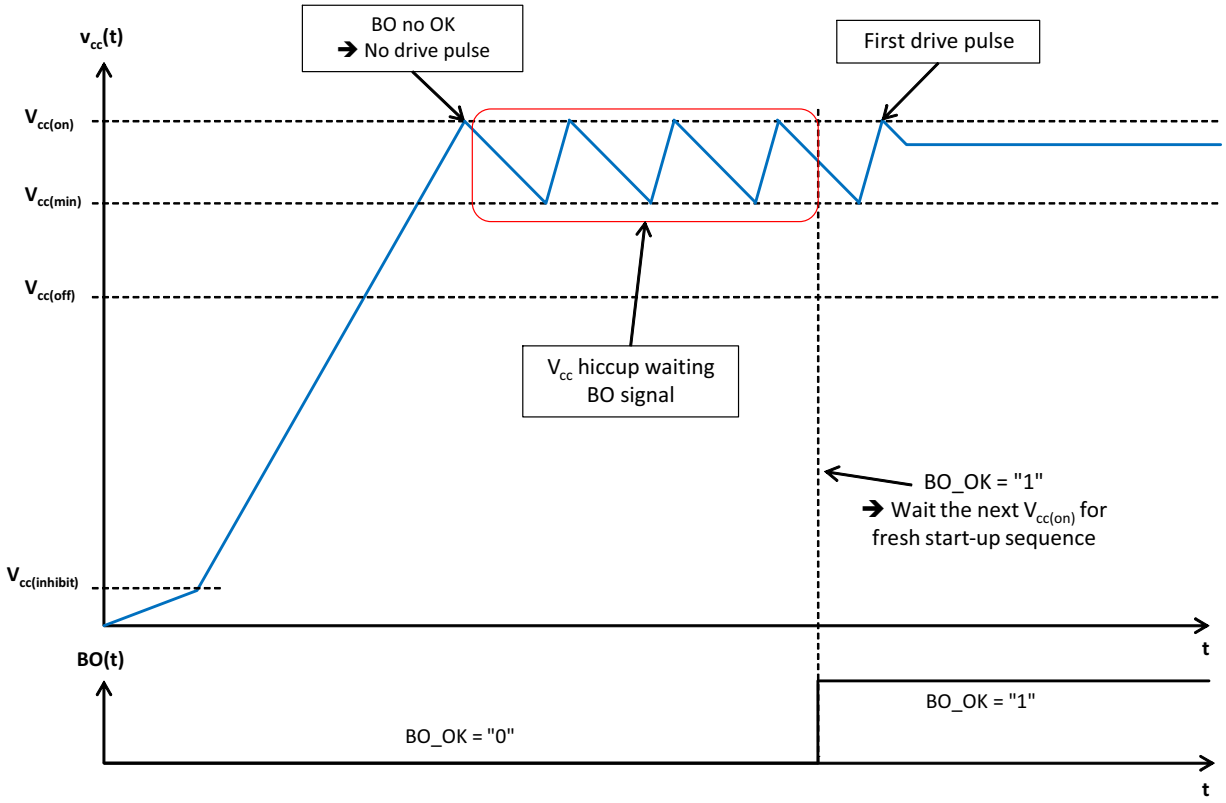


Figure 36. BO Event before Start-Up

OVER POWER PROTECTION

Over Power Protection (OPP) is a known means to limit the output power runaway at high mains. Several elements such as propagation delays and operating mode explain why a converter operated at high line delivers more power than at low line. NCP1239 senses the input voltage via HV pin. This line voltage is transformed into a current information further applied to the current sense pin (CS). A resistor placed in series from the sense resistor to the CS pin will create an offset voltage proportional to the input voltage variation. An added current sink will ensure a zero OPP current at low line (125 V dc), leaving the converter power capability intact in the lowest operating voltage. Figure 37 presents the internal simplified architecture of this OPP circuitry.

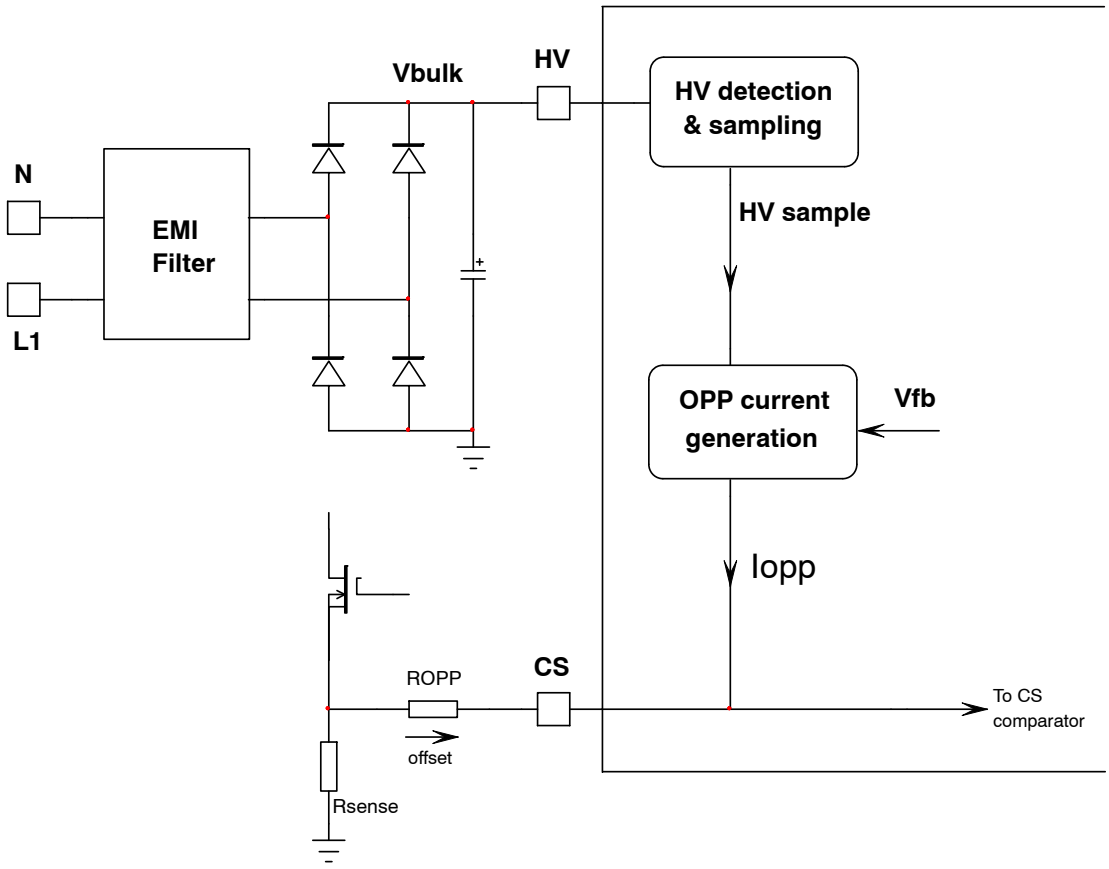


Figure 37. Over Power Protection is Provided via the Bulk Voltage Present on HV Pin

The HV voltage will be transformed into a current equal to 67.5 µA when the HV pin is biased to 125 V. However, there is an internal fixed sink of 67.5 µA. Therefore, the net current flowing into R_{OPP} is 0 at this low-voltage input (≤ 125 V dc), ensuring an almost non-compensated converter at low line: at a 115-V rms input (162 V dc), the current from the OTA block will induce a 87.5-µA current, turning into a 20-µA offset current flowing into R_{OPP}. Now, assume a 260-V rms input voltage (365 V dc), the controller will generate an offset current of:

$$365 \cdot 0.54\,u - 67.5\,u = 130\,\mu A \qquad \text{(eq. 8)}$$

Assume we need to reduce the maximum peak current setpoint by 250 mV to limit the maximum power at the considered 260-V rms input. In that case, we will need to generate a 250-mV offset across R_{OPP}. With a 130-µA current, R_{OPP} should be equal to:

$$\frac{250\,m}{130\,u} = 192\,k\Omega \qquad \text{(eq. 9)}$$

A small 100−220-pF capacitor closely connected between the CS and GND pins will form an effective noise filter and nicely improves the converter immunity. Now, with this 1.92-kΩ resistance, the low-line 20-µA offset current will incur a 38-mV drop, which, in relationship to a 800-mV maximum peak, generates a small 5% reduction. Assuming a full DCM operation, the power would be reduced by 0.95^2 or 9.75% only. Please note that the OPP current is clamped for a HV pin voltage greater than 365 V dc. Should you lift the pin above this voltage, there will be no increase of the OPP current.

The offset voltage can affect the standby power performance by reducing the peak current setpoint in light-load conditions. For this reason, it is desirable to cancel

its action as soon as frequency folback occurs. A typical curve variation is shown in Figure 38. At low power, below the frequency folback starting point, 100% of the OPP current is internally absorbed and no offset is created through the CS pin. When feedback increases again and reaches the frequency foldback point, as the frequency goes up, OPP starts to build up and reaches its full value at V_{FOLD} + 0.7 V.

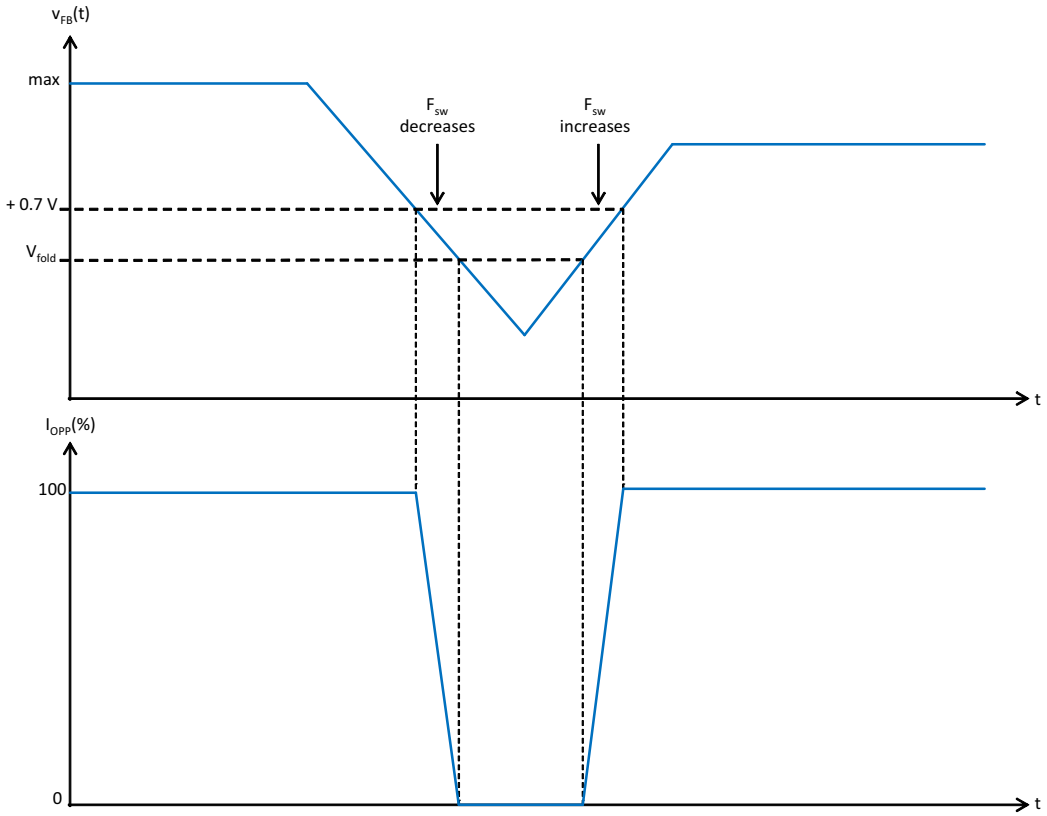


Figure 38. The OPP Current is Applied when the Feedback Voltage Exceeds the Folback Point. It is 0 below it

FAULT INPUT

The NCP1239 includes a dedicated fault input accessible via the fault pin. Figure 39 shows the architecture of the fault input. The controller can be latched by pulling up the pin above the upper fault threshold, $V_{FAULT(OVP)}$, typically 3.0 V. An active clamp prevents the Fault pin voltage from reaching the $V_{FAULT(OVP)}$ if the pin is open. To reach the upper threshold, the external pull-up current has to be higher than the pull-down capability of the clamp.

$$\frac{V_{FAULT(OVP)} - V_{FAULT(clamp)}}{R_{FAULT(clamp)}} = \frac{3\ V - 1.35\ V}{1.35\ k\Omega}, \qquad \text{(eq. 10)}$$

i.e. approximately 1.2 mA

This function is typically used to detect a V_{CC} or auxiliary winding over-voltage by means of a Zener diode generally in series with a small resistor (see Figure 39).

Neglecting the resistor voltage drop, the OVP threshold is then:

$$V_{AUX(OVP)} = V_Z + V_{FAULT(OVP)} \qquad \text{(eq. 11)}$$

where V_Z is the Zener diode Voltage.

The controller can also be latched off if the fault pin voltage, V_{FAULT}, is pulled below the lower fault threshold, $V_{FAULT(OTP)}$, typically 0.4 V. This capability is normally used for detecting an over-temperature fault by means of an NTC thermistor. A pull up current source I_{OTP}, (typically 45 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{FAULT(OTP)}$.

The circuit detects an over-temperature situation when:

$$R_{NTC} \cdot I_{OTP} = V_{FAULT(OTP)} \qquad \text{(eq. 12)}$$

Hence, the OTP protection trips when

$$R_{NTC} = \frac{V_{FAULT(OTP)}}{I_{OTP}} = 8.9\ k\Omega\ \text{(Typically)} \qquad \text{(eq. 13)}$$

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{FAULT(OTP)}$. This current source is enabled once V_{CC} reaches $V_{CC(min)}$. A bypass capacitor is usually connected between the Fault and GND pins. It will take some time for V_{FAULT} to reach its steady state value once I_{OTP} is enabled. Therefore, the lower fault comparator (i.e. over-temperature detection) is ignored during soft-start. In addition, in order to speed up this fault pin capacitor, OTP current is doubled during the soft-start period.

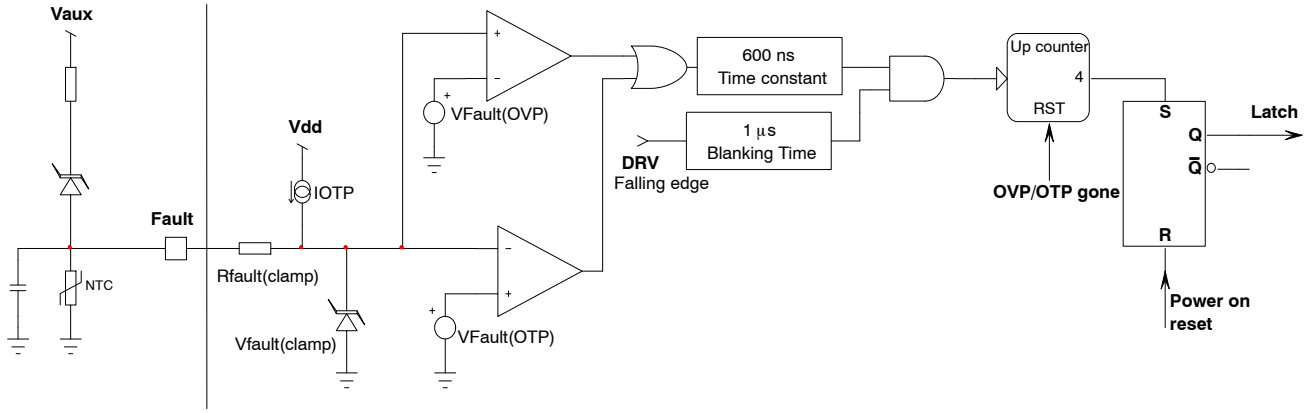


Figure 39. Fault Detection Schematic

As a matter of fact, the controller operates normally while the fault pin voltage is maintained within the upper and lower fault thresholds. Upper and lower fault detectors have blanking delays to prevent noise from triggering them. Both OVP and OTP comparator output are validated only if its high-state duration lasts a minimum of 600 ns. Below this value, the event is ignored. Then, a counter ensures that OVP/OTP events occurred for 4 successive drive clock pulses before actually latching the part.

When the part is latched-off, the drive is immediately turned off and V_{CC} goes in endless hiccup mode. The power supply needs to be un-plugged to reset the part ($V_{CC(reset)}$ or BO event). Please note that this protection on the Fault pin is autorecovery for the E, K, M, P and Q versions.

AUTO-RECOVERY SHORT-CIRCUIT PROTECTION

In case of output short-circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than the timer's programmed value, the driving pulses are stopped and a 1-s auto-recovery timer starts. If V_{CC} voltage is below $V_{CC(min)}$, HV current source is activated to build up the voltage to $V_{CC(on)}$. On the contrary, if V_{CC} voltage is above $V_{CC(min)}$, HV current source is not activated, V_{CC} falls down as the auxiliary pulses are missing and the controller waits that $V_{CC(min)}$ is crossed to enable the stat-up current source. During the timer count down, the controller purposely ignores the re-start when V_{CC} crosses $V_{CC(on)}$ and waits for another V_{CC} cycle. By lowering the duty cycle in fault condition, it naturally reduces the average input power and the rms current in the output cable. Illustration of such principle appears in Figure 40. Please note that soft-start is activated upon re-start attempt.

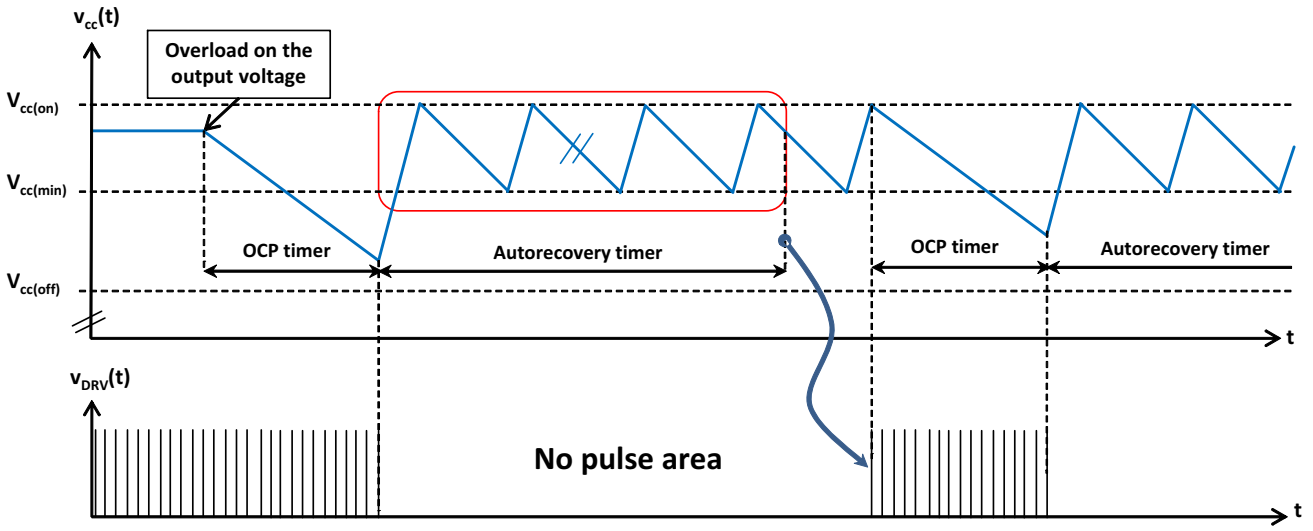


Figure 40. An Auto-Recovery Hiccup Mode is Entered in Case a Faulty Event Longer than 64 ms is Acknowledged by the Controller

The hiccup is operating regardless of the brown-out level. However, when the internal comparator toggles indicating that the controller recovers from a brown-out situation (the input line was ok, then too low and back again to normal), the hiccup is interrupted and the controller re-starts to the next available $V_{CC(on)}$. Figure 41 displays the resulting waveform: the controller is protecting the converter against an overload. The mains suddenly went down, and then back again at a normal level. Right at this moment, the hiccup logic receives a reset signal and ignores the next hiccup to immediately initiate a re-start signal.

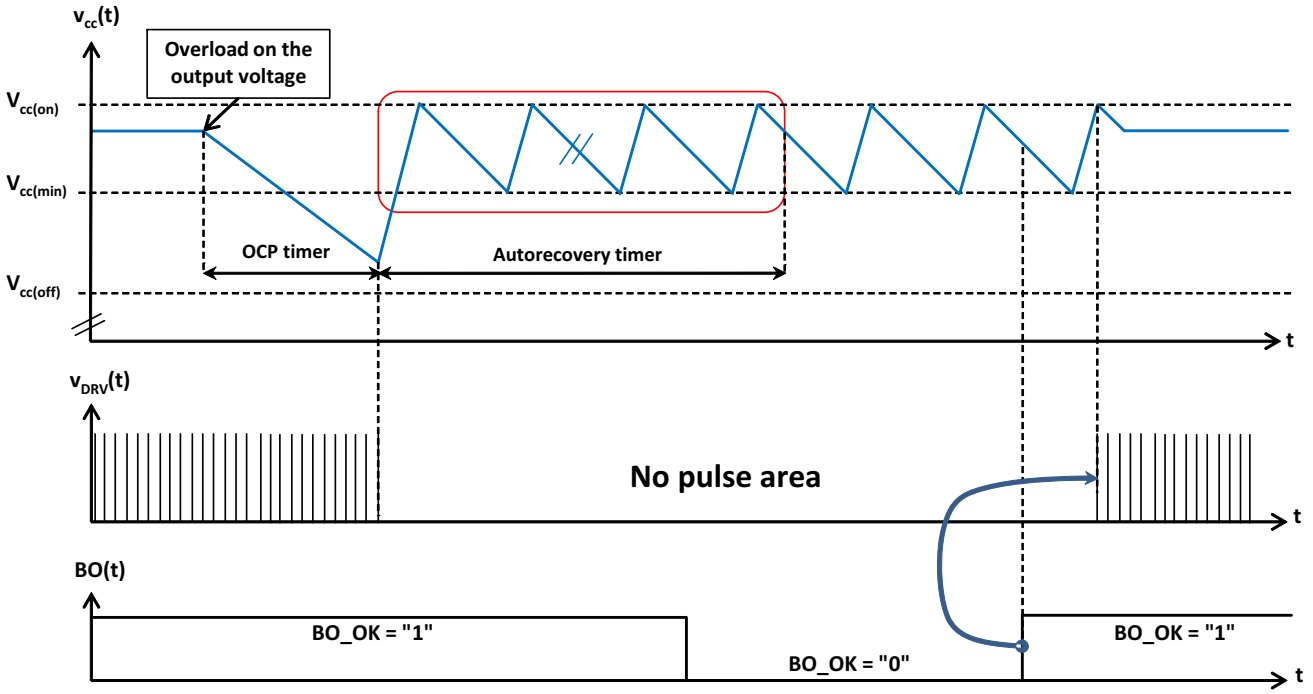


Figure 41. BO Event in Auto-Recovery or Latch Mode

LATCHED SHORT CIRCUIT PROTECTION WITH PRE-SHORT

In some applications, the controller must be fully latched in case of an output short circuit presence. When the error flag is asserted, meaning the controller is asked to deliver its full peak current, upon timer completion, the controller latches off: all pulses are immediately stopped and V_{CC} hiccups between the two levels, $V_{CC(on)}$ and $V_{CC(min)}$. However, in presence of a small V_{CC} capacitor, it can very well be the case where the stored energy does not give enough time to let the timer elapse before V_{CC} touches the $V_{CC(off)}$. When this happens, the latch is not acknowledged since the timer countdown has been prematurely aborted. To avoid this problem, NCP1239 combines the error flag assertion together with the UVLO flag: upon start up, as maximum power is asked to increase V_{OUT}, the error flag is temporarily raised until regulation is met. If during the time the flag is raised an UVLO event is detected, the part latches off immediately. When latched, V_{CC} hiccups between the two levels, $V_{CC(on)}$ and $V_{CC(min)}$ until a reset occurs (Brown-out event or V_{CC} cycled down below $V_{CC(reset)}$). In normal operation, if a UVLO event is detected for any reason while the error flag is not asserted, the controller will naturally resume operations. Please also note that this pre-short protection is activated only during start-up sequence. In normal operation, even if an UVLO event occurs while the error flag is asserted, the controller will enters in auto-recovery mode. Details of this behavior are given in Figure 42.

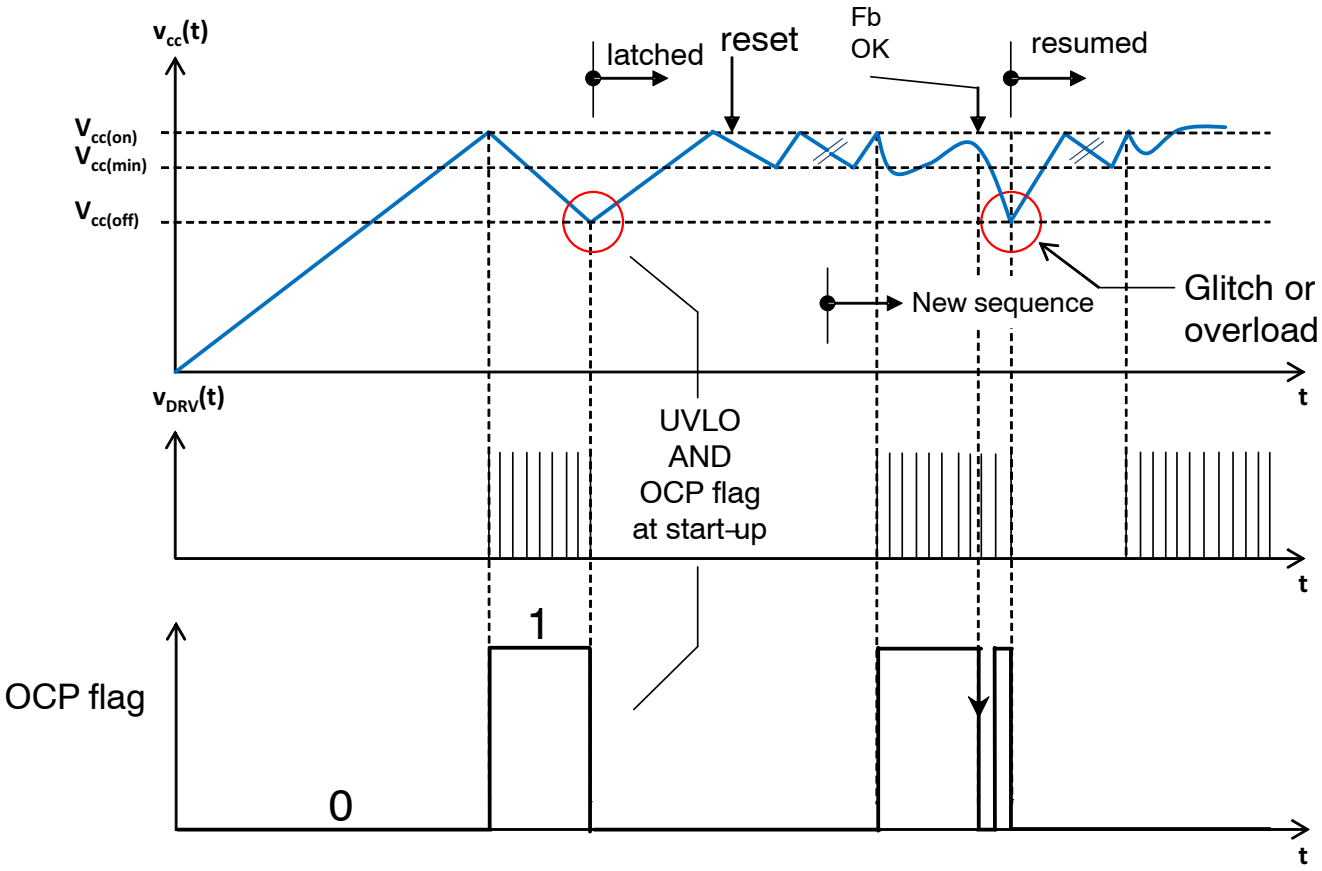


Figure 42. UVLO Event during Start-Up Sequence and in Normal Operation

LATCHING OR AUTO-RECOVERY MODE

The B, C, D, E, K, L, M, N, P, Q and R versions are auto-recovery. When an overload fault is detected, they stop generating drive pulses and V_{CC} hiccups between $V_{CC(min)}$ and $V_{CC(on)}$ during the auto-recovery timer before initiate a fresh start-up sequence with soft-start.

The A, F, G, H, I and J versions latch off when they detect an overload situation. In this condition, the circuit stops generating drive pulses and let V_{CC} drop down. When V_{CC} has reached 10-$V_{CC(min)}$ level, the circuit charged up V_{CC} to $V_{CC(on)}$. The controller enters in an endless hiccup mode. The device cannot recover operation until V_{CC} drops below $V_{CC(reset)}$ or brownout recovery signal is applied. Practically, the power supply must be unplugged to be reset ($V_{CC} < V_{CC(reset)}$). Please note that the controller always enters in auto-recovery mode when the UVLO event occurs without internal error flag signal (ie: without overload).

FREQUENCY FOLDBACK

The reduction of no-load standby power associated with the need for improving the efficiency, requires to change the traditional fixed-frequency type of operation. This controller implements a switching frequency folback when the feedback voltage passes below a certain level, V_{FOLD}, set at 1.9 V. At this point, the oscillator turns into a Voltage-Controlled Oscillator (VCO) and reduces switching frequency down to a feedback voltage of 1.5 V where switching frequency is 26 kHz typically. Below 1.5 V, the frequency is fixed and cannot go further down. The peak current setpoint is free to follow the feedback voltage from 3.2 V (full power) down to 1 V. At 1 V, as both frequency and peak current are frozen (250 mV or ≈31% of the maximum 0.8-V setpoint) the only way to further reduce the transmitted power is to enter skip cycle. This is what happens when the feedback voltage drops below 0.8 V typically. Figure 43 depicts the adopted scheme for the part.

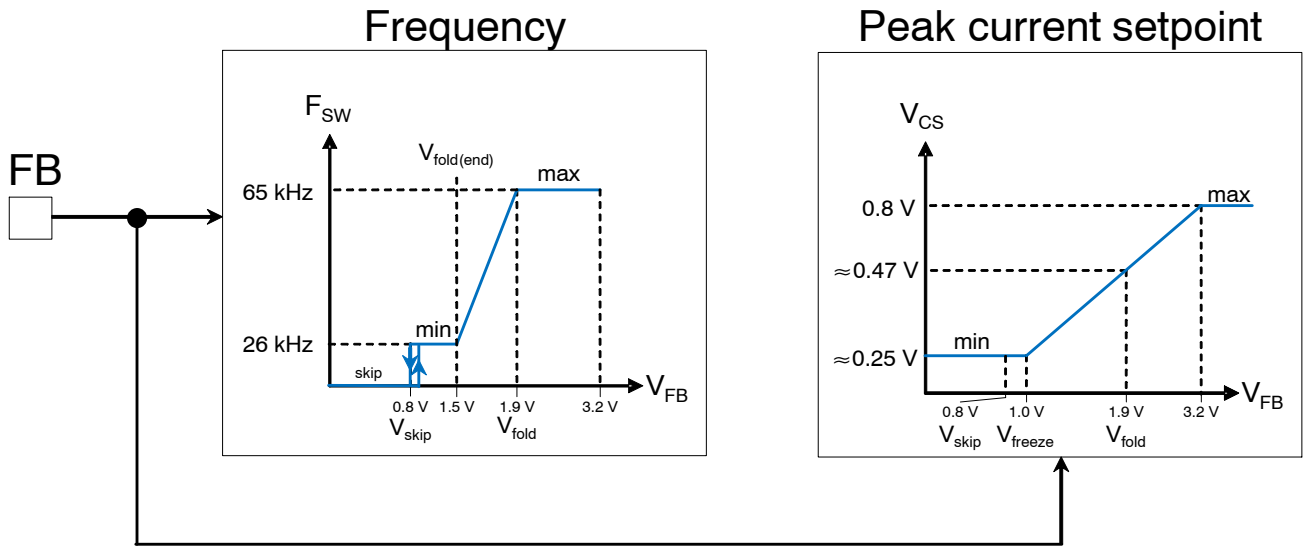


Figure 43. By Observing the Voltage on the Feedback Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

SLOPE COMPENSATION

Slope compensation is a known means to fight sub-harmonic oscillations in peak-current mode controlled power converters (flyback in our case). By adding an artificial ramp to the current sense information or subtracting it from the feedback voltage, you implement slope compensation. How much compensation do you need? The simplest way is to consider the primary-side inductor downslope and apply 50% of its value for slope compensation. For instance, assume a 65-kHz/19-V output flyback converter whose transformer turns ratio 1:N is 1:0.25. The primary inductor is 600 µH. As such, assuming a 1-V forward drop of the output rectifier, the downslope is evaluated to:

$$S_{OFF} = \frac{V_{OUT} + V_f}{NL_p} = \frac{19 + 1}{0.25 \cdot 600\ u} = \quad \text{(eq. 14)}$$

$$= 133\ kA/s \text{ or } 133\ mA/\mu s$$

If we have a 0.33-Ω sense resistor, then the current downslope turns into a voltage downslope whose value is simply:

$$S'_{OFF} = S_{OFF} \cdot R_{SENSE} = \quad \text{(eq. 15)}$$

$$= 133\ m \cdot 0.33 \approx 44\ mV/\mu s$$

50% of this value is 22 mV/µs. The internal slope compensation level is typically 29 mV/µs (for the 65-kHz version) so it will nicely compensate this design example. What if my converter is under compensated? You can still add compensation ramp via a simple *RC* arrangement showed in Figure 44. Please look at AND8029 available from www.onsemi.com regarding calculation details of this configuration.

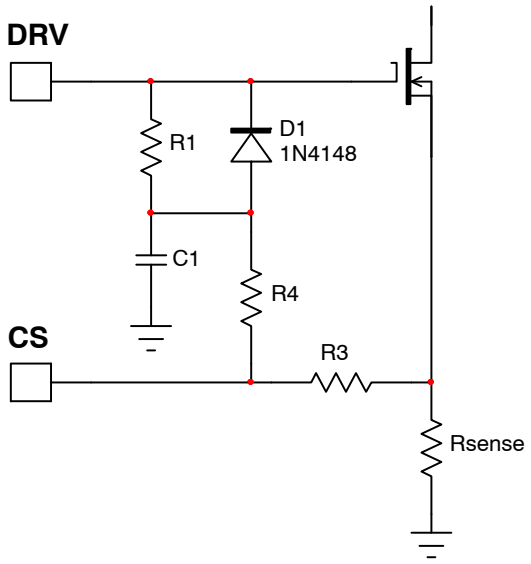


Figure 44. An Easy Means to Add Slope Compensation is by Using an Extra *RC* Network Building a Ramp from the Drive Signal

A 2ND OVER-CURRENT COMPARATOR FOR ABNORMAL OVER-CURRENT FAULT DETECTION

A severe fault like a winding short-circuit can cause the switch current to increase very rapidly during the on-time. The current sense signal significantly exceeds V_{ILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the power switch current can become huge causing system damage.

The NCP1239 protects against this fault by adding an additional comparator for abnormal over-current fault detection. The current sense signal is blanked with a shorter LEB duration, t_{LEB2}, typically 120 ns, before applying it to the abnormal over-current fault comparator. The voltage threshold of the comparator, V_{ILIM2}, typically 1.2 V, is set 50 % higher than V_{LIMIT1}, to avoid interference with normal operation. Four consecutive abnormal over-current faults cause the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Over-Current Comparator.

Please note that abnormal over−current fault is following the timer−based short−circuit protection behavior (auto−recovery or latching off).

OVER-VOLTAGE PROTECTION ON V_{CC} PIN

The NCP1239 hosts a dedicated comparator on the V_{CC} pin. When the voltage on this pin exceeds 25.5 V typically (32.0 V for F, J, M and N versions) for more than 20 μs, a signal is sent to the internal latch and the controller immediately stops the driving pulses while remaining in a lockout state. Depending controller options, this OVP on V_{CC} pin can be auto-recovery or latched. For latching-off versions, the part can be reset by cycling down its V_{CC}, for instance by pulling off the power plug but also if a brown-out recovery is sensed by the controller. This technique offers a simple and cheap means to protect the converter against optocoupler.

PROTECTING FROM A FAILURE OF THE CURRENT SENSING

A 1-μA (typically) pull-up current source, I_{CS}, pulls up the CS pin to disable the controller if the pin is left open.

In addition the maximum duty ratio limit (80% typically) avoids that the MOSFET stays permanently on if the switch current cannot reach the setpoint when for instance, the input voltage is low or if the CS pin is grounded. In this case, the OCP timer is activated. If the timer elapses, the controller enters in auto-recovery or endless hiccup mode depending on the controller option. This unexpected operation can lead to deep CCM with destructive consequences.

SOFT-START

Soft-start is achieved by ramping up an internal reference, V_{SSTART}, and comparing it to current sense signal. V_{SSTART} ramps up from 0 V once the controller powers up. The setpoint rise is then limited by the V_{SSTART} ramp so that a gradual increase of the power switch current during start-up. The soft-start duration (that is, the time necessary for the ramp to reach the V_{ILIM1} steady state current limit), t_{SSTART}, is typically 8 ms.

DRIVER

The NCP1239 maximum supply voltage, $V_{CC(max)}$, is 25.5 V (32.0 V for F and J versions). Typical high-voltage MOSFETs have a maximum gate-source voltage rating of 20 V. The DRV pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$ is typically 13.5 V with a maximum limit of 16 V.

THERMAL SHUTDOWN

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 20°C.

The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$ or a brown-out fault is detected. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

Table 5. ORDERING INFORMATION

Device	Marking	Freq.	OCP Protection	V_{CC} OVP Protection	Fault Pin Protection	BO Levels	Package	Shipping†
NCP1239AD65R2G	1239A065	65 kHz	Latch	Latch	Latch	110/101	SOIC−7 (Pb-Free)	2500 / Tape & Reel
NCP1239BD65R2G	1239B065	65 kHz	Auto-Recovery	Latch	Latch	110/101		
NCP1239CD65R2G	1239C065	65 kHz	Auto-Recovery	Auto-Recovery	Latch	110/101		
NCP1239DD65R2G	1239D065	65 kHz	Auto-Recovery	Latch	Latch	101/95		
NCP1239ED65R2G	1239E065	65 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	110/101		
NCP1239FD65R2G	1239F065	65 kHz	Latch	Latch	Latch	229/176		
NCP1239HD65R2G	1239H065	65 kHz	Latch	Latch	Latch	229/224		
NCP1239ID65R2G	1239I065	65 kHz	Latch	Latch	Latch	101/95		
NCP1239JD65R2G	1239J065	65 kHz	Latch	Latch	Latch	101/95		
NCP1239KD65R2G	1239K065	65 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	110/101		
NCP1239LD65R2G	1239L065	65 kHz	Auto-Recovery	Latch	Latch	82/77		
NCP1239MD65R2G	1239M065	65 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	229/224		
NCP1239ND65R2G	1239N065	65 kHz	Auto-Recovery	Auto-Recovery	Latch	229/224		
NCP1239PD65R2G	1239P065	65 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	82/79		
NCP1239QD65R2G	1239Q065	65 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	82/79		
NCP1239RD65R2G	1239R065	65 kHz	Auto-Recovery	Latch	Latch	101/95		
NCP1239AD100R2G	1239A100	100 kHz	Latch	Latch	Latch	110/101		
NCP1239BD100R2G	1239B100	100 kHz	Auto-Recovery	Latch	Latch	110/101		
NCP1239DD100R2G	1239D100	100 kHz	Auto-Recovery	Latch	Latch	110/95		
NCP1239ED100R2G	1239E100	100 kHz	Auto-Recovery	Auto-Recovery	Auto-Recovery	110/101		
NCP1239GD100R2G	1239G100	100 kHz	Latch	Latch	Latch	95/86		
NCP1239LD100R2G	1239L100	100 kHz	Auto-Recovery	Latch	Latch	82/77		

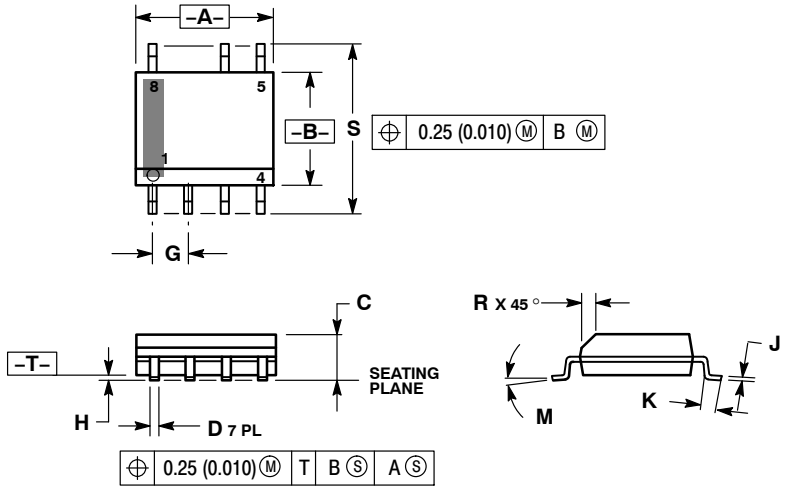
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−7
CASE 751U
ISSUE E

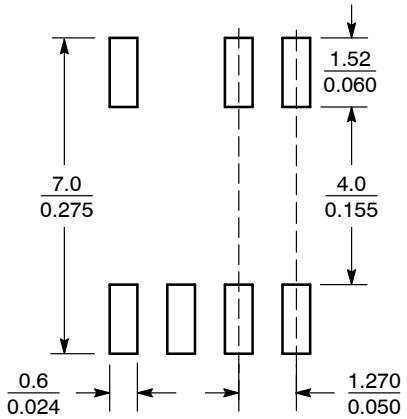
DATE 20 OCT 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

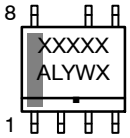
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−7
CASE 751U
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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