



**THE DATASHEET OF
DAC7612UB/2K5G4**





DAC7612

Dual, 12-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 3.7mW
- **FAST SETTling:** 7 μ s to 1 LSB
- **1mV LSB WITH 4.095V FULL-SCALE RANGE**
- **COMPLETE WITH REFERENCE**
- **12-BIT LINEARITY AND MONOTONICITY OVER INDUSTRIAL TEMP RANGE**
- **3-WIRE INTERFACE:** Up to 20MHz Clock
- **SMALL PACKAGE:** 8-Lead SOIC

APPLICATIONS

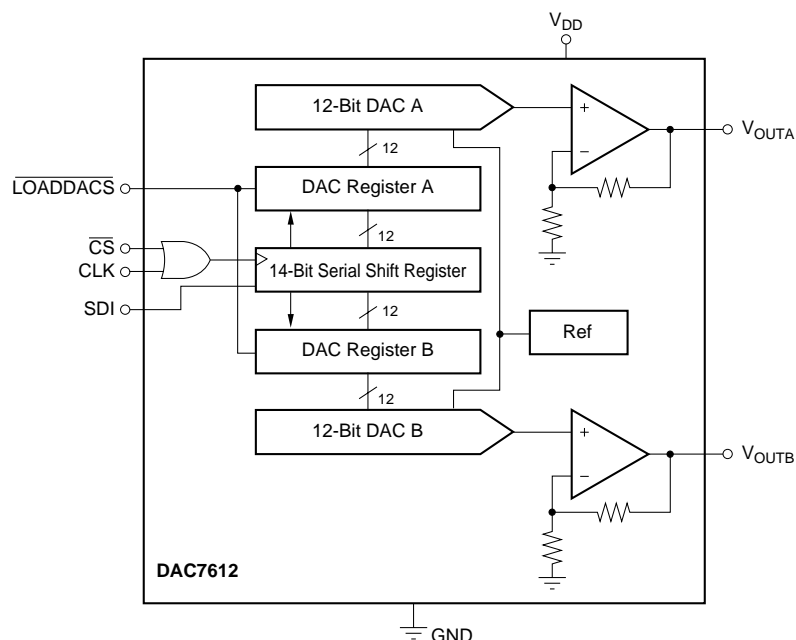
- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **CLOSED-LOOP SERVO-CONTROL**
- **PC PERIPHERALS**
- **PORTABLE INSTRUMENTATION**

DESCRIPTION

The DAC7612 is a dual, 12-bit digital-to-analog converter (DAC) with guaranteed 12-bit monotonicity performance over the industrial temperature range. It requires a single +5V supply and contains an input shift register, latch, 2.435V reference, a dual DAC, and high speed rail-to-rail output amplifiers. For a full-scale step, each output will settle to 1 LSB within 7 μ s while only consuming 3.7mW.

The synchronous serial interface is compatible with a wide variety of DSPs and microcontrollers. Clock (CLK), Serial Data In (SDI), Chip Select (\overline{CS}) and Load DACs (LOADDACs) comprise the serial interface.

The DAC7612 is available in an 8-lead SOIC package and is fully specified over the industrial temperature range of -40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, and $V_{DD} = +5\text{V}$, unless otherwise noted.

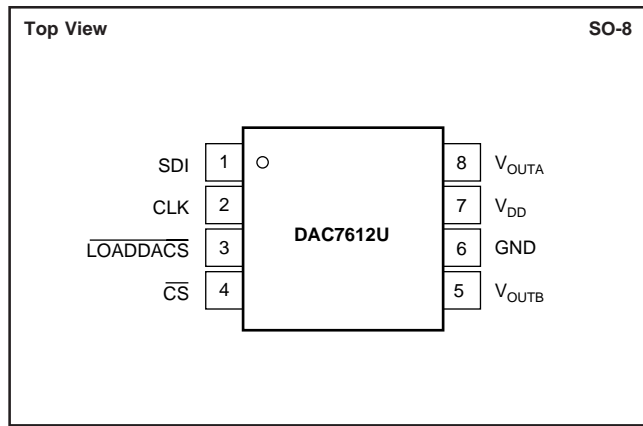
PARAMETER	CONDITIONS	DAC7612U			DAC7612UB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
RESOLUTION		12			*			Bits	
ACCURACY									
Relative Accuracy ⁽¹⁾	Guaranteed Monotonic Code 000 _H Code 000 _H Code FFF _H Code FFF _H	-2	±1/2	+2	-1	±1/4	+1	LSB	
Differential Nonlinearity		-1	±1/2	+1	-1	±1/4	+1	LSB	
Zero-Scale Error		-1	+1	+3	*	*	*	LSB	
Zero Scale Match		1/2				1/2	2	LSB	
Full-Scale Voltage		4.079	4.095	4.111	4.087	4.095	4.103	V	
Full-Scale Match		1/2				1/2	2	LSB	
ANALOG OUTPUT									
Output Current	Code 800 _H	±5	±7		*	*		mA	
Load Regulation	$R_{LOAD} \geq 402\Omega$, Code 800 _H		1	3		*		LSB	
Capacitive Load	No Oscillation		500			*		pF	
Short-Circuit Current			±15			*		mA	
Short-Circuit Duration	GND or V_{DD}		Indefinite			*			
DIGITAL INPUT									
Data Format	Serial Straight Binary CMOS					*			
Data Coding						*			
Logic Family						*			
Logic Levels									
V_{IH}		0.7 • V_{DD}			0.3 • V_{DD}	*			V
V_{IL}					±10		*		V
I_{IH}				±10		*		µA	
I_{IL}						*		µA	
DYNAMIC PERFORMANCE									
Settling Time ⁽²⁾ (t_s)	To ±1 LSB of Final Value		7			*		µs	
DAC Glitch			2.5			*		nV-s	
Digital Feedthrough			0.5			*		nV-s	
POWER SUPPLY									
V_{DD}	$V_{IH} = 5\text{V}$, $V_{IL} = 0\text{V}$, No Load, at Code 000 _H $V_{IH} = 5\text{V}$, $V_{IL} = 0\text{V}$, No Load $\Delta V_{DD} = \pm 5\%$	+4.75	+5.0	+5.25	*	*	*	V	
I_{DD}			0.75	1.5		*	*		mA
Power Dissipation			3.5	7.5		*	*		mW
Power Supply Sensitivity			0.0025	0.002		*	*		%/%
TEMPERATURE RANGE									
Specified Performance		-40		+85	*		*	°C	

* Same specification as for DAC7612U.

NOTES: (1) This term is sometimes referred to as Linearity Error or Integral Nonlinearity (INL). (2) Specification does not apply to negative-going transitions where the final output voltage will be within 3 LSBs of ground. In this region, settling time may be double the value indicated.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	SDI	Serial Data Input. Data is clocked into the internal serial register on the rising edge of CLK.
2	CLK	Synchronous Clock for the Serial Data Input.
3	LOADDACS	Loads the internal DAC registers. All DAC registers are transparent latches and are transparent when LOADDACS is LOW (regardless of the state of CS or CLK).
4	CS	Chip Select. Active LOW.
5	V _{OUTB}	DAC B Output Voltage
6	GND	Ground
7	V _{DD}	Positive Power Supply
8	V _{OUTA}	DAC A Output Voltage

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V _{DD} to GND	-0.3V to 6V
Digital Inputs to GND	-0.3V to V _{DD} + 0.3V
V _{OUT} to GND	-0.3V to V _{DD} + 0.3V
Power Dissipation	325mW
Thermal Resistance, θ_{JA}	150°C/W
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

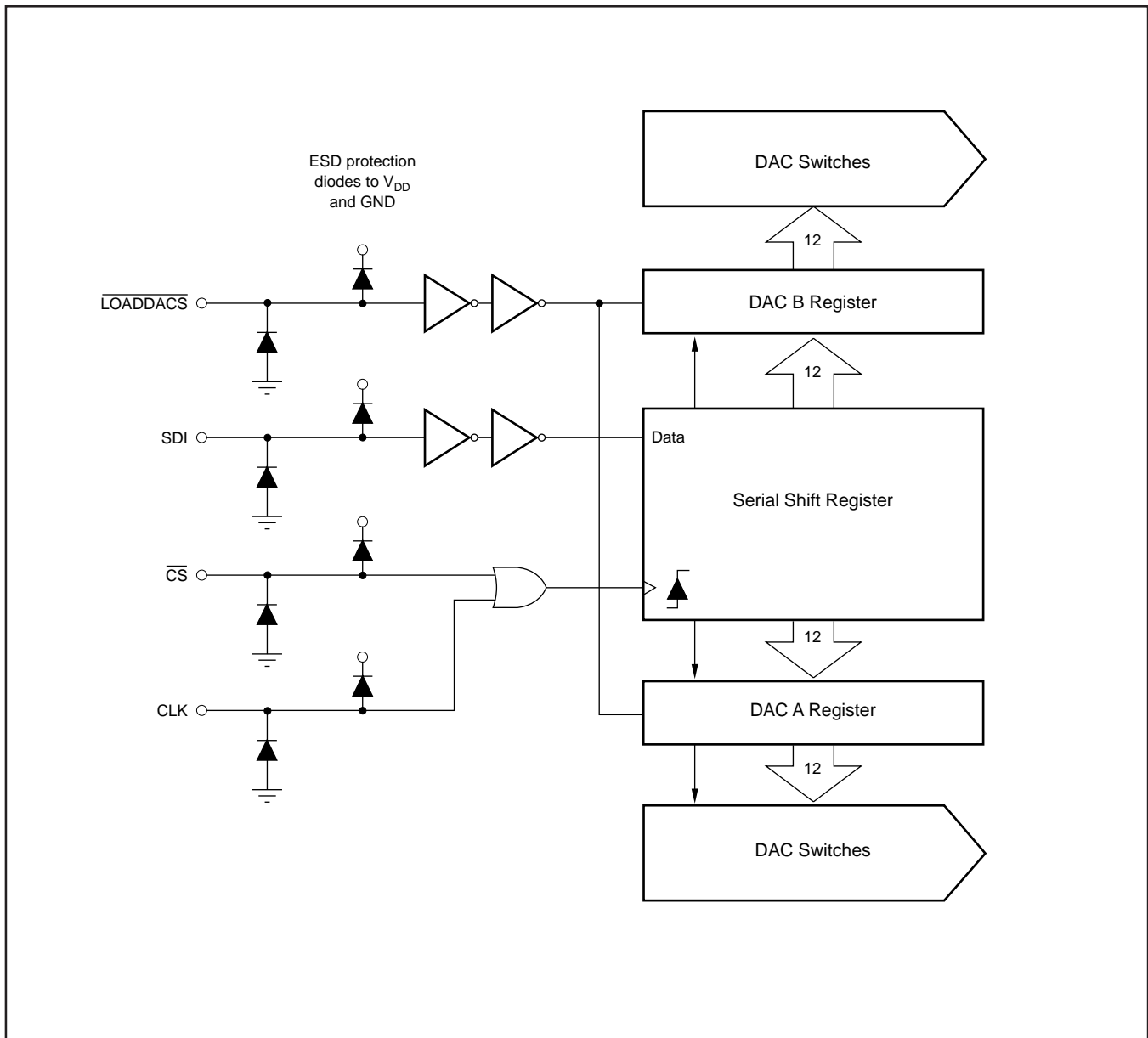
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

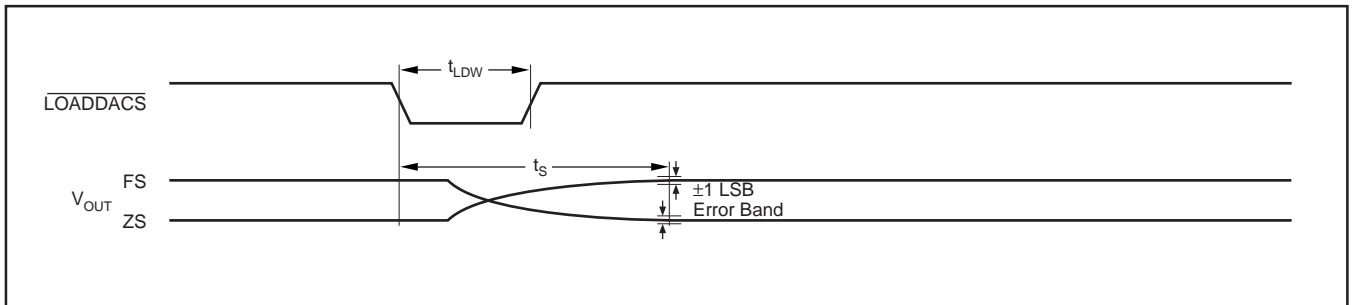
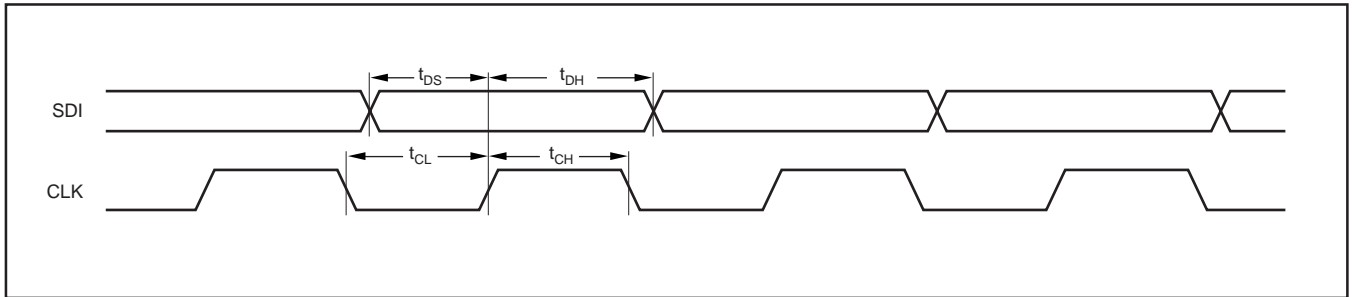
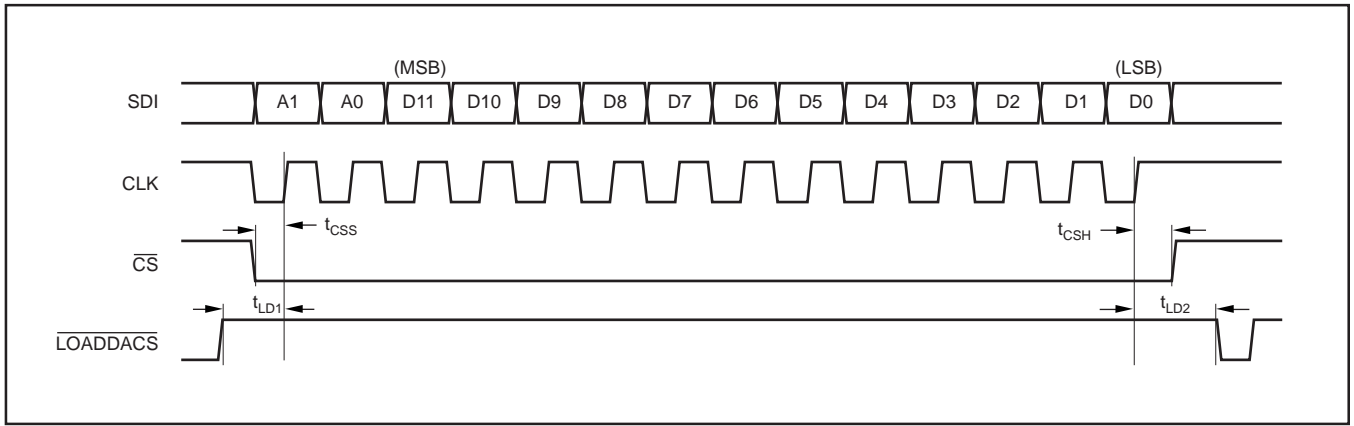
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
DAC7612U	±2	±1	-40°C to +85°C	SO-8	182	DAC7612U	Rails
"	"	"	"	"	"	DAC7612U/2K5	Tape and Reel
DAC7612UB	±1	±1	-40°C to +85°C	SO-8	182	DAC7612UB	Rails
"	"	"	"	"	"	DAC7612UB/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC7612U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

EQUIVALENT INPUT LOGIC



TIMING DIAGRAMS



LOGIC TRUTH TABLE

A1	A0	CLK	\overline{CS}	LOADDACS	SERIAL SHIFT REGISTER	DAC REGISTER A	DAC REGISTER B
X	X	X	H	H	No Change	No Change	No Change
X	X	↑	L	H	Shifts One Bit	No Change	No Change
L	X	X	H ⁽¹⁾	L	No Change	Loads Serial Data Word	Loads Serial Data Word
H	L	X	H	L	No Change	Loads Serial Data Word	No Change
H	H	X	H	L	No Change	No Change	Loads Serial Data Word

↑ Positive Logic Transition; X = Don't Care.

NOTE: (1) A HIGH value is suggested in order to avoid to "false clock" from advancing the shift register and changing the DAC voltage.

DATA INPUT TABLE

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13
A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

TIMING SPECIFICATIONS

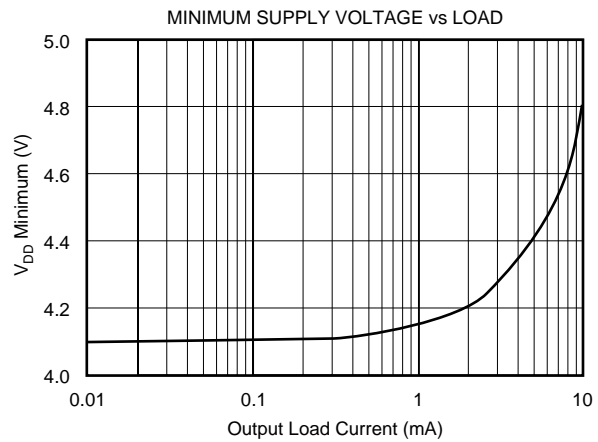
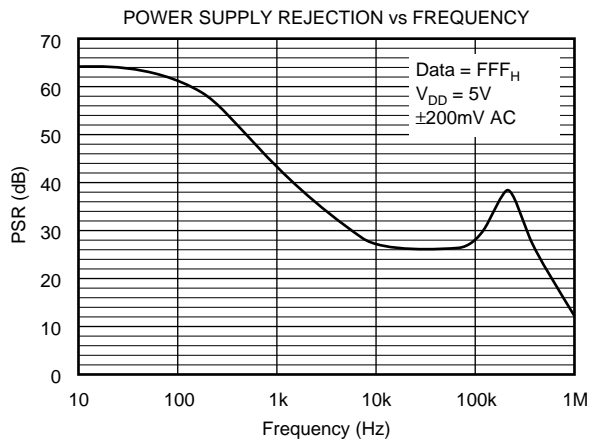
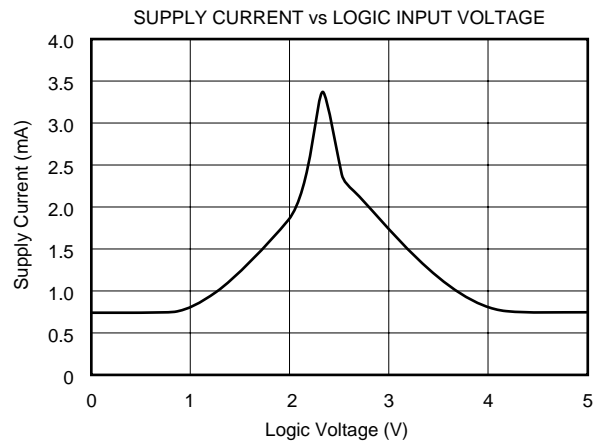
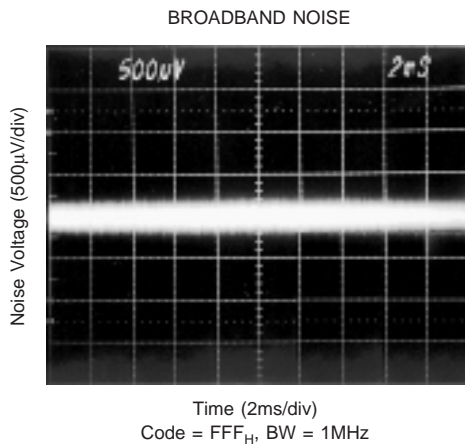
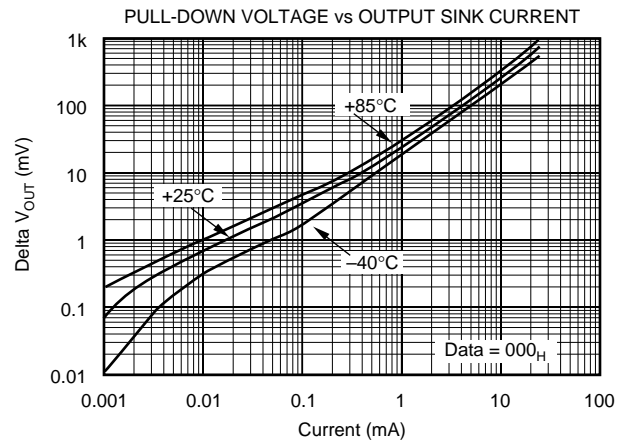
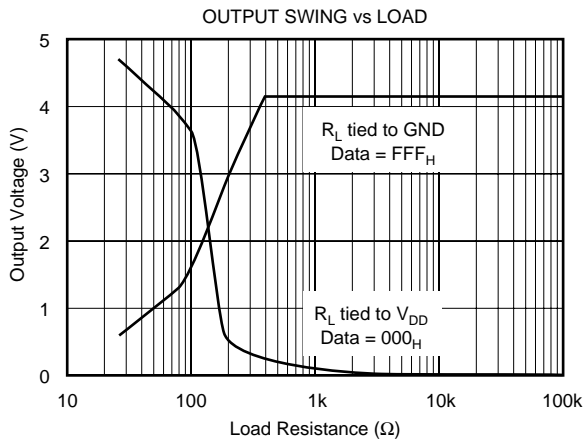
$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and $V_{DD} = +5\text{V}$.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CH}	Clock Width HIGH	30			ns
t_{CL}	Clock Width LOW	30			ns
t_{LDW}	Load Pulse Width	20			ns
t_{DS}	Data Setup	15			ns
t_{DH}	Data Hold	15			ns
t_{LD1}	Load Setup	15			ns
t_{LD2}	Load Hold	10			ns
t_{CSS}	Select	30			ns
t_{CSH}	Deselect	20			ns

NOTE: All input control signals are specified with $t_R = t_F = 5\text{ns}$ (10% to 90% of +5V) and timed from a voltage level of 2.5V. These parameters are guaranteed by design and are not subject to production testing.

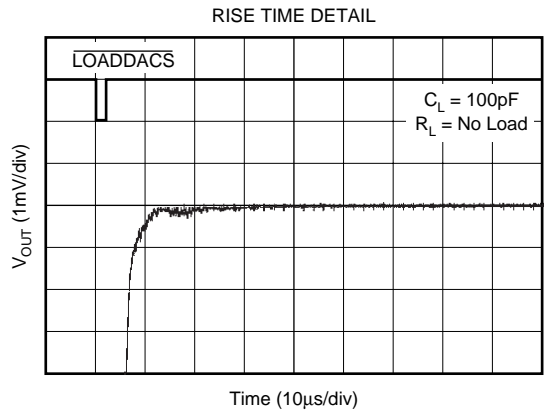
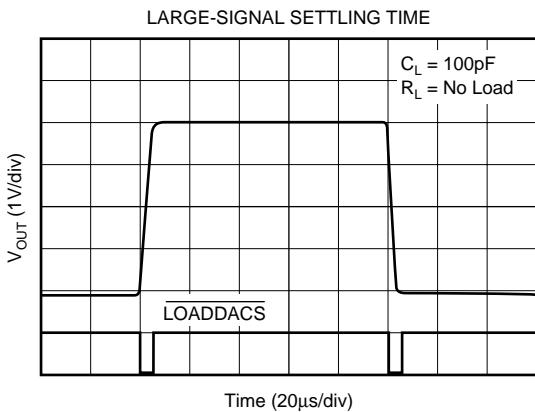
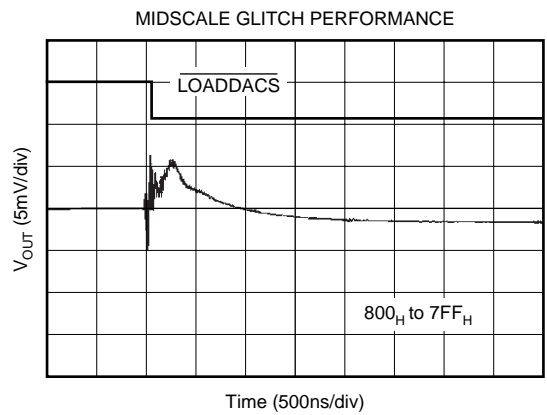
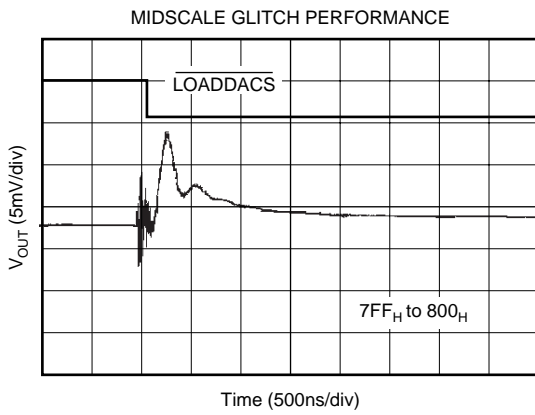
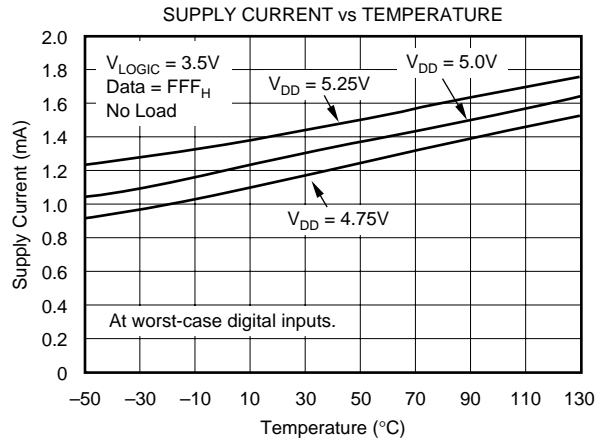
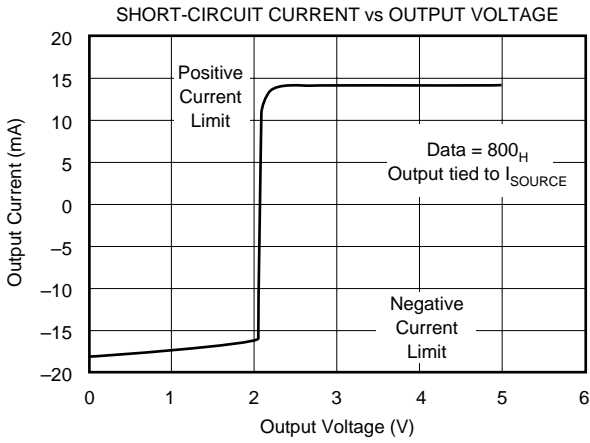
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ$, and $V_{DD} = 5V$, unless otherwise specified.



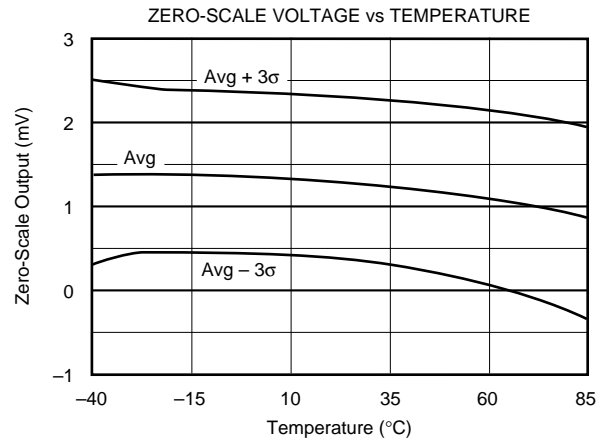
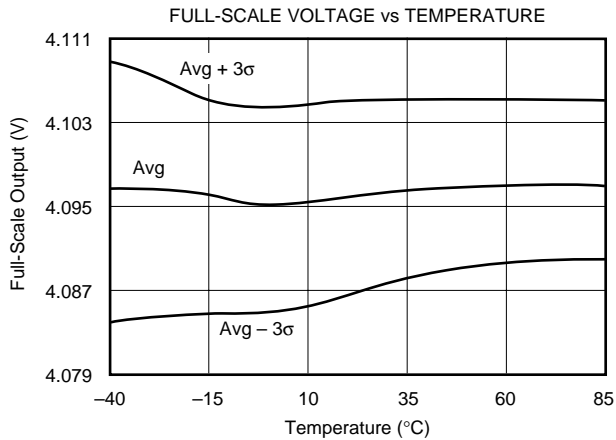
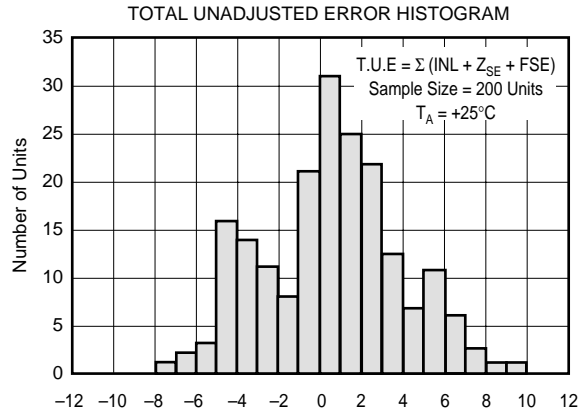
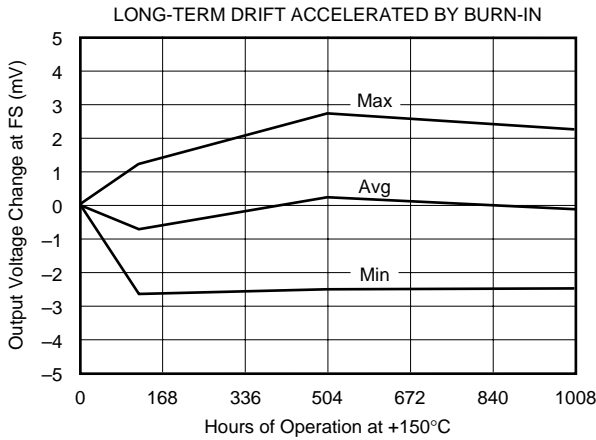
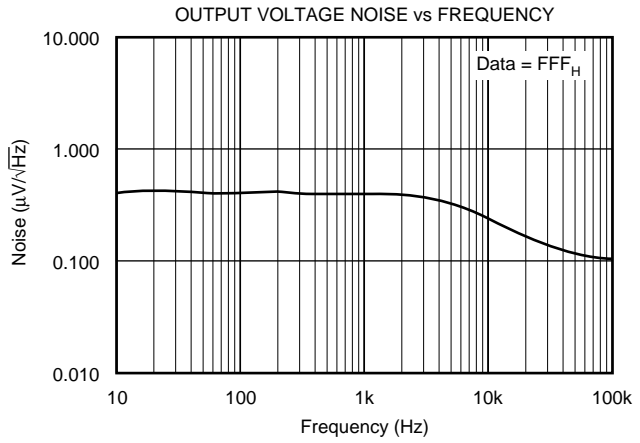
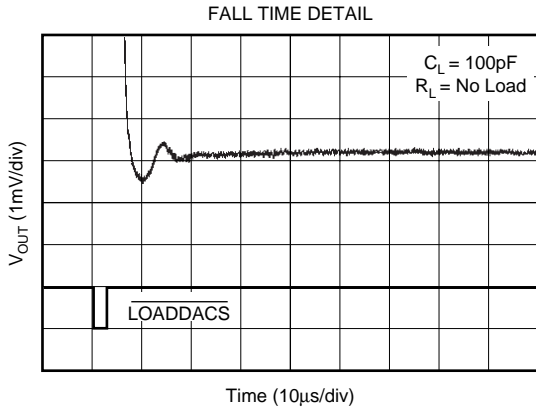
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ$, and $V_{DD} = 5V$, unless otherwise specified.



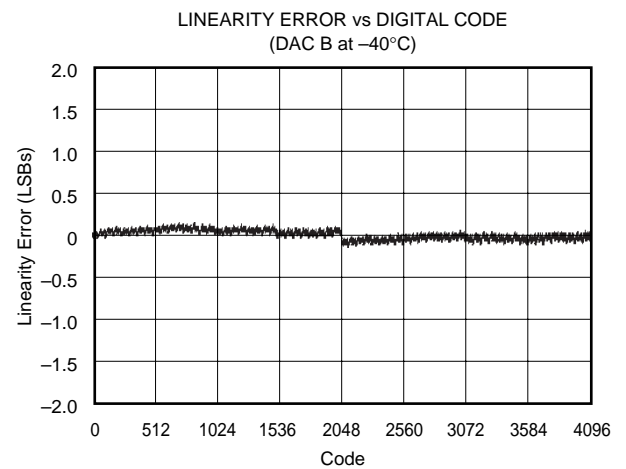
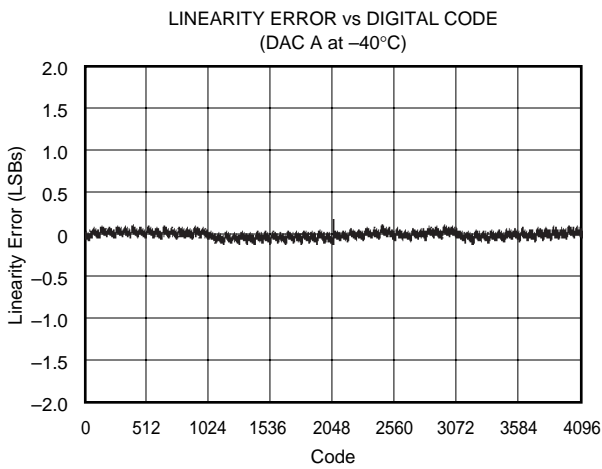
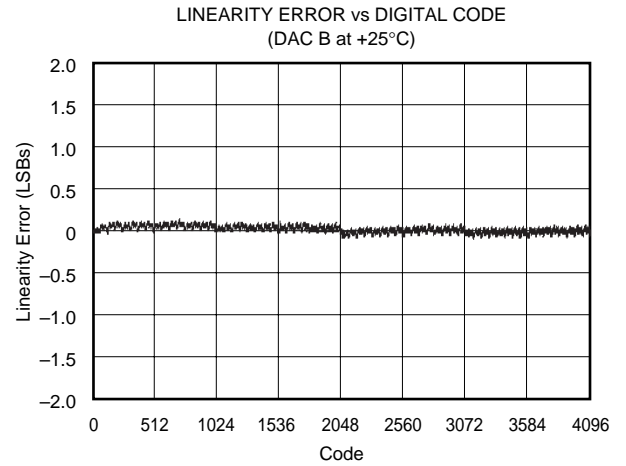
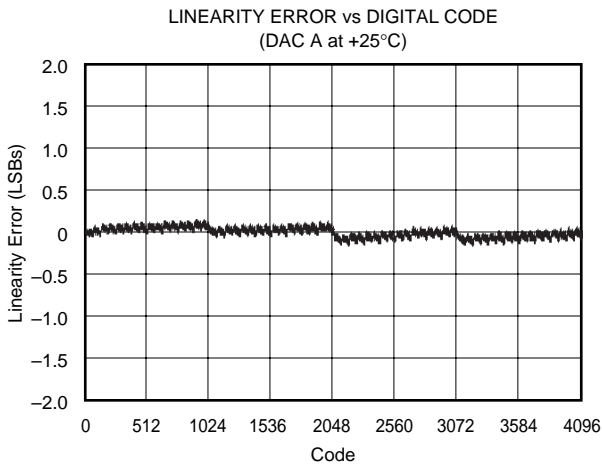
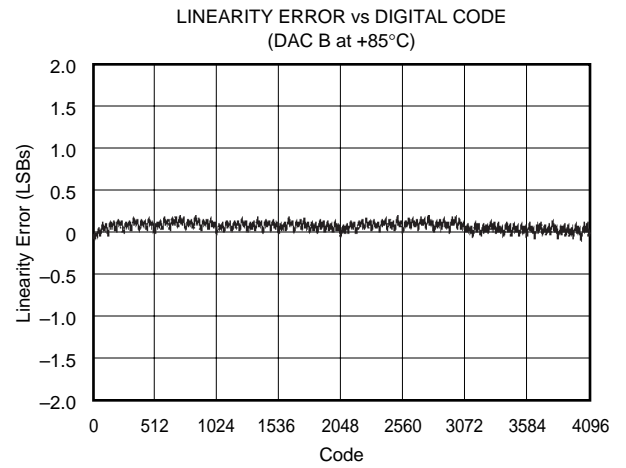
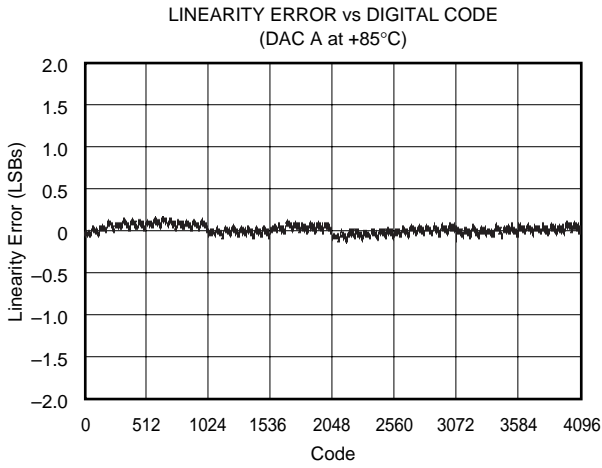
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ$, and $V_{DD} = 5V$, unless otherwise specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ$, and $V_{DD} = 5V$, unless otherwise specified.



OPERATION

The DAC7612 is a dual, 12-bit digital-to-analog converter (DAC) complete with a serial-to-parallel shift register, DAC registers, laser-trimmed 12-bit DACs, on-board reference, and rail-to-rail output amplifiers. Figure 1 shows the basic operation of the DAC7612.

INTERFACE

Figure 1 shows the basic connection between a microcontroller and the DAC7612. The interface consists of a Serial Clock (CLK), Serial Data (SDI), and a Load DAC signal (LOADDACS). In addition, a chip select (\overline{CS}) input is available to enable serial communication when there are multiple serial devices. Loading either DAC A or DAC B is done by shifting 14 serial bits in via the SDI input. The first 2 bits represent the address of the DAC to be updated and the

next 12 bits are the code (MSB-first) sent to the DAC. The data format is Straight Binary and is loaded MSB-first into the shift registers after loading the address bits. Table I shows the relationship between input code and output voltage.

The digital data into the DAC7612 is double-buffered. This means that new data can be entered into the chosen DAC without disturbing the old data and the analog output of the converter. At some point after the data has been entered into the serial shift register, this data can be transferred into the DAC registers. This transfer is accomplished with a HIGH to LOW transition of the $\overline{LOADDACS}$ pin. The $\overline{LOADDACS}$ pin makes the DAC registers transparent. If new data is shifted into the shift register while $\overline{LOADDACS}$ is LOW, the DAC output voltages will change as each new bit is entered. To prevent this, $\overline{LOADDACS}$ must be returned HIGH prior to shifting in new serial data.

DIGITAL-TO-ANALOG CONVERTER

The internal DAC section is a 12-bit voltage output device that swings between ground and the internal reference voltage. The DAC is realized by a laser-trimmed R-2R ladder network which is switched by N-channel MOSFETs. Each DAC output is internally connected to a rail-to-rail output operational amplifier.

OUTPUT AMPLIFIER

A precision, low-power amplifier buffers the output of each DAC section and provides additional gain to achieve a 0V to 4.095V range. Each amplifier has low offset voltage, low

DAC7612 Full-Scale Range = 4.095V Least Significant Bit = 1mV		
DIGITAL INPUT CODE STRAIGHT OFFSETBINARY	ANALOG OUTPUT (V)	DESCRIPTION
FFF _H	+4.095	Full Scale
801 _H	+2.049	Midscale + 1 LSB
800 _H	+2.048	Midscale
7FF _H	+2.047	Midscale - 1 LSB
000 _H	0	Zero Scale

TABLE I. Digital Input Code and Corresponding Ideal Analog Output.

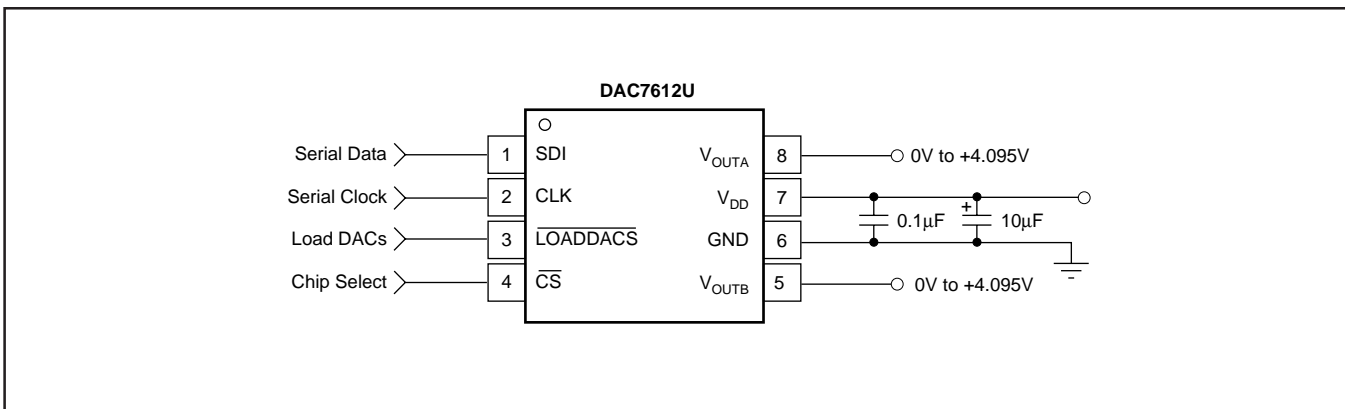


FIGURE 1. Basic Operation of the DAC7612.

noise, and a set gain of 1.682V/V (4.095/2.435). See Figure 2 for an equivalent circuit schematic of the analog portion of the DAC7612.

The output amplifier has a 7 μ s typical settling time to ± 1 LSB of the final value. Note that there are differences in the settling time for negative-going signals versus positive-going signals.

The rail-to-rail output stage of the amplifier provides the full-scale range of 0V to 4.095V while operating on a supply voltage as low as 4.75V. In addition to its ability to drive resistive loads, the amplifier will remain stable while driving capacitive loads of up to 500pF. See Figure 3 for an equivalent circuit schematic of the amplifier's output driver and the Typical Performance Curves section for more information regarding settling time, load driving capability, and output noise.

POWER SUPPLY

A BiCMOS process and careful design of the bipolar and CMOS sections of the DAC7612 result in a very low power device. Bipolar transistors are used where tight matching and low noise are needed to achieve analog accuracy, and CMOS transistors are used for logic, switching functions and for other low power stages.

If power consumption is critical, it is important to keep the logic levels on the digital inputs (SDI, CLK, CS, LOADDACS) as close as possible to either V_{DD} or ground. This will keep the CMOS inputs (see "Supply Current vs Logic Input Voltages" in the Typical Performance Curves) from shunting current between V_{DD} and ground.

The DAC7612 power supply should be bypassed as shown in Figure 1. The bypass capacitors should be placed as close to the device as possible, with the 0.1 μ F capacitor taking priority in this regard. The "Power Supply Rejection vs Frequency" graph in the Typical Performance Curves section shows the PSRR performance of the DAC7612. This should be taken into account when using switching power supplies or DC/DC converters.

In addition to offering guaranteed performance with V_{DD} in the 4.75V to 5.25V range, the DAC7612 will operate with reduced performance down to 4.5V. Operation between 4.5V and 4.75V will result in longer settling time, reduced performance, and current sourcing capability. Consult the " V_{DD} vs Load Current" graph in the Typical Performance Curves section for more information.

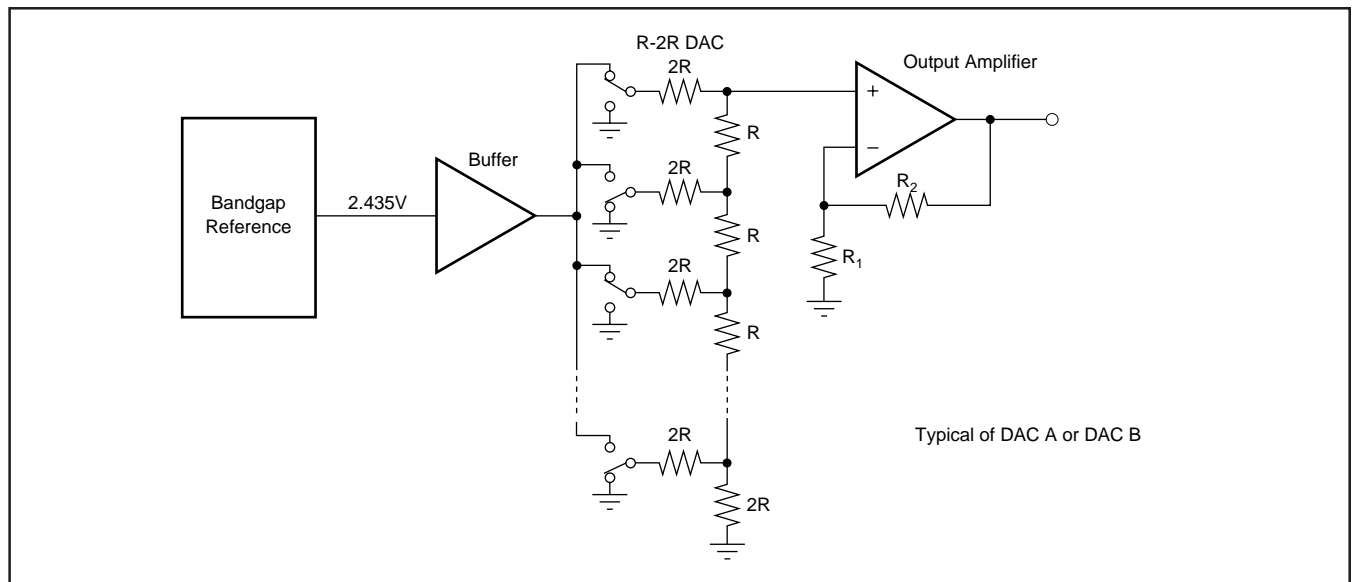


FIGURE 2. Simplified Schematic of Analog Portion.

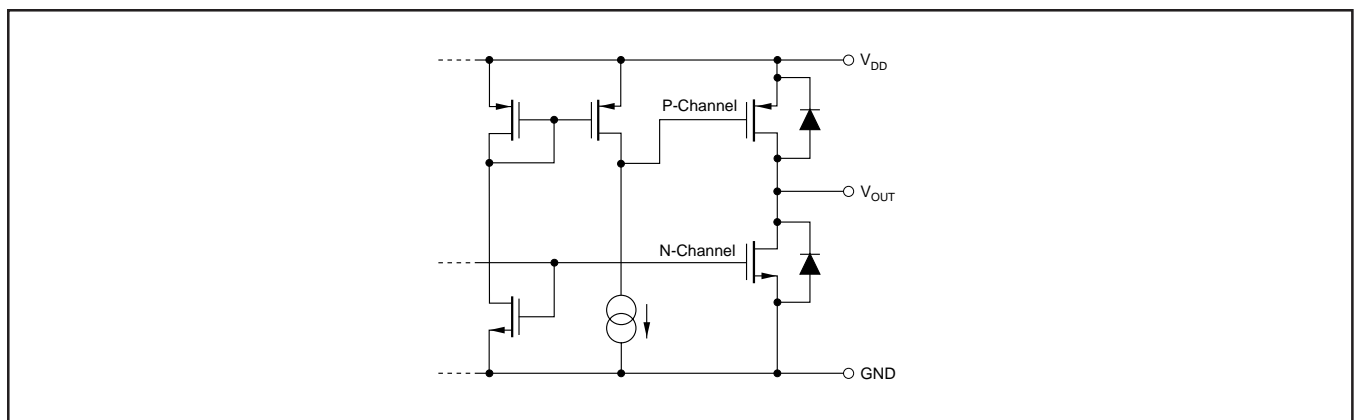


FIGURE 3. Simplified Driver Section of Output Amplifier.

APPLICATIONS

POWER AND GROUNDING

The DAC7612 can be used in a wide variety of situations—from low power, battery operated systems to large-scale industrial process control systems. In addition, some applications require better performance than others, or are particularly sensitive to one or two specific parameters. This diversity makes it difficult to define definite rules to follow concerning the power supply, bypassing, and grounding. The following discussion must be considered in relation to the desired performance and needs of the particular system.

A precision analog component requires careful layout, adequate bypassing, and a clean, well-regulated power supply. As the DAC7612 is a single-supply, +5V component, it will often be used in conjunction with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance.

Because the DAC7612 has a single ground pin, all return currents, including digital and analog return currents, must flow through this pin. The GND pin is also the ground

reference point for the internal bandgap reference. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they are connected at the power entry point of the system (see Figure 4).

The power applied to V_{DD} should be well regulated and low-noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between V_{DD} and V_{OUT} .

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 10 μ F and 0.1 μ F capacitors shown in Figure 4 are strongly recommended and should be installed as close to V_{DD} and ground as possible. In some situations, additional bypassing may be required such as a 100 μ F electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

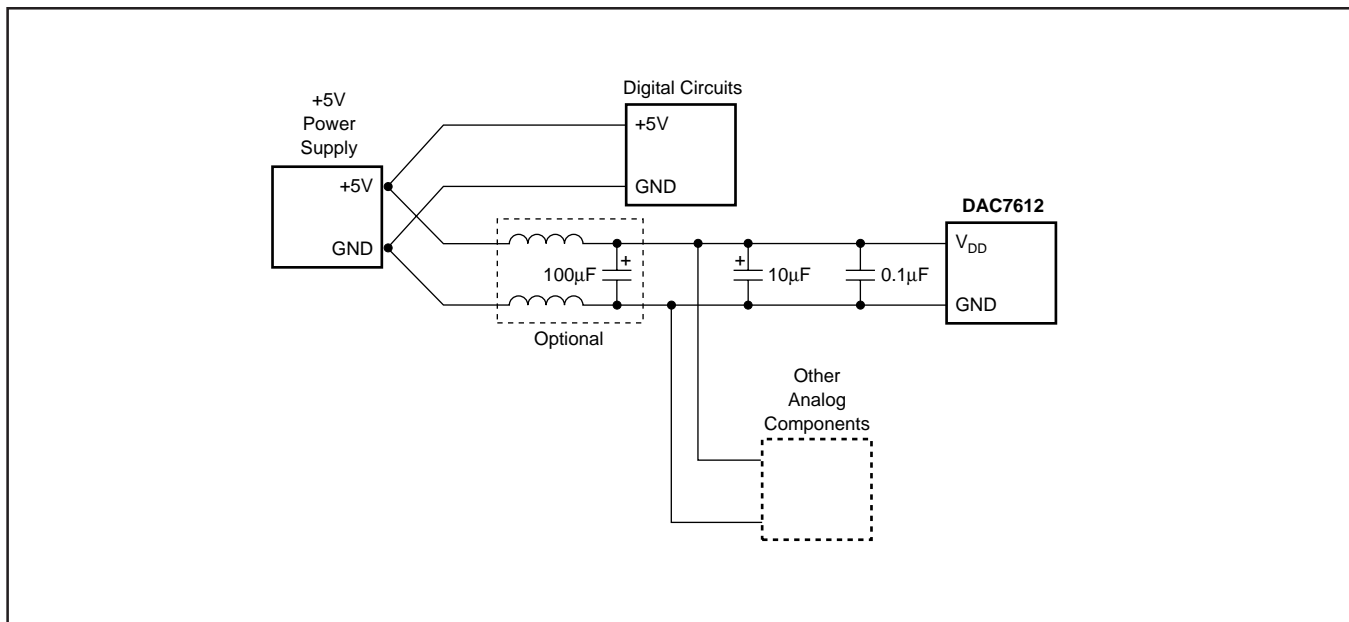


FIGURE 4. Suggested Power and Ground Connections for a DAC7612 Sharing a +5V Supply with a Digital System.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC7612U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612UB/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7612UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

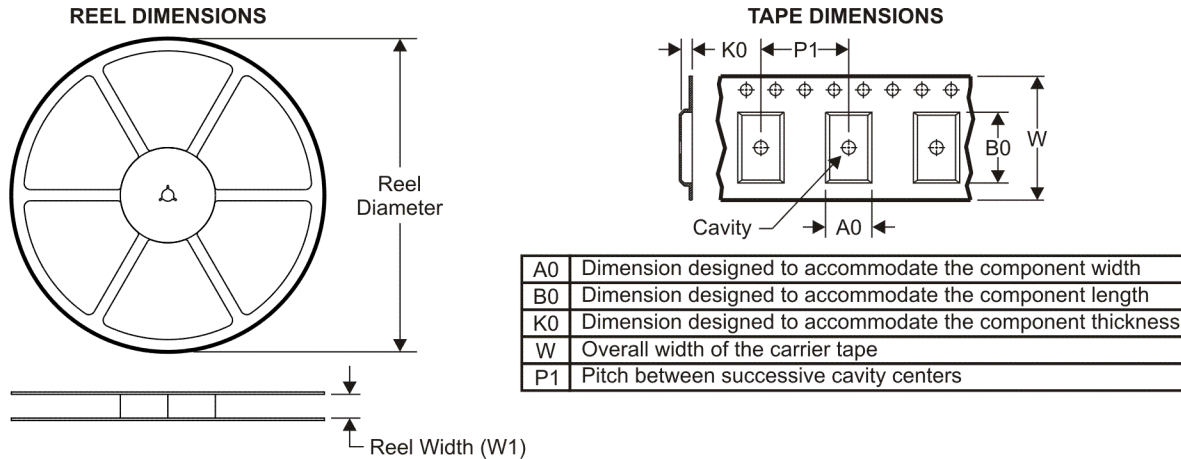
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7612U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC7612UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7612U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
DAC7612UB/2K5	SOIC	D	8	2500	346.0	346.0	29.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View DAC7612UB/2K5G4 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management