THE DATASHEET OF

SL28541BZC-2

SL28541-2

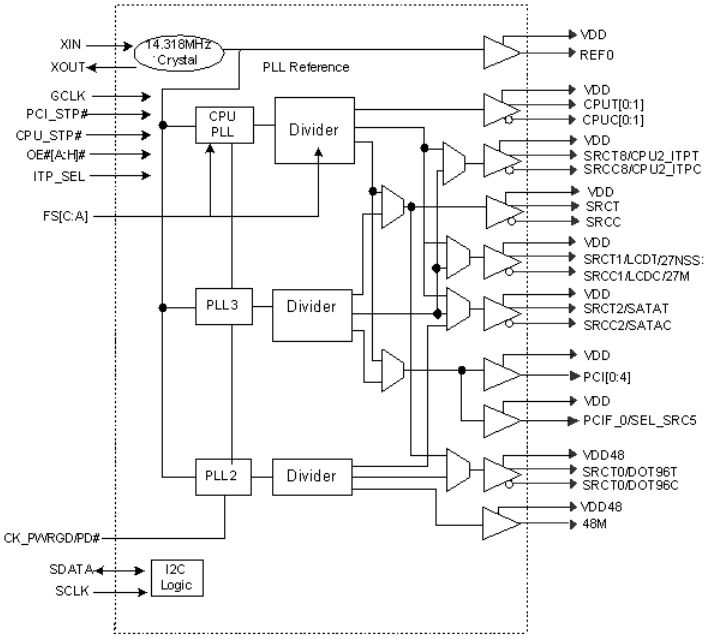
Clock Generator for Intel® Mobile Chipset

Features

- **Intel® CK505 Rev. 1.0 Compliant**
- **Low power push-pull type differential output buffers**
- **Integrated voltage regulator**
- **Integrated resistors on differential clocks**
- **Scalable low voltage VDD_IO (1.05V to 3.3V)**
- **8-step programmable drive strength for single-ended clocks**
- **Differential CPU clocks with selectable frequency**
- **100 MHz Differential SRC clocks**
- **100 MHz Differential LCD clock**
- **96 MHz Differential DOT clock**
- **48 MHz USB clock**
- **33 MHz PCI clocks**
- **27 MHz Video clocks**
- **Buffered Reference Clock 14.318 MHz**
- **14.318 MHz Crystal Input or Clock Input**
- **Low-voltage frequency select input**
- **I^2C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **Industrial Temperature -40°C to 85°C**
- **3.3V Power supply**
- **56-pin TSSOP packages**

CPU	SRC	PCI	REF	DOT96	USB_48	LCD	27M
x2 / x3	x5/9	x6	x 1	x 1	x 1	x1	x2

Block Diagram



Pin Configurations

PCI0/OE#_0/2_A	1	56	SCLK
VDD_PCI	2	55	SDATA
PCI1/OE#_0/2_A	3	54	REF0/FSC/TEST_SEL
PCI2/TME	4	53	VDD_REF
PCI3	5	52	XIN/CLKIN
PCI4/GCLK_SEL	6	51	XOUT
PCIF0/ITP_EN	7	50	VSS_REF
VSS_PCI	8	49	FSB/TEST_MODE
VDD_48	9	48	CKPWRGD/PD#
USB_48/ FSA	10	47	VDD_CPU
VSS_48	11	46	CPU0
VDD_IO	12	45	CPU#0
SRC0/DOT96	13	44	VSS_CPU
SRC0#/DOT96#	14	43	CPU1
VSS_IO	15	42	CPU1#
VDD_PLL3	16	41	VDD_CPU_IO
SRC1/LCD100/27M_NSS	17	40	NC
SRC1#/LCD100#/27M_SS	18	39	SRC8/ CPU2_ITP
VSS_PLL3	19	38	SRC8#/ CPU2_ITP#
VDD_PLL3_IO	20	37	VDD_SRC_IO
SRC2/SATA	21	36	SRC7/OE#_8
SRC2#/SATA#	22	35	SRC7#/OE#_6
VSS_SRC	23	34	VSS_SRC
SRC3/OE#_0/2_B	24	33	SRC6
SRC3#/OE#_1/4_B	25	32	SRC#
VDD_SRC_IO	26	31	VDD_SRC
SRC4	27	30	PCI_STP#
SRC4#	28	29	CPU_STP#

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56 TSSOP Pin Definition

Pin No.	Name	Type	Description
1	PCI0/OE#_0/2_A	I/O, SE	3.3V, 33MHz clock/3.3V OE# Input mappable via I2C to control either SRC0 or SRC2. *(Default PCI0, 33MHz clock)*
2	VDD_PCI	PWR	3.3V Power supply for PCI PLL.
3	PCI1/OE#_1/4_A	I/O, SE	3.3V, 33MHz clock/3.3V OE# Input mappable via I2C to control either SRC1 or SRC4. *(Default PCI1, 33MHz clock)*
4	PCI2/TME	I/O, SE	3.3V tolerance input for overclocking enable pin/3.3V, 33MHz clock. *(Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications)*
5	PCI3	O, SE,	33 MHz clock.
6	PCI4 / GCLK_SEL	I/O, SE	33 MHz clock output/3.3V-tolerant input for selecting graphic clock source on pin 13, 14, 17and 18 Sampled on CKPWRGD assertion GCLK_SEL: 0 → Pin13: DOT96T, Pin14: DOT96C, Pin17: SRC1T/LCD_100T, Pin 18: SRC1C/LCD_100C GCLK_SEL: 1 → Pin13: SRCT0, Pin14: SRCC0, Pin17: 27M_NSS, Pin 18: 27M_SS
7	PCIF_0/ITP_EN	I/O, SE	3.3V LVTTL input to enable SRC8 or CPU2_ITP/33 MHz clock output. (sampled on the CK_PWRGD assertion) 1 = CPU2_ITP, 0 = SRC8
8	VSS_PCI	GND	Ground for outputs.
9	VDD_48	PWR	3.3V Power supply for outputs and PLL.
10	USB_48/FSA	I/O	3.3V tolerant input for CPU frequency selection/fixed 3.3V, 48MHz clock output. (*Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications)*
11	VSS_48	GND	Ground for outputs.
12	VDD_IO	PWR	0.7V Power supply for outputs.
13	SRC0/DOT96	O, DIF	100MHz Differential serial reference clocks/Fixed 96MHz clock output. *(Selected via I2C default is SRC0)*
14	SRC0#/DOT96#	O, DIF	100MHz Differential serial reference clocks/Fixed 96MHz clock output. *(Selected via I2C default is SRC0)*
15	VSS_IO	GND	Ground for PLL2.
16	VDD_PLL3	PWR	3.3V Power supply for PLL3
17	SRC1/LCD100/27_NSS	O, DIF, SE	True 100 MHz differential serial reference clock output/True 100 MHz LCD video clock output / Non-spread 27-MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion.
18	SRC1#/LCD100#/27_SS	O, DIF, SE	Complementary 100 MHz differential serial reference clock output/Complementary 100 MHz LCD video clock output /Spread 27 MHz video clock output. Selected via GCLK_SEL at CKPWRGD assertion.
19	VSS_PLL3	GND	Ground for PLL3.
20	VDD_PLL3_IO	PWR	IO Power supply for PLL3 outputs.
21	SRC2/SATA	O, DIF	100MHz Differential serial reference clocks.
22	SRC2#/SATA#	O, DIF	100MHz Differential serial reference clocks.
23	VSS_SRC	GND	Ground for outputs.
24	SRC3/OE#_0/2_B	I/O, Dif	100MHz Differential serial reference clocks / 3.3V OE#_0/2_B, input, mappable via I2C to control either SRC0 or SRC2. *(Default SRC3, 100MHz clock)*
25	SRC3#OE#_1/4_B	I/O, Dif	100MHz Differential serial reference clocks / 3.3V OE#_1/4_B input, mappable via I2C to control either SRC1 or SRC4. *(Default SRC3, 100MHz clock)*
26	VDD_SRC_IO	PWR	IO power supply for SRC outputs.

56 TSSOP Pin Definition (continued)

Pin No.	Name	Type	Description
27	SRC4	O, DIF	100MHz Differential serial reference clocks.
28	SRC4#	O, DIF	100MHz Differential serial reference clocks.
29	CPU_STP#	I	3.3V tolerant input for stopping CPU outputs
30	PCI_STP#	I	3.3V tolerant input for stopping PCI and SRC outputs
31	VDD_SRC	PWR	3.3V Power supply for SRC PLL.
32	SRC6#	O, DIF	100MHz Differential serial reference clocks.
33	SRC6	O, DIF	100MHz Differential serial reference clocks.
34	VSS_SRC	GND	Ground for outputs.
35	SRC7#/OE#_6	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#6 Input controlling SRC6. *(Default SRC7, 100MHz clock)*.
36	SRC7/OE#_8	I/O, Dif	100MHz Differential serial reference clocks/3.3V OE#8 Input controlling SRC8. *(Default SRC7, 100MHz clock)*.
37	VDD_SRC_IO	PWR	0.7V power supply for SRC outputs.
38	SRC8#/CPU2#_ITP#	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 at CKPWRGD assertion = SRC8 ITP_EN = 1 @ CKPWRGD assertion = CPU2 *(Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
39	SRC8/CPU2_ITP	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 at CKPWRGD assertion = SRC8 ITP_EN = 1 @ CKPWRGD assertion = CPU2 *(Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
40	NC	NC	No Connect
41	VDD_CPU_IO	PWR	IO Power supply for CPU outputs.
42	CPU1#	O, DIF	Differential CPU clock outputs. (*Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
43	CPU1	O, DIF	Differential CPU clock outputs. (*Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2)*
44	VSS_CPU	GND	Ground for outputs.
45	CPU#0	O, DIF	Differential CPU clock outputs.
46	CPU0	O, DIF	Differential CPU clock outputs.
47	VDD_CPU	PWR	3.3V Power supply for CPU PLL.
48	CKPWRGD/PD#	I	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, FS_D, SRC5_SEL, and ITP_EN. After CKPWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW).
49	FSB/TEST_MODE	I	3.3V tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
50	VSS_REF	GND	Ground for outputs.
51	XOUT	O, SE	14.318MHz Crystal output. *(Float XOUT if using CLKIN)*
52	XIN/CLKIN	I	14.318MHz Crystal input or 3.3V, 14.318MHz input clock signal.
53	VDD_REF	PWR	3.3V Power supply for outputs and also maintains SMBUS registers during power-down.
54	REF0/FSC/TEST_SEL	I/O	3.3V tolerant input for CPU frequency selection/fixed 14.318MHz clock output. Selects test mode if pulled to V_{IHFS_C} when CKPWRGD is asserted HIGH. *Refer to DC Electrical Specifications table for* V_{ILFS_C}, V_{IMFS_C}, V_{IHFS_C} *specifications.*
55	SMB_DATA	I/O	SMBus compatible SDATA.

56 TSSOP Pin Definition (continued)

Pin No.	Name	Type	Description
56	SMB_CLK	I	SMBus compatible SCLOCK.

Table 1. Frequency Select Pin (FSA, FSB and FSC)

FSC	FSB	FSA	CPU	SRC	PCIF/PCI	27MHz	REF	DOT96	USB
0	0	0	266 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz						
0	1	0	200 MHz						
0	1	1	166 MHz						
1	0	0	333 MHz						
1	0	1	100 MHz						
1	1	0	400 MHz						
1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Frequency Select Pin (FSA, FSB and FSC)

Apply the appropriate logic levels to FSA, FSB, and FSC inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FSA, FSB, and FSC input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FSA, FSB, FSC, and CKPWRGD transitions are ignored except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits

Table 3. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	HW	FS_C	CPU Frequency Select Bit, set by HW
6	HW	FS_B	CPU Frequency Select Bit, set by HW
5	HW	FS_A	CPU Frequency Select Bit, set by HW
4	0	iAMT_EN	Set via SMBus or by combination of PWRDWN, CPU_STP, and PCI_STP 0 = Legacy Mode, 1 = iAMT Enabled
3	0	RESERVED	RESERVED
2	0	SRC_Main_SEL	Select source for SRC clock 0 = SRC_MAIN = PLL1, *PLL3_CFG Table applies* 1 = SRC_MAIN = PLL3, *PLL3_CFG Table does not apply*
1	0	SATA_SEL	Select source of SATA clock 0 = SATA = SRC_MAIN, 1= SATA = PLL2
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	SRC0_SEL	Select for SRC0 or DOT96 0 = SRC0, 1 = DOT96 When GCLK_SEL=0, this bit is 1. When GCLK_SEL=1, this bit is 0
6	0	PLL1_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
5	0	PLL3_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
4	0	PLL3_CFB3	Bit 4:1 only applies when SRC_Main_SEL = 0 See*Table 8*: PLL3 / SE configuration table
3	0	PLL3_CFB2	
2	1	PLL3_CFB1	
1	0	PLL3_CFB0	
0	1	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	REF	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
6	1	USB	Output enable for USB 0 = Output Disabled, 1 = Output Enabled
5	1	PCIF0	Output enable for PCIF0 0 = Output Disabled, 1 = Output Enabled
4	1	PCI4	Output enable for PCI4 0 = Output Disabled, 1 = Output Enabled
3	1	PCI3	Output enable for PCI3 0 = Output Disabled, 1 = Output Enabled
2	1	PCI2	Output enable for PCI2 0 = Output Disabled, 1 = Output Enabled
1	1	PCI1	Output enable for PCI1 0 = Output Disabled, 1 = Output Enabled
0	1	PCI0	Output enable for PCI0 0 = Output Disabled, 1 = Output Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	SRC[T/C]8/CPU2_ITP	Output enable for SRC8 or CPU2_ITP 0 = Output Disabled, 1 = Output Enabled
3	1	SRC[T/C]7	Output enable for SRC7 0 = Output Disabled, 1 = Output Enabled
2	1	SRC[T/C]6	Output enable for SRC6 0 = Output Disabled, 1 = Output Enabled
1	1	RESERVED	RESERVED
0	1	SRC[T/C]4	Output enable for SRC4 0 = Output Disabled, 1 = Output Enabled

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	SRC[T/C]3	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
6	1	SRC[T/C]2/SATA	Output enable for SRC2/SATA 0 = Output Disabled, 1 = Output Enabled
5	1	SRC[T/C]1/LCD_100M[T/C]	Output enable for SRC1/LCD_100M 0 = Output Disabled, 1 = Output Enabled
4	1	SRC[T/C]0/DOT96[T/C]	Output enable for SRC0/DOT96 0 = Output Disabled, 1 = Output Enabled
3	1	CPU[T/C]1	Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled
2	1	CPU[T/C]0	Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled
1	1	PLL1_SS_EN	Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
0	1	PLL3_SS_EN	Enable PLL3s spread modulation 0 = Spread Disabled, 1 = Spread Enabled

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	CR#_A_EN	Enable CR#_A (clk req) 0 = Disabled, 1 = Enabled,
6	0	CR#_A_SEL	Set CR#_A → SRC0 or SRC2 0 = CR#_A→SRC0, 1 = CR#_A→SRC2
5	0	CR#_B_EN	Enable CR#_B(clk req) 0 = Disabled, 1 = Enabled,
4	0	CR#_B_SEL	Set CR#_B → SRC1 or SRC4 0 = CR#_B→SRC1, 1 = CR#_B→SRC4
3	0	CR#_C_EN	Enable CR#_C (clk req) 0 = Disabled, 1 = Enabled
2	0	CR#_C_SEL	Set CR#_C → SRC0 or SRC2 0 = CR#_C→SRC0, 1 = CR#_C→SRC2
1	0	CR#_D_EN	Enable CR#_D (clk req) 0 = Disabled, 1 = Enabled

Byte 5: Control Register 5 (continued)

Bit	@Pup	Name	Description
0	0	CR#_D_SEL	Set CR#_D → SRC1 or SRC4 0 = CR#_D→SRC1, 1 = CR#_D→SRC4

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	CR#_E_EN	Enable CR#_E (clk req) → SRC6 0 = Disabled, 1 = Enabled
6	0	CR#_F_EN	Enable CR#_F (clk req) → SRC8 0 = Disabled, 1 = Enabled
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	LCD_100_STP_CTRL	If set, LCD_100 stop with PCI_STP# 0 = Free running, 1 = PCI_STP# stoppable
0	0	SRC_STP_CTRL	If set, SRCs stop with PCI_STP# 0 = Free running, 1 = PCI_STP# stoppable

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	1	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	Device_ID3	0000 = CK505 Yellow Cover Device, 56-pin TSSOP 0001 = CK505 Yellow Cover Device, 64-pin TSSOP 0010 = CK505 Yellow Cover Device, 48-pin QFN (Reserved) 0011 = CK505 Yellow Cover Device, 56-pin QFN (Reserved) 0100 = CK505 Yellow Cover Device, 64-pin QFN 0101 = CK505 Yellow Cover Device, 72-pin QFN (Reserved) 0110 = CK505 Yellow Cover Device, 48-pin SSOP (Reserved) 0111 = CK505 Yellow Cover Device, 48-pin SSOP (Reserved) 1000 = Reserved 1001 = CY28548 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
6	0	Device_ID2	
5	0	Device_ID1	
4	0	Device_ID0	
3	0	Reserved	Reserved
2	0	Reserved	Reserved

Byte 8: Control Register 8 (continued)

Bit	@Pup	Name	Description
1	1	27M_NSS_OE	Output enable for 27M_NSS 0 = Output Disabled, 1 = Output Enabled
0	1	27M_SS_OE	Output enable for 27M_SS 0 = Output Disabled, 1 = Output Enabled

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	PCIF_0_with PCI_STP#	Allows control of PCIF_0 with assertion of PCI_STP# 0 = Free running PCIF, 1 = Stopped with PCI_STP#
6	HW	TME_STRAP	Trusted mode enable strap status 0 = Normal, 1 = No overclocking
5	1	REF_DSC1	REF drive strength 1 of 2 *(See Byte 17 and 18 for more setting)* 0 = Low, 1 = High
4	0	TEST_MODE_SEL	Mode select either REF/N or tri-state 0 = All output tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allow entry into test mode 0 = Normal operation, 1 = Enter test mode
2	1	I2C_VOUT<2>	Differential Amplitude Configuration I2C_VOUT[2,1,0] 000 = 0.63V 001 = 0.71V 010 = 0.77V 011 = 082V 100 = 0.86V 101 = 0.90V (default) 110 = 0.93V 111 = unused
1	0	I2C_VOUT<1>	
0	1	I2C_VOUT<0>	

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	HW	GCLK_SEL latch	Readback of GCLK_SEL latch 0 = DOT96/LCD_100, 1 = SRC0/27 MHz
6	1	PLL3_EN	PLL3 power down 0 = Power down, 1 = Power up
5	1	PLL2_EN	PLL2 power down 0 = Power down, 1 = Power up
4	1	SRC_DIV_EN	SRC divider disable 0 = Disabled, 1 = Enabled
3	1	PCI_DIV_EN	PCI divider disable 0 = Disabled, 1 = Enabled
2	1	CPU_DIV_EN	CPU divider disable 0 = Disabled, 1 = Enabled
1	1	CPU1 Stop Enable	Enable CPU_STP# control of CPU1 0 = Free running, 1= Stoppable
0	1	CPU0 Stop Enable	Enable CPU_STP# control of CPU0 0 = Free running, 1= Stoppable

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	Reserved	Reserved

Byte 11: Control Register 11 (continued)

6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 12: Byte Count

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	BC5	Byte count register for block read operation. The default value for Byte count is 19. In order to read beyond Byte 19, the user should change the byte count limit.to or beyond the byte that is desired to be read.
4	1	BC4	
3	0	BC3	
2	0	BC2	
1	1	BC1	
0	1	BC0	

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	1	USB_BIT1	USB drive strength 1 of 3*(See Byte 17 for more setting)* 0 = Low, 1= High
6	1	PCI/ PCIF_BIT1	PCI drive strength 1 of 3*(See Byte 17 & 18 for more setting)* 0 = Low, 1 = High
5	0	PLL1_Spread	Select percentage of spread for PLL1 0 = 0.5%, 1=1%
4	1	SATA_SS_EN	Enable SATA spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
3	1	CPU[T/C]2	Allow control of CPU2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
2	1	SE1/SE2_BIT_1	SE1 and SE2 Drive Strength Setting 1 of 3 *(See Byte 17 and 18 for more setting)* 0 = Low, 1= High
1	1	Reserved	Reserved
0	1	SW_PCI	SW PCI_STP# Function 0 = SW PCI_STP assert, 1 = SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs are stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs are resumed in a synchronous manner with no short pulses.

Byte 14: Control Register 14

Bit	@Pup	Name	Description

Byte 14: Control Register 14

7	0	CPU_DAF_N7	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] are used to determine the CPU output frequency.
6	0	CPU_DAF_N6	
5	0	CPU_DAF_N5	
4	0	CPU_DAF_N4	
3	0	CPU_DAF_N3	
2	0	CPU_DAF_N2	
1	0	CPU_DAF_N1	
0	0	CPU_DAF_N0	

Byte 15: Control Register 15

Bit	@Pup	Name	Description
7	0	CPU_DAF_N8	See Byte 14 for description
6	0	CPU_DAF_M6	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] are used to determine the CPU output frequency.
5	0	CPU_DAF_M5	
4	0	CPU_DAF_M4	
3	0	CPU_DAF_M3	
2	0	CPU_DAF_M2	
1	0	CPU_DAF_M1	
0	0	CPU_DAF_M0	

Byte 16: Control Register 16

Bit	@Pup	Name	Description
7	0	PCI-E_N7	PCI-E Dial-A-Frequency® Bit N7
6	0	PCI-E_N6	PCI-E Dial-A-Frequency Bit N6
5	0	PCI-E_N5	PCI-E Dial-A-Frequency Bit N5
4	0	PCI-E_N4	PCI-E Dial-A-Frequency Bit N4
3	0	PCI-E_N3	PCI-E Dial-A-Frequency Bit N3
2	0	PCI-E_N2	PCI-E Dial-A-Frequency Bit N2
1	0	PCI-E_N1	PCI-E Dial-A-Frequency Bit N1
0	0	PCI-E_N0	PCI-E Dial-A-Frequency Bit N0

Byte 17: Control Register 17

Bit	@Pup	Name	Description
7	0	SMSW_EN	Enable Smooth Switching 0 = Disabled, 1= Enabled
6	0	SMSW_SEL	Smooth switch select 0 = CPU_PLL, 1 = SRC_PLL
5	0	SE1/SE2_BIT0	SE1 and SE2 drive strength Setting 2 of 3*(see Byte 18 for more setting)* 0 = Low, 1= High
4	0	Prog_PCI-E_EN	Programmable PCI-E frequency enable 0 = Disabled, 1= Enabled
3	0	Prog_CPU_EN	Programmable CPU frequency enable 0 = Disabled, 1= Enabled
2	0	REF_BIT0	REFdrive strength strength Setting 2 of 3*(see Byte 18 for more setting)* 0 = Low, 1= High
1	0	USB_BIT0	USB drive strength strength Setting 2 of 3*(see Byte 18 for more setting)* 0 = Low, 1= High
0	0	PCI/ PCIF_BIT0	PCI drive strength strength Setting 2 of 3*(see Byte 18 for more setting)* 0 = Low, 1= High

Byte 18: Control Register 18

7	0	REF_BIT2	Drive Strength Control
6	0	RESERVED	
5	1	RESERVED	
4	0	RESERVED	
3	0	USB_BIT2	
2	0	PCI/PCIF_BIT2	
1	0	SE1/SE2_BIT2	
0	0	RESERVED	

	BIT_2 (Byte18)	BIT_1 (Various Bytes)	BIT_0 (Byte 17)	Buffer Strength
	1	1	1	Strongest
	1	1	0	
	1	0	1	
	1	0	0	
	0	1	1	
Default	0	1	0	
	0	0	1	

Table 5. Output Driver Status during PCI-STP# and CPU-STP#

		PCI_STP# Asserted	CPU_STP# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Driven low	Running	Driven low
	Non stoppable	Running	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven high	Clock driven Low or 20K pulldown
		Clock# driven low	Clock# driven low	
	Non stoppable	Running	Running	

Table 6. Output Driver Status

	All Single-ended Clocks		All Differential Clocks except CPU1		CPU1	
	w/o Strap	w/ Strap	Clock	Clock#	Clock	Clock#
Latches Open State	Low	Hi-z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
Powerdown	Low	Hi-z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
M1	Low	Hi-z	Low or 20K pulldown	Low	Running	Running

Table 7. PLL3/SE Configuration Table

GCLK_SEL	B1b4	B1b3	B1b2	B1b1	Pin 17 (MHz)	Pin 18 (MHz)	Spread (%)	Comment
0	0	0	0	0	PLL3 Disabled			
0	0	0	0	1	100	100	0.5	SRC1 from SRC_Main
0	0	0	1	0	100	100	0.5	LCD_100 from PLL3
0	0	0	1	1	100	100	1	LCD_100 from PLL3
0	0	1	0	0	100	100	1.5	LCD_100 from PLL3
0	0	1	0	1	100	100	2	LCD_100 from PLL3
0	0	1	1	0	N/A	N/A	N/A	N/A
0	0	1	1	1	N/A	N/A	N/A	N/A
0	1	0	0	0	N/A	N/A	N/A	N/A
0	1	0	0	1	N/A	N/A	N/A	N/A
0	1	0	1	0	N/A	N/A	N/A	N/A
0	1	0	1	1	N/A	N/A	N/A	N/A
0	1	1	0	0	N/A	N/A	none	N/A
0	1	1	0	1	N/A	N/A	N/A	N/A
0	1	1	1	0	N/A	N/A	N/A	N/A
0	1	1	1	1	N/A	N/A	N/A	N/A
1	0	0	0	0	N/A	N/A	N/A	
1	0	0	0	1	27M_NSS	27M_SS	0.5	27M_SS from PLL3
1	0	0	1	0	27M_NSS	27M_SS	0.5	27M_SS from PLL3
1	0	0	1	1	27M_NSS	27M_SS	1	27M_SS from PLL3
1	0	1	0	0	27M_NSS	27M_SS	1.5	27M_SS from PLL3
1	0	1	0	1	27M_NSS	27M_SS	2	27M_SS from PLL3
1	0	1	1	0	N/A	N/A	N/A	
1	0	1	1	1	N/A	N/A	N/A	
1	1	0	0	0	N/A	N/A	N/A	
1	1	0	0	1	N/A	N/A	N/A	
1	1	0	1	0	N/A	N/A	N/A	
1	1	0	1	1	N/A	N/A	N/A	
1	1	1	0	0	N/A	N/A	N/A	
1	1	1	0	1	N/A	N/A	N/A	

Table 8. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SL28541-2 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the SL28541-2 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

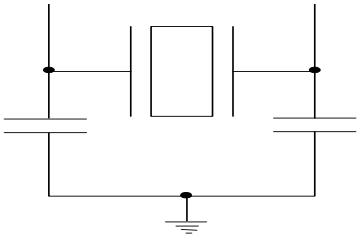


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

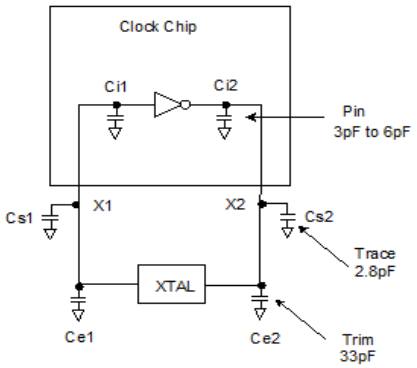


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires, etc.)

Dial-A-Frequency® (CPU and SRC Clocks)

This feature allows the user to over-clock their system by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation:

Fcpu = G * N/M or Fcpu=G2 * N, where G2 = G / M.

- "N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.
- "G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See *Table 1*, *Frequency Select Table* for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in *Table 1*, *Frequency Select Table*.

In this mode, the user writes the desired N and M values into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the N value.

Associated Register Bits

- *CPU_DAF Enable* – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU_DAF_N register. Note that the CPU_DAF_N and M register must contain valid values before CPU_DAF is set. Default = 0, (No DAF).
- *CPU_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1*, *Frequency Select Table*.
- *CPU DAF M* – There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in *Table 1*, *Frequency Select Table*
- *SRC_DAF Enable* – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC_DAF_N register. Note that the SRC_DAF_N register must contain valid values before SRC_DAF is set. Default = 0, (No DAF).
- *SRC_DAF_N* – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in *Table 1*, *Frequency Select Table*.

Smooth Switching

The device contains one smooth switch circuit that is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667 µs. The frequency overshoot and undershoot is less than 2%.

The Smooth Switch circuit assigns auto or manual. In Auto mode, clock generator assigns smooth switch automatically when the PLL does overclocking. For manual mode, assign

the smooth switch circuit to PLL via Smbus. By default the smooth switch circuit is set to auto mode. PLL can be over-clocked when it does not have control of the smooth switch circuit but it is not guaranteed to transition to the new frequency without large frequency glitches.

Do not enable over-clocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

PD_RESTORE

If a '0' is set for Byte 0 bit 0 then, upon assertion of PD# LOW, the SL28541-2 initiates a full reset. The result of this is that the clock chip emulates a cold power on start and goes to the "Latches Open" state. If the PD_RESTORE bit is set to a '1' then the configuration is stored upon PD# asserted LOW. Note that if the iAMT bit, Byte 0 bit 3, is set to a '1' then the PD_RESTORE bit must be ignored. In other words, in Intel iAMT mode, PD# reset is not allowed.

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. *Figure 4* is an example showing the relationship of clocks coming up.

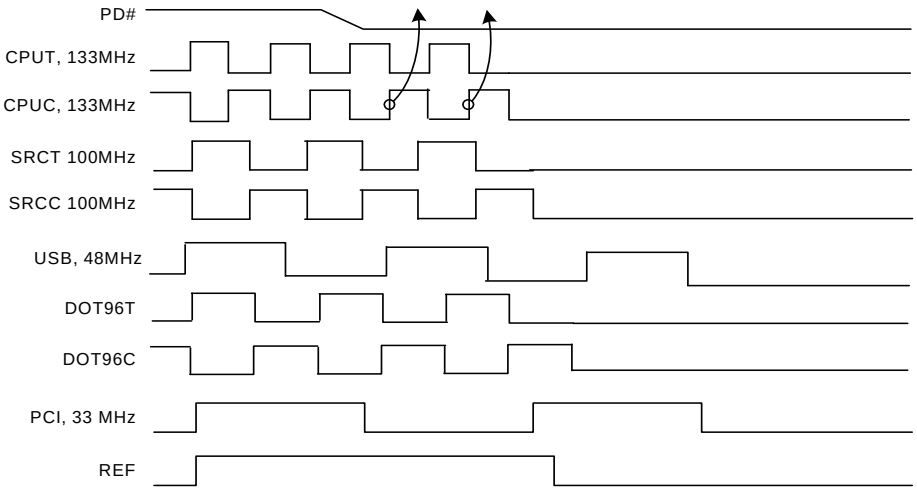


Figure 3. Power down Assertion Timing Waveform

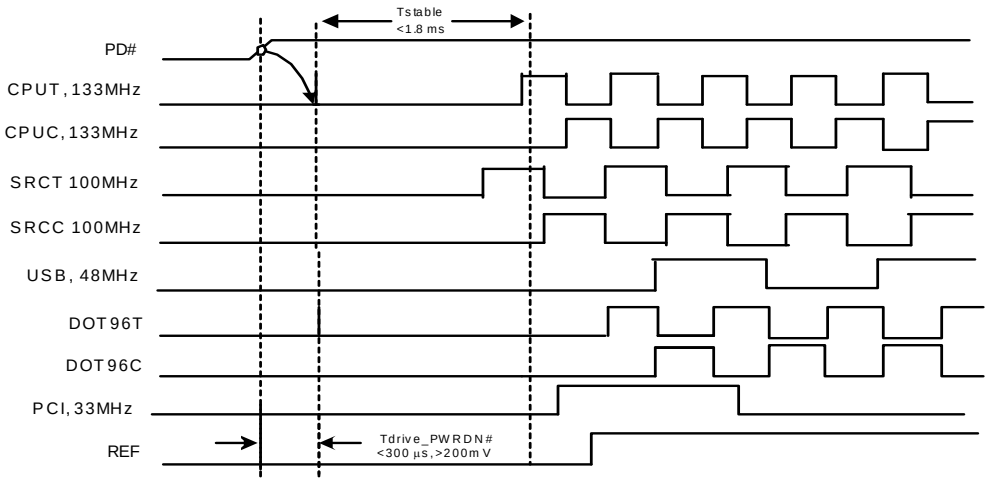


Figure 4. Power down Deassertion Timing Waveform

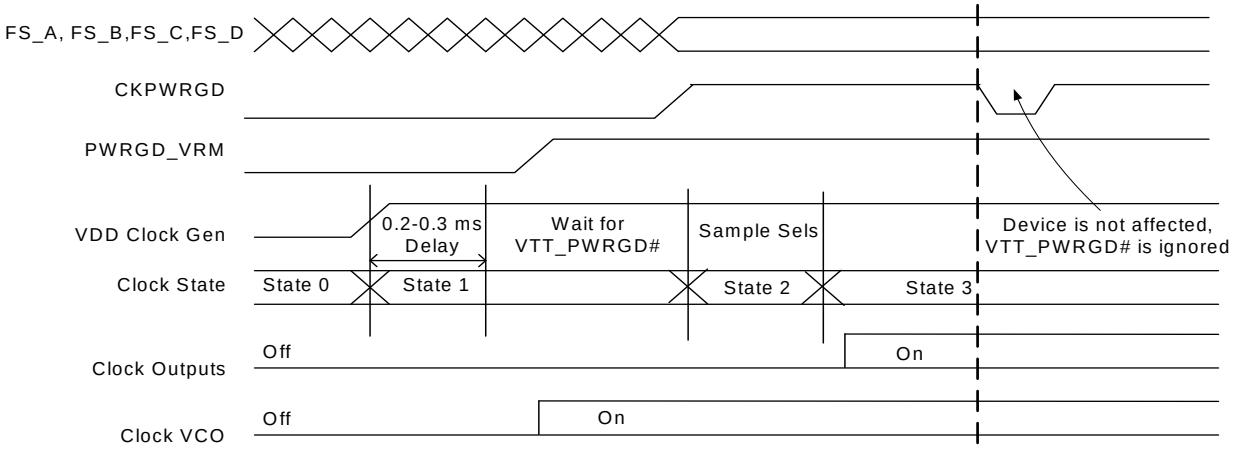


Figure 5. CKPWRGD Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

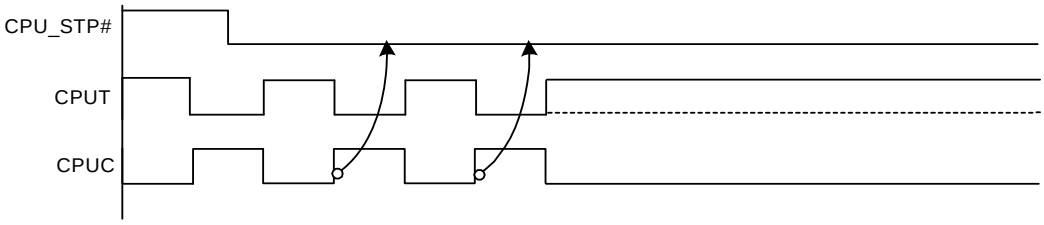


Figure 6. CPU_STP# Assertion Waveform

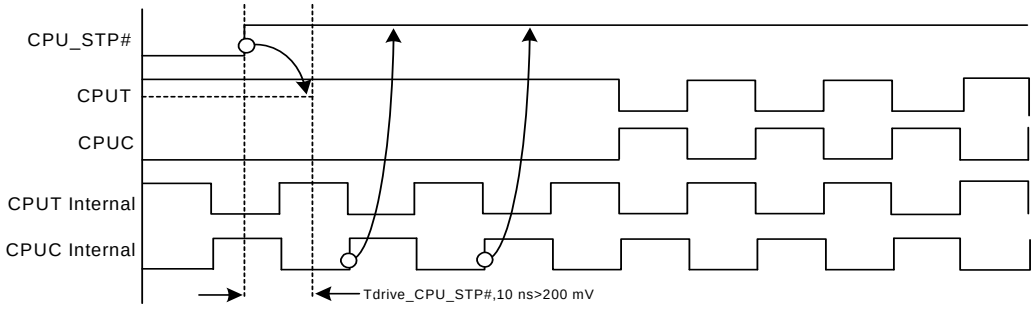


Figure 7. CPU_STP# Deassertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 8*.) The PCIF clocks are affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

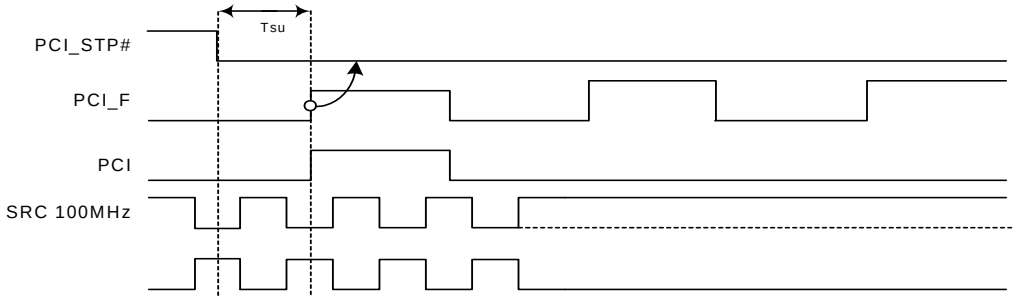


Figure 8. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal causes all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods, after PCI_STP# transitions to a HIGH level.

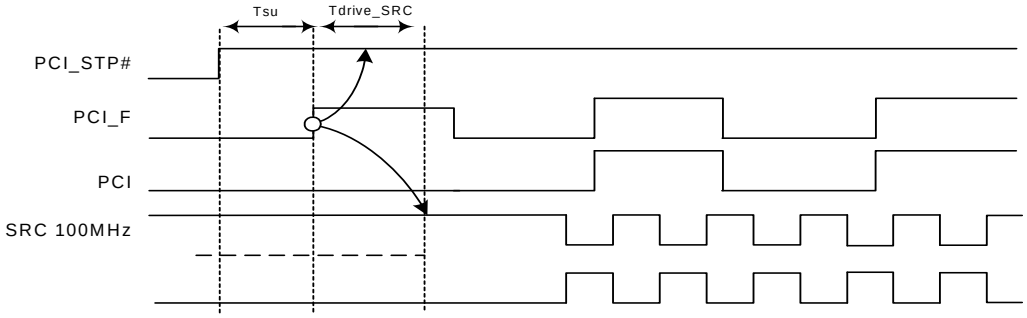


Figure 9. PCI_STP# Deassertion Waveform

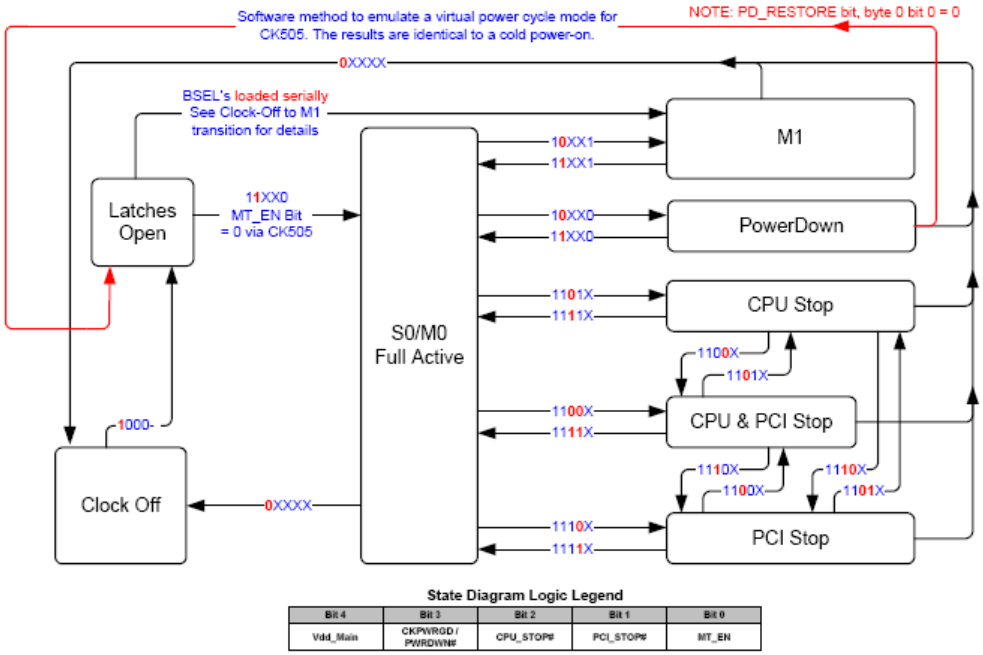


Figure 10. Clock Generator Power up/Run State Diagram

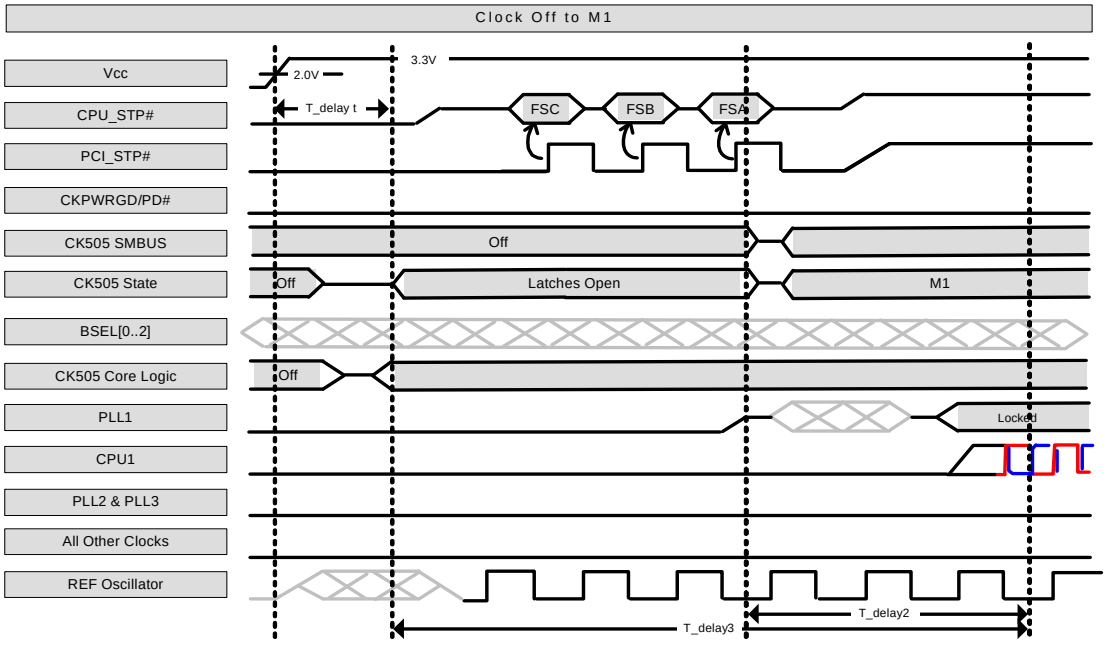


Figure 11. BSEL Serial Latching

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Supply Voltage	Functional	–	4.6	V
V_{DD_IO}	IO Supply Voltage	Functional		3.465	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Commercial Temperature, Operating Ambient	Functional	0	85	°C
	Industrial Temperature, Operating Ambient		-40	+85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22-A114)	2000	–	V
UL-94	Flammability Rating	UL (CLASS)	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	1.5	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
$V_{IHFS\_C\_TEST}$	FS_C Input High Voltage		2	V_{DD} + 0.3	V
$V_{IMFS\_C\_NORMAL}$	FS_C Input Middle Voltage		0.7	1.5	V
$V_{ILFS\_C\_NORMAL}$	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
$V_{DD\ IO}$	Low Voltage IO Supply Voltage		1	3.465	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
IDD_{PWRDWN}	Power Down Current			1	mA
I_{DD}	Dynamic Supply Current		–	250	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device operates reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy		–	300	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
I_{IL}	Input LowCurrent	XIN / CLKIN pin, 0 < VIN <0.8	–	20	uA
I_{IH}	Input HighCurrent	XIN / CLKIN pin, VIN = VDD	–	35	uA
CPU at 0.7V					
T_{DC}	CPU Clock Duty Cycle	Measured at 0V differential at 0.1s	**45**	**55**	%
T_{PERIOD}	100 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**9.99900**	**10.00100**	ns
T_{PERIOD}	133 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**7.49925**	**7.50075**	ns
T_{PERIOD}	166 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**5.99940**	**6.00060**	ns
T_{PERIOD}	200 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**4.99950**	**5.00050**	ns
T_{PERIOD}	266 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**3.74963**	**3.75038**	ns
T_{PERIOD}	333 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**2.99970**	**3.00030**	ns
T_{PERIOD}	400 MHz CPU Clock Period	Measured at 0V differential at 0.1s	**2.49975**	**2.50025**	ns
$T_{PERIODSS}$	100 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**10.02406**	**10.02607**	ns
$T_{PERIODSS}$	133 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**7.51804**	**7.51955**	ns
$T_{PERIODSS}$	166 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**6.01444**	**6.01564**	ns
$T_{PERIODSS}$	200 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**5.01203**	**5.01303**	ns
$T_{PERIODSS}$	266 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**3.75902**	**3.75978**	ns
$T_{PERIODSS}$	333 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**3.00722**	**3.00782**	ns
$T_{PERIODSS}$	400 MHz CPU Clock Period, SSC	Measured at 0V differential at 0.1s	**2.50601**	**2.50652**	ns
$T_{PERIODAbs}$	100 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**9.91400**	**10.0860**	ns
$T_{PERIODAbs}$	133 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**7.41425**	**7.58575**	ns
$T_{PERIODAbs}$	166 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**5.91440**	**6.08560**	ns
$T_{PERIODAbs}$	200 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**4.91450**	**5.08550**	ns
$T_{PERIODAbs}$	266 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**3.66463**	**3.83538**	ns
$T_{PERIODAbs}$	333 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**2.91470**	**3.08530**	ns
$T_{PERIODAbs}$	400 MHz CPU Clock Absolute period	Measured at 0V differential at 1 clock	**2.41475**	**2.58525**	ns
$T_{PERIODSSAbs}$	100 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**9.91406**	**10.1362**	ns
$T_{PERIODSSAbs}$	133 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**7.41430**	**7.62340**	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODSSAbs}$	166 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**5.91444**	**6.11572**	ns
$T_{PERIODSSAbs}$	200 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**4.91453**	**5.11060**	ns
$T_{PERIODSSAbs}$	266 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**3.66465**	**3.85420**	ns
$T_{PERIODSSAbs}$	333 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**2.91472**	**3.10036**	ns
$T_{PERIODSSAbs}$	400 MHz CPU Clock Absolute period, SSC	Measured at 0V differential at 1 clock	**2.41477**	**2.59780**	ns
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at 0V differential	**–**	**85**	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at 0V differential	**–**	**125**	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	**–**	**100**	ppm
T_{SKEW}	CPU0 to CPU1 Clock Skew	Measured at 0V differential	**–**	**100**	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at 0V differential	**–**	**150**	ps
T_R / T_F	CPU Rising/Falling Slew rate	Measured differentially from ±150 mV	**2.5**	**8**	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	**–**	**20**	%
V_{HIGH}	Voltage High			**1.15**	V
V_{LOW}	Voltage Low		**–0.3**	**–**	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		**300**	**550**	mV
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	**45**	**55**	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	**9.99900**	**10.0010**	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	**10.02406**	**10.02607**	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	**9.87400**	**10.1260**	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	**9.87406**	**10.1762**	ns
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	**–**	**3.0**	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	**–**	**125**	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	**–**	**100**	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	**2.5**	**8**	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	**–**	**20**	%
V_{HIGH}	Voltage High			**1.15**	V
V_{LOW}	Voltage Low		**–0.3**	**–**	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		**300**	**550**	mV
DOT96 at 0.7V					
T_{DC}	DOT96 Duty Cycle	Measured at 0V differential	**45**	**55**	%
T_{PERIOD}	DOT96 Period	Measured at 0V differential at 0.1s	**10.4156**	**10.4177**	ns
$T_{PERIODAbs}$	DOT96 Absolute Period	Measured at 0V differential at 0.1s	**10.1656**	**10.6677**	ns
T_{CCJ}	DOT96 Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	**–**	**250**	ps
L_{ACC}	DOT96 Long Term Accuracy	Measured at 0V differential at 1 clock	**–**	**100**	ppm
T_R / T_F	DOT96 Rising/Falling Slew Rate	Measured differentially from ±150 mV	**2.5**	**8**	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	**–**	**20**	%
V_{HIGH}	Voltage High			**1.15**	V
V_{LOW}	Voltage Low		**–0.3**	**–**	V

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{OX}	Crossing Point Voltage at 0.7V Swing		**300**	**550**	mV
LCD_100_SSC at 0.7V					
T_{DC}	LCD_100 Duty Cycle	Measured at 0V differential	**45**	**55**	%
T_{PERIOD}	100 MHz LCD_100 Period	Measured at 0V differential at 0.1s	**9.99900**	**10.0010**	ns
$T_{PERIODSS}$	100 MHz LCD_100 Period, SSC -0.5%	Measured at 0V differential at 0.1s	**10.02406**	**10.02607**	ns
$T_{PERIODAbs}$	100 MHz LCD_100 Absolute Period	Measured at 0V differential at 1 clock	**9.74900**	**10.25100**	ns
$T_{PERIODSSAbs}$	100 MHz LCD_100 Absolute Period, SSC	Measured at 0V differential at 1 clock	**9.74906**	**10.3012**	ns
T_{CCJ}	LCD_100 Cycle to Cycle Jitter	Measured at 0V differential	**–**	**250**	ps
L_{ACC}	LCD_100 Long Term Accuracy	Measured at 0V differential	**–**	**100**	ppm
T_R / T_F	LCD_100 Rising/Falling Slew Rate	Measured differentially from ±150 mV	**2.5**	**8**	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	**–**	**20**	%
V_{HIGH}	Voltage High			**1.15**	V
V_{LOW}	Voltage Low		**–0.3**	**–**	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		**300**	**550**	mV
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	**45**	**55**	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	**29.99700**	**30.00300**	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	**30.08421**	**30.23459**	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	**29.49700**	**30.50300**	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	**29.56617**	**30.58421**	ns
T_{HIGH}	Spread Enabled PCIF and PCI high time	Measurement at 2V	**12.27095**	**16.27995**	ns
T_{LOW}	Spread Enabled PCIF and PCI low time	Measurement at 0.8V	**11.87095**	**16.07995**	ns
T_{HIGH}	Spread Disabled PCIF and PCI high time	Measurement at 2.V	**12.27365**	**16.27665**	ns
T_{LOW}	Spread Disabled PCIF and PCI low time	Measurement at 0.8V	**11.87365**	**16.07665**	ns
T_R / T_F	PCIF/PCI Rising/Falling Slew Rate	Measured between 0.8V and 2.0V	**1.0**	**4.0**	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	**–**	**1000**	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	**–**	**500**	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measurement at 1.5V	**–**	**100**	ppm
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	**45**	**55**	%
T_{PERIOD}	Period	Measurement at 1.5V	**20.83125**	**20.83542**	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	**20.48125**	**21.18542**	ns
T_{HIGH}	48_M High time	Measurement at 2V	**8.216563**	**11.15198**	ns
T_{LOW}	48_M Low time	Measurement at 0.8V	**7.816563**	**10.95198**	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	**1.0**	**2.0**	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	**–**	**350**	ps
L_{ACC}	48M Long Term Accuracy	Measurement at 1.5V	**–**	**100**	ppm
27M_NSS/27M_SS at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	**45**	**55**	%
T_{PERIOD}	Spread Disabled 27M Period	Measurement at 1.5V	**37.03594**	**37.03813**	ns
	Spread Enabled 27M Period	Measurement at 1.5V	**37.01299**	**37.13172**	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	**1.0**	**4.0**	V/ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	**250**	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	**50**	ppm
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	**45**	**55**	%
T_{PERIOD}	REF Period	**Measurement at 1.5V**	**69.82033**	**69.86224**	ns
$T_{PERIODAbs}$	REF Absolute Period	**Measurement at 1.5V**	**68.83429**	**70.84826**	ns
T_{HIGH}	REF High time	**Measurement at 2V**	**29.97543**	**38.46654**	ns
T_{LOW}	REF Low time	**Measurement at 0.8V**	**29.57543**	**38.26654**	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	**1.0**	**4.0**	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	**500**	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	**1000**	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	**100**	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	**1.8**	ms
T_{SS}	Stopclock Set-up Time		**10.0**	–	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

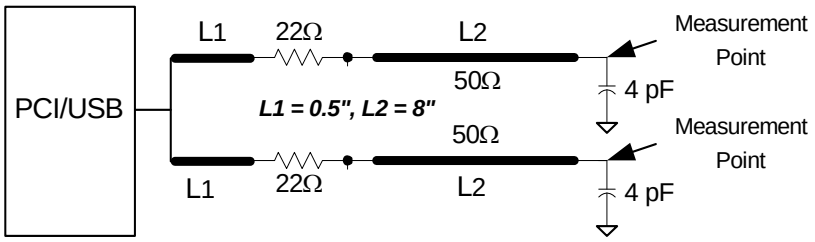


Figure 12. Single-ended PCI and USB Double Load Configuration

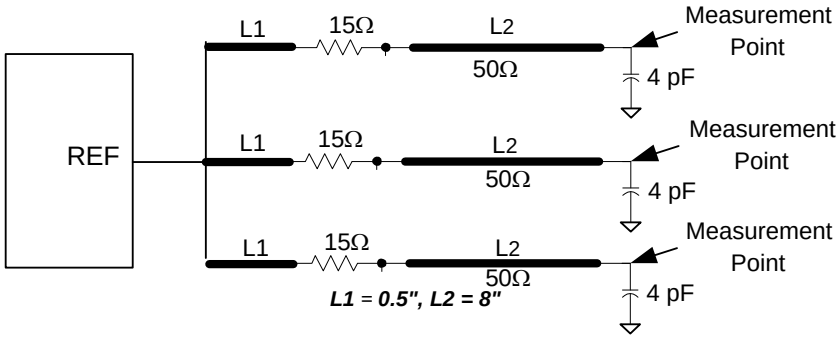


Figure 13. Single-ended REF Triple Load Configuration

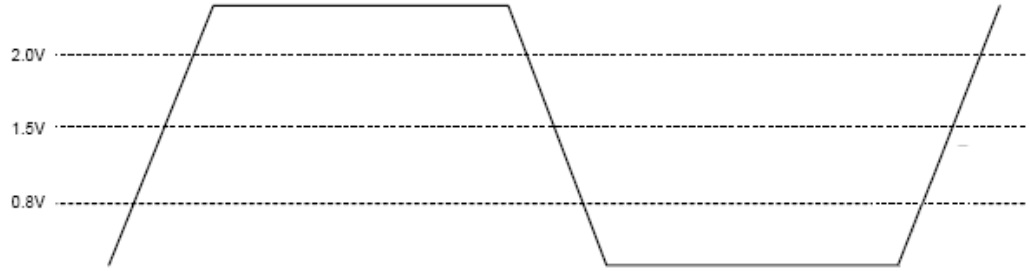


Figure 14. Single-ended Output Signals (for AC Parameters Measurement)

For CPU, SRC, and DOT96 Signals and Reference

This diagram shows the test load configuration for the differential CPU and SRC outputs

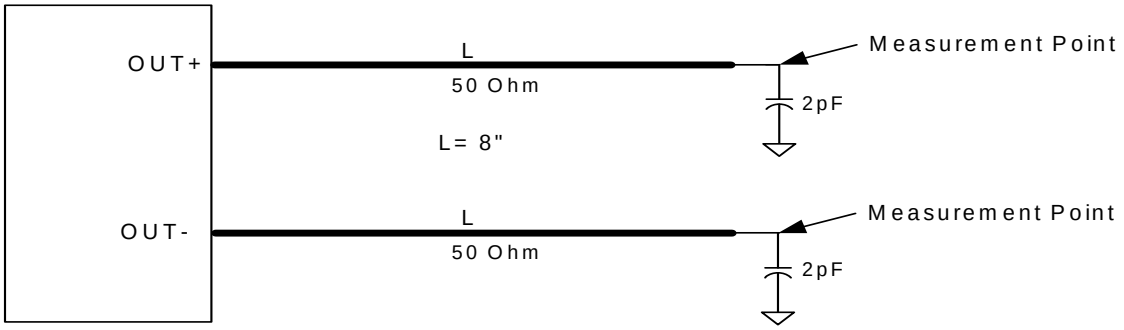


Figure 15. 0.7V Differential Load Configuration

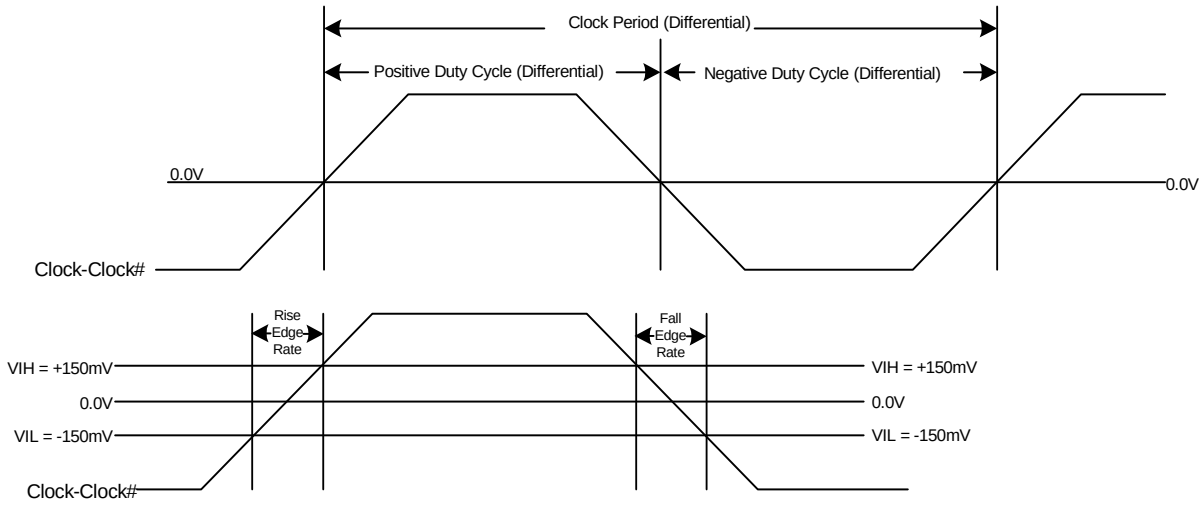


Figure 16. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

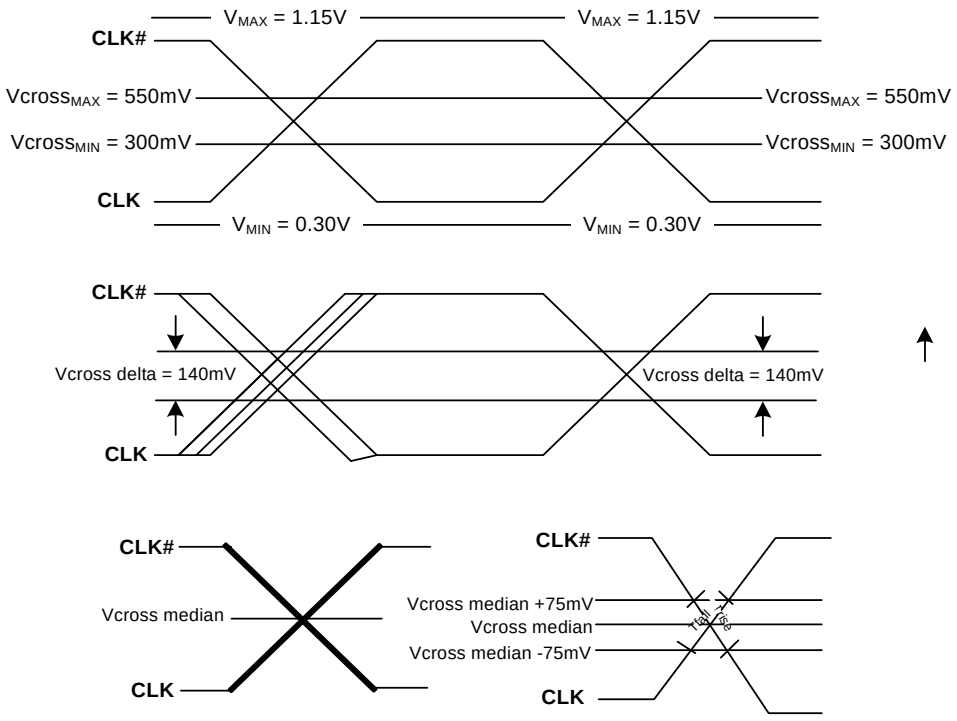


Figure 17. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

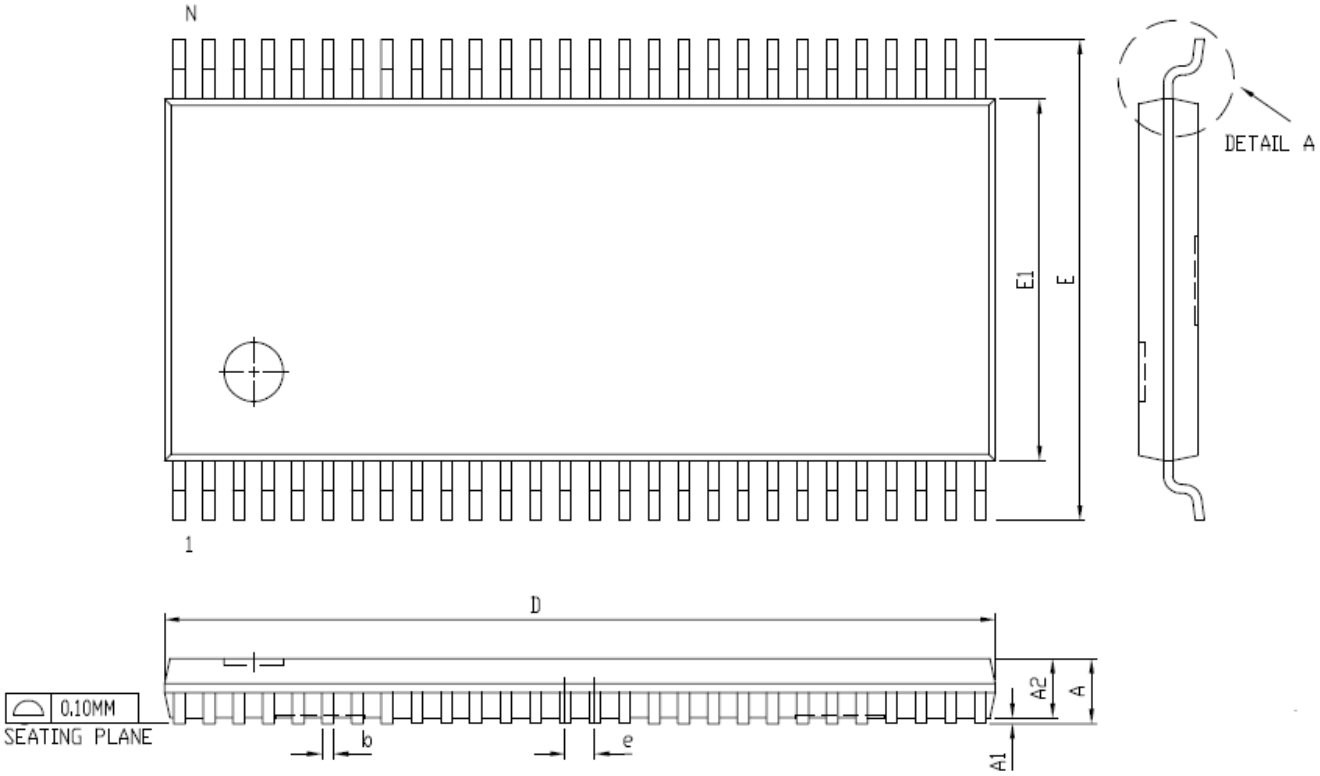
Ordering Information

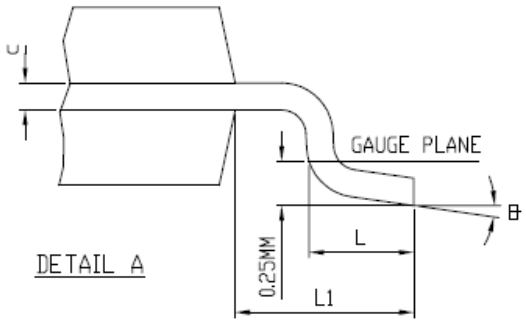
Part Number	Package Type	Product Flow
Lead-free		
SL28541BZC-2	56-pin TSSOP	Commercial, 0° to 85°C
SL28541BZC-2T	56-pin TSSOP–Tape and Reel	Commercial, 0° to 85°C
SL28541BZI-2	56-pin TSSOP	Industrial, -40° to 85°C
SL28541BZI-2T	56-pin TSSOP–Tape and Reel	Industrial, -40° to 85°C

This device is Pb-free, Halogen-free and RoHS compliant.

Package Diagrams

56-Lead Thin Shrunk Small Outline Package





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	1.00	1.05	.031	.039	.041
D	13.90	14.00	14.10	.547	.551	.555
E	8.00	8.10	8.20	.315	.319	.323
E1	6.00	6.10	6.20	.236	.240	.244
L	0.45	0.60	0.75	.018	.024	.030
L1	1.00 REF.			.039 REF.		
b	0.18	0.20	0.25	.007	.008	.010
e	0.50 BSC.			.020 BSC.		
c	0.09		0.20	.004		.008
θ	0		8	0		8
N	56					
REF	JEDEC MO-153 VARIATION EE					

NOTES

1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. LEAD COPLANARITY IS 0.003 INCH MAX.

Document History Page

Document Title: SL28541-2 Clock Generator for Intel®Mobile Chipset DOC #: SP-AP-0064 (Rev. AB)				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0		1/01/07	JMA	New data sheet
1.1		6/15/07	BEN	Change ordering number to SL28541BQC
1.2		9/18/07	BEN	VDDIO range change from 1.25V to 1.05V
1.3		10/31/07	BEN	1. Added 64 TSSOP pin definitions 2. Added 64 TSSOP package dimension 3. Byte1[2] is changed from 0 to 1 and Byte1[1] is changed from 1 to 0 by power up default 4. Changed Byte 13 bit 5 spread percentage from -1% to -0.45% 5. Updated revision ID
1.4		12/15/07	SLI	1. Updated Pin Definition table 2. Updated Table 7. PLL3/SE Configuration Table
1.5		1/23/08	JMA	1. Changed Byte 13 Bit 5 to replace 0.45% spread to 1% spread. 2. Changed 27MHz period spec to be reflect down spread. 3. Changed 27MHz CCJ spec from 200ps to 250ps.
1.6		7/8/08	JMA	1. Changed maximum operating temperature range from 85C to 70C 2. Added note on Pb-free, Halogen-free, and RoHS compliant 3. Added note on extended temperature 4. Added Mitsui package
1.7		2/23/09	JMA	1. Added 64-TSSOP package on page 1. 2. Change operating temperature back to 85C
1.8		3/31/09	JMA	1. Updated QFN packge information 2. Udpated Slew rate measurement for 27MHz clocks 3. Updated Tperiod for CPU clock at 100MHz 4. Corrected Byte 7 Revision ID 5. Corrected Byte 8 Device ID 6. Added PWRDWN IDD Spec
1.9		4/27/09	JMA	1. Corrected Reserved bit in Byte18 2. Corrected Reserved bit in Byte 20 3. Corrected wording for PD to PWRDWN 4. Added “F” in pF in Figure 2 5. Removed Cypress package marking
2.0		9/10/09	JMA	1. Updated QFN package information
AA	1454	04/09’/10	JMA	1. Added CLKIN feature. 2. Updated Absolut spec 3. Move location of Output Drive Satus & PLL3/SE Configue tables 4. Combined commercial and industrial temperature grade 5. Updated VDD_IO voltage
AB	1641	06/08/10	JMA	1. Updated VDDIO max spec 2. Updated block diagram.

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