THE DATASHEET OF

SM802140UMG

SM802140

ClockWorks™ 644.53125MHz LVDS Ultra-Low Jitter, Frequency Synthesizer

General Description

The SM802140 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for clock signals. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes four Differential LVDS clocks at 644.53125MHz

The SM802140 accepts a 20.141601MHz crystal input.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

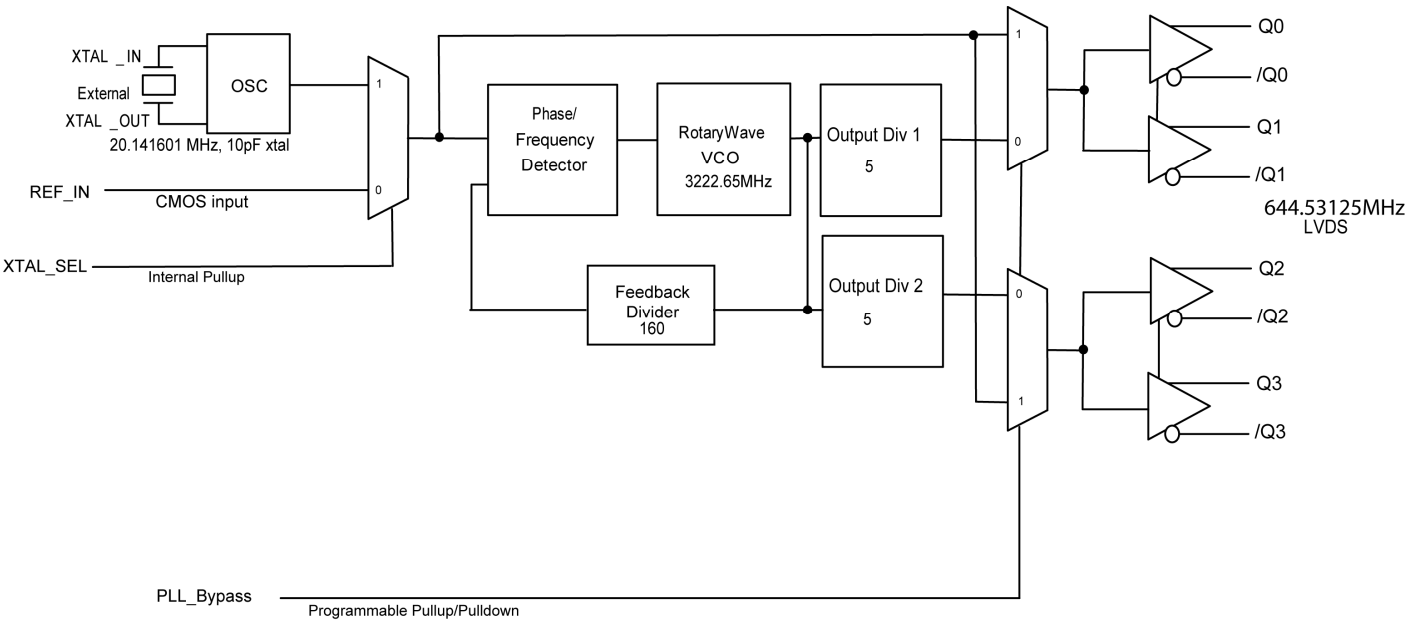
Features

Generates four LVDS clocks output at 644.53125MHz
2.5V or 3.3V operating range
Typical phase jitter @ 644MHz
(1.875MHz to 20MHz): 114 fs (typical) at 3.3V
Industrial temperature range
Green, RoHS, and PFOS compliant
Available in 24-pin 4mm × 4mm QFN package

Applications

40GbE
Serial PMD clock
FPGA Transceiver clock

Block Diagram



ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Micrel, Inc.

Ordering Information

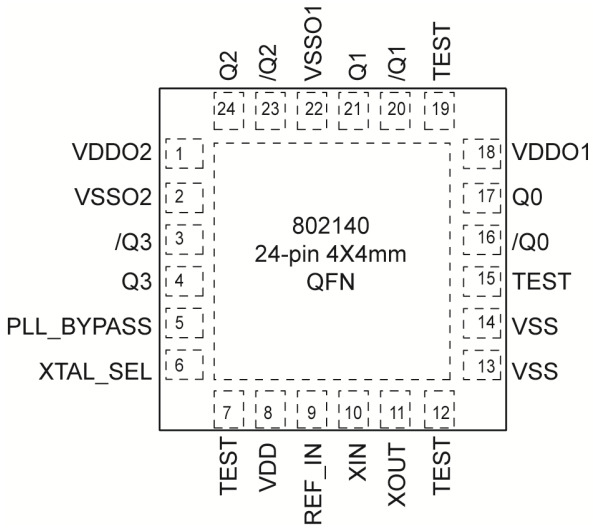
Part Number	Marking	Shipping	Temperature Range	Package
SM802140UMG	802140	Tube	–40°C to +85°C	24-Pin QFN
SM802140UMGTR	802140	Tape and Reel	–40°C to +85°C	24-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration

24-Pin QFN
(Top View)



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
3, 4 16, 17 20, 21 23, 24	/Q3, Q3 /Q0, Q0 /Q1, Q1 /Q2, Q2	O, (DIFF)	LVDS	Differential Clock Outputs at 644.53125MHz
1	VDDO2	PWR		Power Supply for Outputs Q2 and Q3
2	VSSO2	PWR		Power Supply Ground for Outputs Q2 and Q3
5	PLL_BYPASS	I, (SE)	LVCMOS	Bypasses the PLL and Switches the REF_IN or XTAL Frequency to all Outputs 1 = Bypass PLL, output is XTAL or REF_IN 0 = PLL Mode, 45KΩ pull-down
6	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Reference Input Mode 0 = REF_IN, 1 = XTAL, 45KΩ pull-up
7, 12, 15, 19	TEST	I, (SE)	LVCMOS	Test Pins. Do Not Connect These Pins to Anything

Pin Description (Continued)

8	VDD	PWR		Power Supply
9	REF_IN	I, (SE)	LVCMOS	Reference Clock Input
10	XIN	I, (SE)	crystal	Crystal Input, no load caps needed. See Fig. 6.
11	XOUT	O, (SE)	crystal	Crystal Output, no load caps needed. See Fig. 6.
13	VSS	I, (SE)		This Pin is not a Power Supply Ground, but MUST be Tied to VSS
14	VSS (Exposed Pad)	PWR		Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
18	VDDO1	PWR		Power Supply for Outputs Q0 and Q1
22	VSSO1	PWR		Power Supply Ground for Outputs Q0 and Q1

Truth Table

PLL_BYPASS	XTAL_SEL	INPUT	OUTPUT
0	–	–	PLL
1	–	–	XTAL/REF_IN
–	0	REF_IN	–
–	1	XTAL	–

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at hbwhelp@micrel.com

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) .....+4.6V
Input Voltage (V_{IN})..... –0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20sec.)..... 260°C
Case Temperature..... 115°C
Storage Temperature (T_S) ..... –65°C to +150°

Operating Ratings[2]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +2.375V to +3.465V
Ambient Temperature (T_A)..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air.....50°C/W
QFN (ψ_{JB})
Junction-to-Board.....32°C/W

DC Electrical Characteristics[4]

V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDO}	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, V_{DDO}	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD}	Supply current V_{DD} + V_{DDO} Outputs open	644MHz - 4 Diff LVDS outputs	-	204	240	mA

LVCMOS INPUT (XTAL_SEL, PLL_Bypass) DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IN}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

LVDS OUTPUT DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	Figure 1	275	350	475	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF Load [6]		Fundamental, Parallel Resonant		
Frequency			20.141601		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	5	pF
Correlation Drive Level			10	100	uW

AC Electrical Characteristics[4, 5, 6]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

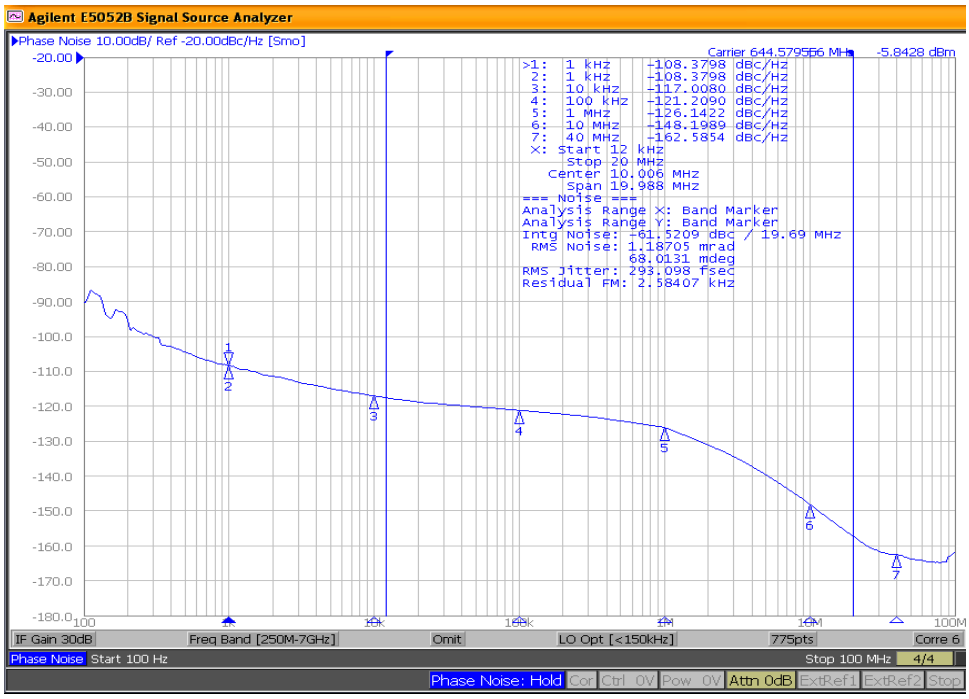
T_A = –40°C to +85°C. R_L = 100Ω across Q and /Q

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency			644.53125		MHz
T_R/T_F	LVDS Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle		48	50	52	%
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter	Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz)		114 293		fs
	Spurious Noise Components	20.141MHz reference Reference 2nd harmonic Reference 3rd harmonic		-82 -78 -85		dBc

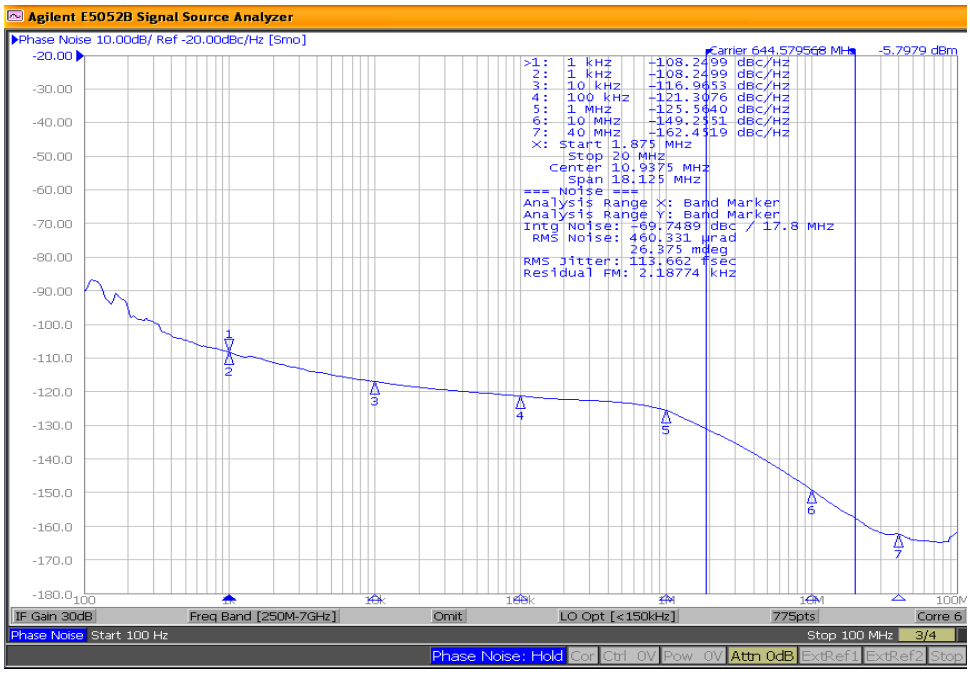
Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.
5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
6. See Application note, “Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers” for further details.
7. Measured using 20.141MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Phase Noise Plots



Phase Noise Plot: 644.53125MHz, 12KHz - 20MHz 293 Fs



Phase Noise Plot: 644.53125MHz, 1.875MHz - 20MHz 114 Fs

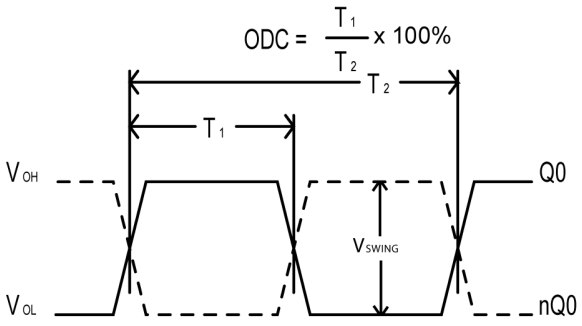


Figure 1. Duty Cycle Timing

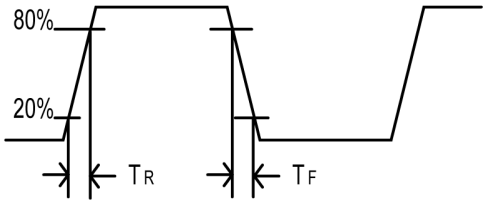


Figure 2. All Outputs Rise/Fall Time

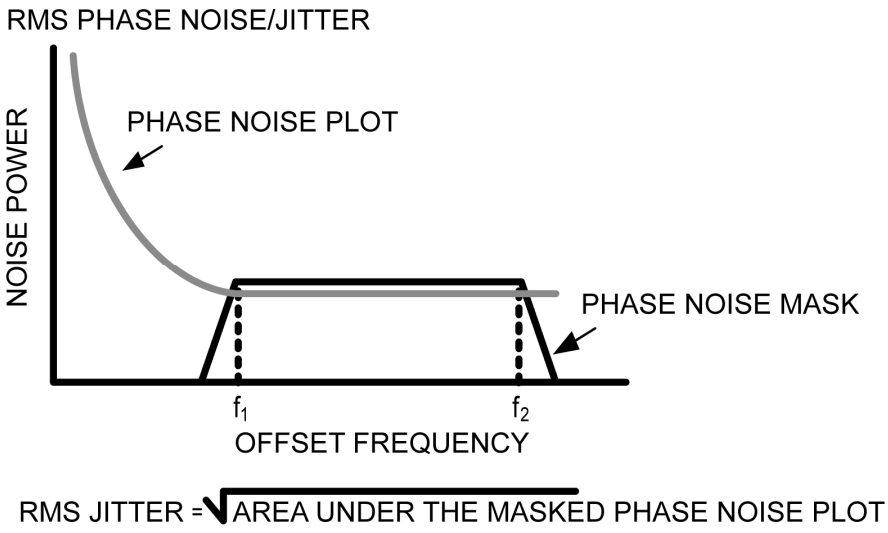


Figure 3. RMS Phase/Noise/Jitter

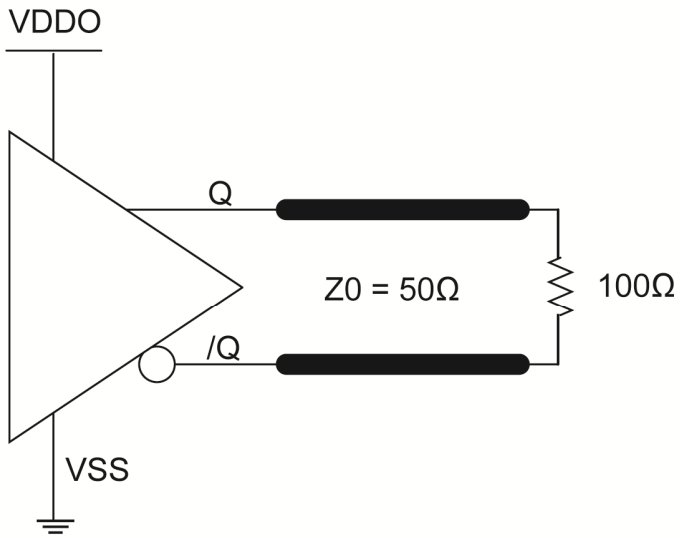


Figure 4. LVDS Output Load and Test Circuit

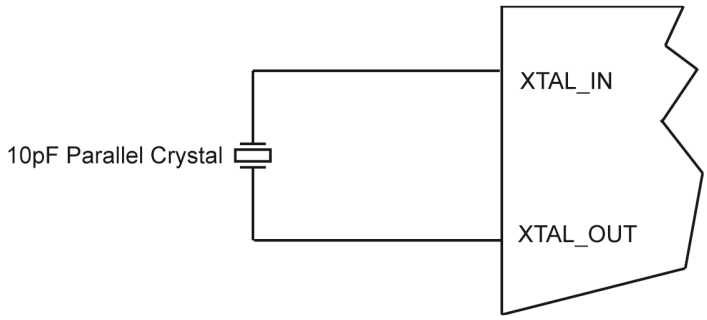
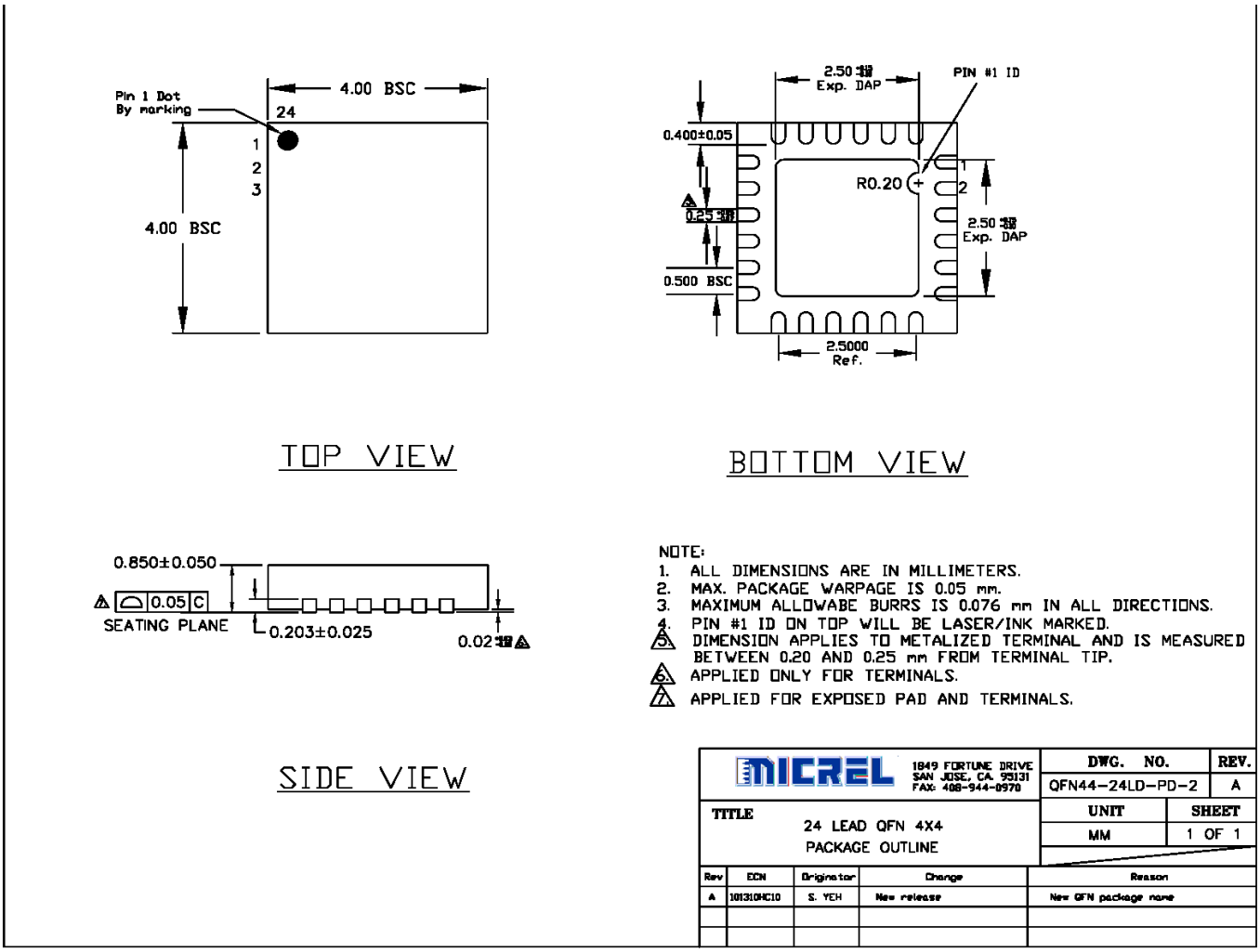


Figure 5. Crystal Input Interface

Package Information



24-Pin QFN

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