THE DATASHEET OF

SI5351A-B06302-GMR

www.win-source.net 0086-755-83957316

Si5351A/B/C-B

I²C-Programmable Any-Frequency CMOS Clock Generator + VCXO

Features

- https://www.skyworksinc.com/Products/Timing/CMOS-Clock-Generators
- Generates up to eight non-integer-related frequencies from 2.5 kHz to 200 MHz
- I²C user definable configuration
- Exact frequency synthesis at each output (0 ppm error)
- Highly linear VCXO
- Optional clock input (CLKIN)
- Low output period jitter: < 70 ps pp, typ
- Configurable spread spectrum selectable at each output
- Operates from a low-cost, fixed frequency crystal: 25 or 27 MHz
- Supports static phase offset
- Programmable rise/fall time control
- Glitchless frequency changes
- Separate voltage supply pins provide level translation:
- Core VDD: 2.5 or 3.3 V
- Output VDDO: 1.8, 2.5, or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption
- Adjustable output delay
- Available in three packages types:
- 10-MSOP: 3 outputs
- 16-QFN (3x3 mm): 4 outputs
- 20-QFN (4x4 mm): 8 outputs
- PCIE Gen 1 compatible
- Supports HCSL compatible swing

Applications

- Audio/video equipment, gaming
- Printers, scanners, projectors
- Handheld Instrumentation
- Laser range finder
- Residential gateways
- Networking/communication
- Servers, storage
- XO replacement

10-MSOP

16-QFN

20-QFN

Ordering Information:
See page 34

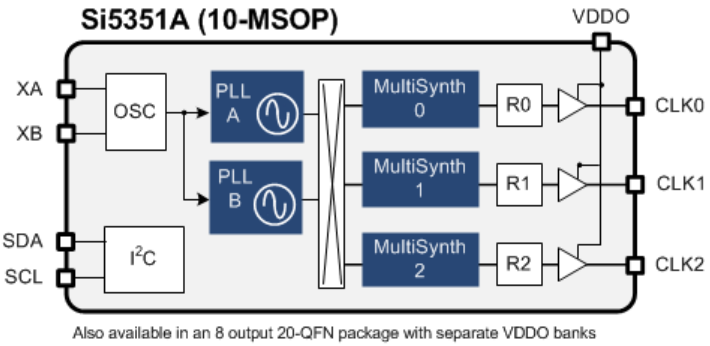
Description

The Si5351 is an I²C configurable clock generator that is ideally suited for replacing crystals, crystal oscillators, VCXOs, phase-locked loops (PLLs), and fanout buffers in cost-sensitive applications.

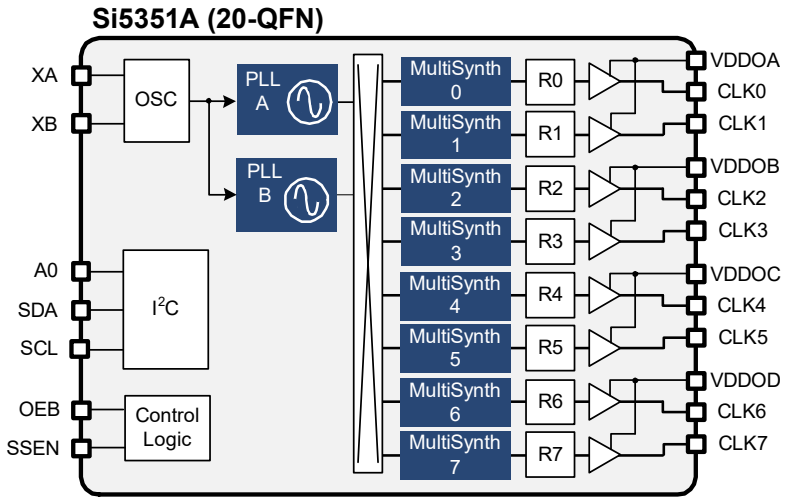
Based on a PLL/VCXO + high resolution MultiSynth fractional divider architecture, the Si5351 can generate any frequency up to 200 MHz on each of its outputs with 0 ppm error. Three versions of the Si5351 are available to meet a wide variety of applications.

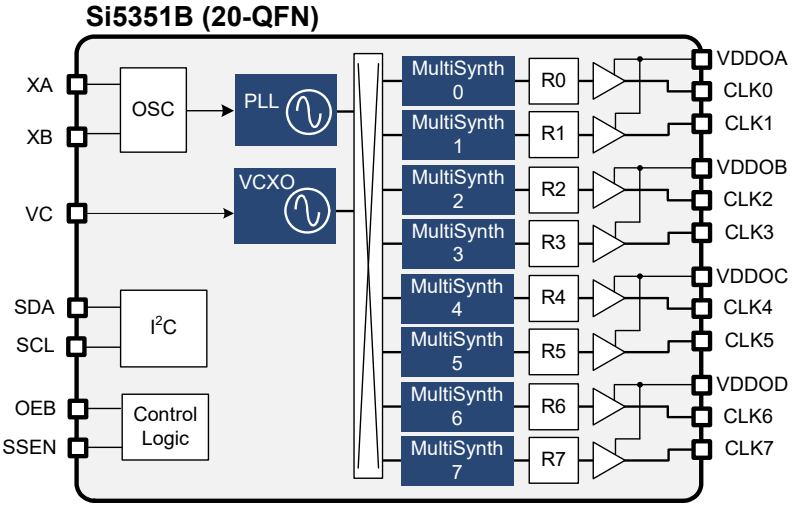
The Si5351A generates up to 8 free-running clocks using an internal oscillator for replacing crystals and crystal oscillators. The Si5351B adds an internal VCXO and provides the flexibility to replace both free-running clocks and synchronous clocks. It eliminates the need for higher cost, custom pullable crystals while providing reliable operation over a wide tuning range. The Si5351C offers the same flexibility but synchronizes to an external reference clock (CLKIN).

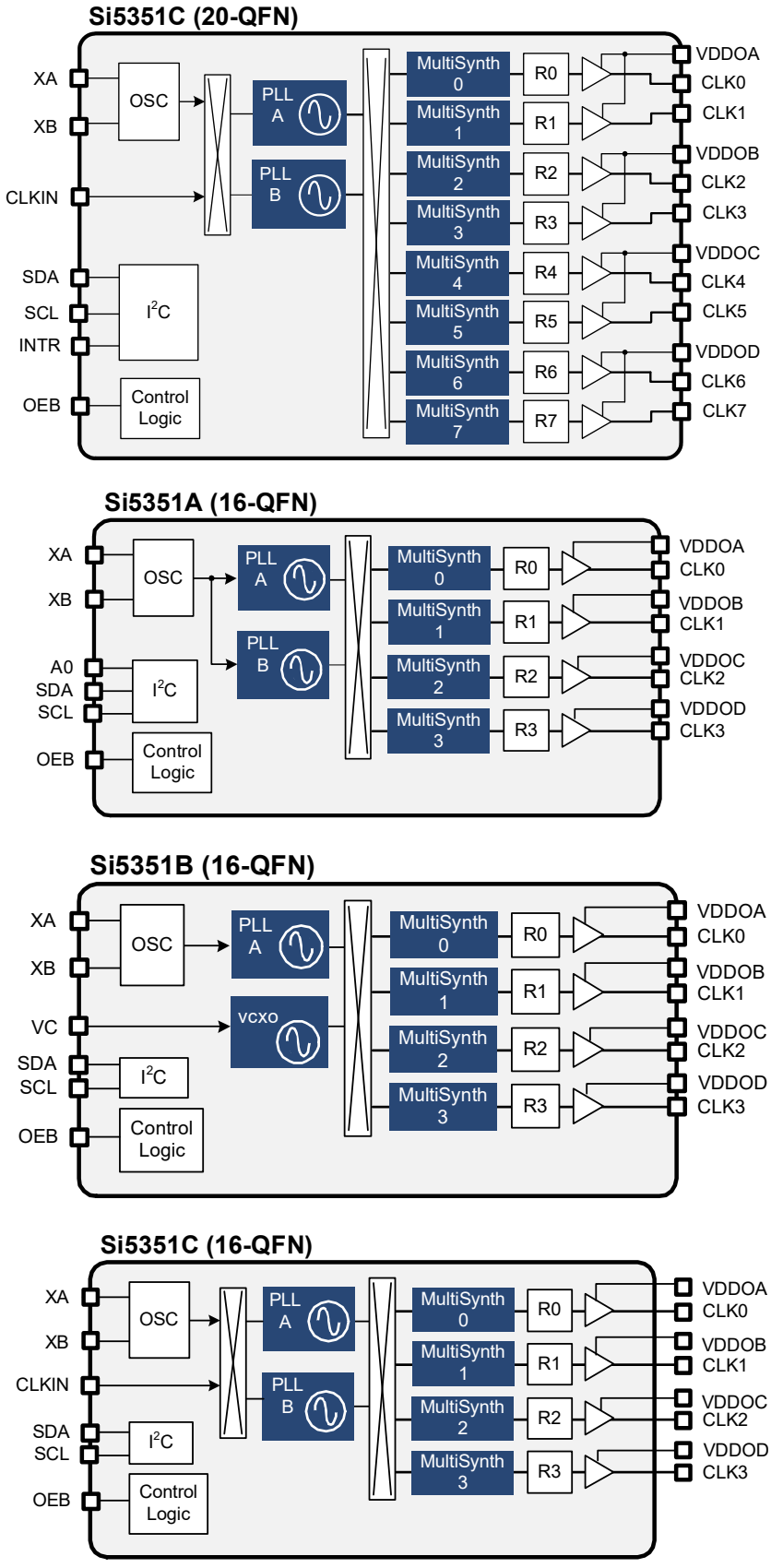
Functional Block Diagrams



Also available in an 8 output 20-QFN package with separate VDDO banks






Si5351C (20-QFN)
XA
XB
CLKIN
SDA
SCL
INTR
OEB
OSC
I2C
Control Logic
PLL A
PLL B
MultiSynth 0
MultiSynth 1
MultiSynth 2
MultiSynth 3
MultiSynth 4
MultiSynth 5
MultiSynth 6
MultiSynth 7
R0
R1
R2
R3
R4
R5
R6
R7
VDDOA
CLK0
CLK1
VDDOB
CLK2
CLK3
VDDOC
CLK4
CLK5
VDDOD
CLK6
CLK7
Si5351A (16-QFN)
XA
XB
A0
SDA
SCL
OEB
OSC
I2C
Control Logic
PLL A
PLL B
MultiSynth 0
MultiSynth 1
MultiSynth 2
MultiSynth 3
R0
R1
R2
R3
VDDOA
CLK0
VDDOB
CLK1
VDDOC
CLK2
VDDOD
CLK3
Si5351B (16-QFN)
XA
XB
VC
SDA
SCL
OEB
OSC
I2C
Control Logic
PLL A
VCXO
MultiSynth 0
MultiSynth 1
MultiSynth 2
MultiSynth 3
R0
R1
R2
R3
VDDOA
CLK0
VDDOB
CLK1
VDDOC
CLK2
VDDOD
CLK3
Si5351C (16-QFN)
XA
XB
CLKIN
SDA
SCL
OEB
OSC
I2C
Control Logic
PLL A
PLL B
MultiSynth 0
MultiSynth 1
MultiSynth 2
MultiSynth 3
R0
R1
R2
R3
VDDOA
CLK0
VDDOB
CLK1
VDDOC
CLK2
VDDOD
CLK3

1. Ordering Guide

Table 1. Si5350/51 Ordering Guide[1,2]

Part Number	I²C or Pin	Frequency Reference	Programmed?	Outputs	Datasheet
Si5351A-B-GT	I²C	XTAL only	Blank	3	Si5351A/B/C-B
Si5351A-B-GM1	I²C	XTAL only	Blank	4	Si5351A/B/C-B
Si5351B-B-GM1	I²C	XTAL and/or Voltage	Blank	4	Si5351A/B/C-B
Si5351C-B-GM1	I²C	XTAL and/or CLKIN	Blank	4	Si5351A/B/C-B
Si5351A-B-GM	I²C	XTAL only	Blank	8	Si5351A/B/C-B
Si5351B-B-GM	I²C	XTAL and/or Voltage	Blank	8	Si5351A/B/C-B
Si5351C-B-GM	I²C	XTAL and/or CLKIN	Blank	8	Si5351A/B/C-B
Si5351A-Bxxxxx-GT	I²C	XTAL only	Factory Preprogrammed	3	Si5351A/B/C-B
Si5351A-Bxxxxx-GM1	I²C	XTAL only	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351B-Bxxxxx-GM1	I²C	XTAL and/or Voltage	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351C-Bxxxxx-GM1	I²C	XTAL and/or CLKIN	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351A-Bxxxxx-GM	I²C	XTAL only	Factory Preprogrammed	8	Si5351A/B/C-B
Si5351B-Bxxxxx-GM	I²C	XTAL and/or Voltage	Factory Preprogrammed	8	Si5351A/B/C-B
Si5351C-Bxxxxx-GM	I²C	XTAL and/or CLKIN	Factory Preprogrammed	8	Si5351A/B/C-B
Si5350A-Bxxxxx-GT	Pin	XTAL only	Factory Preprogrammed	3	Si5350A-B
Si5350A-Bxxxxx-GM1	Pin	XTAL only	Factory Preprogrammed	4	Si5350A-B
Si5350A-Bxxxxx-GM	Pin	XTAL only	Factory Preprogrammed	8	Si5350A-B
Si5350B-Bxxxxx-GT	Pin	XTAL and/or Voltage	Factory Preprogrammed	3	Si5350B-B
Si5350B-Bxxxxx-GM1	Pin	XTAL and/or Voltage	Factory Preprogrammed	4	Si5350B-B
Si5350B-Bxxxxx-GM	Pin	XTAL and/or Voltage	Factory Preprogrammed	8	Si5350B-B
Si5350C-Bxxxxx-GT	Pin	XTAL and/or CLKIN	Factory Preprogrammed	3	Si5350C-B
Si5350C-Bxxxxx-GM1	Pin	XTAL and/or CLKIN	Factory Preprogrammed	4	Si5350C-B
Si5350C-Bxxxxx-GM	Pin	XTAL and/or CLKIN	Factory Preprogrammed	8	Si5350C-B

Notes:
1. XTAL = 25/27 MHz, Voltage = 0 to VDD, CLKIN = 10 to 100 MHz. "xxxxx" = unique custom code.
2. Create custom, factory preprogrammed parts using ClockBuilder Pro.

2. Technical Support Resources

Table 2. Technical Support Resources

Resource	URL
Si5350/51 Frequently Asked Questions	https://www.skyworksinc.com/en/Products/Timing
ClockBuilder Pro (CBPro) Software	https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software
Si535x Development Kits	https://www.skyworksinc.com/en/Products/Timing/Evaluation-Kits/si535x-b20qfn-evb-evaluation-kit

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3. Electrical Specifications

Table 3. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		3.0	3.3	3.60	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		1.71	1.8	1.89	V
			2.25	2.5	2.75	V
			3.0	3.3	3.60	V

Notes: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
VDD and VDDOx can be operated at independent voltages.
Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD.

Table 4. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Enabled 3 outputs	—	22	35	mA
		Enabled 4 outputs	—	24	38	mA
		Enabled 8 outputs	—	27	45	mA
Output Buffer Supply Current (Per Output)*	I_{DDOx}	C_L = 5 pF	—	2.2	5.6	mA
Input Current	I_{CLKIN}	CLKIN, SDA, SCL Vin < 3.6 V	—	—	10	µA
	I_{VC}	VC	—	—	30	µA
Output Impedance	Z_O	3.3 V VDDO, default high drive	—	50	—	Ω

***Note:** Output clocks less than or equal to 100 MHz.

Table 5. AC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power-up Time	T_{RDY}	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	2	10	ms
Power-up Time, PLL Bypass Mode	T_{BYP}	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	0.5	1	ms
Output Enable Time	T_{OE}	From OEB pulled low to valid clock output, C_L = 5 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T_{FREQ}	f_{CLKn} > 1 MHz	—	—	10	µs
Output Phase Offset	P_{STEP}		—	333	—	ps/step
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread. Selectable in 0.1% steps.	–0.1	—	–2.5	%
		Center spread. Selectable in 0.1% steps.	±0.1	—	±1.5	%
Spread Spectrum Modulation Rate	SS_{MOD}		30	31.5	33	kHz
VCXO Specifications (Si5351B Only)						
VCXO Control Voltage Range	Vc		0	V_{DD}/2	V_{DD}	V
VCXO Gain (configurable)	Kv	Vc = 10–90% of V_{DD}, V_{DD} = 3.3 V	18	—	150	ppm/V
VCXO Control Voltage Linearity	KVL	Vc = 10–90% of V_{DD}	–5	—	+5	%
VCXO Pull Range (configurable)	PR	V_{DD} = 3.3 V*	±30	0	±240	ppm
VCXO Modulation Bandwidth			—	10	—	kHz
***Note:** Contact Skyworks Solutions for 2.5 V VCXO operation.						

Table 6. Input Clock Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		25	—	27	MHz
CLKIN Input Low Voltage	V_{IL}		–0.1	—	0.3 x V_{DD}	V
CLKIN Input High Voltage	V_{IH}		0.7 x V_{DD}	—	3.60	V
CLKIN Frequency Range	f_{CLKIN}		10	—	100	MHz

Table 7. Output Clock Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range[1]	F_{CLK}		0.0025	—	200	MHz
Load Capacitance	C_L		—	—	15	pF
Duty Cycle	DC	$F_{CLK} \leq$ 160 MHz, Measured at $V_{DD}/2$	45	50	55	%
		F_{CLK} > 160 MHz, Measured at $V_{DD}/2$	40	50	60	%
Rise/Fall Time	t_r	20%–80%, C_L = 5 pF, Default high drive strength	—	1	1.5	ns
	t_f		—	1	1.5	ns
Output High Voltage	V_{OH}	C_L = 5 pF	V_{DD} – 0.6	—	—	V
Output Low Voltage	V_{OL}		—	—	0.6	V
Period Jitter[2,3]	J_{PER}	16, 20-QFN, 4 outputs running, 1 per VDDO	—	40	95	ps, pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	ps, pk-pk
Cycle-to-Cycle Jitter[2,3]	J_{CC}	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps, pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	ps, pk
Period Jitter VCXO[2,3]	J_{PER_VCXO}	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	95	ps, pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	ps, pk-pk
Cycle-to-Cycle Jitter VCXO[2,3]	J_{CC_VCXO}	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps, pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	ps, pk

Notes:

1. Only two unique frequencies above 112.5 MHz can be simultaneously output.
2. Measured over 10K cycles. Jitter is only specified at the default high drive strength (50 Ω output impedance).
3. Jitter is highly dependent on device frequency configuration. Specifications represent a “worst case, real world” frequency plan; actual performance may be substantially better. Three-output 10 MSOP package measured with clock outputs of 74.25, 24.576, and 48 MHz. Eight-output 20-QFN package measured with clock outputs of 33.333, 74.25, 27, 24.576, 22.5792, 28.322, 125, and 48 MHz. Four-output 16-QFN package measured with clock outputs of 33.333, 27, 28.322, and 48 MHz.

Table 8. Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	25	—	27	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	W
Crystal Max Drive Level	d_L	100	—	—	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitance in addition to external 2 pF load capacitance (e.g., by using 4 pF capacitors on XA and XB).
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 9. I²C Specifications (SCL,SDA)[1]

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
LOW Level Input Voltage	V_{ILI2C}		–0.5	0.3 x V_{DDI2C}	–0.5	0.3 x V_{DDI2C}[2]	V
HIGH Level Input Voltage	V_{IHI2C}		0.7 x V_{DDI2C}	3.6	0.7 x V_{DDI2C}[2]	3.6	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		—	—	0.1	—	V
LOW Level Output Voltage (open drain or open collector) at 3 mA Sink Current	V_{OLI2C}[2]	V_{DDI2C}[2] = 2.5/3.3 V	0	0.4	0	0.4	V
Input Current	I_{II2C}		–10	10	–10	10	µA
Capacitance for Each I/O Pin	C_{II2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus Timeout	T_{TO}	Timeout Enabled	25	35	25	35	ms

Notes:
1. Refer to NXP's UM10204 I²C-bus specification and user manual, revision 03.
2. Only I²C pullup voltages (VDDI2C) of 2.25 to 3.63 V are supported.

Table 10. Thermal Characteristics (2-Layer Board)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1]	10-MSOP	150	°C/W
			16-QFN	103	°C/W
			20-QFN	74.9	°C/W
Thermal Resistance Junction to Board	Ψ_{JB}	Still Air[1]	10-MSOP	82	°C/W
			16-QFN	37	°C/W
			20-QFN	9.94	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}	Still Air[1]	10-MSOP	0.84	°C/W
			16-QFN	4.26	°C/W
			20-QFN	1.3	°C/W

Notes:
1. Based on environment and board designed per JESD51-2A and JESD51-3.

Table 11. Thermal Characteristics (4-Layer Board)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1]	10-MSOP	126	°C/W
			16-QFN	65	°C/W
			20-QFN	41	°C/W
Thermal Resistance Junction to Board	θ_{JB}	Junction to Board[2]	10-MSOP	84	°C/W
			16-QFN	48	°C/W
			20-QFN	16	°C/W
	Ψ_{JB}	Still Air[1]	10-MSOP	83	°C/W
			16-QFN	31	°C/W
			20-QFN	8.1	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}	Still Air[1]	10-MSOP	0.74	°C/W
			16-QFN	3.8	°C/W
			20-QFN	0.98	°C/W

Notes:
1. Based on environment and board designed per JESD51-2A, JESD51-5, and JESD51-7.
2. Based on conditions set in JESD51-8.

Table 12. Thermal Characteristics (Junction-to-Case)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Case[1]	θ_{JC}	Still Air	10-MSOP	36	°C/W
			16-QFN	82	°C/W
			20-QFN	51	°C/W

Notes:
1. Based on board designed per JESD51-1 (Top center of packages used).

Table 13. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	V_{IN_CLKIN}	CLKIN, SCL, SDA	–0.5 to 3.8	V
	V_{IN_VC}	VC	–0.5 to (VDD+0.3)	V
	$V_{IN_XA/B}$	Pins XA, XB	–0.5 to 1.3 V	V
Junction Temperature	T_J		–55 to 150	°C
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[2]	T_P		20–40	Sec

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

4. Functional Description

The Si5351 is a versatile I^2C programmable clock generator that is ideally suited for replacing crystals, crystal oscillators, VCXOs, PLLs, and buffers. A block diagram showing the general architecture of the Si5351 is shown in Figure 1. The device consists of an input stage, two synthesis stages, and an output stage.

The input stage accepts an external crystal (XTAL), a control voltage input (VC), or a clock input (CLKIN) depending on the version of the device (A/B/C). The first stage of synthesis multiplies the input frequencies to an high-frequency intermediate clock, while the second stage of synthesis uses high resolution MultiSynth fractional dividers to generate the desired output frequencies. Additional integer division is provided at the output stage for generating output frequencies as low as 2.5 kHz. Crosspoint switches at each of the synthesis stages allows total flexibility in routing any of the inputs to any of the outputs.

Because of this high resolution and flexible synthesis architecture, the Si5351 is capable of generating synchronous or free-running non-integer related clock frequencies at each of its outputs, enabling one device to synthesize clocks for multiple clock domains in a design.

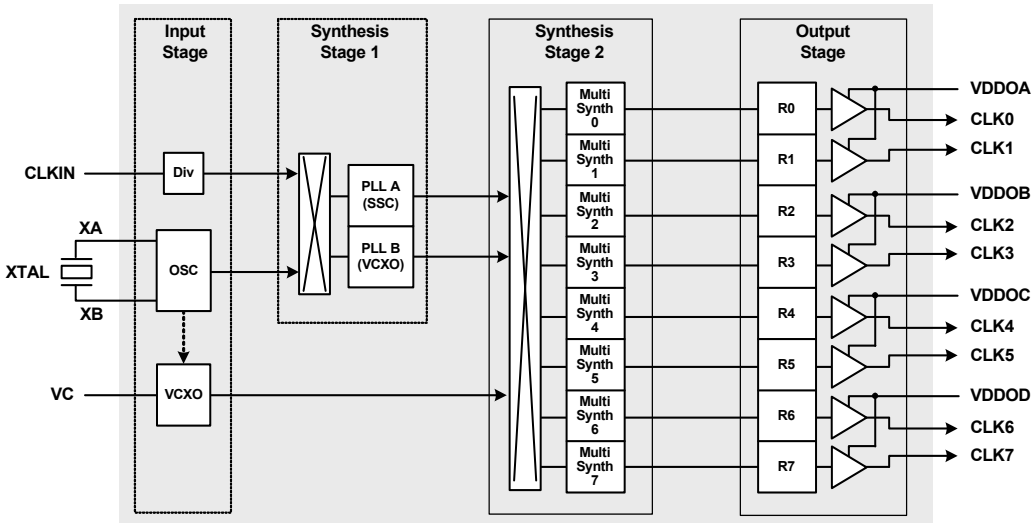


Figure 1. Si5351 Block Diagram

4.1. Input Stage

4.1.1. Crystal Inputs (XA, XB)

The Si5351 uses a fixed-frequency standard AT-cut crystal as a reference to the internal oscillator. The output of the oscillator can be used to provide a free-running reference to one or both of the PLLs for generating asynchronous clocks. The output frequency of the oscillator will operate at the crystal frequency, either 25 MHz or 27 MHz. The crystal is also used as a reference to the VCXO to help maintain its frequency accuracy.

Internal load capacitors are provided to eliminate the need for external components when connecting a crystal to the Si5351. The total internal XTAL load capacitance (C_L) can be selected to be 0, 6, 8, or 10 pF. Crystals with alternate load capacitance requirements are supported using additional external load capacitance ≤ 2 pF (e.g., by using ≤ 4 pF capacitors on XA and XB) as shown in Figure 2. Refer to application note AN551 for crystal recommendations.

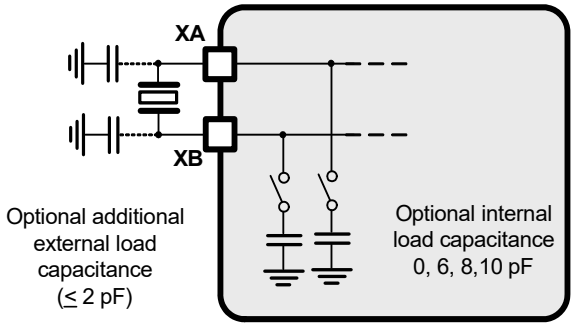


Figure 2. External XTAL with Optional Load Capacitors

4.1.2. External Clock Input (CLKIN)

The external clock input is used as a clock reference for the PLLs when generating synchronous clock outputs. CLKIN can accept any frequency from 10 to 100 MHz. A divider at the input stage limits the PLL input frequency to 30 MHz.

4.1.3. Voltage Control Input (VC)

The VCXO architecture of the Si5351B eliminates the need for an external pullable crystal. Only a standard, low-cost, fixed-frequency (25 or 27 MHz) AT-cut crystal is required.

The tuning range of the VCXO is configurable allowing for a wide variety of applications. Key advantages of the VCXO design in the Si5351 include high linearity, a wide operating range (linear from 10 to 90% of VDD), and reliable startup and operation. Refer to Table 5 on page 9 for VCXO specification details.

A unique feature of the Si5351B is its ability to generate multiple output frequencies controlled by the same control voltage applied to the VC pin. This replaces multiple PLLs or VCXOs that would normally be locked to the same reference. An example is illustrated in Figure 3 on page 16.

4.2. Synthesis Stages

The Si5351 uses two stages of synthesis to generate its final output clocks. The first stage uses PLLs to multiply the lower frequency input references to a high-frequency intermediate clock. The second stage uses high-resolution MultiSynth fractional dividers to generate the required output frequencies. Only two unique frequencies above 112.5 MHz can be simultaneously output. For example, 125 MHz (CLK0), 130 MHz (CLK1), and 150 MHz (CLKx) is not allowed. Note that multiple copies of frequencies above 112.5 MHz can be provided, for example, 125 MHz could be provided on four outputs (CLKS0-3) simultaneously with 130 MHz on four different outputs (CLKS4-7).

A crosspoint switch at the input of the first stage allows each of the PLLs to lock to the CLKIN or the XTAL input. This allows each of the PLLs to lock to a different source for generating independent free-running and synchronous clocks. Alternatively, both PLLs could lock to the same source. The crosspoint switch at the input of the second stage allows any of the MultiSynth dividers to connect to PLLA or PLLB. This flexible synthesis architecture allows any of the outputs to generate synchronous or non-synchronous clocks, with spread spectrum or without spread spectrum, and with the flexibility of generating non-integer related clock frequencies at each output.

All VCXO outputs are generated by PLLB only. The Multisynth high-resolution dividers synthesizes the VCXO output's center frequency up to 112.5 MHz. The center frequency is then controlled (or pulled) by the VC input. An interesting feature of the Si5351 is that the VCXO output can be routed to more than one MultiSynth divider. This creates a VCXO with multiple output frequencies controlled from one VC input as shown in Figure 3.

Frequencies down to 2.5 kHz can be generated by applying the R divider at the output of the Multisynth (see Figure 3 below).

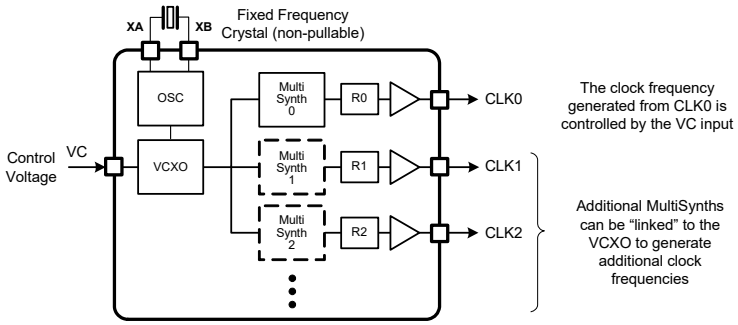


Figure 3. Using the Si5351 as a Multi-Output VCXO

4.3. Output Stage

An additional level of division (R) is available at the output stage for generating clocks as low as 2.5 kHz. All output drivers generate CMOS level outputs with separate output voltage supply pins (VDDOx) allowing a different voltage signal level (1.8, 2.5, or 3.3 V) at each of the four 2-output banks.

4.4. Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Note that spread spectrum is not available on clocks synchronized to PLLB or to the VCXO.

Spread spectrum can be set to “Always Enabled” when creating a custom part in ClockBuilder Pro. The Si5351A/B variants also have a SSEN control pin. See "4.5.2. Spread Spectrum Enable (SSEN)—Si5351A and Si5351B Only" on page 17 for more details.

The Si5351 supports several levels of spread spectrum allowing the designer to chose an ideal compromise between system performance and EMI compliance.

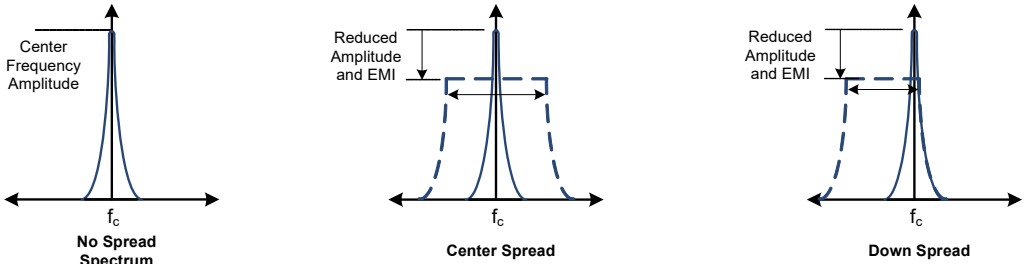


Figure 4. Available Spread Spectrum Profiles

4.5. Control Pins (OEB, SSEN)

The Si5351 offers control pins for enabling/disabling clock outputs and spread spectrum.

4.5.1. Output Enable (OEB)

The output enable pin allows enabling or disabling outputs clocks. Output clocks are enabled when the OEB pin is held low, and disabled when pulled high. When disabled, the output state is configurable as output high, output low, or high-impedance.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is pulled low. When OEB is pulled high, the clock is allowed to complete its full clock cycle before going into a disabled state.

4.5.2. Spread Spectrum Enable (SSEN)—Si5351A and Si5351B Only

This control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

4.6. Status Pins (INTR)

The Si5351C, in the 20-QFN package, includes an interrupt pin (INTR). This is an open drain status pin, requiring a 4.7 kΩ pullup resistor to Vdd. The pin will be pulled low when the Si5351C encounters an interrupt, such as crystal reference loss, external input clock loss, or loss-of-lock on either PLLA or PLLB.

ClockBuilder Pro will automatically configure the interrupt mask when a frequency plan is created, so irrelevant interrupts are ignored. For example, if a frequency plan does not use PLLB, the LOL_B interrupt will not cause the INTR pin to go low. The interrupt status registers can be viewed at any time through I^2C to get more details on the type of interrupt thrown. For more information on the status registers and the mask registers, see “AN619: Manually Generating an Si5351 Register Map” for 10MSOP and 20-QFN devices” or “AN1234: Manually Generating a Si5351 Register Map for 16-QFN Devices”.

5. I²C Interface

Many of the functions and features of the Si5351 are controlled by reading and writing to the RAM space using the I²C interface. The following is a list of the common features that are controllable through the I²C interface. For a complete listing of available I²C registers and programming steps, see AN619 or AN1234.

Read Status Indicators

- Crystal Reference Loss of signal, LOS_XTAL, reg0[3]
- CLKIN Loss of signal, LOS_CLKIN, reg0[4]
- PLLA and/or PLLB Loss of lock, LOL_A or LOL_B, reg0[6:5]

- Configuration of multiplication and divider values for the PLLs, MultiSynth dividers
- Configuration of the Spread Spectrum profile (down or center spread, modulation percentage)
- Control of the cross point switch selection for each of the PLLs and MultiSynth dividers
- Set output clock options
  - Enable/disable for each clock output
  - Invert/non-invert for each clock output
  - Output divider values (2^n, n=1.. 7)
  - Output state when disabled (stop hi, stop low, Hi-Z)
  - Output phase offset

The I²C interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 5. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification.

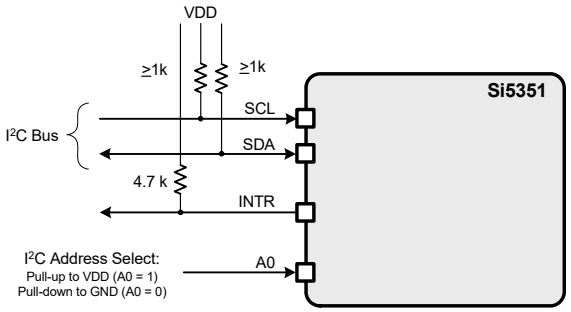


Figure 5. I²C and Control Signals

The 7-bit device (slave) address of the Si5351 consist of a 6-bit fixed address plus a user selectable LSB bit as shown in Figure 6. The LSB bit is selectable as 0 or 1 using the optional A0 pin which is useful for applications that require more than one Si5351 on a single I²C bus. Only the Si5351A 20-QFN and Si5351A 16-QFN have the A0 LSB pin option. If a part does not have the A0 pin, the default address is 0x60 with the A0 bit set to 0.

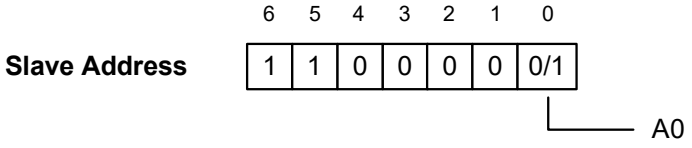


Figure 6. Si5351 I²C Slave Address

Data is transferred MSB first in 8-bit words as specified by the I2C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 7. A write burst operation is also shown where every additional data word is written using to an auto-incremented address.

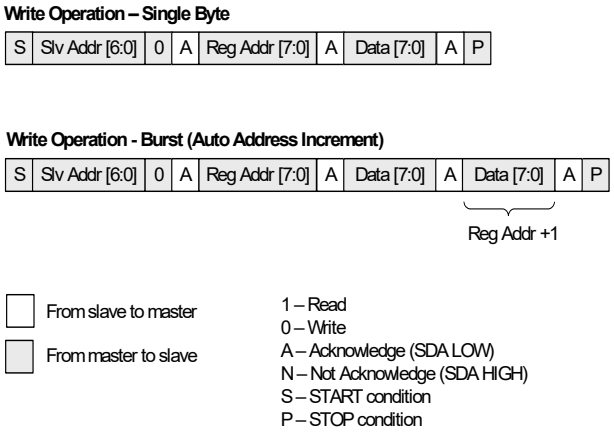


Figure 7. I2C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 8.

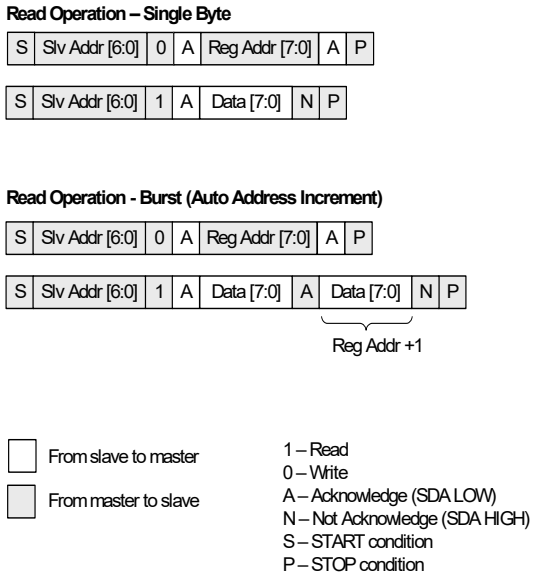


Figure 8. I2C Read Operation

AC and DC electrical specifications for the SCL and SDA pins are shown in Table 9. The timing specifications and timing diagram for the I2C bus is compatible with the I2C-Bus Standard. SDA timeout is supported for compatibility with SMBus interfaces.

6. Configuring the Si5351

The Si5351 is a highly flexible clock generator which is entirely configurable through its I^2C interface. The device's default configuration is stored in non-volatile memory (NVM) as shown in Figure 9. The NVM is a one time programmable memory (OTP) which can store a custom user configuration at power-up. This is a useful feature for applications that need a clock present at power-up (e.g., for providing a clock to a processor).

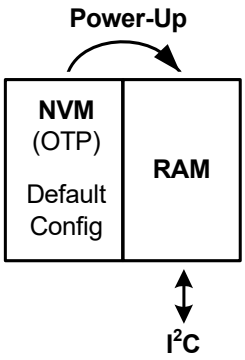


Figure 9. Si5351 Memory Configuration

During a power cycle the contents of the NVM are copied into random access memory (RAM), which sets the device configuration that will be used during normal operation. Any changes to the device configuration after power-up are made by reading and writing to registers in the RAM space through the I^2C interface.

6.1. Writing a Custom Configuration to RAM

To simplify device configuration, Skyworks Solutions has released the ClockBuilder Pro. The software serves two purposes: to configure the Si5351 with optimal configuration based on the desired frequencies and to control the EVB when connected to a host PC.

The optimal configuration can be saved from the software in text files that can be used in any system, which configures the device over I^2C. ClockBuilder Pro can be downloaded from https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software

Once the configuration file has been saved, the device can be programmed via I^2C by following the steps shown in Figure 10.

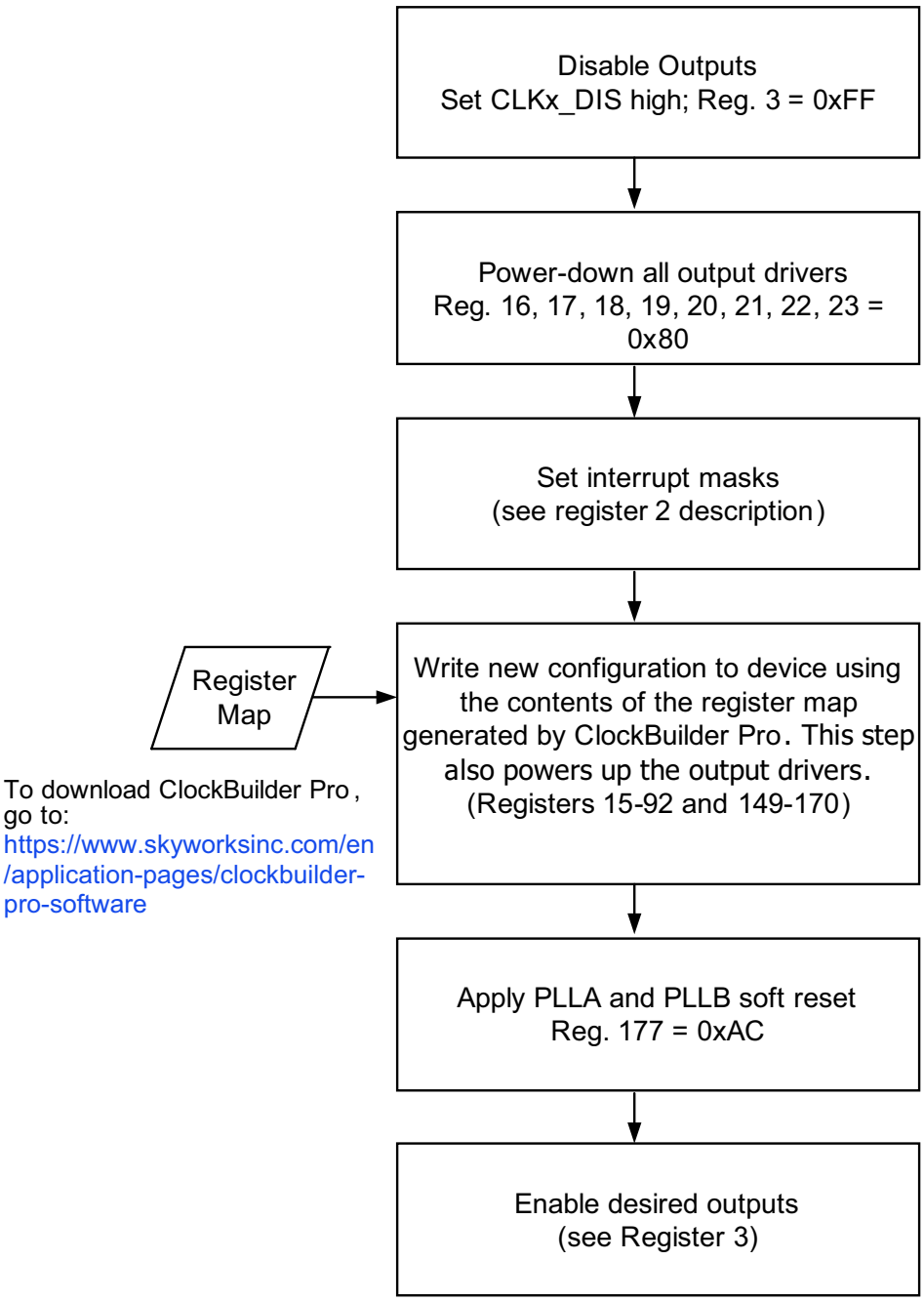


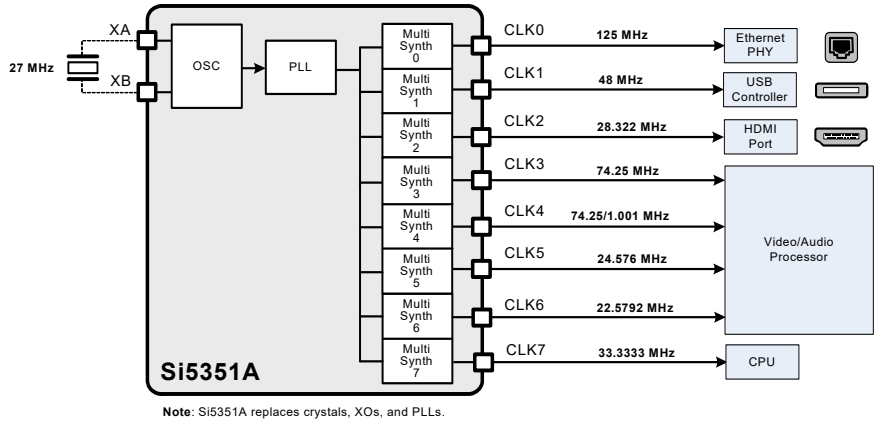
Figure 10. I²C Programming Procedure

6.2. Si5351 Application Examples

The Si5351 is a versatile clock generator which serves a wide variety of applications. The following examples show how it can be used to replace crystals, crystal oscillators, VCXOs, and PLLs.

6.3. Replacing Crystals and Crystal Oscillators

Using an inexpensive external crystal, the Si5351A can generate up to 8 different free-running clock frequencies for replacing crystals and crystal oscillators. A 4-output with separate VDDO for each output and a 3-output version are also available in small 16-QFN and 10-MSOP packages, respectively, for applications that require fewer clocks. An example is shown in Figure 11.

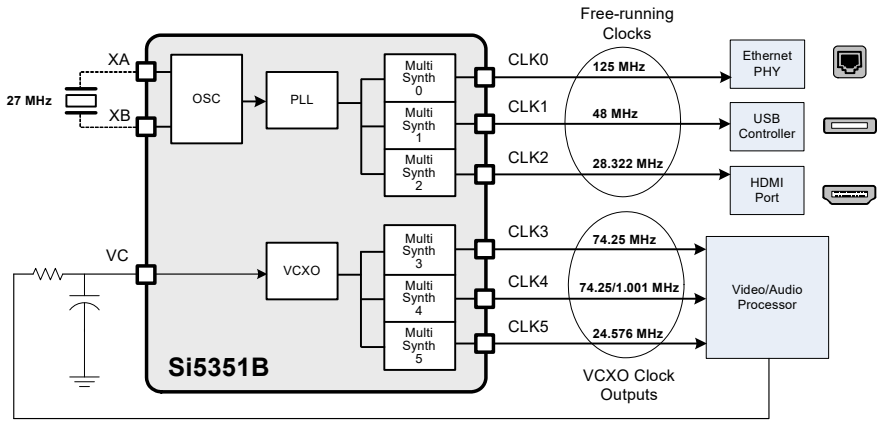


Note: Si5351A replaces crystals, XOs, and PLLs.

Figure 11. Using the Si5351A to Replace Multiple Crystals, Crystal Oscillators, and PLLs

6.4. Replacing Crystals, Crystal Oscillators, and VCXOs

The Si5351B combines free-running clock generation and a VCXO in a single package for cost sensitive video applications. An example is shown in Figure 12.



Note: F_{BW} = 10 kHz

Figure 12. Using the Si5351B to Replace Crystals, Crystal Oscillators, VCXOs, and PLLs

6.5. Replacing Crystals, Crystal Oscillators, and PLLs

The Si5351C generates synchronous clocks for applications that require a fully integrated PLL instead of a VCXO. Because of its dual PLL architecture, the Si5351C is capable of generating both synchronous and free-running clocks. An example is shown in Figure 13.

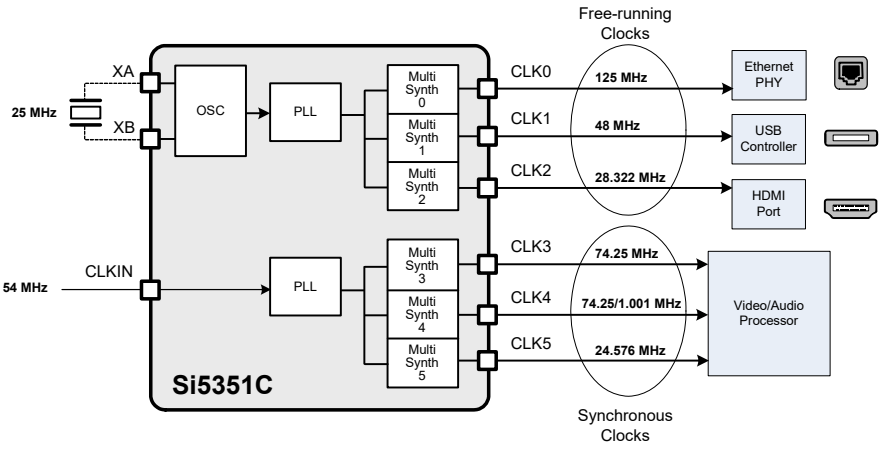
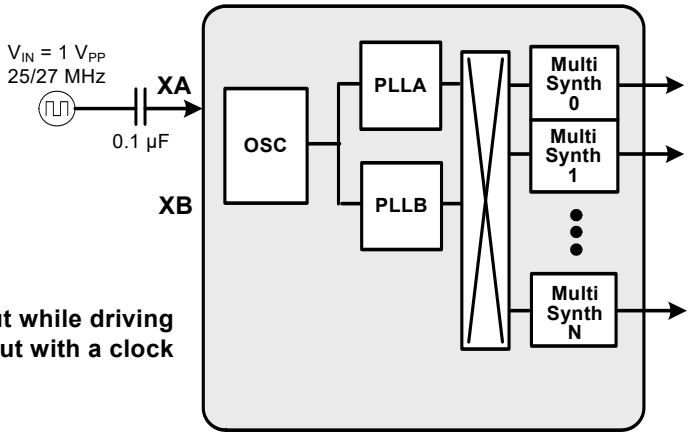


Figure 13. Using the Si5351C to Replace Crystals, Crystal Oscillators, and PLLs

6.6. Applying a Reference Clock at XTAL Input

The Si5351 can be driven with a clock signal through the XA input pin. This is especially useful when in need of generating clock outputs in two synchronization domains. With the Si5351C, one reference clock can be provided at the CLKIN pin and at XA.



Note: Float the XB input while driving the XA input with a clock

Figure 14. Si5351 Driven by a Clock Signal

6.7. HCSL Compatible Outputs

The Si5351 can be configured to support HCSL compatible swing when the VDDO of the output pair of interest is set to 2.5 V (i.e., VDDOA must be 2.5 V when using CLK0/1; VDDOB must be 2.5 V for CLK2/3 and so on).

The circuit in the figure below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair. See register setting CLKx_INV. This functionality is only supported for Si5351 in 10-MSOP or 20-QFN packages.

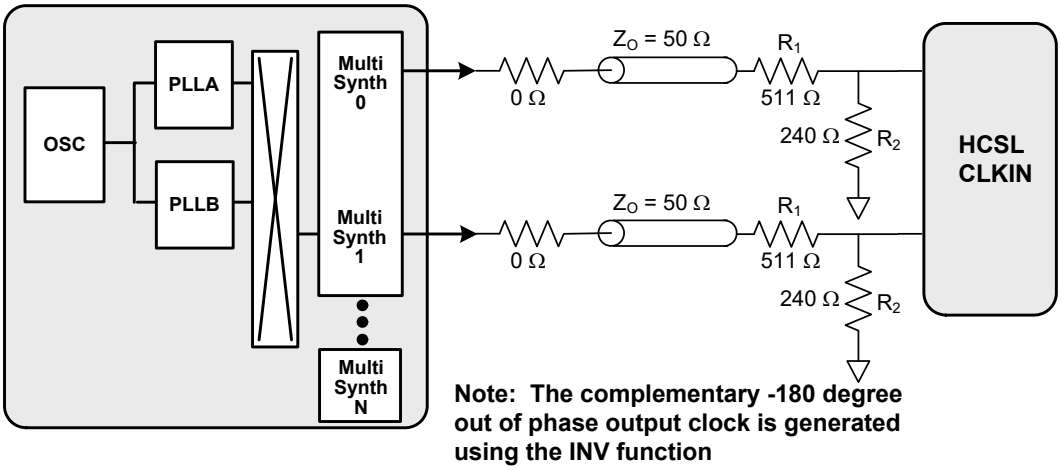


Figure 15. Si5351 Output is HCSL Compatible

7. Design Considerations

The Si5351 is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance. Refer to “AN554: Si5350/51 PCB Layout Guide” for additional layout recommendations.

7.1. Power Supply Decoupling/Filtering

The Si5351 has built-in power supply filtering circuitry and extensive internal Low Drop Out (LDO) voltage regulators to help minimize the number of external bypass components. All that is recommended is one 0.1 to 1.0 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDOx pins as possible without using vias.

7.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD. Unused VDDOx pins should be tied to VDD.

7.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

7.4. External Crystal Load Capacitors

The Si5351 provides the option of using internal and external crystal load capacitors. If internal load capacitance is insufficient, capacitors of value ≤ 2 pF may be used to increased equivalent load capacitance. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

7.5. Unused Pins

Unused voltage control pin should be tied to GND.

Unused CLKIN pin should be tied to GND.

Unused XA/XB pins should be left floating. Refer to "6.6. Applying a Reference Clock at XTAL Input" on page 23 when using XA as a clock input pin.

Unused output pins (CLK0–CLK7) should be left floating.

Unused VDDOx pins should be tied to VDD.

7.6. Trace Characteristics

The Si5351A/B/C features various output current drive strengths. It is recommended to configure the trace characteristics as shown in Figure 16 when the default high drive strength is used.

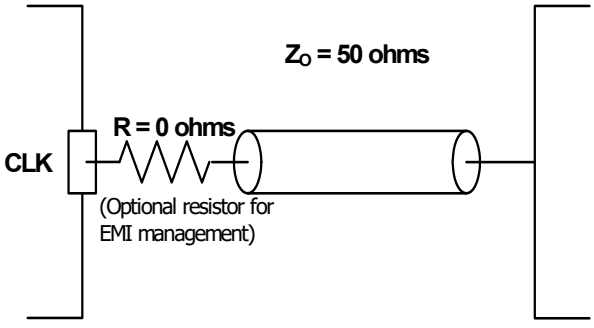


Figure 16. Recommended Trace Characteristics with Default Drive Strength Setting

8. Register Map Summary

For many applications, the Si5351's register values are easily configured using ClockBuilder Pro software. However, for customers interested in using the Si5351 in operating modes beyond the capabilities available with ClockBuilder Pro, see AN619 or AN1234.

9. Register Descriptions

Refer to either AN619 for 10MSOP and 20QFN devices or AN1234 for 16-QFN devices. These application notes provide detailed descriptions of the Si5351 registers and their use.

10. Si5351 Pin Descriptions

10.1. Si5351A 20-pin QFN

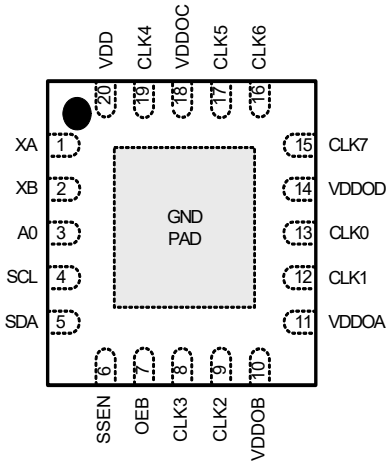


Figure 17. Si5351A 20-QFN Top View

Table 14. Si5351A Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
CLK0	13	O	Output clock 0.
CLK1	12	O	Output clock 1.
CLK2	9	O	Output clock 2.
CLK3	8	O	Output clock 3.
CLK4	19	O	Output clock 4.
CLK5	17	O	Output clock 5.
CLK6	16	O	Output clock 6.
CLK7	15	O	Output clock 7.
A0	3	I	I^2C address bit.
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
SSEN	6	I	Spread spectrum enable. High = enabled, Low = disabled.
OEB	7	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	P	Core voltage supply pin. See 7.2.
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1. See 7.2.
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3. See 7.2.
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5. See 7.2.
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7. See 7.2.
GND	Center Pad	P	Ground. Use multiple vias to ensure a solid path to GND.

1. I = Input, O = Output, P = Power.
2. Input pins are not internally pulled up.

10.2. Si5351B 20-Pin QFN

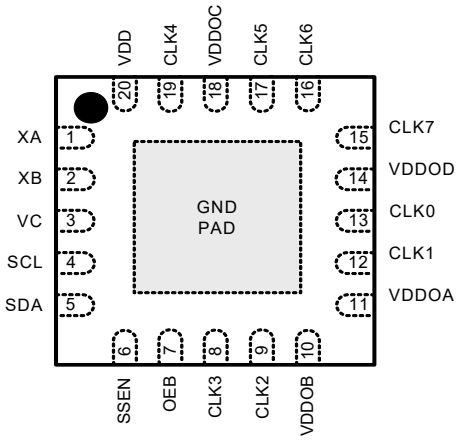


Figure 18. Si5351B 20-QFN Top View

Table 15. Si5351B Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	1	I	Input pin for external crystal
XB	2	I	Input pin for external crystal
CLK0	13	O	Output clock 0
CLK1	12	O	Output clock 1
CLK2	9	O	Output clock 2
CLK3	8	O	Output clock 3
CLK4	19	O	Output clock 4
CLK5	17	O	Output clock 5
CLK6	16	O	Output clock 6
CLK7	15	O	Output clock 7
VC	3	I	VCXO control voltage input
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
SSEN	6	I	Spread spectrum enable. High = enabled, Low = disabled.
OEB	7	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	P	Core voltage supply pin
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1. See 7.2
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3. See 7.2
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5. See 7.2
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7. See 7.2
GND	Center Pad	P	Ground

1. I = Input, O = Output, P = Power
2. Input pins are not internally pulled up.

10.3. Si5351C 20-Pin QFN

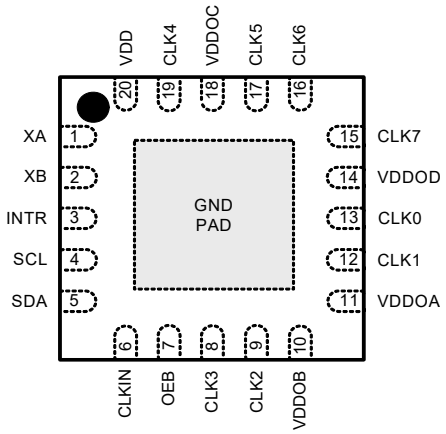


Figure 19. Si5351C 20-QFN Top View

Table 16. Si5351C Pin Descriptions

Pin Name	Pin Number 20-QFN	Pin Type[1]	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
CLK0	13	O	Output clock 0.
CLK1	12	O	Output clock 1.
CLK2	9	O	Output clock 2.
CLK3	8	O	Output clock 3.
CLK4	19	O	Output clock 4.
CLK5	17	O	Output clock 5.
CLK6	16	O	Output clock 6.
CLK7	15	O	Output clock 7.
INTR	3	O	Interrupt pin. Open drain active low output, requires a pull-up resistor greater than 4.7 kΩ.
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
CLKIN	6	I	PLL clock input.
OEB	7	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	P	Core voltage supply pin
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1. See 7.2
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3. See 7.2
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5. See 7.2
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7. See 7.2
GND	Center Pad	P	Ground.

Notes:
1. I = Input, O = Output, P = Power.
2. Input pins are not internally pulled up.

10.4. Si5351A 16-Pin QFN

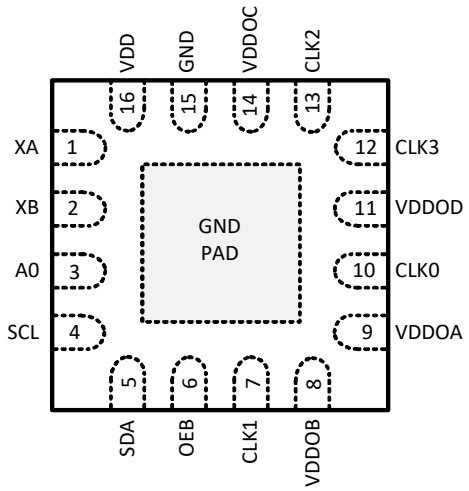


Figure 20. Si5351A 16-QFN Top View

Table 17. Si5351A Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
CLK0	10	O	Output Clock 0.
CLK1	7	O	Output Clock 1.
CLK2	13	O	Output Clock 2.
CLK3	12	O	Output Clock 3.
A0	3	I	I^2C address bit.
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
OEB	6	I	Output driver enable. Low = Enabled; High = Disabled.
VDD	16	P	Core voltage supply pin. See “7.2. Power Supply Sequencing”
VDDOA	9	P	Output voltage supply pin for CLK0. See “7.2. Power Supply Sequencing” .
VDDOB	8	P	Output voltage supply pin for CLK1. See “7.2. Power Supply Sequencing” .
VDDOC	14	P	Output voltage supply pin for CLK2. See “7.2. Power Supply Sequencing” .
VDDOD	11	P	Output voltage supply pin for CLK3. See “7.2. Power Supply Sequencing” .
GND	15	GND	Ground.
GND PAD	Center Pad	GND	Ground pad. Use multiple vias to ensure a solid path to Ground.

Notes:
1. I = Input, O = Output, P= Power, GND = Ground Input pins are not internally pulled up.

10.5. Si5351B 16-Pin QFN

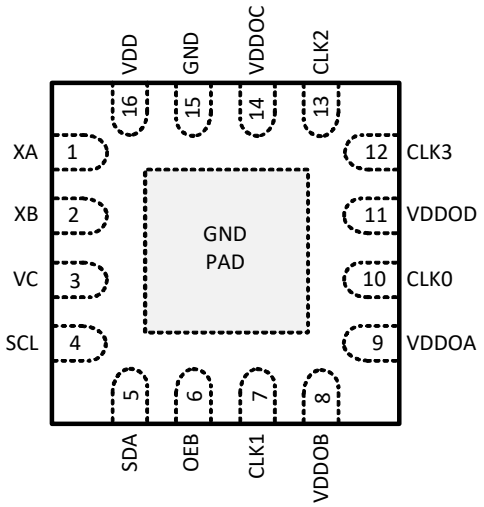


Figure 21. Si5351B 16-QFN Top View*

Table 18. Si5351B Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
CLK0	10	O	Output Clock 0.
CLK1	7	O	Output Clock 1.
CLK2	13	O	Output Clock 2.
CLK3	12	O	Output Clock 3.
VC	3	I	VCXO control voltage input
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
OEB	6	I	Output driver enable. Low = Enabled; High = Disabled.
VDD	16	P	Core voltage supply pin. See “7.2. Power Supply Sequencing”
VDDOA	9	P	Output voltage supply pin for CLK0. See “7.2. Power Supply Sequencing” .
VDDOB	8	P	Output voltage supply pin for CLK1. See “7.2. Power Supply Sequencing” .
VDDOC	14	P	Output voltage supply pin for CLK2. See “7.2. Power Supply Sequencing” .
VDDOD	11	P	Output voltage supply pin for CLK3. See “7.2. Power Supply Sequencing” .
GND	15	GND	Ground.
GND PAD	Center Pad	GND	Ground pad. Use multiple vias to ensure a solid path to Ground

Notes:
1. I = Input, O = Output, P= Power, GND = Ground Input pins are not internally pulled up.

10.6. Si5351C 16-Pin QFN

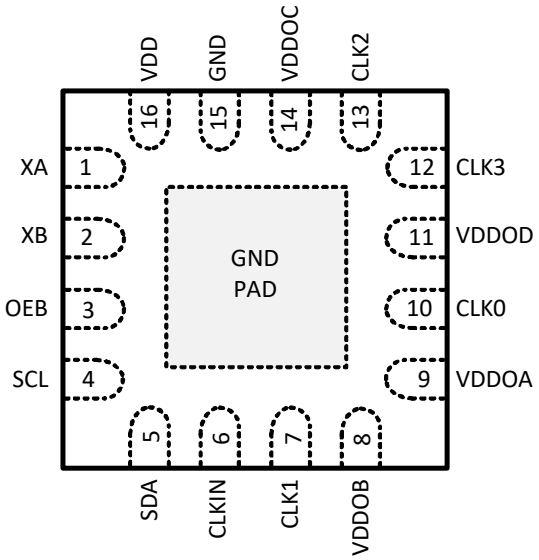


Figure 22. Si5351C 16-QFN Top View

Table 19. Si5351C Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
CLK0	10	O	Output Clock 0.
CLK1	7	O	Output Clock 1.
CLK2	13	O	Output Clock 2.
CLK3	12	O	Output Clock 3.
CLKIN	6	I	PLL clock input
SCL	4	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
OEB	3	I	Output driver enable. Low = Enabled; High = Disabled.
VDD	16	P	Core voltage supply pin. See “7.2. Power Supply Sequencing”
VDDOA	9	P	Output voltage supply pin for CLK0. See “7.2. Power Supply Sequencing”
VDDOB	8	P	Output voltage supply pin for CLK1. See “7.2. Power Supply Sequencing”
VDDOC	14	P	Output voltage supply pin for CLK2. See “7.2. Power Supply Sequencing”
VDDOD	11	P	Output voltage supply pin for CLK3. See “7.2. Power Supply Sequencing”
GND	15	GND	Ground.
GND PAD	Center Pad	GND	Ground pad. Use multiple vias to ensure a solid path to Ground.

Notes:
1. I = Input, O = Output, P= Power, GND = Ground Input pins are not internally pulled up.

10.7. Si5351A 10-Pin MSOP

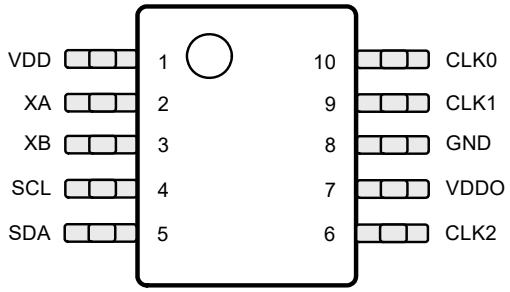


Figure 23. Si5351A 10-MSOP Top View

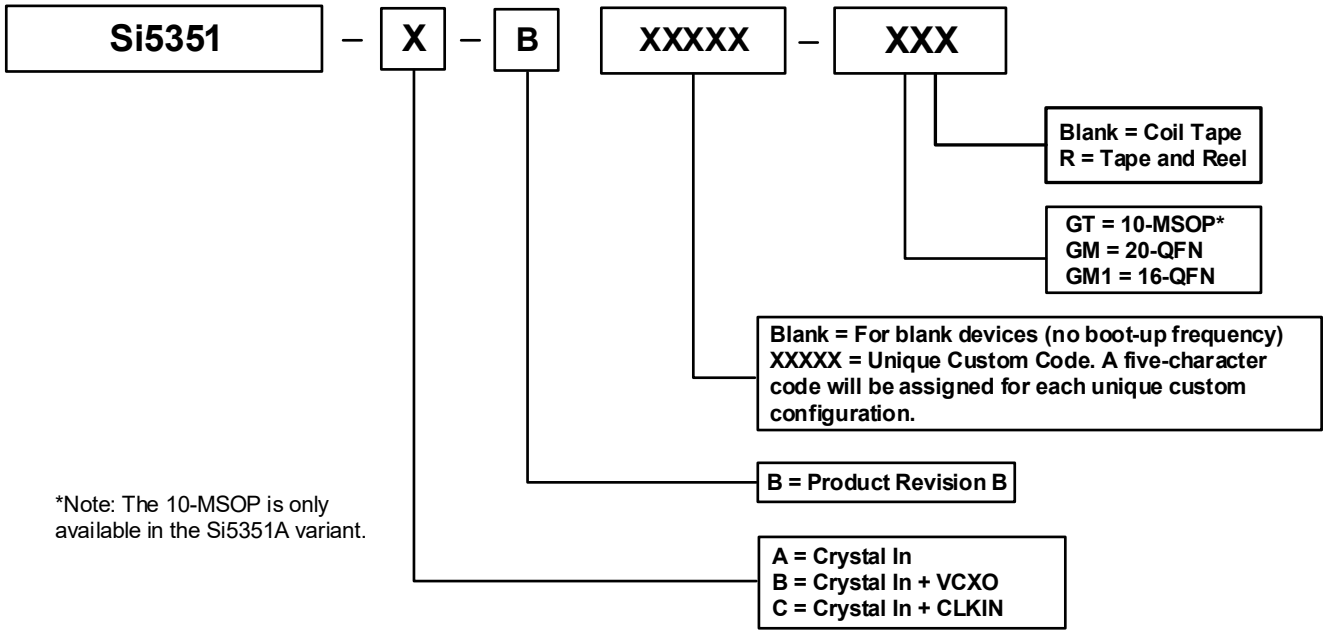
Table 20. Si5351A 10-MSOP Pin Descriptions

Pin Name	Pin Number	Pin Type*	Function
	10-MSOP		
XA	2	I	Input pin for external crystal.
XB	3	I	Input pin for external crystal.
CLK0	10	O	Output clock 0.
CLK1	9	O	Output clock 1.
CLK2	6	O	Output clock 2.
SCL	4	I	Serial clock input for the I^2C bus. This pin must be pulled-up using a pull-up resistor of at least 1 kΩ.
SDA	5	I/O	Serial data input for the I^2C bus. This pin must be pulled-up using a pull-up resistor of at least 1 kΩ.
VDD	1	P	Core voltage supply pin.
VDDO	7	P	Output voltage supply pin for CLK0, CLK1, and CLK2. See "7.2. Power Supply Sequencing" on page 25.
GND	8	P	Ground.
***Note:** I = Input, O = Output, P = Power			

11. Ordering Information

Factory pre-programmed Si5351 devices (e.g., with bootup frequencies) can be requested using the ClockBuilder Pro available at:https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software.
A unique part number is assigned to each custom configuration as indicated in Figure 24. Blank, un-programmed Si5351 devices (with no boot-up frequency) do not contain a custom code.

The Si5351x-B20QFN-EVB evaluation kit, along with ClockBuilder Pro, enables easy testing of any Si5351A/B/C frequency plan. ClockBuilder Pro makes it simple to emulate all three Si5351 packages, including the 10-MSOP, 20-QFN, and 16-QFN, on the same evaluation board.



Evaluation Boards

Si535x-B20QFN-EVB – For evaluation of:
Si5351A-B-GM (20-QFN)
Si5351B-B-GM (20-QFN)
Si5351C-B-GM (20-QFN)

Figure 24. Device Part Numbers

12. Packaging

12.1. 20-pin QFN Package Outline

Figure 25 shows the package details for the Si5351 in a 20-QFN package. Table 21 lists the values for the dimensions shown in the illustration.

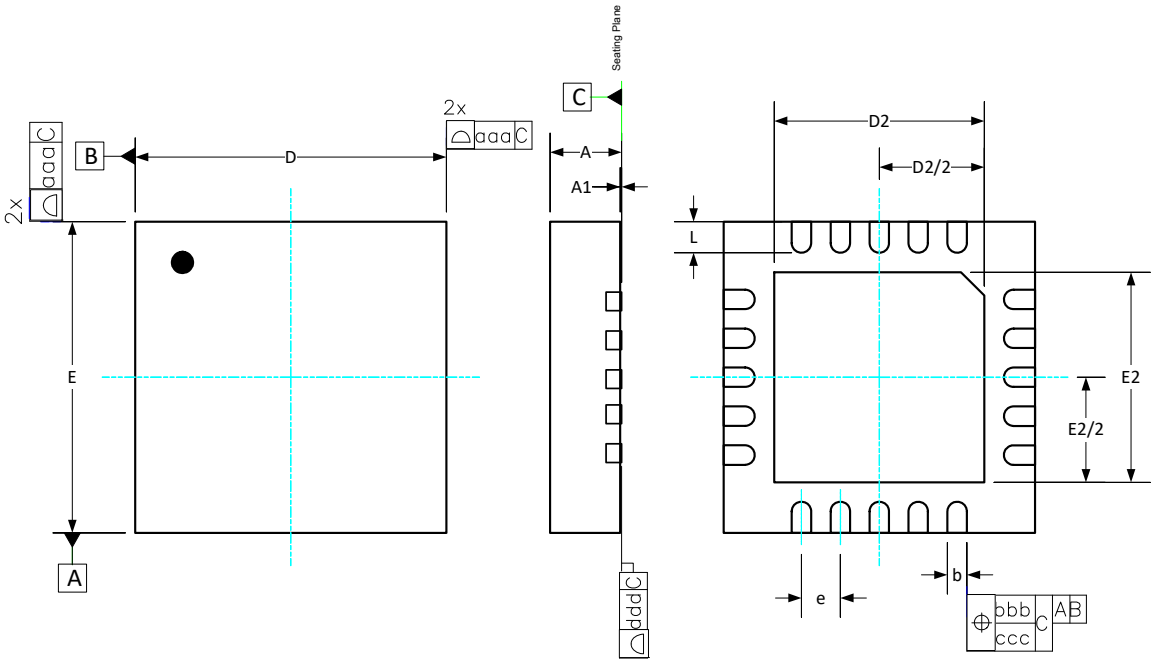


Figure 25. 20-Pin QFN Package Drawing

Table 21. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220, variation VGGD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.2. Land Pattern: 20-Pin QFN

Figure 26 shows the recommended land pattern details for the Si5351 in a 20-Pin QFN package. Table 22 lists the values for the dimensions shown in the illustration.

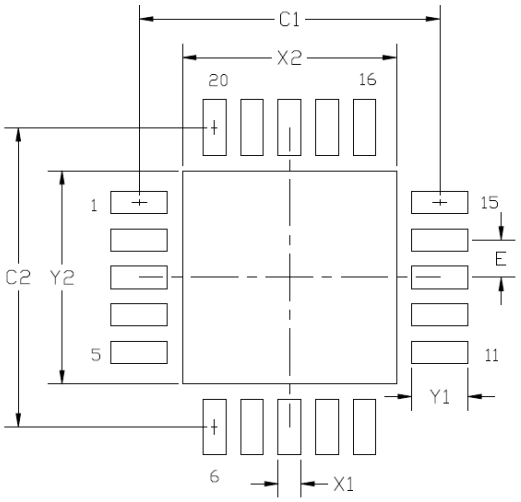


Figure 26. 20-Pin QFN Land Pattern

Table 22. PCB Land Pattern Dimensions

Symbol	Millimeters
C1	4.0
C2	4.0
E	0.50 BSC
X1	0.30
X2	2.70
Y1	0.80
Y2	2.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body components.

12.3. 16-Pin QFN Package Outline

Figure 27 shows the package details for the Si5351 in a 16-QFN package. Table 23 lists the values for the dimensions shown in the illustration.

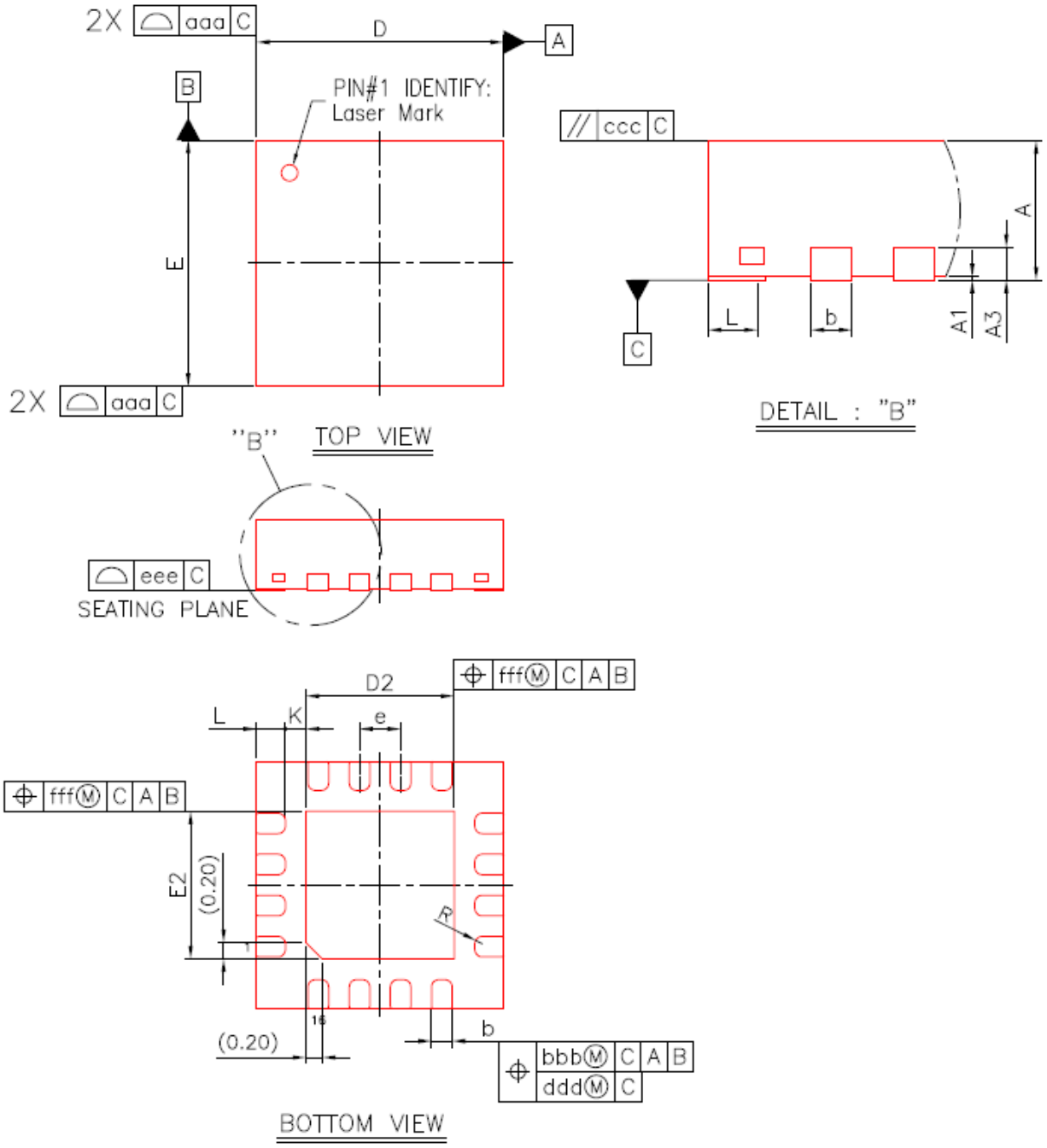


Figure 27. 16-Pin QFN Package Drawing

Table 23. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		3.0 BSC	
D2	1.70	1.80	1.90
e		0.50 BSC	
E		3.0 BSC	
E2	1.70	1.80	1.90
L	0.25	0.35	0.45
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.4. Land Pattern: 16-Pin QFN

Figure 28 shows the recommended land pattern details for the Si5351 in a 16-Pin QFN package. Table 24 lists the values for the dimensions shown in the illustration.

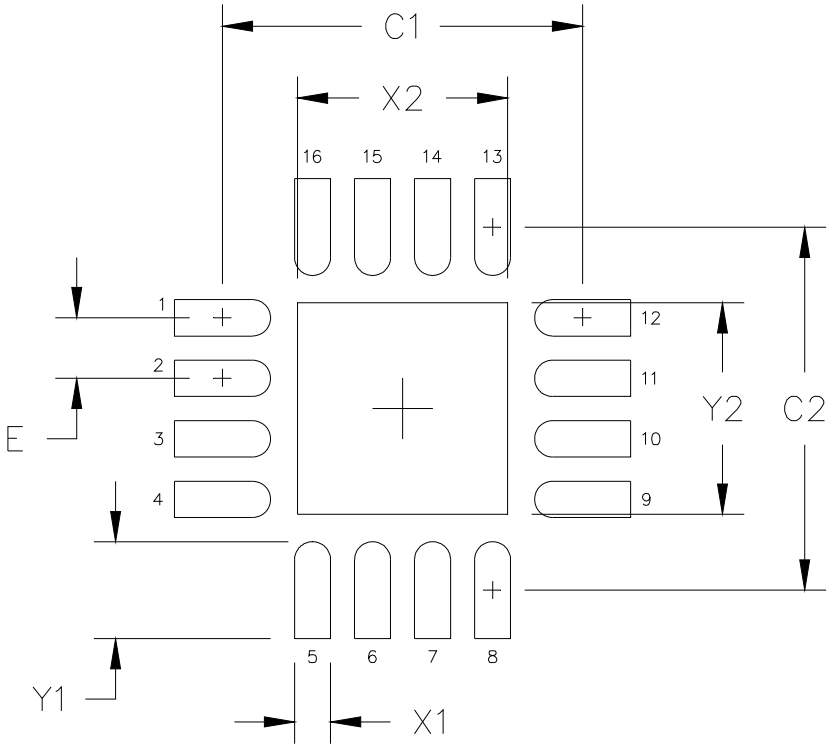


Figure 28. 16-Pin QFN Land Pattern

Table 24. PCB Land Pattern Dimensions

Symbol	Millimeters
C1	3.00
C2	3.00
E	0.50
X1	0.30
Y1	0.75
X2	1.80
Y2	1.80

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This land pattern design is based on IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2x2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body components.
11. The above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

12.5. 10-Pin MSOP Package Outline

Figure 29 illustrates the package details for the Si5351 in a 10-pin MSOP package. Table 25 lists the values for the dimensions shown in the illustration.

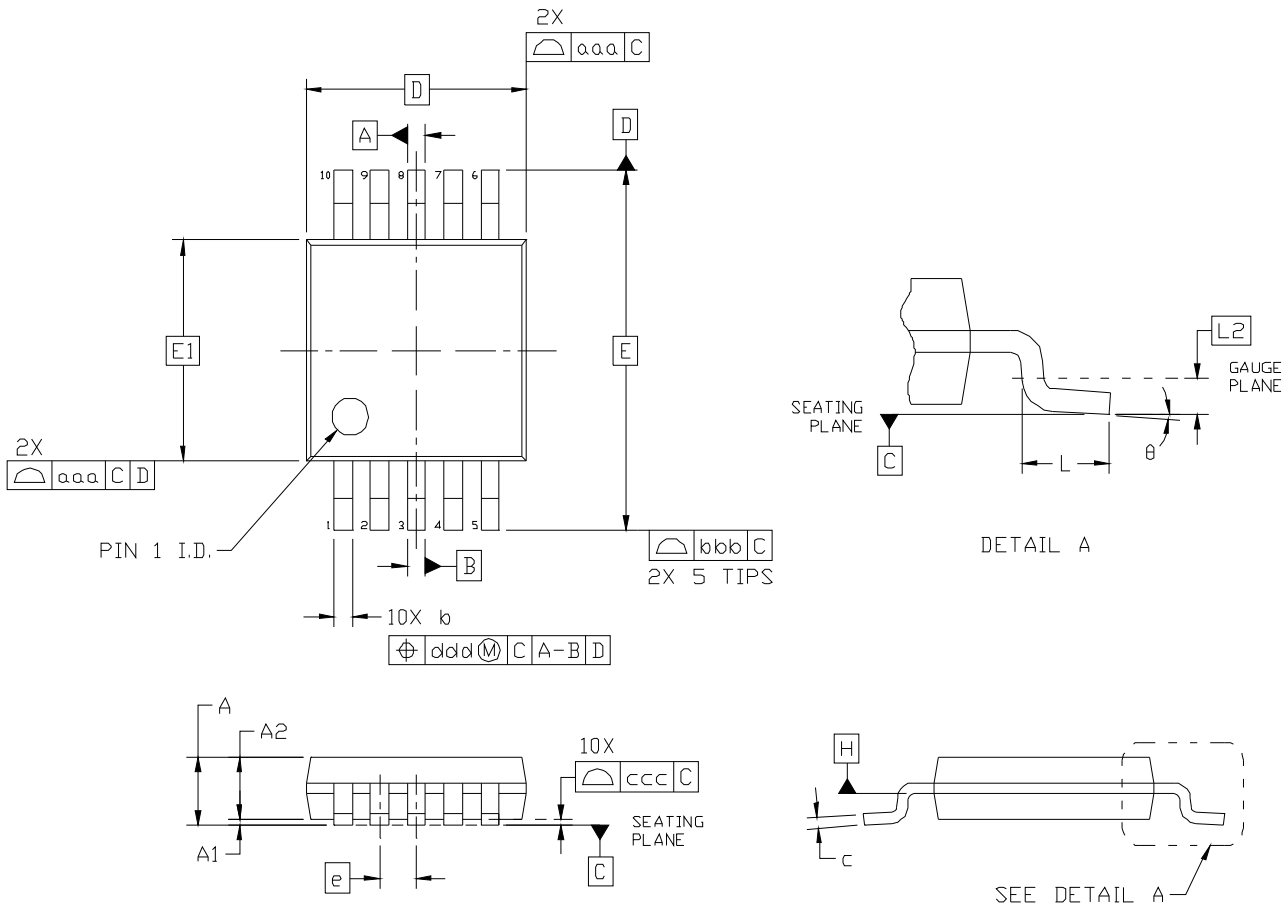


Figure 29. 10-pin MSOP Package Drawing

Table 25. 10-MSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.6. Land Pattern: 10-Pin MSOP

Figure 30 shows the recommended land pattern details for the Si5351 in a 10-Pin MSOP package. Table 26 lists the values for the dimensions shown in the illustration.

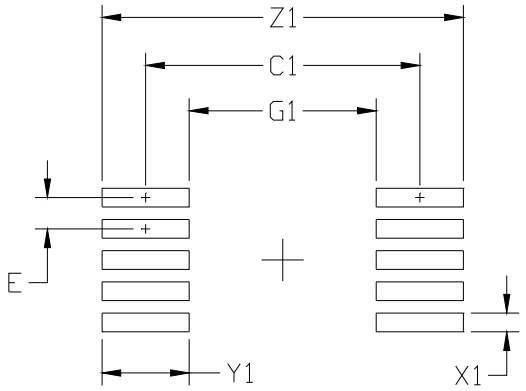


Figure 30. 10-Pin MSOP Land Pattern

Table 26. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
C1	4.40 REF	
E	0.50 BSC	
G1	3.00	—
X1	—	0.30
Y1	1.40 REF	
Z1	—	5.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body components.

13. Top Marking

13.1. 20-Pin QFN Top Marking

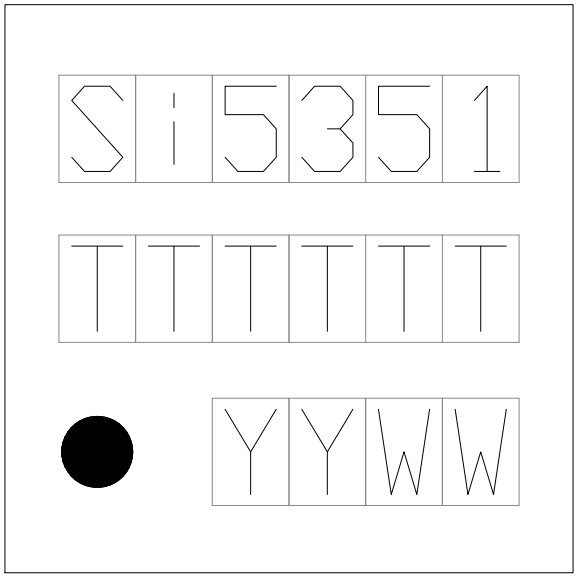


Figure 31. 20-Pin QFN Top Marking

13.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Filled Circle = 0.50 mm Diameter (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	Si5351
Line 2 Mark Format:	TTTTTT = Mfg Code*	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.
***Note:** The code shown in the “TTTTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

13.3. 16-Pin QFN Top Marking

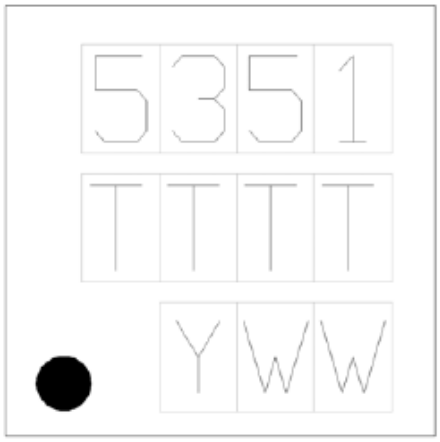


Figure 32. 16-Pin QFN Top Marking

13.4. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	5351
Line 2 Mark Format:	TTTT = Mfg Code*	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YWW = Date Code	Assigned by the Assembly House. Y = Last digit of the current year. WW = Work week of the assembly date.
***Note:** The code shown in the “TTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

13.5. 10-Pin MSOP Top Marking

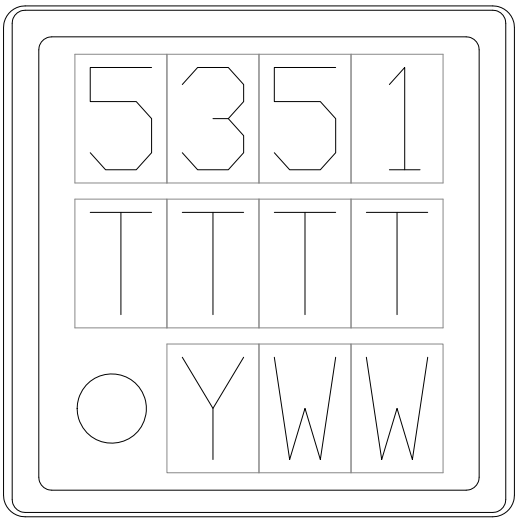


Figure 33. 10-Pin MSOP Top Marking

13.6. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Mold Dimple (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	5351
Line 2 Mark Format:	TTTT = Mfg Code*	Line 2 from the “Markings” section of the Assembly Purchase Order form.
Line 3 Mark Format:	YWW = Date Code	Assigned by the Assembly House. Y = Last Digit of Current Year (Ex: 2013 = 3) WW = Work Week of Assembly Date.
***Note:** The code shown in the “TTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

Revision History

Revision 1.3

March, 2020

- Updated " Functional Block Diagrams" on page 2 with Si5351A 20-QFN and 16-QFN block diagrams.
- Updated "1. Ordering Guide" on page 4.
- Updated Table 4, “DC Characteristics,” on page 8 to include 16-QFN data.
- Updated thermal characteristics tables to include Table 10 (2-Layer Board), Table 11 (4-Layer Board), and Table 12 (Junction-to-Case).
- Updated "4.4. Spread Spectrum" on page 17.
- Added "4.6. Status Pins (INTR)" on page 17.
- Updated "5. I2C Interface" on page 18 with LSB pin option clarification.
- Updated "6. Configuring the Si5351" on page 20 with ClockBuilder Pro.
- Updated "6.3. Replacing Crystals and Crystal Oscillators" on page 22.
- Updated "6.7. HCSL Compatible Outputs" on page 24.
- Updated "8. Register Map Summary" on page 26.
- Updated "9. Register Descriptions" on page 26.
- Updated "10. Si5351 Pin Descriptions" on page 27 with 16-QFN pin descriptions and Ground Pad description.
- Updated "10.3. Si5351C 20-Pin QFN" on page 29.
- Updated Figure 24, “Device Part Numbers,” on page 34.
- Updated "11. Ordering Information" on page 34.
- Updated "12. Packaging" on page 35 with 16-QFN package information.
- Updated "13. Top Marking" on page 44 with 16-QFN top mark.

Revision 1.1

August, 2018

- Updated "11. Ordering Information" on page 34.
  - Changed “Blank = Bulk” to “Blank = Coil Tape” in Figure 24.

Revision 1.0

April, 2015

- Extended frequency range from 8 kHz-160 MHz to 2.5 kHz-200 MHz.
- Updated block diagrams for clarity.
- Added complete Si5350/1 family table, Table 1.
- Added top mark information.
- Added land pattern drawings.
- Added PowerUp Time, PLL Bypass mode, Table 4.
- Clarified Down Spread step sizes in Table 4.
- Updated max jitter specs (typ unchanged) in Table 6.
- Clarified power supply sequencing requirement, Section 6.2.

Revision 0.75

October, 2012

- Initial release.

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