THE DATASHEET OF

SI51218-A07909-GMR

Si51218 Data Sheet

Three Output Factory Programmable Clock Generator

The factory programmable Si51218 is a low power, small footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates up to 3 outputs from 32.768 kHz to 170 MHz. The device is factory programmed to provide customized output frequencies and control input such as power down and output enable.

Applications

- Crystal/XO replacement
- Digital media players
- Portable devices
- DTV/IPTV

KEY FEATURES

- Generates up to 3 LVCMOS clock outputs from 32.768 kHz to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable OE input function

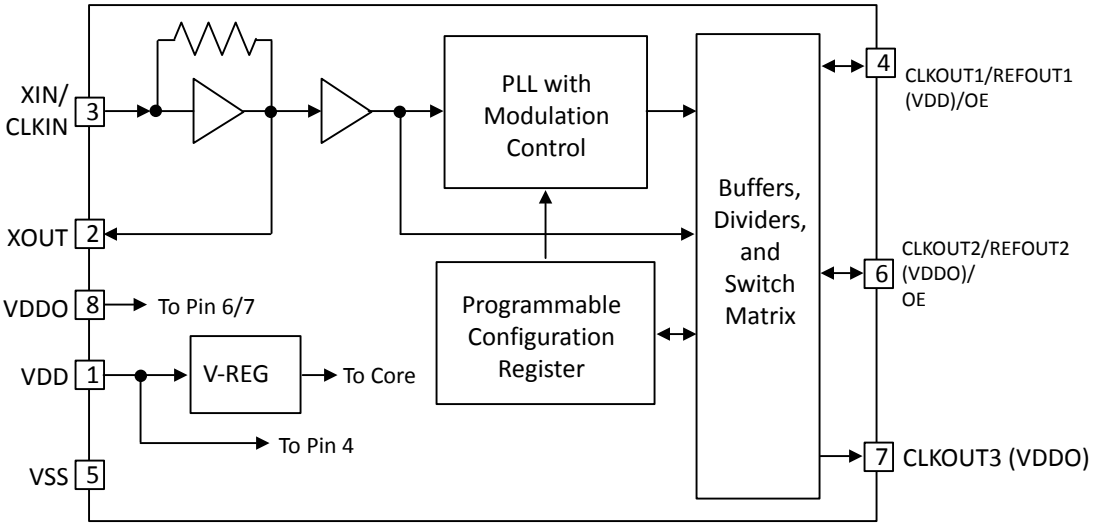


Table of Contents

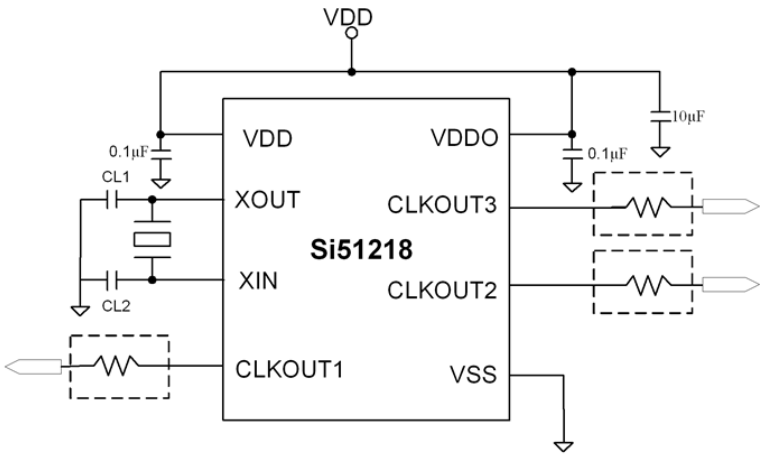
1. Feature List

The Si51218 highlighted features are listed below.

- Generates up to 3 LVCMOS clock outputs from 32.768 kHz to 170 MHz
- Accepts crystal or reference clock input
  - 3 to 165 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable OE input function
- Low power dissipation
- Separate voltage supply pins
  - V_{DD} = 2.5 to 3.3 V
  - V_{DDO} = 1.8 to 3.3 V ($V_{DDO} \leq V_{DD}$)
- Low cycle-cycle jitter
- Ultra small 8-pin TDFN package (1.4 mm x 1.6 mm)

2. Design Considerations

2.1 Typical Application Schematic



Dotted lines show optional termination resistors

2.2 Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1 µF must be used between VDD and VSS on pins 1 and 8. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin. In addition, a 10 µF capacitor should be placed between VDD and VSS.

Crystal and Crystal Load: Only use a parallel resonant fundamental AT cut crystal. Do not use higher overtone crystals. To meet the crystal initial accuracy specification (in ppm) make sure that the external crystal load capacitor is matched to the crystal load specification. To determine the value of CL1 and CL2, use the following formula:

$CL1 = CL2 = 2CL - (Cpin + Cp)$;

where CL is the load capacitance stated by the crystal manufacturer,

Cpin is the Si51218 pin capacitance (3 pF), and

Cp is the parasitic capacitance of the PCB traces.

Example: If a crystal with CL = 12 pF specification is used and Cp = 1 pF (parasitic PCB capacitance on PCB), 19 pF external capacitors from pins XIN (pin 3) and XOUT (Pin 2) to VSS are required. Users must verify Cp value.

Table 2.1. Crystal Specifications

Equivalent Series Resistance (ESR)	Crystal Output Capacitance (CO)	Load Capacitance (CL)
≤ 50 Ω	≤ 3 pF	≤ 13 pF

3. Electrical Specifications

Table 3.1. DC Electrical Specifications

(V_{DD} = 2.5 V ±10%, or V_{DD} = 3.3V ±-10%, V_{DDO} = V_{DD}, C_L = 10 pF, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	V_{DD}= 3.3 V ± 10%	2.97	3.3	3.63	V
		V_{DD}= 2.5 V ± 10%	2.25	2.5	2.75	V
	V_{DDO}	$V_{DDO} \le V_{DD}$	1.71	—	3.6	V
Output High Voltage	V_{OH}	I_{OH}= –4 mA V_{DDX} = V_{DD} or V_{DDO}	V_{DDX} – 0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}= 4 mA	—	—	0.3	V
Input High Voltage	V_{IH}	CMOS Level	0.7 V_{DD}	—	—	V
Input Low Voltage	V_{IL}	CMOS Level	—	—	0.3 V_{DD}	V
Operating Supply Current[1]	I_{DD}	F_{IN} = 20 MHz, CLKOUT1 = 32.768 kHz, REFOUT2 = 20 MHz, CLKOUT3 = 26 MHz, C_L= 5 pF, V_{DD} = V_{DDO} = 3.3 V	—	7.6	9	mA
Nominal Output Impedance	Z_O		—	30	—	Ω
Internal Pull-up/Pull-down Resistor	R_{PUP}/R_{PD}	Pin 6	—	150k	—	Ω
Input Pin Capacitance	C_{IN}	Input pin capacitance	—	3	5	pF
Load Capacitance	C_L		—	—	10	pF

Note:

1. I_{DD} depends on input and output frequency configurations.

Table 3.2. AC Electrical Specifications

(V_{DD} = 2.5 V ±10%, or V_{DD} = 3.3 V ±10%, V_{DDO} = V_{DD}, C_L = 10 pF, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	F_{IN1}	Crystal input	8	—	48	MHz
Input Frequency Range	F_{IN2}	Reference clock Input	3	—	165	MHz
Output Frequency Range	F_{OUT}	CLKOUT1: 32.768 kHz to 170 MHz CLKOUT2/3: 3 MHz to 170 MHz	0.032768	—	170	MHz
Frequency Accuracy	F_{ACC}	Configuration dependent	—	0	—	ppm
Output Duty Cycle	DC_{OUT}	Measured at V_{DDO}/2 $F_{OUT} \le$ 75 MHz	45	50	55	%
		Measured at V_{DDO}/2 F_{OUT} > 75 MHz	40	50	60	%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Duty Cycle	DC_{IN}	CLKIN, CLKOUT through PLL	30	50	70	%
Output Rise/Fall Time	t_r/t_f	C_L= 10 pF, 20 to 80%	—	1	2	ns
Period Jitter	PJ_1	CLKOUT1/2/3, at the same frequency	—	12	20	ps rms
	PJ_2	CLKOUT1/2/3, at different output frequencies[1]	—	30	95[2]	ps rms
	PJ_3	CLKOUT1/3 at 32.768 kHz, V_{DD} = V_{DDO} = 3.3 V		1500[2]		ps
Cycle-to-Cycle Jitter	CCJ_1	CLKOUT1/2/3, at the same frequency	—	85	150	ps
	CCJ_2	CLKOUT1/2/3, at different output frequencies[1]	—	145	290[2]	ps
Power-up Time	t_{PU}	Time from 0.9 V_{DD} to valid frequencies at all clock outputs	—	1.2	5	ms
Output Enable Time	t_{OE}	Time from OE rising edge to active at outputs SSCLK1/2 (asynchronous), F_{OUT} = 133 MHz	—	15	—	ns
Output Disable Time	t_{OD}	Time from OE falling edge to active at outputs SSCLK1/2 (asynchronous), F_{OUT} = 133 MHz	—	15	—	ns

Note:

1. Example frequency configurations:
   - 8 MHz, 100 MHz, 75 MHz
   - 48 MHz, 100 MHz, 66 2/3 MHz
   - 96 MHz, 133 1/3 MHz, 133 1/3 MHz
2. Jitter performance depends on configuration and programming parameters.

Table 3.3. Absolute Maximum Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		–0.5	—	4.2	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	V_{DD}+0.5	V
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional, I-Grade	–40	—	85	°C
Temperature, Junction	T_J	Functional, power is applied	—	—	125	°C
Temperature, Soldering	T_{Sol}	Non-functional	—	—	260	°C
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22-A114)	–4000	—	4000	V
ESD Protection (Charge Device Model)	ESD_{CDM}	JEDEC (JESD 22-C101)	–1500	—	1500	V
ESD Protection (Machine Model)	ESD_{MM}	JEDEC (JESD 22-A115)	–200	—	200	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Note: 1. While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.						

Table 3.4. Thermal Characteristics

Parameter	Symbol	Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air	170.8	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still air	V_{DD}+0.5	°C/W

4. Functional Description

4.1 Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 3.0 to 165.0 MHz.

4.2 Output Frequency Range and Outputs

Up to three outputs can be programmed as CLKOUT or REFOUT. The CLKOUT1 synthesized frequencies can have values from 32.768 kHz to 170 MHz. REFOUT is the buffered output of the oscillator and is the same frequency as the input frequency. By using only low cost, fundamental mode crystals, the Si51218 can synthesize output frequencies up to 170 MHz (CLKOUT2/3), eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). The 32.768 kHz output can replace the 32.768 kHz crystal, which is widely used in many embedded and mobile systems. This reduces the cost while improving the system clock accuracy, performance, and reliability.

4.3 Output Enable (OE)

The Si51218 pin 4 and pin 6 can be programmed as OE input. OE only disables the output buffers to Hi-Z. The OE function is asynchronous. Any requirement for synchronous operations (like glitchless output clock switching) needs to be handled externally.

5. Pin Description

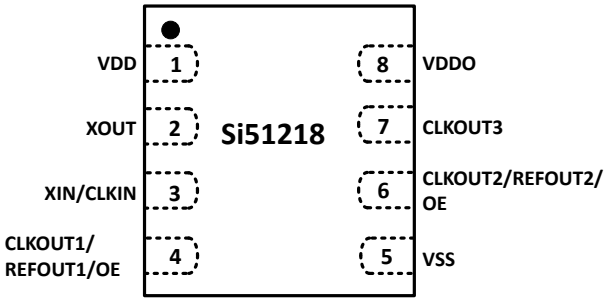


Figure 5.1. 8-Pin TDFN

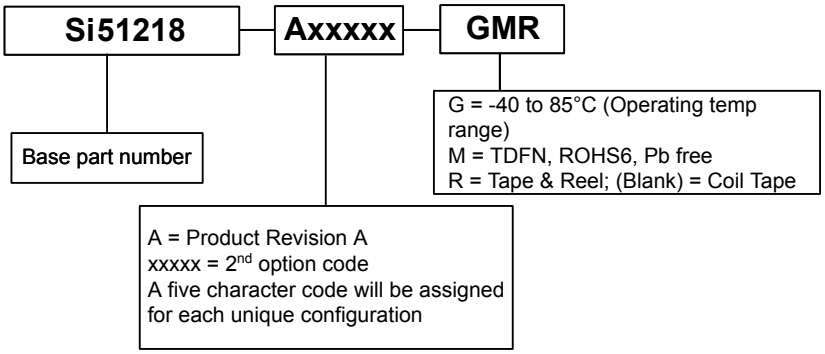
Table 5.1. Si51218 8-Pin Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
3	XIN/CLKIN	I	External crystal and clock input.
4	CLKOUT1/REFOUT1/OE	I/O	Programmable CLKOUT1 or REFOUT1 output or OE control input. The frequency at this pin is synthesized by the internal PLL if programmed as CLKOUT1. If programmed as REFOUT1, the output clock is a buffered output of the crystal or reference clock input.
5	VSS	GND	Ground.
6	CLKOUT2/REFOUT2/OE	I/O	Programmable CLKOUT2 or REFOUT2 output or OE control input. The frequency at this pin is synthesized by the internal PLL if programmed as CLKOUT2. This output clock can also be the buffered output (REFOUT2) of the crystal or reference clock input. It is powered by the V_{DDO} pin (pin 8).
7	CLKOUT3	O	Programmable CLKOUT3 output. The frequency at this pin is synthesized by the internal PLL. It is powered by the V_{DDO} pin (pin 8).
8	VDDO	PWR	1.8 to 3.3 V output power supply to CLKOUT2/3 (pin 6/7).

6. Ordering Guide

Table 6.1. Si51218 Ordering Guide

Part Number	Package Type	Temperature
Si51218-Axxxxx-GM	8-pin TDFN	Industrial, –40 to 85 °C
Si51218-Axxxxx-GMR	8-pin TDFN—Tape and Reel	Industrial, –40 to 85 °C



7. Package Outline

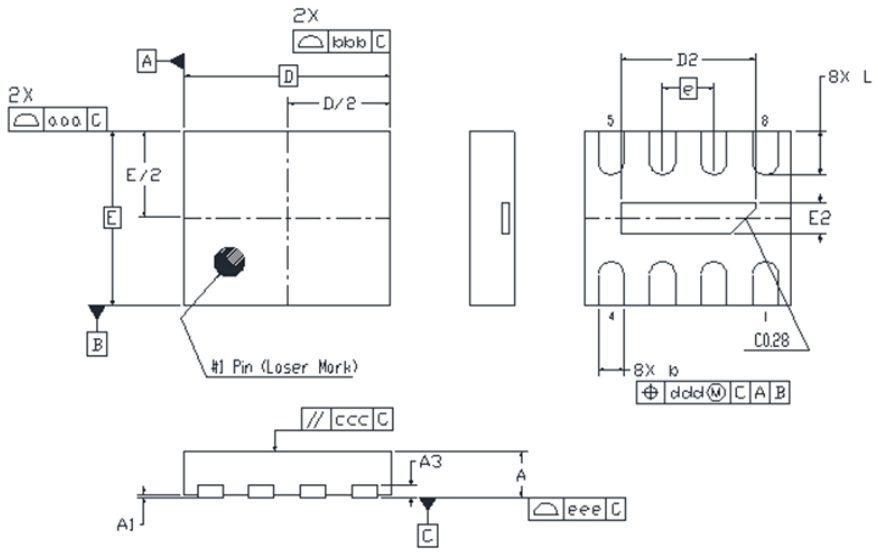


Figure 7.1. 8-pin TDFN

Table 7.1. Si51218 Package Dimensions

Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		1.60 BSC	
D2	1.00	1.05	1.10
e		0.40 BSC	
E		1.40 BSC	
E2	0.20	0.25	0.30
L	0.30	0.35	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.07	
eee		0.08	

Dimension	Min	Nom	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted..
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the device. The table below lists the values for the dimensions shown in the illustration.

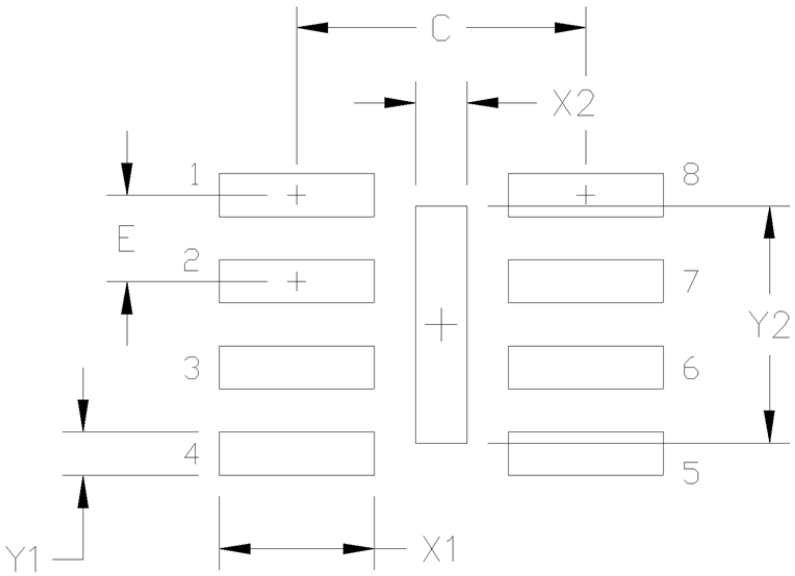


Figure 8.1. Si51218 8-pin TDFN PCB Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
C	1.40
E	0.40
X1	0.75
Y1	0.20
X2	0.25
Y2	1.10

9. Revision History

Revision 1.1

- Updated key features.
- Updated block diagram.
- Updated 2. Design Considerations.
- Updated 3. Electrical Specifications.
- Updated 6. Ordering Guide.

Revision 1.0

- Updated max output frequency to 170 MHz.
- Updated max clock input frequency to 165 MHz.
- Updated Operating Temperature to Industrial temperature, –40 °C to 85 °C.
- Removed programmable output rise/fall time.
- Updated Table 3.1 DC Electrical Specifications on page 5.
- Updated Table 3.2 AC Electrical Specifications on page 5.
- Updated pin descriptions in Pin Descriptions table.
- Updated customized part numbering nomenclature in 6. Ordering Guide.
- Added land pattern drawing.
- Removed FSEL and PD functions.

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