THE DATASHEET OF

SI5395B-A10465-GM

www.win-source.net 0086-755-83957316

Si5395/94/92 Data Sheet

12-Channel, Any-Frequency, Any-Output Jitter Attenuator/Clock Multiplier with Ultra-Low Jitter

The Si5395/94/92 Jitter attenuators combine fourth-generation DSPLL™ and MultiSynth™ technologies to deliver ultra-low jitter (69 fs) for high performance applications like 56G SerDes. They are used in applications that demand the highest level of integration and jitter performance. All PLL components are integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions. Device grades J/K/L/M/E have an integrated reference to save board space, improve system reliability and reduces the effect of acoustic emissions noise caused by temperature ramps. Grades A/B/C/D/P use an external crystal (XTAL) or crystal oscillator (XO) reference.

The Si5395/94/92 support free-run, synchronous and holdover modes as well as enhanced hitless switching, minimizing the phase transients associated when switching between input clocks. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) so they always power up with a known frequency configuration. Programming the Si5395/94/92 is easy with Skyworks' ClockBuilder™ Pro software. Factory preprogrammed devices are also available.

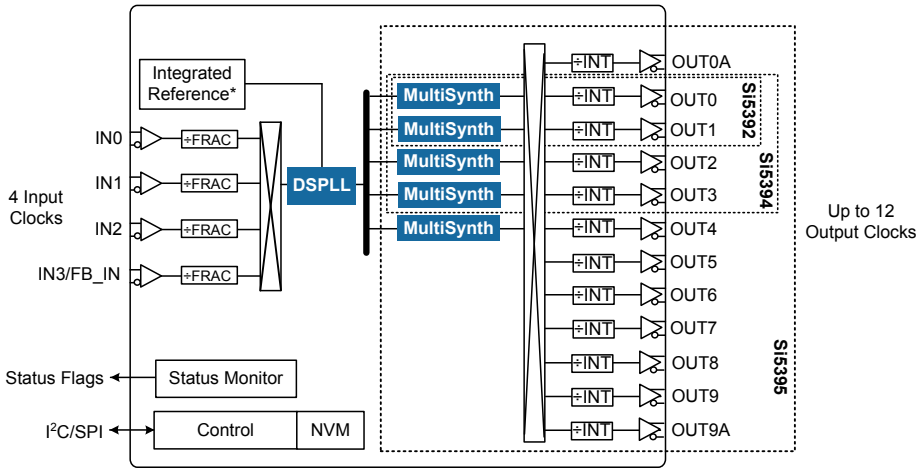
For more information, visit https://www.skyworksinc.com/en/Products/Timing page.

Applications:

- 56G/112G PAM4 SerDes clocking
- OTN muxponders and transponders
- 10/40/100/200/400G networking line cards
- 10/40/100/400 GbE Synchronous Ethernet (ITU-T G.8262)
- Medical imaging
- Test and measurement

KEY FEATURES

- Generates any combination of output frequencies from any input frequency
- Ultra low phase jitter:
  - 69 fs RMS (Grade P)
  - 71 fs RMS (Grade E)
  - 85 fs RMS (integer mode)
  - 100 fs RMS (fractional mode)
- Enhanced hitless switching minimizes output phase transients (0.2 ns typ)
- Input frequency range
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Meets G.8262, E.8262.1 EEC Standards
- Status monitoring
- Si5395: 4 input, 12 output (64-QFN/LGA)
- Si5394: 4 input, 4 output (44-QFN/LGA)
- Si5392: 4 input, 2 output (44-QFN/LGA)
- External reference: Grades A/B/C/D/P
- Integrated reference: Grades J/K/L/M/E
- Drop-in compatible with Si5345/44/42



*Only for Si539x J/K/L/M/E grades. Si539x A/B/C/D/P grades have external reference (XTAL or XO)

1. Features List

The Si5395/94/92 features are listed below:

- Generates any output frequency in any format from any input frequency
- External XTAL or XO reference (A/B/C/D/P)
- Integrated reference (J/K/L/M/E)
- Ultra-low phase jitter of 69 fs (P-Grade)
- Dynamic phase adjust
- Input frequency range
  - Differential: 8 kHz–750 MHz
  - LVCMOS: 8 kHz–250 MHz
- Output frequency range
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Programmable jitter attenuation bandwidth: 0.1 Hz to 4 kHz
- Meets requirements of:
  - ITU-T G.8262 (SyncE) EEC Options 1 and 2
  - ITU-T G.8262.1 (Enhanced SyncE) eEEC
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Enhanced hitless switching for 8 kHz, 19.44 MHz, 25 MHz inputs and other frequencies
- Locks to gapped clock inputs
- Free-run and holdover modes
- Drop-in compatible with Si5345/44/42
- Optional zero delay mode
- Fast-lock acquisition for low nominal bandwidths
- Independent Frequency-on-the fly for each MultiSynth
- DCO mode: as low as 0.001 ppb step size
- Core voltage
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output clock supply pins
  - 3.3 V, 2.5 V, or 1.8 V
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro software simplifies device configuration
- Si5395: 4 input, 12 output
  - Grade A/B/C/D/P: 64-QFN 9×9 mm
  - Grade J/K/L/M/E: 64-LGA 9x9 mm
- Si5394: 4 input, 4 output
  - Grade A/B/C/D/P: 44-QFN 7×7 mm
  - Grade J/K/L/M/E: 44-LGA 7x7 mm
- Si5392: 4 input, 2 output
  - Grade A/B/C/D/P: 44-QFN 7×7 mm
  - Grade J/K/L/M/E: 44-LGA 7x7 mm
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Related Documents

Table 2.1. Related Documentation and Software

Document/Resource	Description/URL
Si5395/94/92 Family Reference Manual	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si5395-94-92-family.pdf
Crystal Reference Manual (Grades A/B/C/D/P only)	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
UG387: Si5392 Evaluation Board User's Guide	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/ug387-si5392-evb.pdf
UG334: Si5394 Evaluation Board User's Guide	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/ug334-si5394evb.pdf
UG335: Si5395 Evaluation Board User's Guide	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/ug335-si5395evb.pdf
AN1151: Using the Si539x in 56G SerDes Applications	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1151-using-si539x.pdf
AN1155: Differences between Si5342-47 and Si5392-97	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1151-using-si539x.pdf
AN1178: Frequency-On-the-Fly for Skyworks Jitter Attenuators and Clock Generators	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1178-frequency-otf-jitter-atten-clock-gen.pdf
Quality and Reliability	https://www.skyworksinc.com/Quality
Development Kits	https://www.skyworksinc.com/en/Products/Timing
ClockBuilder Pro (CBPro) Software	https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software

3. Ordering Guide

Table 3.1. Si5395/94/92 A/B/C/D/P Ordering Guide (External Reference)

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Reference
Si5395					
Si5395A-A-GM[1, 2]	4/12	0.0001 to 1028 MHz	Integer and Fractional	64-QFN 9×9 mm	External
Si5395B-A-GM[1, 2]		0.0001 to 350 MHz			
Si5395C-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5395D-A-GM[1, 2]		0.0001 to 350 MHz			
Si5395P-A-GM[1, 2]		Up to 3 domains (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5394					
Si5394A-A-GM[1, 2]	4/4	0.0001 to 1028 MHz	Integer and Fractional	44-QFN 7×7 mm	External
Si5394B-A-GM[1, 2]		0.0001 to 350 MHz			
Si5394C-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5394D-A-GM[1, 2]		0.0001 to 350 MHz			
Si5394P-A-GM[1, 2]		Up to 2 domains (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5392					
Si5392A-A-GM[1, 2]	4/2	0.0001 to 1028 MHz	Integer and Fractional	44-QFN 7×7 mm	External
Si5392B-A-GM[1, 2]		0.0001 to 350 MHz			
Si5392C-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5392D-A-GM[1, 2]		0.0001to 350 MHz			
Si5392P-A-GM[1, 2]		1 domain (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5395/94/92 Evaluation Board					
Si5395A-A-EVB	12-output	Any-frequency, any Output	—	64-QFN EVB	—
Si5395P-A-EVB	12-output	Low jitter clocks for 56G PAM4 SerDes	—	64-QFN EVB	—
Si5394A-A-EVB	4-output	Any-frequency, any Output	—	44-QFN EVB	—
Si5394P-A-EVB	4-output	Low jitter clocks for 56G PAM4 SerDes	—	44-QFN EVB	—

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Skyworks and the ClockBuilder Pro software utility. Custom part number format is “Si5395A-Axxxxx-GM” where “xxxxx” is a unique numerical sequence representing the preprogrammed configuration.

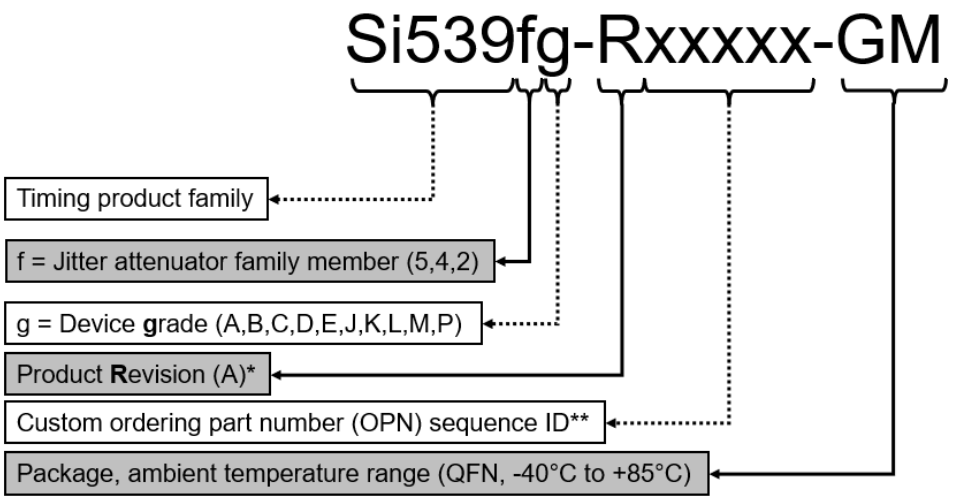
Table 3.2. Si5395/4/2 J/K/L/M/E Ordering guide (Integrated Reference)

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Reference
Si5395					
Si5395J-A-GM[1, 2]	4/12	0.0001 to 1028 MHz	Integer and Fractional	64-LGA 9×9 mm	Internal
Si5395K-A-GM[1, 2]		0.0001 to 350 MHz			
Si5395L-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5395M-A-GM[1, 2]		0.0001 to 350 MHz			
Si5395E-A-GM[1, 2]		Up to 3 domains (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5394					
Si5394J-A-GM[1, 2]	4/4	0.0001 to 1028 MHz	Integer and Fractional	44-LGA 7×7 mm	Internal
Si5394K-A-GM[1, 2]		0.0001 to 350 MHz			
Si5394L-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5394M-A-GM[1, 2]		0.0001 to 350 MHz			
Si5394E-A-GM[1, 2]		Up to 2 domains (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5392					
Si5392J-A-GM[1, 2]	4/2	0.0001 to 1028 MHz	Integer and Fractional	44-LGA 7×7 mm	Internal
Si5392K-A-GM[1, 2]		0.0001 to 350 MHz			
Si5392L-A-GM[1, 2]		0.0001 to 1028 MHz	Integer Only		
Si5392M-A-GM[1, 2]		0.0001to 350 MHz			
Si5392E-A-GM[1, 2]		1 domain (Section 4.9.2 Grades P and E)	Precision Calibration		
Si5395/94/92 Evaluation Board					
Si5395J-A-EVB	12-output	Any-frequency, any Output	—	64-LGA EVB	—
Si5395E-A-EVB	12-output	Low jitter clocks for 56G PAM4 SerDes	—	64-LGA EVB	—
Si5394J-A-EVB	4-output	Any-frequency, any Output	—	44-LGA EVB	—
Si5394E-A-EVB	4-output	Low jitter clocks for 56G PAM4 SerDes	—	44-LGA EVB	—
Si5392J-A-EVB	2-output	Any-frequency, any Output	—	44-LGA EVB	—
Si5392E-A-EVB	2-output	Low jitter clocks for 56G PAM4 SerDes	—	44-LGA EVB	—

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Reference

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Skyworks and the ClockBuilder Pro software utility. Custom part number format is “Si5395J-Axxxxx-GM” where “xxxxx” is a unique numerical sequence representing the preprogrammed configuration.



*See Ordering Guide table for current product revision.
** (Optional) 5 digits; assigned by ClockBuilder Pro for Custom, factory-preprogrammed OPN devices only;
(The “xxxxx” field is not included for “Base” OPNs).

Figure 3.1. Ordering Part Number Fields

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4. Functional Description

The Si5392-95's internal DSPLL provides jitter attenuation and any-frequency multiplication of the selected input frequency. Fractional input dividers (P) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. The high-performance MultiSynth dividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency.

4.1 Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

4.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection for Grade A/B/C/D. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. For grade P and E devices, the DSPLL bandwidth is fixed at 100 Hz.

4.3 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings of in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

4.4 Modes of Operation

Once initialization is complete the DSPLL operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

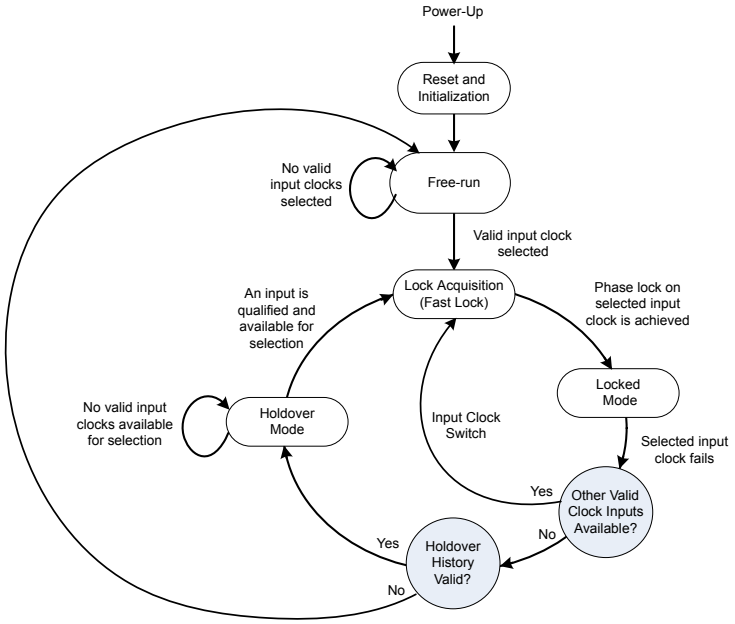


Figure 4.1. Modes of Operation

4.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period, downloads default register values and configuration data from NVM, and performs other initialization tasks. To communicate with the device through the serial interface, wait untl the initialization period is complete. No clocks will be generated until the initialization is complete.

Clocks that feature the integrated crystal may require a slightly longer settling time compared to the external crystal device. See the Reference Manual for more details.

Two types of resets are available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit.

A soft reset bypasses the NVM download. It is used to initiate register configuration changes.

4.4.2 Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

4.4.3 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls in to the input clock frequency.

4.4.4 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See 4.8.4 LOL Detection for more details on the operation of the loss-of-lock circuit.

4.4.5 Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

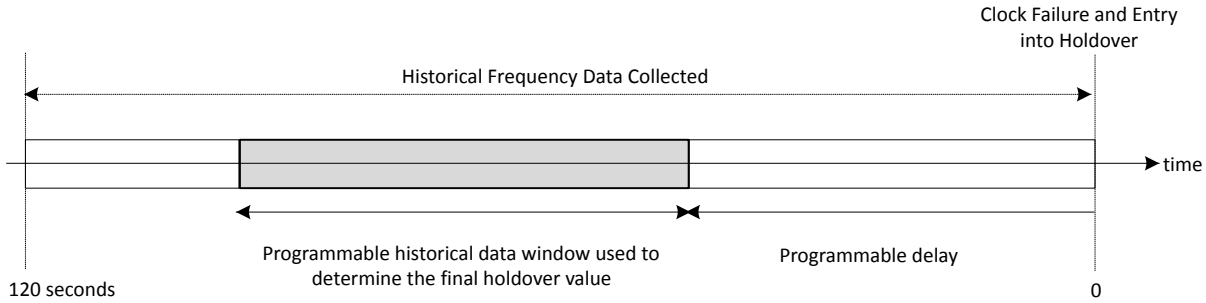


Figure 4.2. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

The DSPLL output frequency when exiting holdover can be ramped (recommend). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 4.7.4 Frequency Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

4.4.6 Frequency-on-the-Fly (FOTF)

The Si5395/94/92 use register writes to support frequency-on-the-fly to allow frequency changes on one MultiSynth without affecting the clocks generated from other MultiSynths. See the Si5395-94-92 Family Reference Manual and AN1178: Frequency-On-the-Fly for Skyworks Jitter Attenuators and Clock Generators for more details.

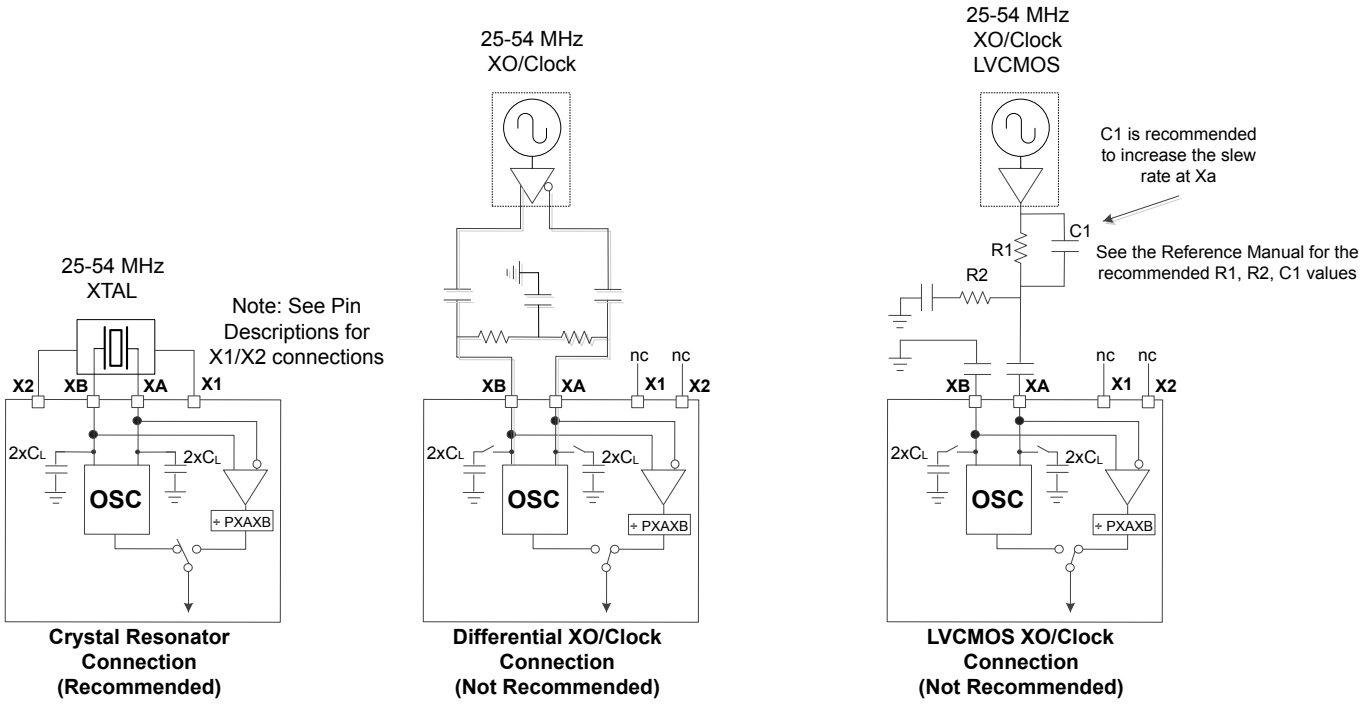
4.5 Digitally Controlled Oscillator (DCO) Mode (Grade A/B/C/D and J/K/L/M)

The output MultiSynths support a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increment (FINC) or decrement (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Any number of MultiSynths can be updated at once or independently controlled. The DCO mode is available when the DSPLL is operating in either free-run or locked mode.

4.6 External Reference (Grade A/B/C/D/P Only)

An external crystal (XTAL) or crystal oscillator (XO) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in the figure below. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 5.12 External Crystal Specifications for Grades A/B/C/D/P on page 39 for crystal specifications. For the A/B/C/D grades, a crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. The P grade devices must use a high quality 48 MHz crystal to achieve the ultra low jitter specification. The family referernce manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. For SyncE pizza box applications (e.g. loop bandwidth set to 0.1 Hz), a TCXO is required on the XA/XB reference to minimize wander and to provide a stable holdover reference. See the Si5395-94-92 Family Reference Manual for more information. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in the REFCLK mode. Refer to Table 5.3 Input Clock Specifications on page 26 for REFCLK requirements when using this mode. A PREF divider is available to accommodate external clock frequencies higher than 54 MHz. Frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.



Note: XA and XB must not exceed the maximum input voltage listed in Table 5.3 Input Clock Specifications on page 24

Figure 4.3. Crystal Resonator and External Reference Clock Connection Options

Note that connecting an external reference to a device that already has an integrated reference (grades J/K/L/M/E) is not allowed. Doing so could lead to internal damage to the circuits.

4.7 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize to the DSPLL. The inputs accept three formats of input clock: Standard Differential/Single-Ended, Standard LVCMOS or Pulsed CMOS (See Family Reference Manual for more details). Input selection can be manual (pin or register controlled) or automatic with user definable priorities.

4.7.1 Manual Input Selection (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable (default) or register selectable. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 4.1. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

4.7.2 Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

4.7.3 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz; however, for optimum hitless switching performance, higher input frequencies are recommended.

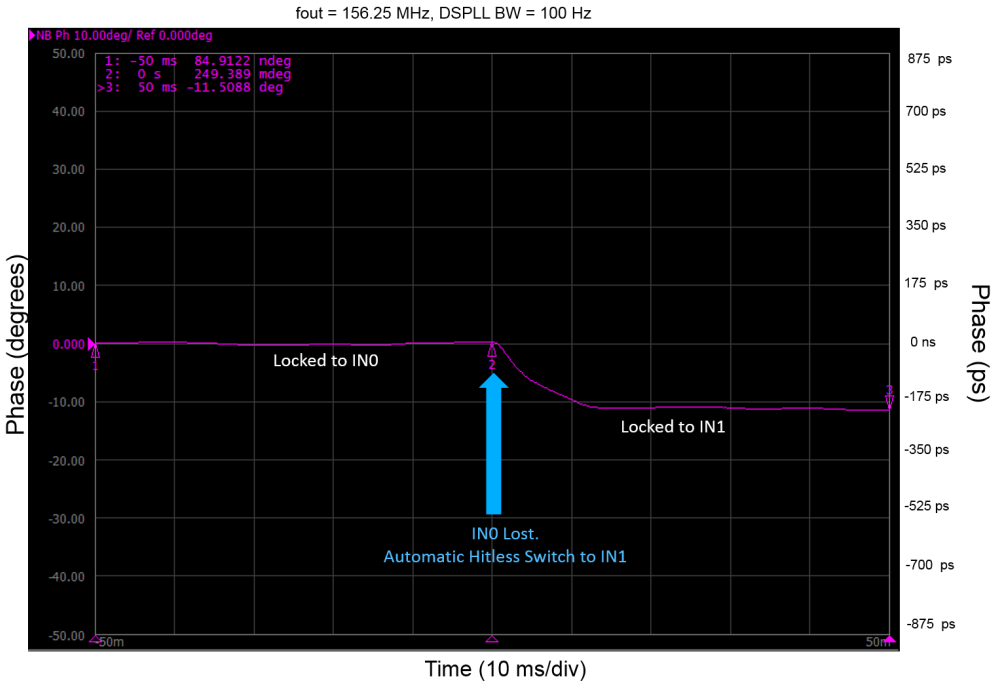


Figure 4.4. Output Phase Transient—Hitless Switching between Two 25 MHz Inputs (0 ppm, 180 Degree Phase Shift)

4.7.4 Frequency Ramped Input Switching

The ramped input switching feature is enabled/disabled depending on both the frequency of the Phase-Frequency detector (Fpfd) and the difference in input frequencies (Zero-PPM vs non-zero PPM). The table below shows the selection criteria to enable ramped input switching. The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see 4.4.5 Holdover Mode and the Si5395-94-92 Family Reference Manual.

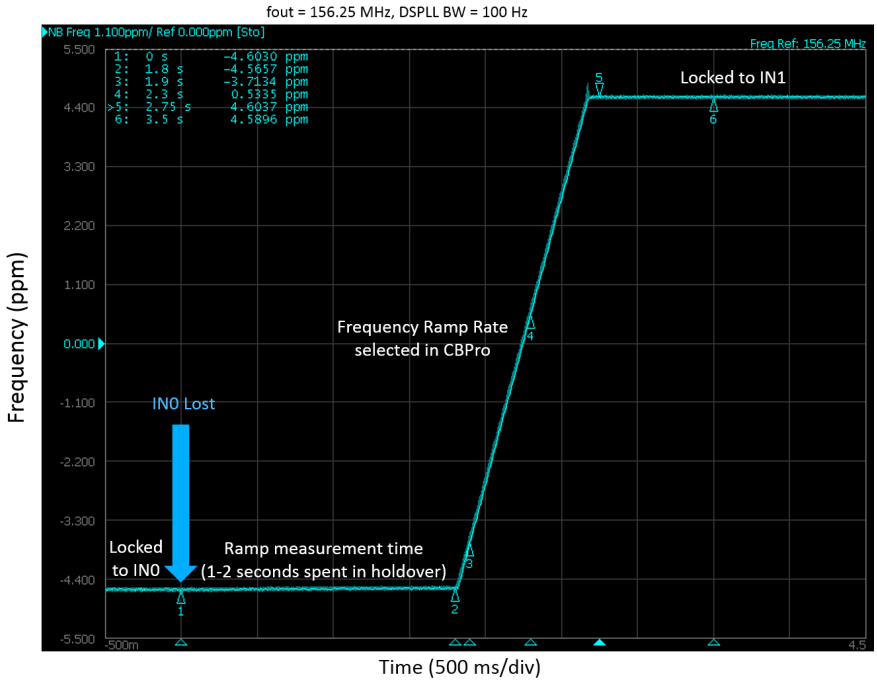


Figure 4.5. Output Frequency Transient—Ramped Switching between Two 8 kHz Inputs (±4.6 ppm Offset)

Table 4.2. Recommended Ramped Input Switching Settings for Internal Clock Switches

Maximum Input Frequency Difference	Fpfd[1] < 500 kHz	Fpfd[1] ≥ 500 kHz
0 ppm Frequency Locked	Ramped Exit from Holdover	
≤ 10 ppm	Ramped Input Switching and Ramped Exit from Holdover	Ramped Exit from Holdover
> 10 ppm	Ramped Input Switching and Ramped Exit from Holdover	

Note:
1. The Fpfd value is determineby various requirements of the frequency plan and is displayed in the CBPro project file.

Always enable hitless switching and enable phase buildout on holdover exit. See the latest version of CBPro to properly configure the device.

.

4.7.5 Glitchless Input Switching

The glitchless switching feature allows the DSPLL to switch between two input clock frequencies that are up to ±500 ppm apart without an abrupt phase change at the output. The DSPLL will pull-in to the new frequency using a ramped frequency step (if ramping is enabled) or using Fastlock/nominal lock parameters (if ramping is disabled).

The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency.

4.7.6 Synchronizing to Gapped Input Clocks (Grade A/B/C/D and J/K/L/M Only)

The DSPLL supports locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the following figure. For more information on gapped clocks, see "AN561: Introduction to Gapped Clocks and PLLs".

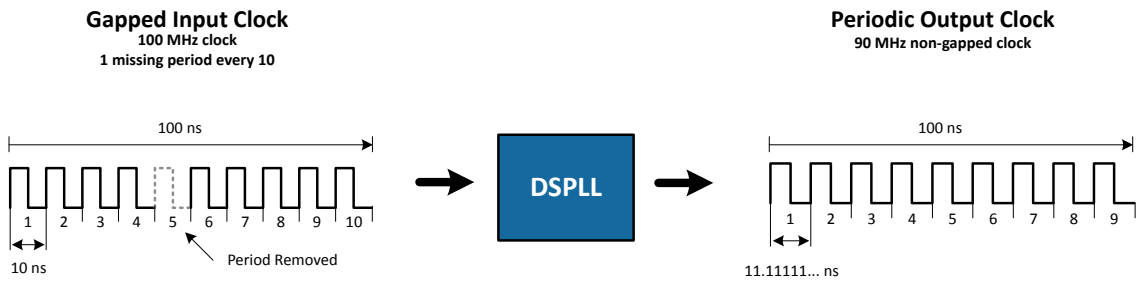


Figure 4.6. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 34 when the switch occurs during a gap in either input clock.

4.8 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss Of Lock (LOL) indicator, which is asserted when the DSPLL loses synchronization.

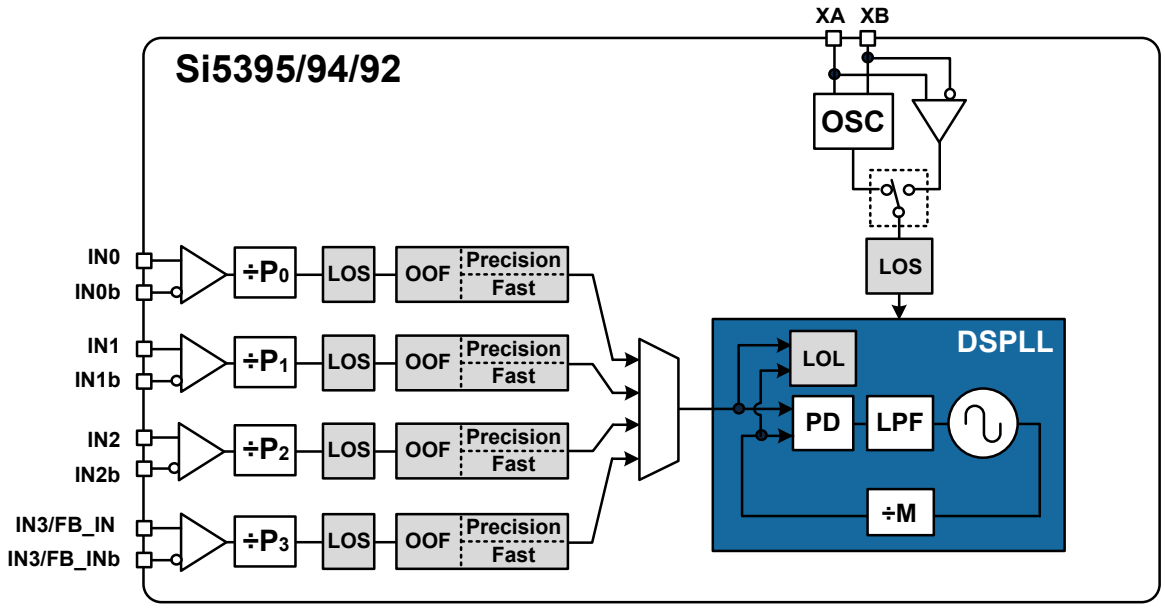


Figure 4.7. Si5395/94/92 Fault Monitors

4.8.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

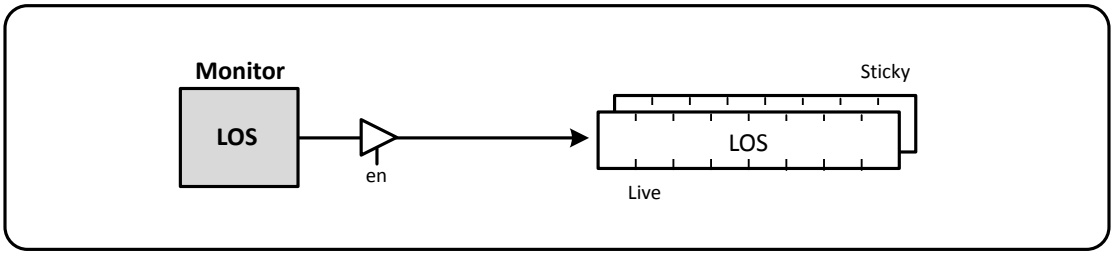


Figure 4.8. LOS Status Indicators

4.8.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

4.8.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

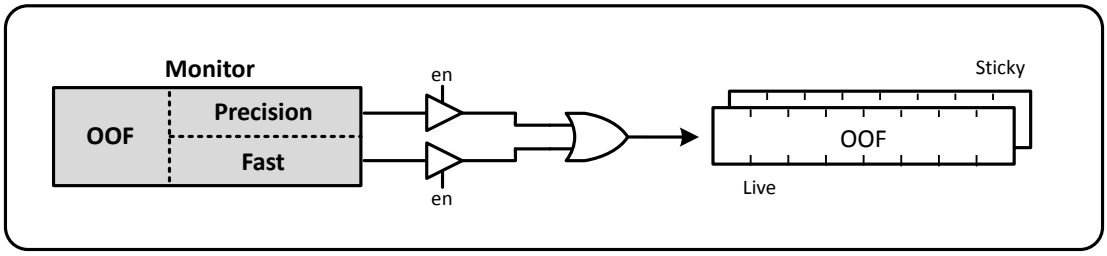


Figure 4.9. OOF Status Indicator

4.8.3.1 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable up to ±512 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

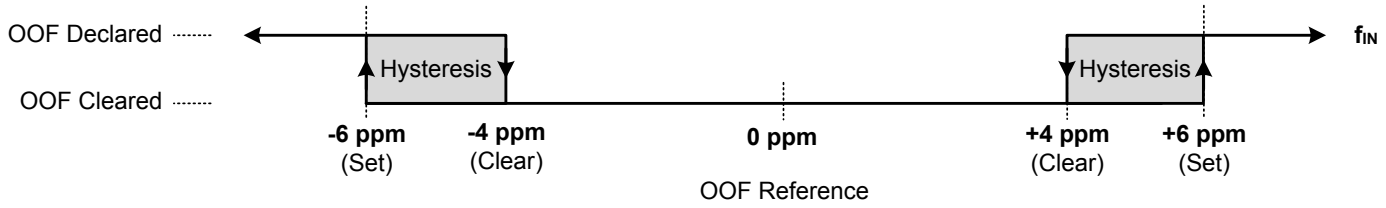


Figure 4.10. Example of Precise OOF Monitor Assertion and Deassertion Triggers

4.8.3.2 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

4.8.4 LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

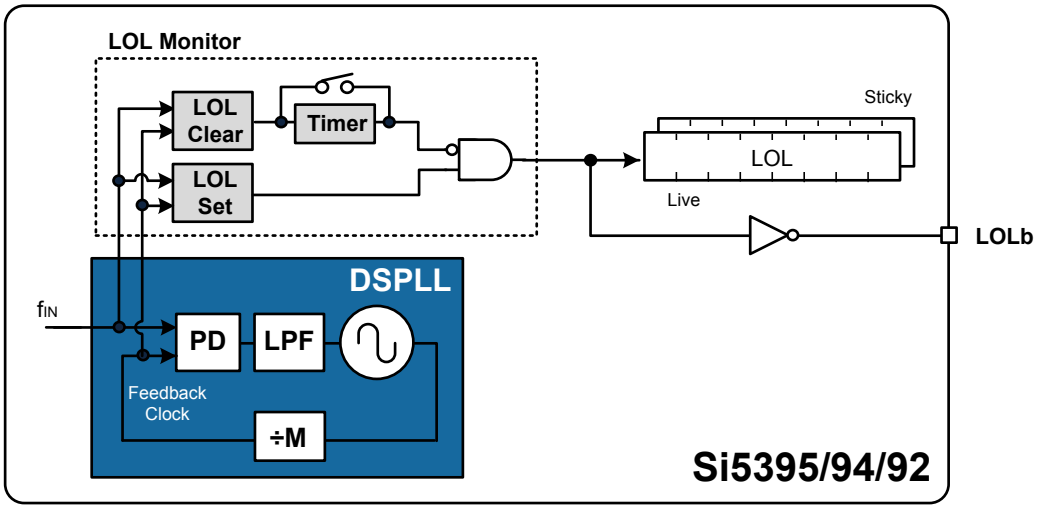


Figure 4.11. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 1 ppm frequency difference is shown in the following figure.

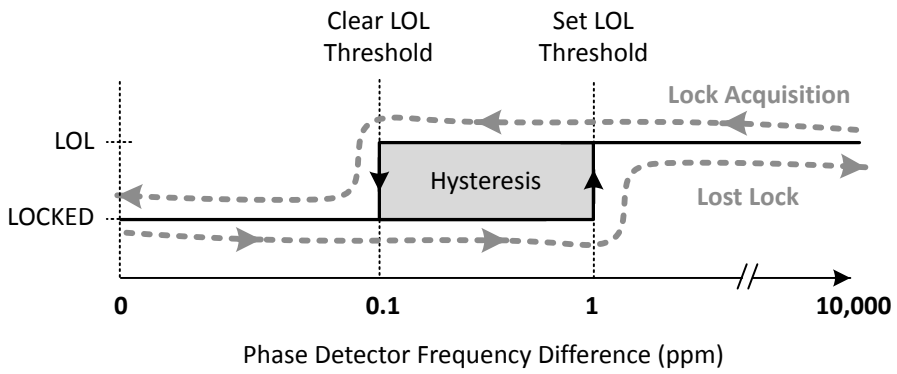


Figure 4.12. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

4.8.5 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt.

4.9 Outputs

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

4.9.1 Grade A/B/C/D and J/K/L/M

The Si539x "standard" grades A/B/C/D (external reference) and J/K/L/M (integrated reference) can generate any output frequency in any format with best-in-class jitter. These devices are available as a preprogrammed option or can be written to the device via I^2C. The input/output frequency plan determines whether the output divider operates in integer or fractional mode. In the fractional mode, the device can generate any output frequency or any format from any input frequency with best-in-class jitter. Some frequency plans allow the user to use an integer mode that delivers even lower jitter. See the Si5395-94-92 Family Reference Manual for more details.

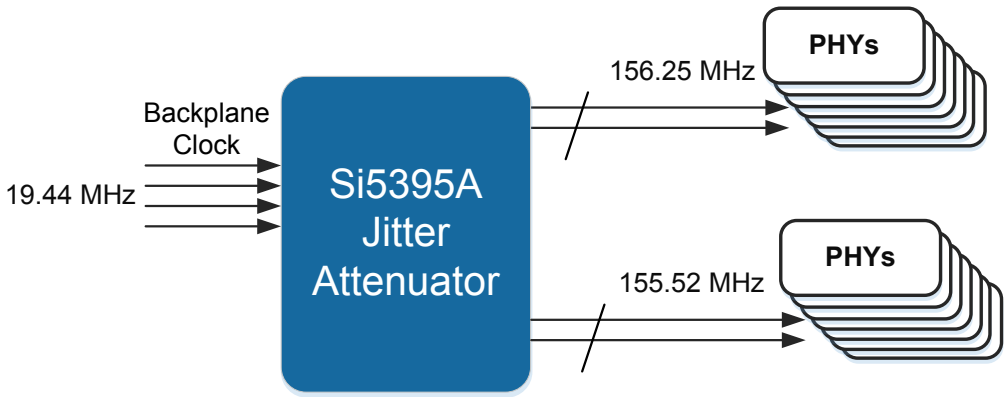


Figure 4.13. Si5395 A/B/C/D/J/K/L/M Jitter Attenuator

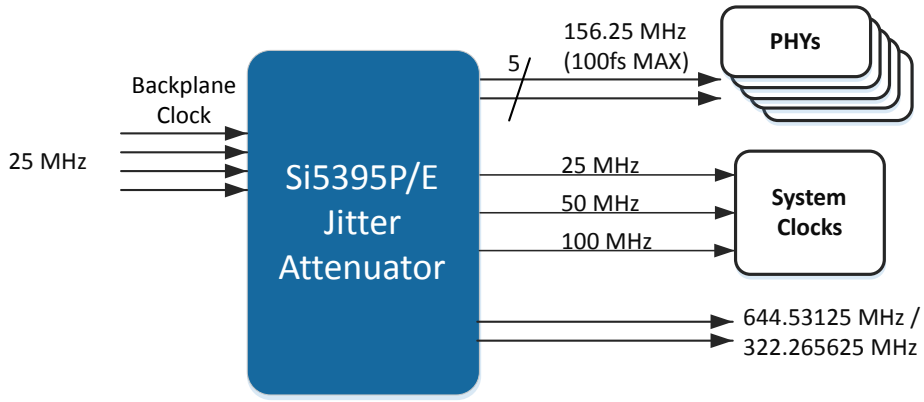
4.9.2 Grades P and E

Some applications, like 56G PAM4 SerDes, require even higher performance (< 100fs MAX) than is already provided by standard Skyworks jitter attenuators (<140fs MAX). The Si539x grades P (external reference) and E (integrated reference) are Precision grade jitter attenuators that calibrate out linearity errors to deliver the world's best jitter performance over a wide range of frequency plans.

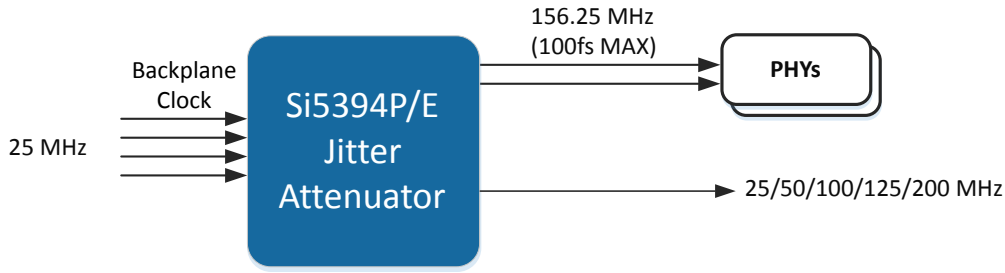
The Si5392P/E can support 1 clock domain while the Si5394P/E supports 1 or 2 clock domains and the Si5395P/E can support 1, 2 or 3 clock domains while delivering guaranteed low jitter of 100fs MAX on the primary SerDes clocks. The frequencies supported by the 3 domains are

- Domain#1 (Si5395/94/92 P/E) - 156.25/312.5/625 MHz
- Domain#2 (Si5395/94 P/E) - 25/50/100/125/200/156.25/312.5/625 MHz
- Domain#3 (Si5395 P/E) - 25/50/100/125/200/156.25/312.5/625/322.265625/644.53125 MHz

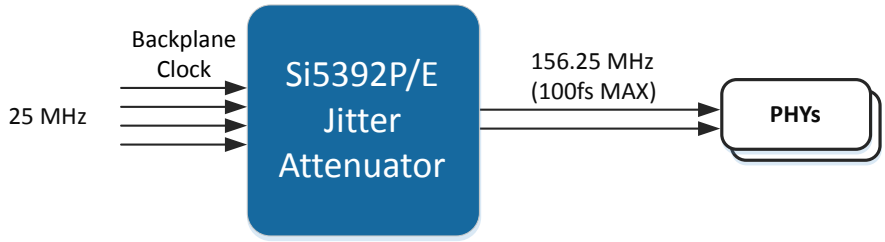
The examples below show examples of how each of the 3 devices can be used as jitter attenuators in 56G Pam4 SerDes applications.



Si5395P/E typical 56G SerDes application (up to 3 domains)



Si5394P/E typical 56G SerDes application (up to 2 domains)



Si5392P/E typical 56G SerDes application (1 domain)

Figure 4.14. Typical Grade P and Grade E 56G SerDes Applications

The external reference used on the XA/XB pins of the P grade is restricted to a 48 MHz crystal. No other values of crystal or other reference sources like XO or VCXO are allowed. If the design requires other crystal frequencies, then the standard Si539xA/B/C/D should be used instead of the Si539xP.

To deliver guaranteed jitter performance 100fs MAX on the 56 G Pam4 SerDes clocks, the additional system clocks must follow some specific design rules. Additionally, the device input clocks should be traceable back to a Stratum 3 primary reference clock. See the Si5395/94/92 Family Reference manual for more details on these design rules.

4.9.3 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

4.9.4 Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

4.9.5 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes are programmable so that LVDS specifications can be met and for the best signal integrity with different supply voltages. When DC coupling the output driver, it is essential that the receiver have a relatively high common mode impedance so that the common mode current from the output driver is very small.

4.9.6 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances. A source termination resistor is recommended to help match the selected output impedance to the trace impedance, where Rs = Transmission line impedance – Z_O. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO option as shown in the following table.

Table 4.3. Typical Output Impedance (Z_S)

VDDO	CMOS Drive Selections		
	OUTx_CMOS_DRV = 1	OUTx_CMOS_DRV = 2	OUTx_CMOS_DRV = 3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.9.7 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

4.9.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTx pin is generated with the same polarity (in phase) as the clock on the OUTxb pin. The polarity of these clocks is configurable, enabling complementary clock generation and/or inverted polarity with respect to other output drivers.

4.9.9 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high, all outputs are disabled. When held low, the outputs are enabled. Outputs in the enabled state can be individually disabled through register control.

4.9.10 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high.

4.9.11 Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

4.9.12 Input/Output Skew Control

The input-output skew can be adjusted in dynamic mode. The dynamic phase adjust will allow the device to dynamically and glitchlessly change the output phase using register writes with the device still powered up. The skew value may change after each reset or power cycle. See the family reference manual for more details.

4.9.13 Zero Delay Mode (Grades A/B/C/D and J/K/L/M)

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below. (Zero delay mode is only available for clock inputs that are higher than 128 kHz.)

This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. Note that the hitless switching feature is not available when zero delay mode is enabled.

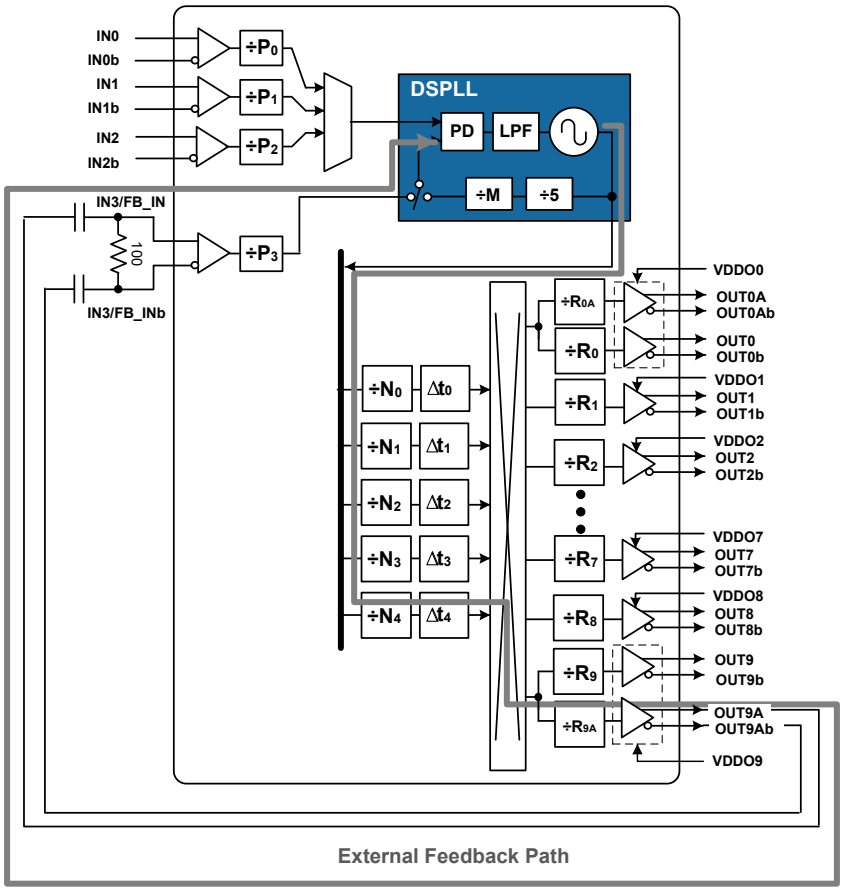


Figure 4.15. Si5395 Zero Delay Mode Setup

4.9.14 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers that are connected to the same N divider.

4.10 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Si5395-94-92 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.11 In-Circuit Programming

The Si5395/94/92 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5395-94-92 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.12 Serial Interface

Configuration and operation of the Si5395/94/92 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Si5395-94-92 Family Reference Manual for details.

4.13 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

4.14 Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. Refer to the Si5395-94-92 Family Reference Manual for a complete list of register descriptions and settings. It is strongly recommended that ClockBuilder Pro be used to create and manage register settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

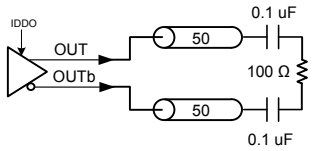
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1, 2, 3]	I_{DD}	Si5395	—	150	300	mA
		Si5394/92	—	125	250	mA
	I_{DDA}	Si5395	—	125	140	mA
		Si5394/92	—	115	130	mA
Output Buffer Supply Current	I_{DDOx}	2.5 V LVPECL Output[4]	—	22	26	mA
		2.5 V LVDS Output[4]	—	15	18	mA
		3.3 V LVCMOS Output[5]	—	22	30	mA
		2.5 V LVCMOS Output[5]	—	18	23	mA
		1.8 V LVCMOS Output[5]	—	12	16	mA
Total Power Dissipation[6]	P_d	Si5395[1]	—	1000	1400	mW
		Si5394[2]	—	750	1100	mW
		Si5392[3]	—	680	1000	mW

Notes:

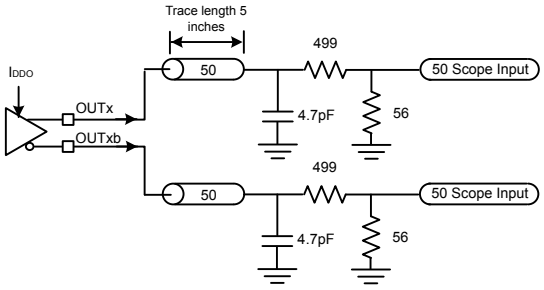
1. Si5395 test configuration: 7 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
2. Si5394 test configuration: 4 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
3. Si5392 test configuration: 2 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
4. Differential outputs enabled at 156.25 MHz and terminated into an ac-coupled 100 Ω load.

Differential Output Test Configuration



5. LVCMOS outputs enabled at 156.25 MHz and measured into a 5 inch 50 Ω PCB trace with 4.7 pF load. Measurements were made with OUTx_CMOS_DRV=3. See Reference Manual for more details on register settings.

LVCMOS Output Test Configuration



6. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 5.3. Input Clock Specifications

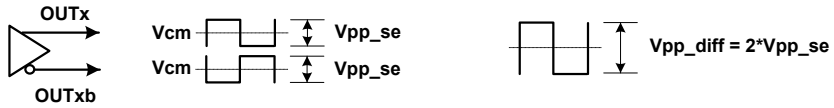
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended - AC Coupled Input Buffer (IN0/IN0b, IN1/IN1b, IN2/IN2b, IN3/FB_IN, IN3b/FB_INb)						
Input Frequency Range	f_{IN}	Differential	0.008	—	750	MHz
		All Single-ended signals (including LVCMOS)	0.008	—	250	MHz
Voltage Swing[1]	V_{IN}	Differential AC-coupled f_{IN} < 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled 250 MHz < f_{IN} < 750 MHz	225	—	1800	mVpp_se
		Single-ended AC-coupled f_{IN} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		—	2.4	—	pF
Input Resistance Differential	R_{IN_DIFF}		—	16	—	kΩ
Input Resistance Single-Ended	R_{IN_SE}		—	8	—	kΩ
LVCMOS / Pulsed CMOS DC-Coupled Input Buffer (IN0, IN1, IN2, IN3/FB_IN)[4]						
Input Frequency	f_{IN_CMOS}	Standard CMOS & Non-standard CMOS	0.008	—	250	MHz
		Pulsed CMOS	0.008	—	1	MHz
Input Voltage[5]	V_{IL}	Standard CMOS	—	—	0.5	V
		Non-standard CMOS & Pulsed CMOS	—	—	0.4	V
	V_{IH}	Standard CMOS	1.3	—	—	V
		Non-standard CMOS & Pulsed CMOS	0.8	—	—	V
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC	Standard CMOS & Non-standard CMOS	40	—	60	%
		Pulsed CMOS	5		95	
Minimum Pulse Width	PW	Standard CMOS & Non-standard CMOS (250 MHz @ 40% Duty Cycle)	1.6	—	—	ns
		Pulsed CMOS (1 MHz @ 40% Duty Cycle)	50	—	—	
Input Resistance	R_{IN}		—	8	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFCLK (Applied to XA/XB) (Grade A/B/C/D)						
REFCLK Frequency	f_{IN_REF}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
		TCXO frequency for SyncE applications. Jitter performance may be reduced.	—	40	—	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
Input Differential Voltage Swing	V_{IN_DIFF}		365		2500	mVpp_diff
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%

Note:

1. Voltage swing is specified as single-ended mVpp.



2. Recommended for specified jitter performance. Slew rate can go lower, but jitter performance could degrade if the minimum slew rate specification is not met (see the Si5395-94-92 Family Reference Manual).
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN_Vpp_se}) / SR$.
4. Standard, Non-standard and Pulsed CMOS refer to different formats of CMOS each with a voltage swing of 1.8V, 2.5V or 3.3V +/-5%.
   - Standard CMOS refers to the industry standard LVCMOS signal.
   - Non-standard CMOS refers to a signal that has been attenuated/level-shifted in order to comply with the specified non-standard VIL and VIH specifications.
   - Pulsed CMOS refers to a signal that has been attenuated/level-shifted and has a low/high duty cycle and must be dc coupled. A typical application example is a low-frequency video frame sync pulse.

   Refer to the Si5395-94-92 Family Reference Manual for the recommended connections/termination for the different modes.
5. CMOS signals that exceed 3.3 V + 5% can be used as inputs as long as a resistive attenuation network is used to guarantee that the input voltage at the pin does not violate the device's input ratings. Please refer to the Si5395-94-92 Family Reference Manual for the recommended connections/termination for this mode.

Table 5.4. Serial and Control Input Pin Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5395 Serial and Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, A1/SDO, SCLK, A0/CSb, FINC, FDEC, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, FINC and FDEC	100	—	—	ns
Update Rate	T_{UR}	FINC and FDEC	1	—	—	µs
Si5394/92 Serial and Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5395-94-92 Family Reference Manual for more details on the proper register settings.

Table 5.5. Differential Clock Output Specifications

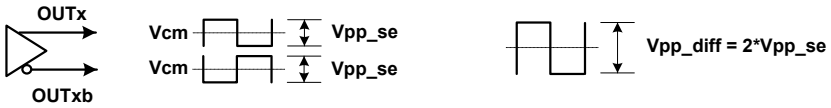
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Si5395/94/92							
Output Frequency	f_{OUT}	MultiSynth not used		0.0001	—	720	MHz
				733.33	—	800.00	MHz
				825	—	1028	MHz
		MultiSynth used		0.0001	—	720	MHz
Duty Cycle[1]	DC	MultiSynth used: f_{OUT} < 400 MHz		48	—	52	%
		MultiSynth used: 400 MHz < f_{OUT} <= 720 MHz		45	—	55	%
		MultiSynth not used: f_{OUT} < 1028 MHz		25	—	75	%
Output Voltage Swing[2]	VOUT	V_{DDO} = 3.3 V, 2.5 V, 1.8 V	LVDS	350	450	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	630	780	950	mVpp_se
Common Mode Voltage[2, 3] (100 Ω load line-to-line)	VCM	V_{DDO} = 3.3 V	LVDS	1.1	1.2	1.3	V
			LVPECL	1.9	2.0	2.1	V
		V_{DDO} = 2.5 V	LVPECL LVDS	1.1	1.2	1.3	V
		V_{DDO} = 1.8 V	sub-LVDS	0.8	0.9	1.0	V
Output-to-Output Skew (Same MultiSynth)	T_{SKS}	f_{OUT} = 712.5 MHz (LVDS)		—	0	75	ps
Out-Outb Skew on one output	TSK_OUT	Measured from positive to negative output pins (LVDS)		—	0	50	ps
Rise and Fall Times[2]	t_r/t_f	f_{OUT} > 100 MHz (20% to 80%)		—	100	200	ps
Differential Output Impedance	ZO			—	100	—	Ω
Power Supply Noise Rejection[3]	PSRR	10 kHz sinusoidal noise		—	–101	—	dBc
		100 kHz sinusoidal noise		—	–96	—	dBc
		500 kHz sinusoidal noise		—	–99	—	dBc
		1 MHz sinusoidal noise		—	–97	—	dBc
Output-to-Output Crosstalk[4]	XTALK	Si5395		—	–72	—	dBc
		Si5394/92		—	–88	—	dBc

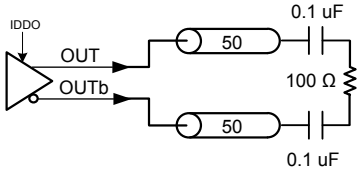
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. Duty cycle can vary depending on frequency plan (output frequency and divide ratios).
2. Output amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. Note that the maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5395-94-92 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.



Differential Output Test Configuration



3. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 5.6. LVCMOS Clock Output Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

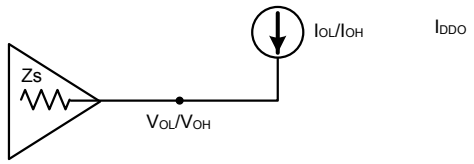
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		44	—	56	%
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –12 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –17 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –8 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –11 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –5 mA	V_{DDO} x 0.85	—	—	V
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 12 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 17 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 8 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 11 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 5 mA	—	—	V_{DDO} x 0.15	V
Rise and Fall Times[3]	t_r/t_f	(20% to 80%)	V_{DDO} = 3.3V	—	400	600	ps
			V_{DDO} = 2.5 V	—	450	600	ps
			V_{DDO} = 1.8 V	—	550	750	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5395-94-92 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration.

DC Test Configuration



3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 4.7 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

LVCMOS Output Test Configuration

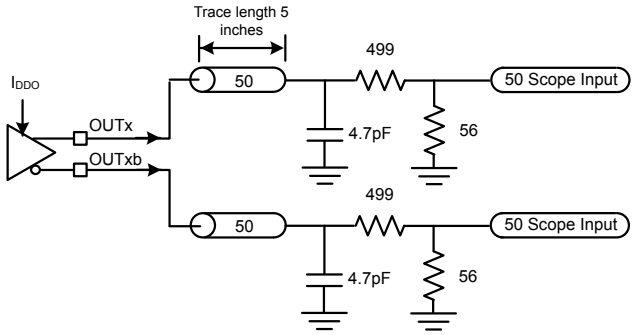


Table 5.7. Output Status Pin Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5395 Status Output Pins (LOLb, INTRb, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5394/92 Status Output Pins (INTRb, SDA/SDIO1[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5394 Status Output Pins (LOLb, LOS_XAXBb) **Si5392 Status Output Pins (LOLb, LOS_XAXBb, LOS0b, LOS1b, LOS2b, LOS3b)**						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. VOL remains valid in all cases.
2. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5395-94-92 Family Reference Manual for more details on the proper register settings.

Table 5.8. Performance Characteristics

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}			0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	Grade A/B/C/D/J/K/L/M	—	30	45	ms
			Grade P/E	—	460	625	ms
PLL Lock Time[2]	t_{ACQ}	With Fastlock enabled, f_{IN} = 19.44 MHz		—	280	300	ms
Output Dynamic Delay Adjustment	t_{DELAY}	f_{VCO} = 14 GHz		—	71.4	—	ps
	t_{RANGE}			—	±1	—	ms
POR to Serial Interface Ready[3]	t_{RDY}			—	—	15	ms
Maximum Phase Transient During a Hitless Switch[4]	t_{SWITCH}	Single automatic/manual switch between two 8 kHz inputs, DSPLL BW = 40 Hz		—	—	1.5	ns
		Single automatic/manual switch between two 2 MHz inputs, DSPLL BW = 400 Hz		—	—	0.3	ns
Zero Delay Mode Input-to-Output Delay Variation[5]	t_{ZDELAY}	Between reference and feedback input with both clocks in LVDS differential format at 128 kHz.		—	—	0.20	ns
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a Loop Bandwidth of 4 Hz		—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1 and 2 for 1G, 10G or 25G Synchronous Ethernet Jitter Modulation Frequency = 10 Hz		—	3180	—	UI pk-pk
Pull-in Range	ω_P			—	500	—	ppm
RMS Phase Jitter (Grade P)[6]	J_{GEN}	f_{in} = f_{out} = 312.5 MHz or 156.25 MHz		—	75	100	fs
		f_{in} = 25 MHz	f_{out} = 156.25 MHz	—	69	90	fs
			f_{out} = 312.5 MHz	—	69	95	fs
			f_{out} = 100 MHz	—	150	200	fs
			f_{out} = 50/25 MHz	—	200	300	fs
			f_{out} = 644.531248 MHz	—	80	—	fs
RMS Phase Jitter (Grade E)[6]	J_{GEN}	f_{in} = f_{out} = 312.5 MHz or 156.25 MHz		—	82	110	fs
		f_{in} = 25 MHz	f_{out} = 156.25 MHz	—	71	100	fs
			f_{out} = 312.5 MHz	—	75	105	fs
			f_{out} = 100 MHz	—	150	200	fs
			f_{out} = 50/25 MHz	—	200	300	fs
			f_{out} = 644.531248 MHz	—	85	—	fs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RMS Phase Jitter (Grade A/B/C/D and J/K/L/M)[7]	J_{GEN}	Output divider Integer Mode	—	85	120	fs
		Output divider Fractional Mode/DCO Mode	—	115	170	fs

Note:

1. Actual loop bandwidth might be lower; please refer to CBPro for actual value for your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal bandwidth set to 100 Hz, fastlock bandwidth set to 1 kHz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator deassertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Higher input frequencies will typically result in higher Fpfd frequencies, which, in turn, will result in better hitless switching performance. It is recommended to use higher input frequencies for the best hitless switching performance.
5. Zero-Delay-Mode is dependent on frequency configuration. Using Fpfd < 128 kHz will result in higher delay values. Ref clock rise time must be <200 ps. Initial Start-Up time can be much higher in Zero Delay mode.
6. Grade P and E are calibrated for optimum performance in 56G/112G SerDes applications at frequencies of 312.5 MHz or 156.25 MHz. Specific layout rules must be followed to achieve optimum performance. For more details, refer to 4.9.2 Grades P and E and the reference manual.
7. Grades A/B/C/D and J/K/L/M are targeted for applications that require more flexibility and set the output divider to Integer or Fractional modes. Integer mode test conditions: f_{in} = 19.44 MHz; f_{out} = 155.52 MHz. Fractional mode test conditions: f_{in} = 19.44 MHz; f_{out} = 125 MHz. All outputs are assumed to be LVPECL. For more details, refer to 4.9.1 Grade A/B/C/D and J/K/L/M.

Table 5.9. I²C Timing Specifications (SCL, SDA)

V_{DD}= 1.8 V ±5%, V_{DDA}= 3.3 V ±5%, V_{DDS}/V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A= –40 to 85 °C

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—		25	35	25	35	ms
Hold time (Repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Setup Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of both SDA and SCL Signals	t_f		—	300	—	300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

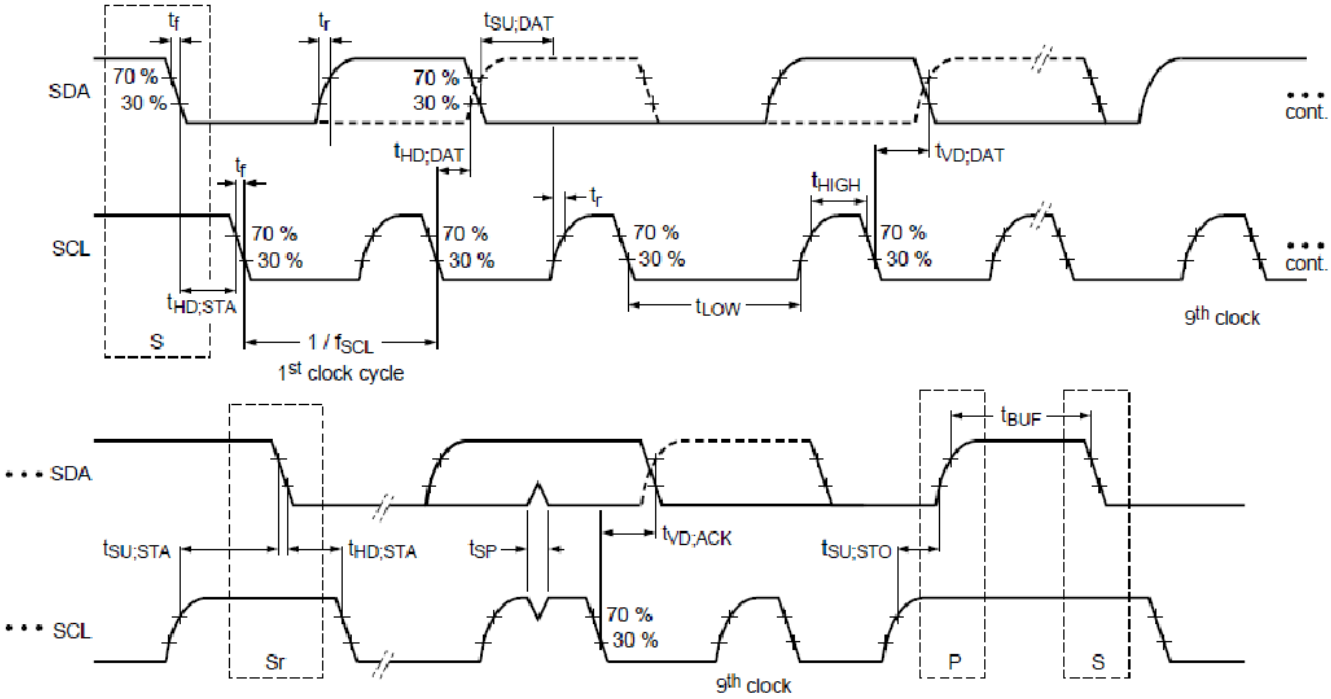


Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	10	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	95	—	—	ns

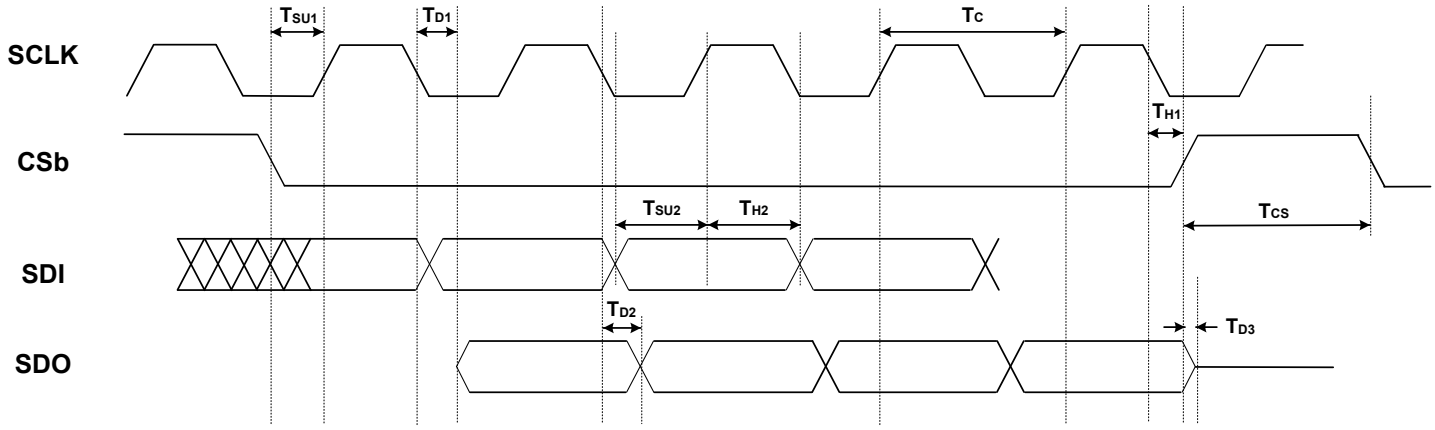


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	10	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, CSb to SCLK Fall	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	95	—	—	ns

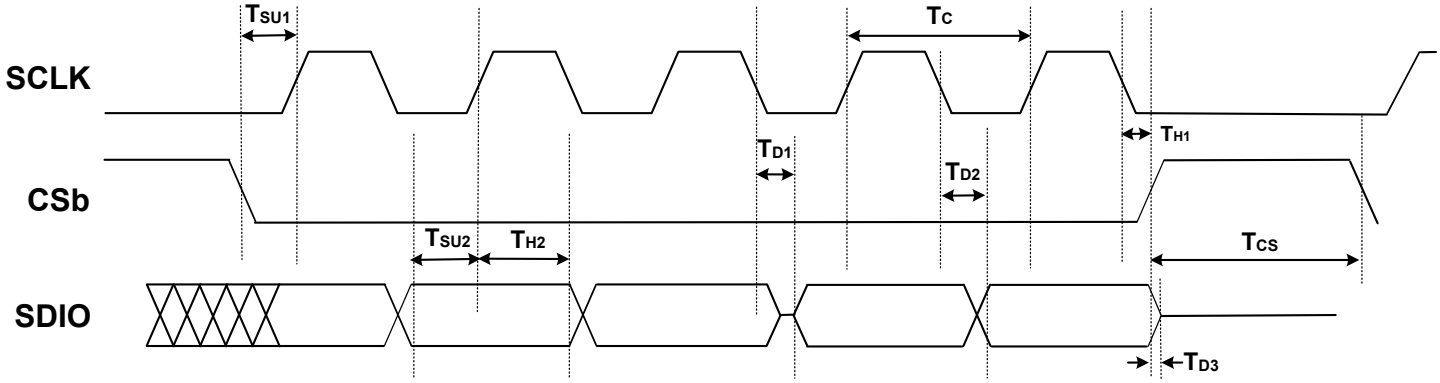


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. External Crystal Specifications for Grades A/B/C/D/P

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	f_{XTAL} (A/B/C/D)	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
	f_{XTAL} (P)	±100 ppm crystal	48	—	48	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance Shunt Capacitance	r_{ESR} C_O	Refer to the Si5395-94-92 Family Reference Manual to determine ESR and shunt capacitance values.				

Note:
1. Refer to the Si534x/8x/9x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 48 to 54 MHz crystals.

Table 5.13. Internal Reference Specifications for Grade J/K/L/M/E[1, 2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Initial Accuracy	—		–8	—	+8	ppm
Frequency Characteristics across Temperature	—	Inclusive of temperature range of –40 to 125 °C, aging at 115 °C and reflow	–88	—	+88	ppm
Activity Dip	—	Frequency Perturbations	–2	—	+2	ppm
Overall Accuracy	—	Inclusive of Initial Accuracy, Frequency Characteristics Across Temperature and Activity Dips (all items listed above)	–98	—	+98	ppm

Note:
1. These devices with integrated reference have been tuned with an internal 48 MHz reference to deliver optimum performance. It is important to note that connecting an external reference to a device that already has an integrated reference is not allowed. Doing so could lead to internal damage to the circuits.
2. Clocks that feature the integrated crystal may require a slightly longer settling time compared to the external crystal device. See the Reference Manual for more details.

Table 5.14. Thermal Characteristics 44-QFN and 44-LGA (Si5392 and Si5394)

Parameter	Symbol	Test Condition	44-QFN	44-LGA	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1, 2]	22.3	25.49	°C/W
		Air Flow 1 m/s[1, 2]	19.4	22.14	°C/W
		Air Flow 2 m/s[1, 2]	18.4	21.13	°C/W
Thermal Resistance Junction to Case	θ_{JC}		10.9	9.87	°C/W
Thermal Resistance Junction to Board	θ_{JB}		9.3	9.52	°C/W
	Ψ_{JB}		9.2	9.58	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	0.81	°C/W

Note:
1. 44-QFN: Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.
2. 44-LGA: Based on 4 layer PCB with dimension 4" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 16 Via to top internal plane of PCB.

Table 5.15. Thermal Characteristics 64-QFN and 64-LGA (Si5395)

Parameter	Symbol	Test Condition	64-QFN	64-LGA	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1, 2]	22	22.3	°C/W
		Air Flow 1 m/s[1, 2]	19.4	19.4	°C/W
		Air Flow 2 m/s[1, 2]	18.3	18.4	°C/W
Thermal Resistance Junction to Case	θ_{JC}		9.5	10.9	°C/W
Thermal Resistance Junction to Board	θ_{JB}		9.4	9.3	°C/W
	Ψ_{JB}		9.3	9.2	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	0.23	°C/W

Note:
1. 64-QFN: Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.
2. 64-LGA: Based on 4 layer PCB with dimension 4" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 16 Via to top internal plane of PCB.

Table 5.16. Absolute Maximum Ratings [1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1} [4]	IN0–IN3/FB_IN	–1.0 to 3.8	V
	V_{I2}	IN_SEL1, IN_SEL0, RSTb, OEb, I2C_SEL, FINC, FDEC, SDI, SCLK, A0/CSb, A1, SDA/SDIO	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Maximum Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20–40	s

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN/LGA and 44-QFN/LGA packages are RoHS compliant.
3. For detailed packaging information, go to https://www.skyworksinc.com/.
4. The minimum voltage at these pins can be as low as –1.0 V when an ac input signal of 8 kHz or greater is applied. See Table 5.3 Input Clock Specifications on page 26 for single-ended ac-coupled f_{IN} < 250 MHz.
5. The device is compliant with JEDEC J-STD-020.

6. Typical Application Schematic

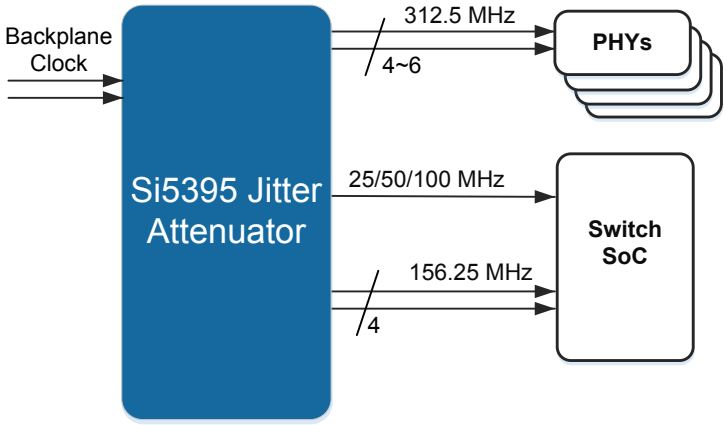


Figure 6.1. Typical 56G SerDes Application

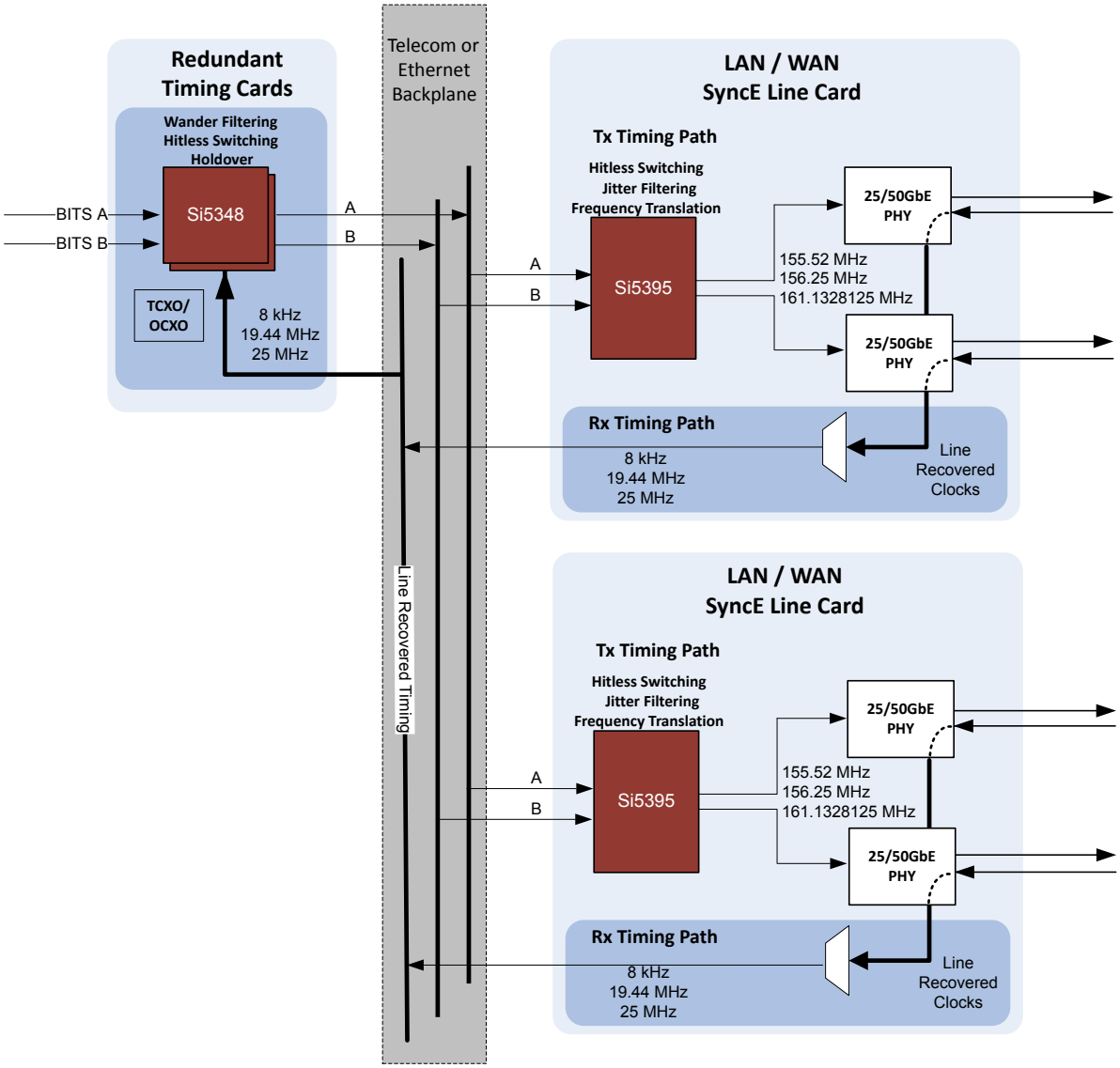


Figure 6.2. SyncE Line Card

7. Detailed Block Diagrams

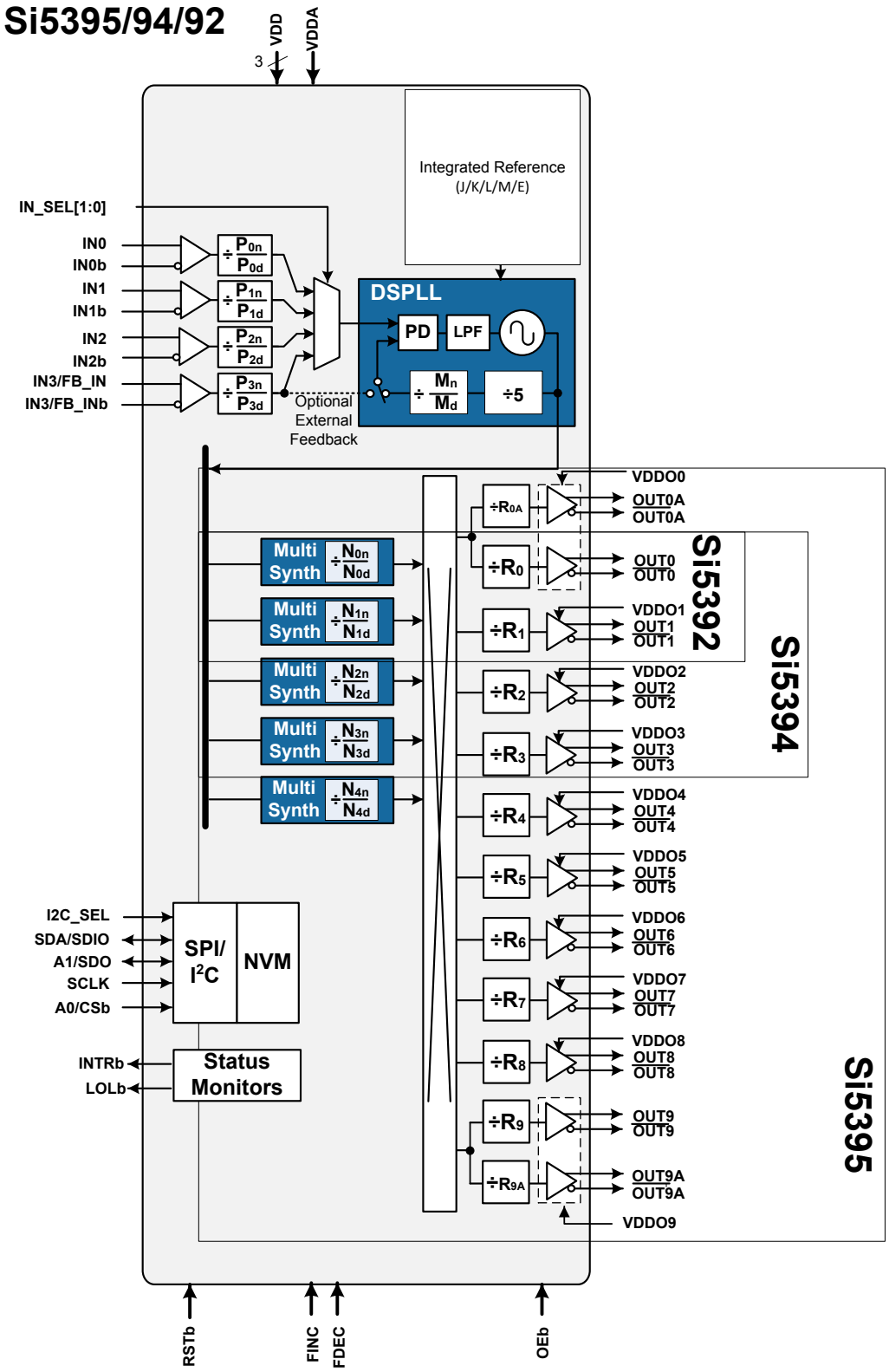


Figure 7.1. Si5392/94/95 Block Diagram

8. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V; V_{DDA} = 3.3 V; V_{DDS} = 3.3 V, 1.8 V; T_A = 25 °C.

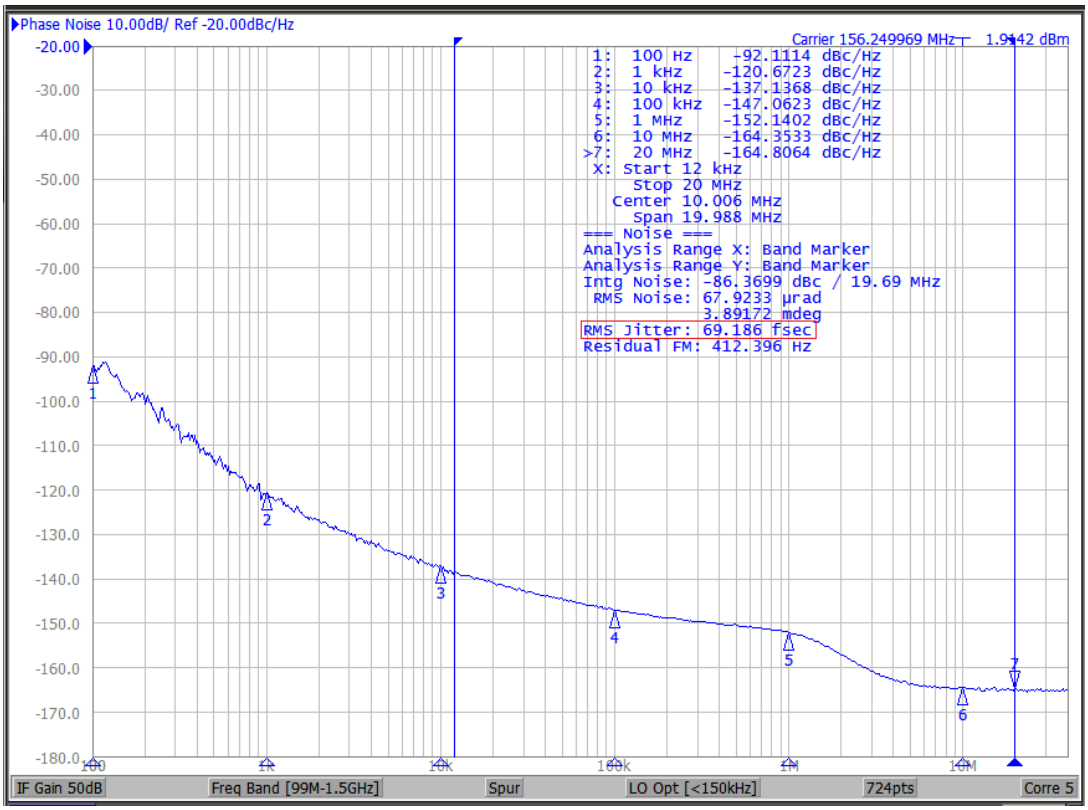


Figure 8.1. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS (Si539x P-Grade)

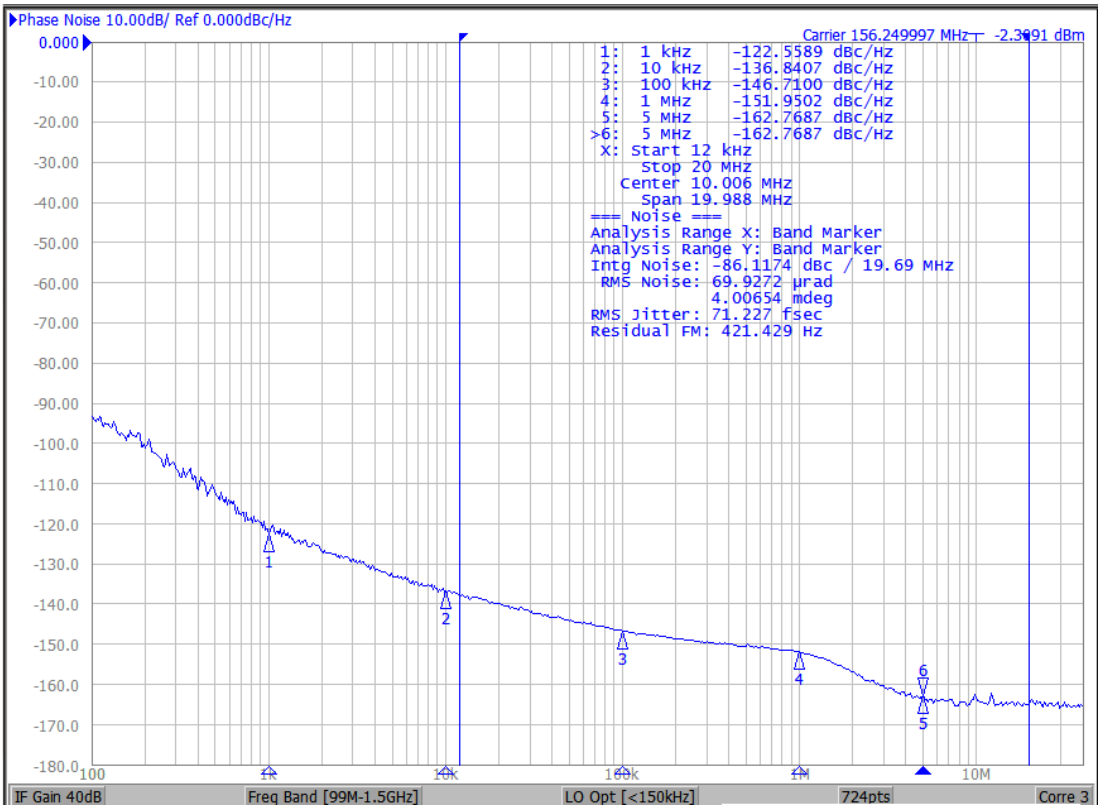


Figure 8.2. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS (Si539x E-Grade)

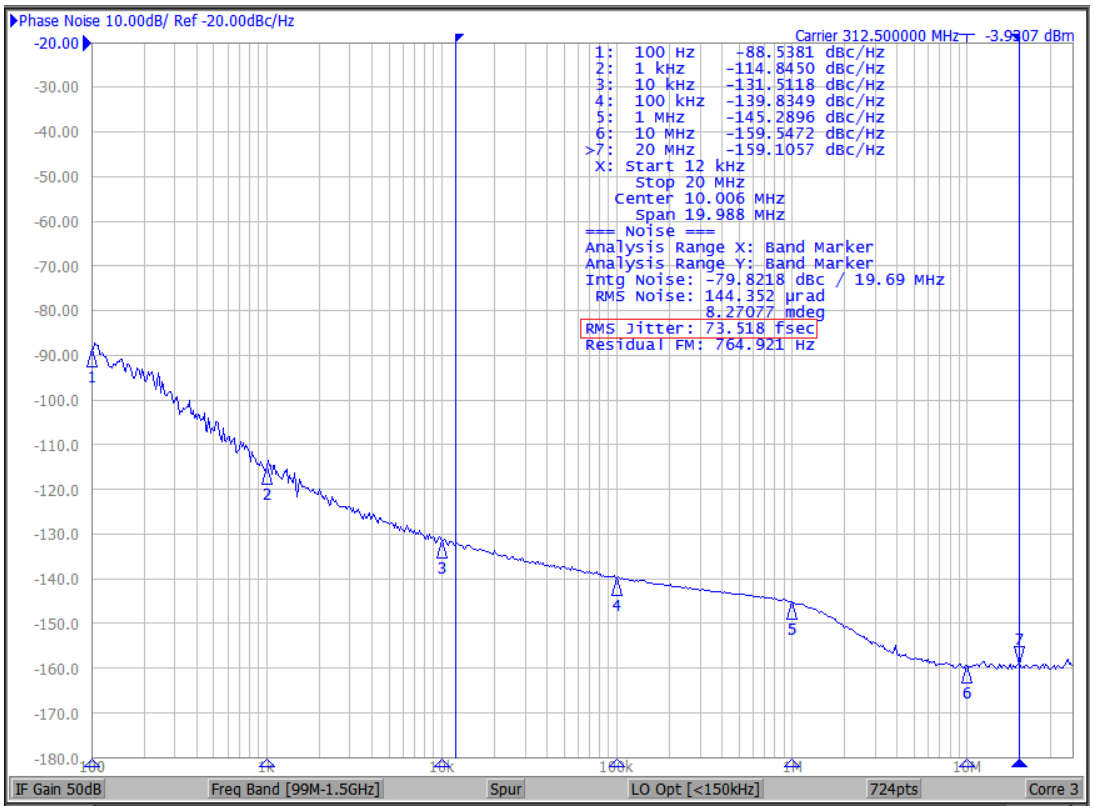


Figure 8.3. Input = 25 MHz; Output = 312.5 MHz, 2.5 V LVDS (Integer Mode)

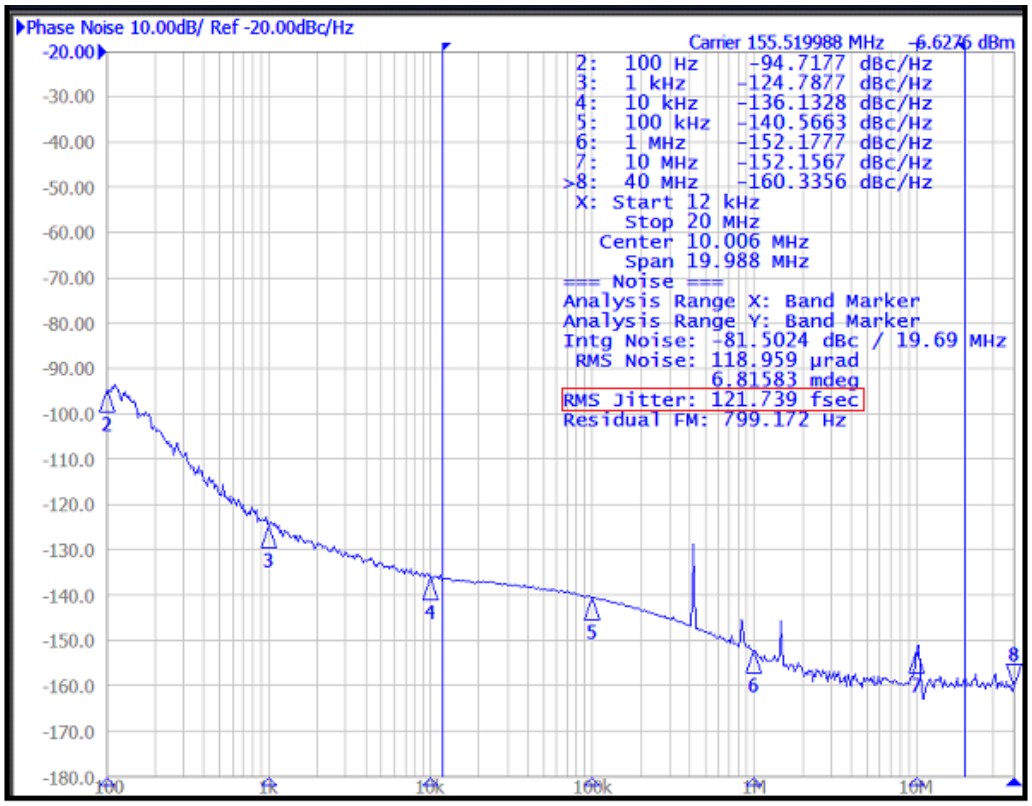
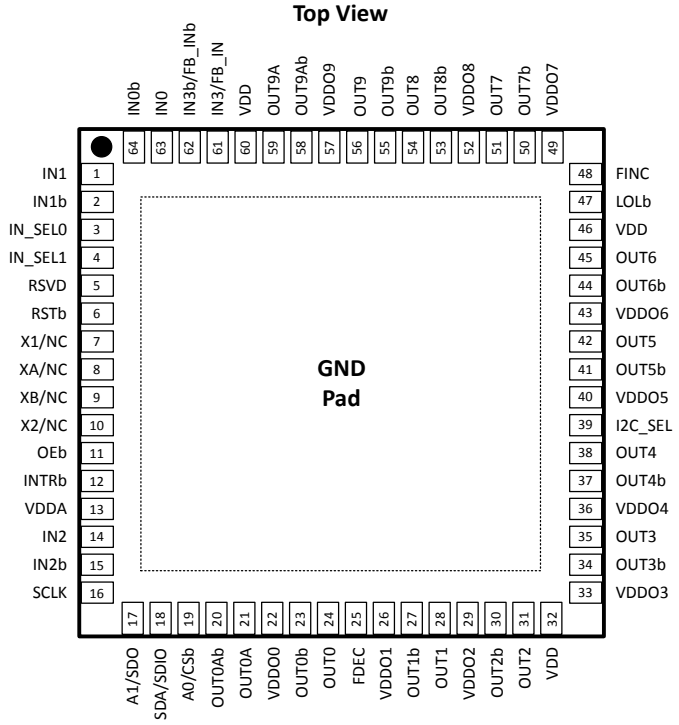


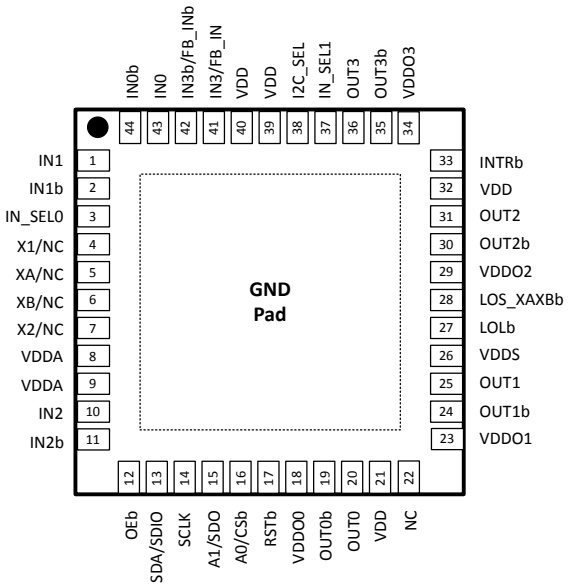
Figure 8.4. Input = 25 MHz; Output = 155.52 MHz, 2.5 V LVDS (Fractional Mode)

9. Pin Descriptions

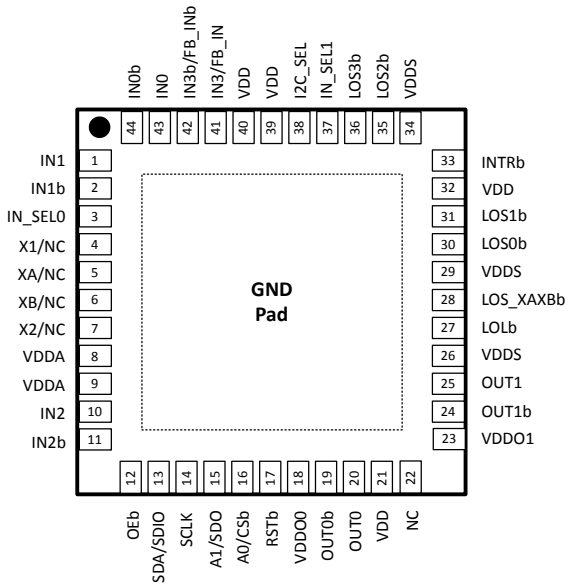
Si5395 (64-QFN and 64-LGA)
Top View



Si5394 (44-QFN and 44-LGA)
Top View



Si5392 (44-QFN and 44-LGA)
Top View



Note: Grades A/B/C/D require external references so these pins can be connected to those references (XTAL, XO, VCXO, and so on). Note that connecting an external reference to a device that already has an internal reference is not recommended and could lead to internal damage to the circuits.

Table 9.1. Si5395/94/92 Pin Descriptions

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
Inputs					
XA/NC	8	5	5	I	**Crystal Input for Grade A/B/C/D/P.** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode. **NC (No-Connect) for Grades J/K/L/M/E.** These devices have an integrated reference and these pins cannot be connected to an external reference. They should be left floating to avoid damage or interference to the internal reference.
XB/NC	9	6	6	I	
X1/NC	7	4	4	I	**XTAL Shield for Grade A/B/C/D/P.** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5395-94-92 Family Reference Manual for layout guidelines. **NC (No-Connect) for Grades J/K/L/M/E** or external reference clocks. These pins should be left disconnected for Grades J/K/L/M/E with integrated reference or when connecting XA/XB pins to an external reference clock (REFCLK)
X2/NC	10	7	7	I	
IN0	63	43	43	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to the Si5395-94-92 Family Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
IN0b	64	44	44	I	
IN1	1	1	1	I	
IN1b	2	2	2	I	
IN2	14	10	10	I	
IN2b	15	11	11	I	
IN3/FB_IN	61	41	41	I	**Clock Input 3/External Feedback Input.** By default these pins are used as the fourth clock input (IN3/IN3b). They can also be used as the external feedback input (FB_IN/FB_INb) for the optional zero delay mode. See 4.9.13 Zero Delay Mode (Grades A/B/C/D and J/K/L/M) for details on the optional zero delay mode.
IN3b/FB_INb	62	42	42	I	

Table 9.2. Si5395/94/92 Pin Descriptions

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
Outputs					
OUT0Ab	20	—	—	O	**Output Clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in the Si5395-94-92 Family Reference Manual. Unused outputs should be left unconnected.
OUT0A	21	—	—	O	
OUT0	24	20	20	O	
OUT0b	23	19	19	O	
OUT1	28	25	25	O	
OUT1b	27	24	24	O	
OUT2	31	31	—	O	
OUT2b	30	30	—	O	
OUT3	35	36	—	O	
OUT3b	34	35	—	O	
OUT4	38	—	—	O	
OUT4b	37	—	—	O	
OUT5	42	—	—	O	
OUT5b	41	—	—	O	
OUT6	45	—	—	O	
OUT6b	44	—	—	O	
OUT7	51	—	—	O	
OUT7b	50	—	—	O	
OUT8	54	—	—	O	
OUT8b	53	—	—	O	
OUT9	56	—	—	O	
OUT9b	55	—	—	O	
OUT9A	59	—	—	O	
OUT9Ab	58	—	—	O	
Serial Interface					
I2C_SEL	39	38	38	I	**I²C Select[2].** This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit.

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
SDA/SDIO	18	13	13	I/O	**Serial Data Interface[2]** This is the bidirectional data pin (SDA) for the I²C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I²C mode, this pin is an open-drain output and must be pulled up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode as the output is a push-pull driver. Tie low when unused.
A1/SDO	17	15	15	I/O	**Address Select 1/Serial Data Output[2]** In I²C mode, this pin is open-drain and functions as the A1 address input pin. It does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this output is a push-pull driver and functions as the serial data output (SDO) pin. It drives high to the voltage selected by the IO_VDD_SEL bit. Leave disconnected when unused.
SCLK	16	14	14	I	**Serial Clock Input[2]** This pin functions as the serial clock input for both I²C and SPI modes. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused.
A0/CSb	19	16	16	I	**Address Select 0/Chip Select[2]** This pin functions as the hardware controlled address A0 in I²C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use.
Control/Status					
INTRb	12	33	33	O	**Interrupt[2]** This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	6	17	17	I	**Device Reset[2]** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use.
OEb	11	12	12	I	**Output Enable[2]** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use.
LOLb	47	—	—	O	**Loss of Lock (Si5395)[2]** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
	—	27	27	O	**Loss of Lock (Si5394/92)[3]** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
LOS0b	—	—	30	O	**Loss of Signal for IN0[3]** This pin indicate a loss of clock at the IN0 pin when low.
LOS1b	—	—	31	O	**Loss of Signal for IN1[3]** This pin indicate a loss of clock at the IN1 pin when low.
LOS2b	—	—	35	O	**Loss of Signal for IN2[3]** This pin indicate a loss of clock at the IN2 pin when low.
LOS3b	—	—	36	O	**Loss of Signal for IN3[3]** This pin indicate a loss of clock at the IN3 pin when low.
LOS_XAXBb	—	28	28	O	**Loss of Signal on XA/XB Pins[3]** This pin indicates a loss of signal at the XA/XB pins when low.
FINC	48	—	—	I	**Frequency Increment Pin[2]** This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.
FDEC	25	—	—	I	**Frequency Decrement Pin[2]** This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.
IN_SEL0	3	3	3	I	**Input Reference Select[2]** The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 4.1 Manual Input Selection Using IN_SEL[1:0] Pins on page 13. These pins are internally pulled low.
IN_SEL1	4	37	37	I	
RSVD	5	—	—	—	**Reserved** These pins are connected to the die. Leave disconnected.
NC	—	22	22		**No Connect** These pins are not connected to the die. Leave disconnected.
Power					
VDD	32	21	21	P	**Core Supply Voltage** The device operates from a 1.8 V supply. A 1.0 µF bypass capacitor should be placed very close to this pin. See the Si5395-94-92 Family Reference Manual for power supply filtering recommendations.
	46	32	32	P	
	60	39	39	P	
	—	40	40	P	
VDDA	13	8	8	P	**Core Supply Voltage 3.3 V** This core supply pin requires a 3.3 V power source. A 1 µF bypass capacitor should be placed very close to this pin. See the Si5395-94-92 Family Reference Manual for power supply filtering recommendations.
	—	9	9	P	

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
VDDS	—	26	26	P	**Status Output Voltage** The voltage on this pin determines VOL/VOH on the Si5392/94 LOLb and LOL_XAXBb. It also determines the levels on the LOS0b, LOS1b, LOS2b, and LOS3b outputs of the Si5392. Connect to either 3.3 V or 1.8 V. A 1.0 µF bypass capacitor should be placed very close to this pin. This voltage must match the IO operating voltage selected for the frequency plan in CBPro.
	—	—	29	P	
	—	—	34	P	
VDDO0	22	18	18	P	**Output Clock Supply Voltage** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	23	23	P	
VDDO2	29	29	—	P	
VDDO3	33	34	—	P	
VDDO4	36	—	—	P	
VDDO5	40	—	—	P	
VDDO6	43	—	—	P	
VDDO7	49	—	—	P	
VDDO8	52	—	—	P	
VDDO9	57	—	—	P	
GND PAD	—	—	—	P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

Note:

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
4. Refer to the Si5395-94-92 Family Reference Manual for more information on register setting names.
5. All status pins except I^2C and SPI are push-pull.

10. Package Outlines

10.1 Si5395 A/B/C/D/P (External Reference) 9x9 mm 64-QFN Package Diagram

The following figure illustrates the package details for the Si5395 A/B/C/D/P. The table lists the values for the dimensions shown in the illustration.

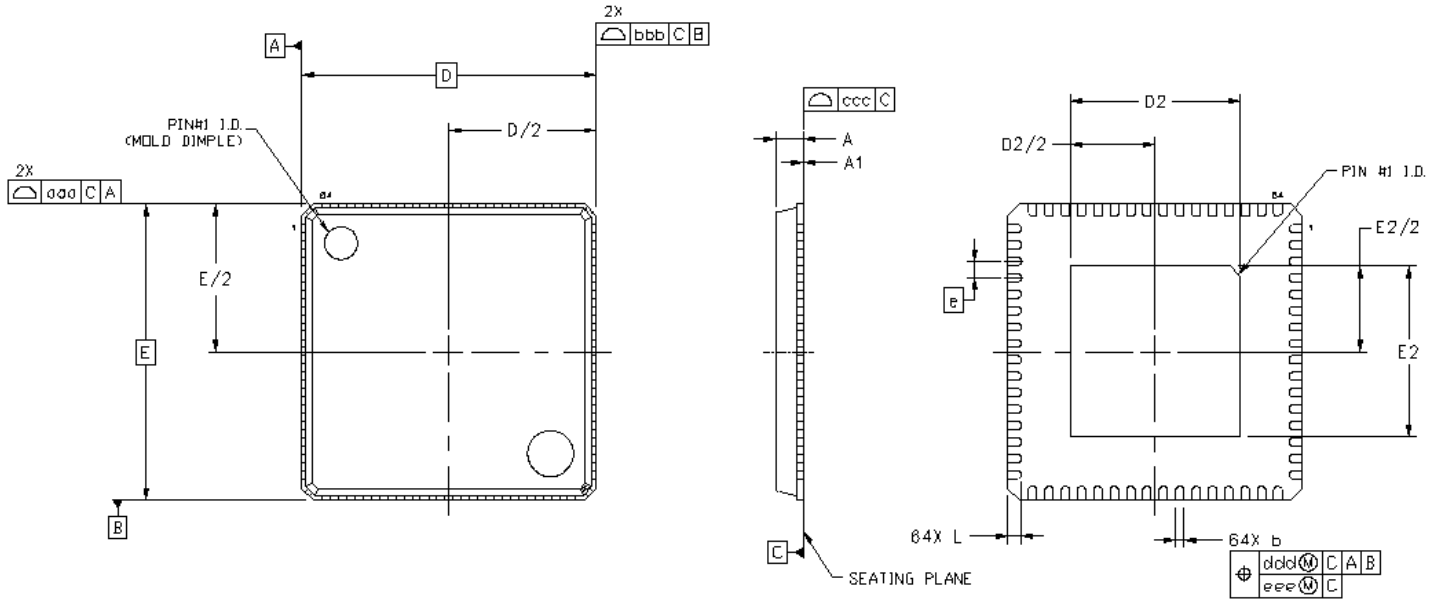


Figure 10.1. 64-Pin Quad Flat No-Lead (QFN)

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 Si5395 J/K/L/M/E (Internal Reference) 9x9 mm 64-LGA Package Diagram

The following figure illustrates the package details for the Si5395 J/K/L/M/E. The table lists the values for the dimensions shown in the illustration.

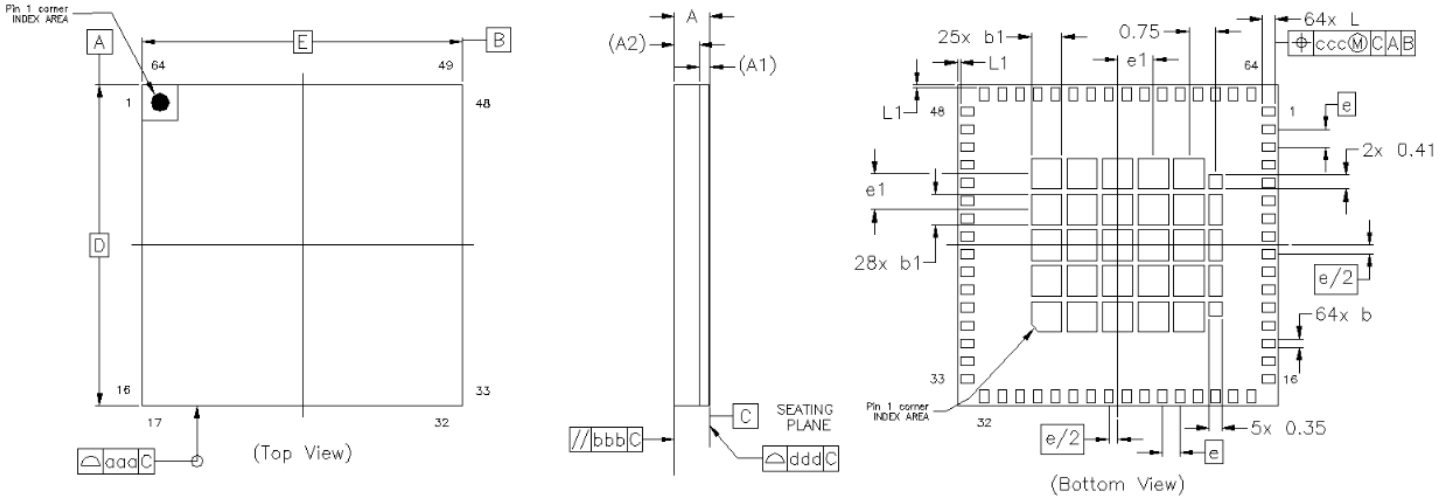


Figure 10.2. 64-Pin LGA

Table 10.2. Package Dimensions

Dimension	Min	Nom	Max
A	0.9	1	1.1
A1		0.26 REF	
A2		0.70 REF	
b	0.2	0.25	0.3
b1	0.8	0.85	0.9
D		9 BSC	
E		9 BSC	
e		0.5 BSC	
e1		1.0 BSC	
L	0.315	0.365	0.415
L1		0.080 REF	
aaa		0.1	
bbb		0.2	
ccc		0.1	
ddd		0.08	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 Si5394 and Si5392 A/B/C/D/P (External Reference) 7x7 mm 44-QFN Package Diagram

The following figure illustrates the package details for the Si5394 and Si5392. The table lists the values for the dimensions shown in the illustration.

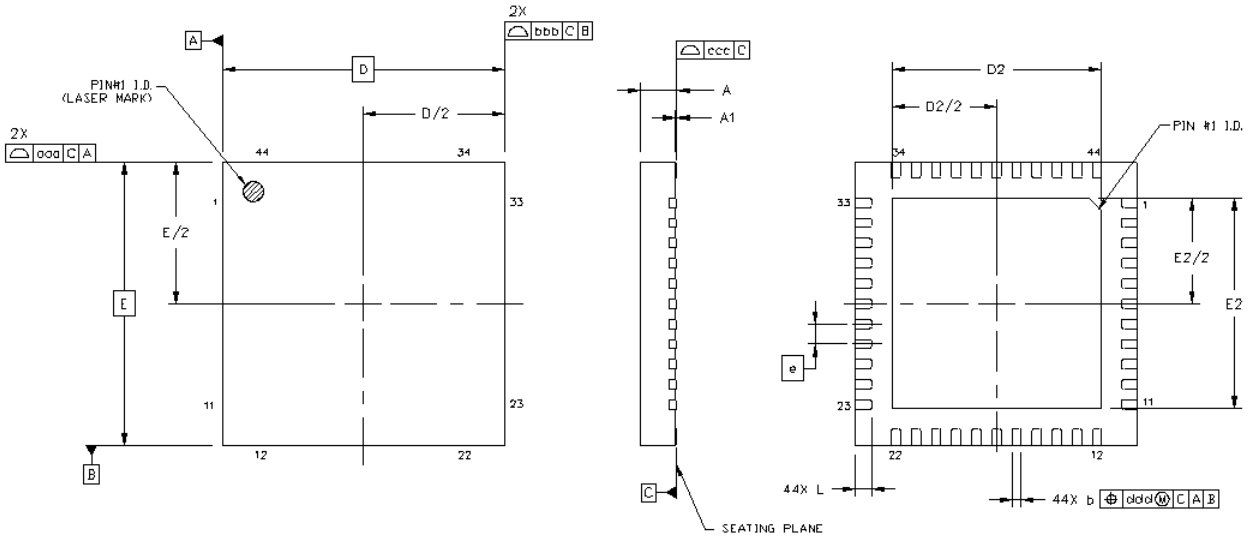


Figure 10.3. 44-Pin Quad Flat No-Lead (QFN)

Table 10.3. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.4 Si5394 and Si5392 J/K/L/M/E (Internal Reference) 7x7 mm 44-LGA Package Diagram

The following figure illustrates the package details for the Si5394J and Si5392J. The table lists the values for the dimensions shown in the illustration.

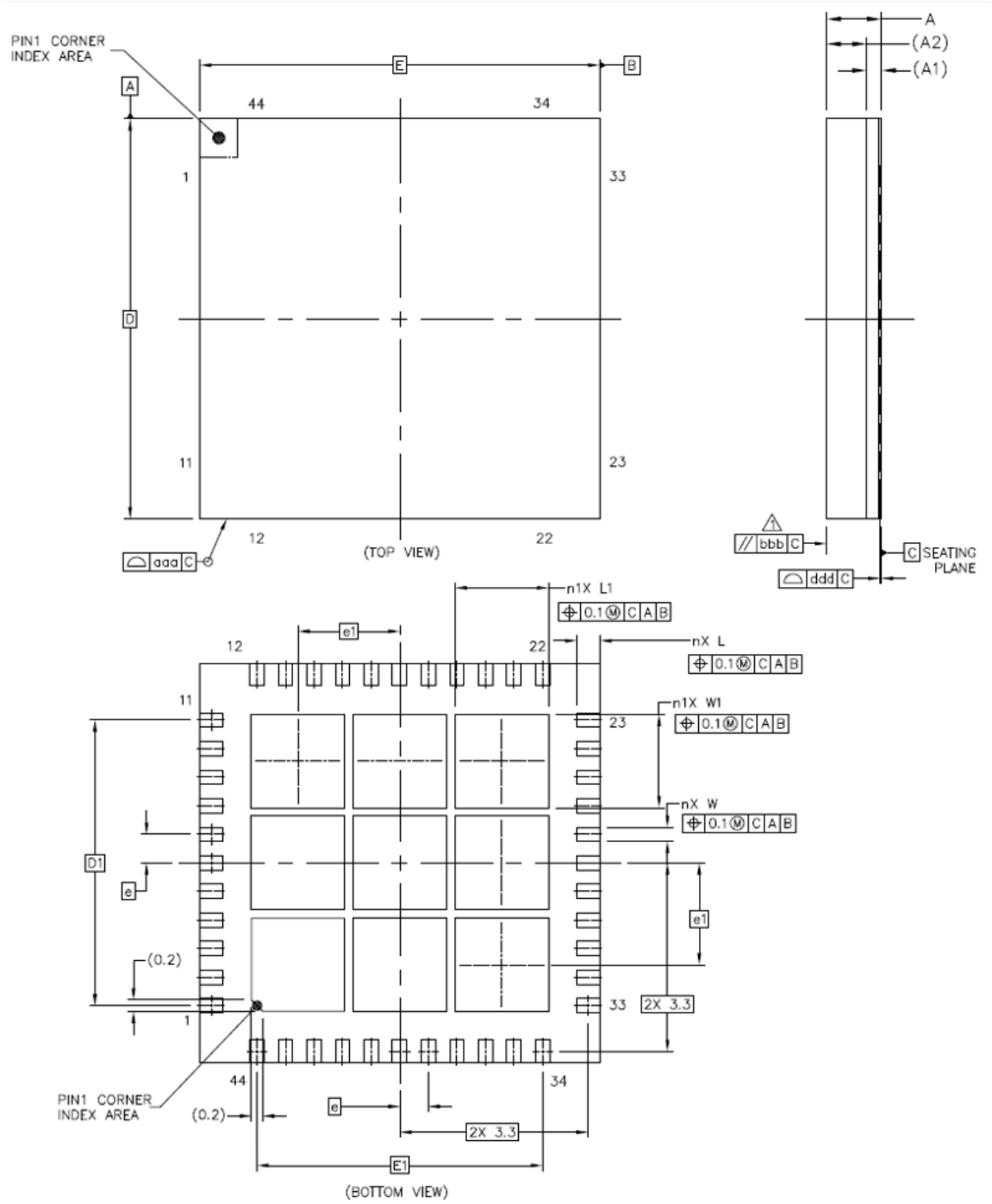


Figure 10.4. 44-Pin LGA

Table 10.4. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.1
A1		0.26 REF	
A2		0.7 REF	
D		7 BSC	
E		7 BSC	
W	0.2	0.25	0.3
L	0.35	0.4	0.45
e		0.5 BSC	
n		44	
D1		5 BSC	
E1		5 BSC	
W1	1.5833	1.6333	1.6833
L1	1.5833	1.6333	1.6833
e1		1.7833	
n1		9	
aaa		0.1	
bbb		0.2	
ddd		0.08	

Note:

1. The dimensions in parenthesis are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerance per ANSI Y14.5M-1994.

11. PCB Land Pattern

The following figure illustrates the PCB land pattern details for the devices. The table lists the values for the dimensions shown in the illustration.

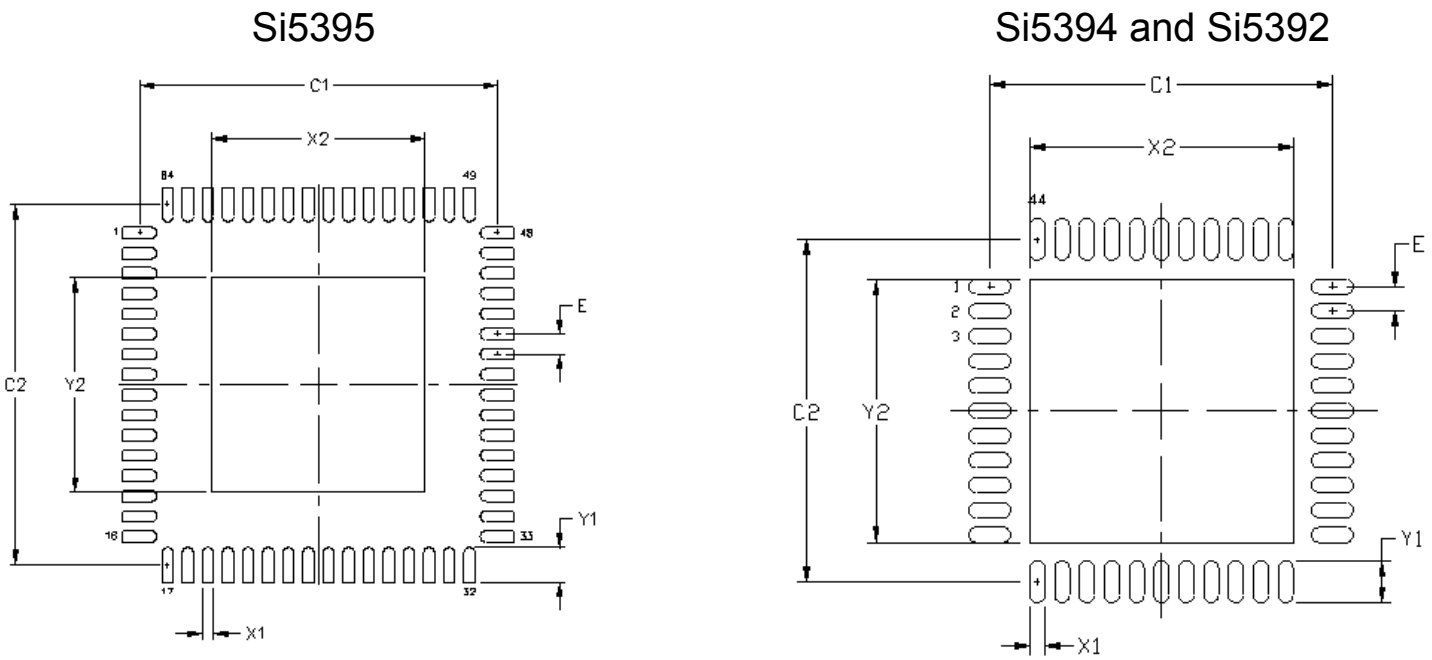


Figure 11.1. PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5395 (Max)	Si5394/92 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electropolished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. The stencil design will need to match the respective ground pads as shown in the Package outline. The stencil aperture to land pad size recommendation is 70% paste coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

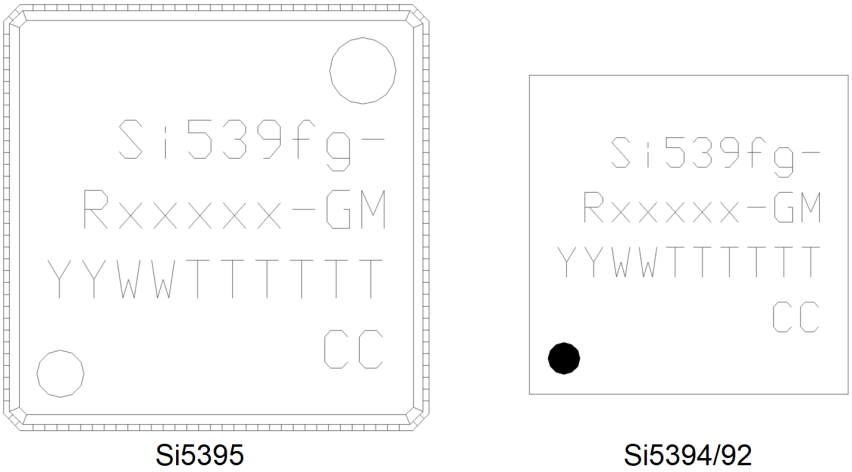


Figure 12.1. Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
1	Si539fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): f = 5: 12-output Si5395 f = 4: 4-output Si5394 f = 2: 2-output Si5392 g = Device Grade (A/B/C/D/P/J/K/L/M/E). See 3. Ordering Guide for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (Refer to 3. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See 3. Ordering Guide for more information. -GM = Package (QFN/LGA) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	CC	CC = TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Revision History

Revision 1.2

July, 2020

- The single center pad on the 7x7 mm 44-LGA Package is divided by soldermask into nine pads (3x3 grid array) to increase mechanical support to the center of the package; there is no change to the PCB layout made or to any of the metal layers of the package.
- Zero-delay mode is specified only for A/B/C/D and J/K/L/M.
- Updated Output Dynamic Delay Adjustment specification by combining fractional and integer specs into a single delay spec.

Revision 1.1

June, 2019

- Added Integrated reference options J/K/L/M/E.

Revision 1.0

April, 2019

- Updated Figure 4.3. Crystal Resonator and External Reference Clock Connection Options
- Updated section 4.9.2 Grade P section to support up to 3 time domains for Si5395, 2 domains for Si5394 and 1 domain for Si5392 (previous version only specified 2 domains for Si5395)
- Table 5.2 DC Characteristics
  - Core supply current IDD/IDDA limits clarified for each device
  - Output Buffer supply conditions clarified
  - Total power dissipation numbers updated
  - Updated test configuration diagrams
- Table 5.3 Input clock specifications
  - Updated Input voltage section of "LVCMOS / Pulsed CMOS DC-Coupled Input Buffer" to include standard CMOS
- Table 5.5 Differential Clock Output Specifications
  - Clarified duty cycle specs for when MultiSynth is used/not used
  - Increased max Rise and Fall times from 150ps to 200ps based on final characterization
- Table 5.6. LVCMOS Clock Output Specifications
  - Updated Min and Max limits for duty cycle
  - Updated test configuration diagrams
- Table 5.8. Performance Characteristics
  - Updated Initial startup time for P-grade devices
  - Updated P-grade jitter numbers to include more domains and finalize test conditions
- Updated Table 5.10. SPI Timing Specifications (4-Wire) table and timing diagram
- Updated Table 5.11. SPI Timing Specifications (3-Wire)
- Changed NC/XA, NC/XB, NC/X1, NC/X2 to XA, XB, X1, X2 respectively since integrated crystal devices are getting their own data sheet

Revision 0.96

June, 2018

- Preliminary data sheet.

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