THE DATASHEET OF

SI5344H-D-GM

Si5344H/42H Rev D

High-Frequency, Ultra-Low Jitter Attenuator Clock with Digitally-Controlled Oscillator

Features

- High-speed outputs generate an ultra-low jitter output up to 2.75 GHz
- Up to four Multi-Synth outputs generate any frequency up to 717.5 MHz
- Input frequency range:
  - 8 kHz to 750 MHz
- Maximum Output frequency:
  - High-Frequency Mode: 2.75 GHz
  - MultiSynth Mode: 717.5 MHz
- Jitter performance:
  High Frequency Mode:
  <50 fs typ (1 MHz–40 MHz)
  MultiSynth Mode:
  <150 fs typ (12 kHz–20 MHz)
- Programmable jitter attenuation bandwidth: 10 Hz to 4 kHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable voltage swing and common mode
  - LVPECL-only in High Frequency Mode
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Automatic free-run and holdover modes
- Glitchless on the fly output frequency changes
- Locks to gapped clock inputs
- DCO mode: as low as 0.001 ppb steps.
- Core voltage
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output supply pins: 3.3 V, 2.5 V, or 1.8 V
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro™ software simplifies device configuration
- Si5342H: 2 input, 2 output, QFN44
- Si5344H, 2 input, 4 output, QFN44
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

Applications

- 100G/200G/400G Optical Transceivers
- Wireless base-stations

Description

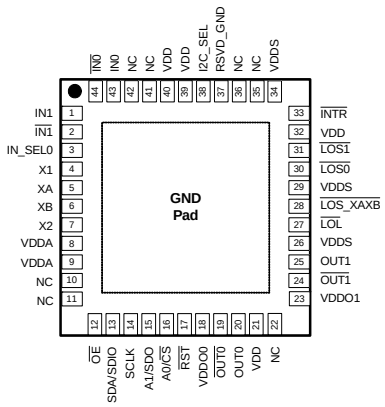
This specialized jitter attenuating clock multiplier combines fourth-generation DSPLL with ultra-low phase jitter and MultiSynth™ technologies to enable high data rate coherent optical transceiver design. Up to four outputs can be assigned to High Frequency Mode capable of up to 2.75 GHz at 50 fs-rms typical phase jitter (1 MHz-40 MHz). Each output may also be configured as MultiSynth Mode any-frequency outputs when added frequency flexibility is required, such as clocking Forward Error Correction (FEC) while still delivering <150 fs-rms typical phase jitter (12 kHz-20 MHz). The Si5344H and Si5342H also feature DCO-control with as low as 0.001 ppb step control and locks to gapped clock inputs.

These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) so that they always power up with a known frequency configuration. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Programming the Si5342H/44H is made easy with Skyworks Solutions' ClockBuilder Pro software. Factory preprogrammed devices are also available.

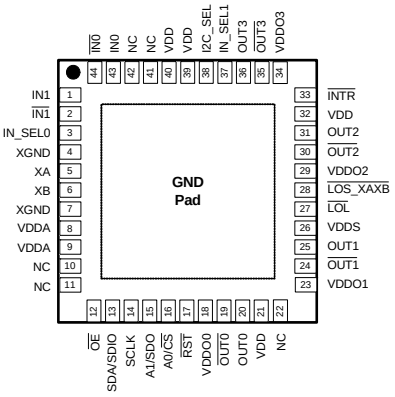
Ordering Information:
See Section 7.

Pin Assignments

Si5342H 44QFN
Top View



Si5344H 44QFN
Top View



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1. Typical Application Schematic

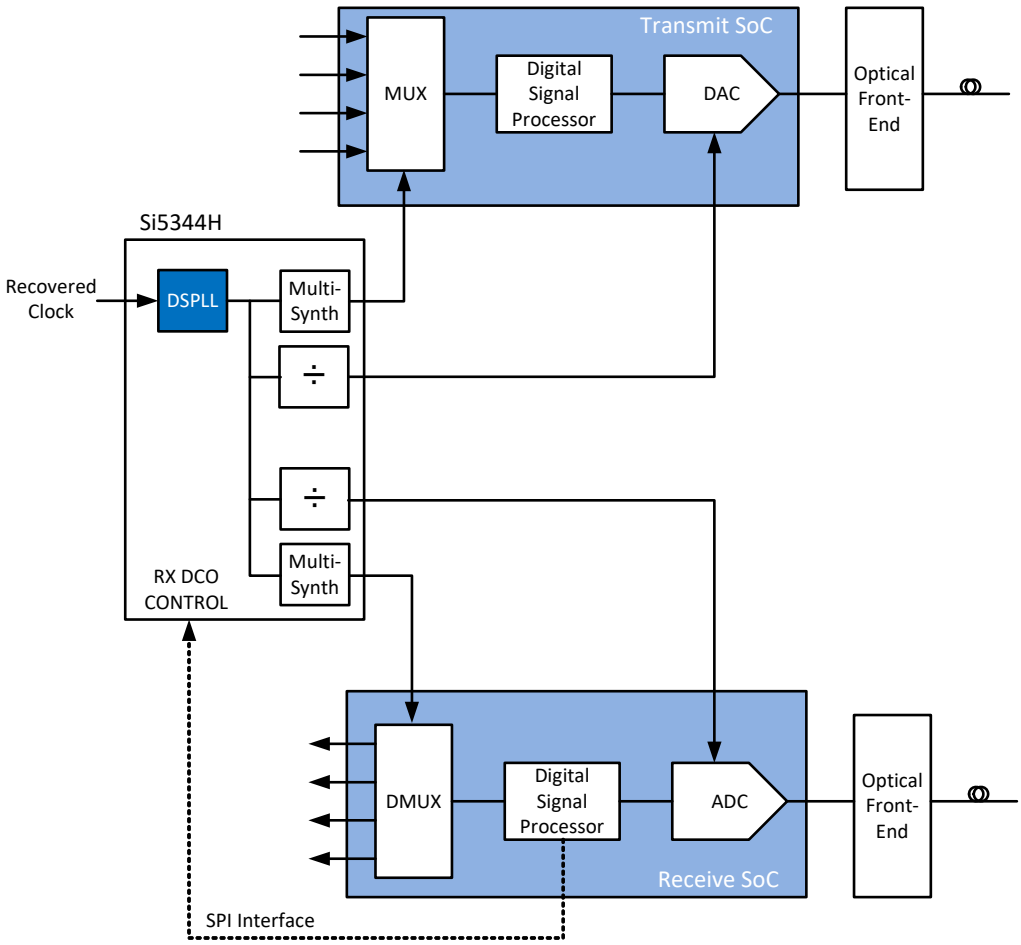


Figure 1. 100G/400G Coherent Optical Transceiver Application Example

2. Electrical Specifications

Table 1. Recommended Operating Conditions*

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

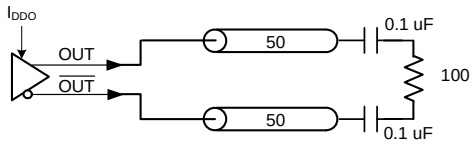
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Si5342H Si5344H		—	145	190	mA
	I_{DDA}			—	120	125	mA
Output Buffer Supply Current	I_{DDOx}	High-Frequency Output Mode (AC-coupled) @2.75GHz		—	45	51	mA
		LVPECL Output @ 156.25 MHz		—	22	26	mA
		LVDS Output @ 156.25 MHz		—	15	18	mA
		3.3 V LVCMOS output @ 156.25 MHz		—	22	30	mA
		2.5 V LVCMOS output @ 156.25 MHz		—	18	23	mA
		1.8 V LVCMOS output @ 156.25 MHz		—	12	16	mA
Total Power Dissipation	P_d	Si5344H	Notes 1, 5	—	900	1000	mW
		Si5342H	Notes 2, 5	—	800	900	mW

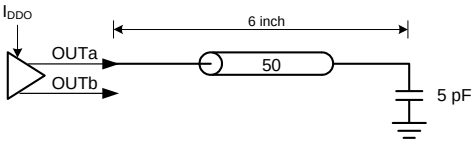
Notes:

1. Si5344H test configuration: 2 x 2.5 V LVDS outputs @ 156.25 MHz, 2 x 2.5 V Differential High-Speed Output Mode (ac-coupled) @ 2.104658 GHz. Excludes power in termination resistors.
2. Si5342H test configuration: 1 x 2.5 V LVDS output @ 156.25 MHz, 1 x 2.5 V Differential High-Speed Output Mode (ac-coupled) @ 2.104658 GHz. Excludes power in termination resistors.
3. Differential outputs terminated into an ac-coupled 100 Ω load.
4. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load. Measurements were made in CMOS3 mode.

Differential Output Test Configuration



LVCMOS Output Test Configuration



5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

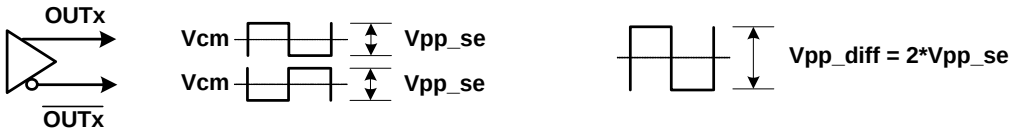
Table 3. Input Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended - AC Coupled (IN0/$\overline{IN0}$, IN1/$\overline{IN1}$)						
Input Frequency Range	f_{IN_DIFF}	Differential	0.008	—	750	MHz
		Single-ended/LVCMOS	0.008	—	250	MHz
Voltage Swing[1]	V_{IN}	Differential AC Coupled f_{in} < 250 MHz	100	—	1800	mVpp_se
		Differential AC Coupled 250 MHz < f_{in} < 750 MHz	225	—	1800	mVpp_se
		Single-Ended AC Coupled[5] f_{in} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	0.3	—	pF
Pulsed CMOS - DC Coupled (IN0, IN1)						
Input Frequency	$f_{IN\_PULSED\_CMOS}$[4]		0.008	—	250	MHz
Input Voltage[4]	V_{IL}		–0.2	—	0.4	V
	V_{IH}		0.8	—	—	V
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (applied to XA/XB)						

Notes:

1. Voltage swing is specified as single-ended mVpp.



2. Imposed for jitter performance.

3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN\_Vpp\_se}) / SR$

4. This mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz that must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low-frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.4 V and 0.8 V, respectively) refer to the input attenuator circuit for dc-coupled pulsed LVCMOS in the Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard Differential or Single-Ended ac-coupled input mode.

5. Refer to the Family Reference Manual if you're using a single-ended AC coupled inputs with voltage swing exceeding 3.4 V.

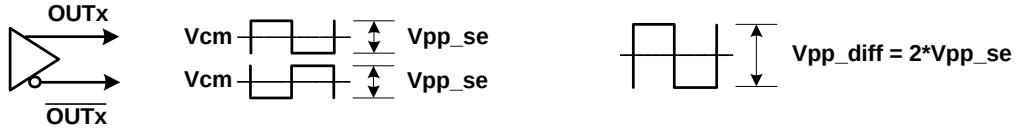
Table 3. Input Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFCLK Frequency	f_{IN_REF}	Frequency range for best output jitter performance	48	—	54	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
Input Differential Voltage Swing	V_{IN_DIFF}		365		2500	mVpp_diff
Slew rate[2, 3]	SR		400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Notes:

1. Voltage swing is specified as single-ended mVpp.



2. Imposed for jitter performance.
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN\_Vpp\_se}) / SR$
4. This mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz that must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low-frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.4 V and 0.8 V, respectively) refer to the input attenuator circuit for dc-coupled pulsed LVCMOS in the Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard Differential or Single-Ended ac-coupled input mode.
5. Refer to the Family Reference Manual if you're using a single-ended AC coupled inputs with voltage swing exceeding 3.4 V.

Table 4. Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Control Input Pins (I2C_SEL, IN_SEL, $\overline{RST}$, $\overline{OE}$, A1, SCLK, A0/$\overline{CS}$, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}*	V
	V_{IH}		0.7 x V_{DDIO}*	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	$\overline{RST}$	100	—	—	ns

***Note:** V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Family Reference Manual or contact Skyworks Solutions for more details on the proper register settings.

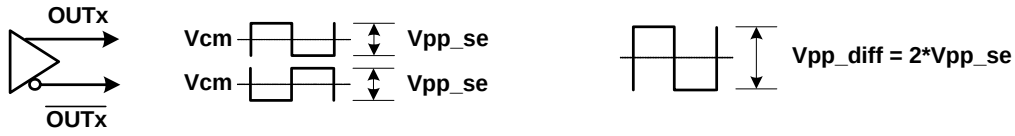
Table 5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency: High-Speed Output	f_{OUT}	MultiSynth not used	0.615	—	1.195833	GHz
		Only AC-coupled 3.3V differential high-speed output is supported for f_{OUT} >1.5 GHz	1.23	—	2.39166	
			2.46	—	2.75	
Output Frequency: MultiSynth Output[2]	f_{OUT}	MultiSynth used for any-frequency support (all output formats)	0.0001	—	717.5	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz	48	—	52	%
		400 MHz < f_{OUT} < 1.37 GHz	45	—	55	
		1.37 GHz <f_{OUT} <2.75 GHz	25	—	75	
Output-Output Skew Using Same MultiSynth	T_{SKS}	Outputs on same MultiSynth (Measured at 717.5 MHz)	—	—	65	ps
Output-Output Skew between MultiSynths	T_{SKD}	Outputs from different MultiSynths (Measured at 717.5 MHz)	—	—	90	ps
OUT-$\overline{OUT}$ Skew	T_{SK_OUT}	Measured from the positive to negative output pins	—	0	50	ps

Note:

1. For normal mode, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. When in LVPECL mode and f_{OUT}>717.5 MHz note V_{OUT} may not meet standard LVPECL levels, but provides the greatest output voltage swing. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.
2. Max frequency using MultiSynth outputs is determined by the VCO frequency. Please use ClockBuilder Pro to determine the maximum output frequency for any given frequency plan.
3. High-speed outputs indicates no multiSynth is used (i.e., not fractional synthesis).



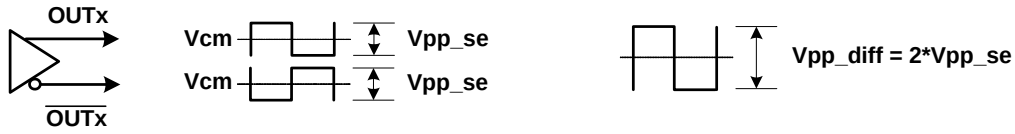
4. Not all combinations of voltage swing and common mode voltages settings are possible. See the reference manual for details.
5. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
6. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 5. Differential Clock Output Specifications (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Swing[1]	**F_{out}>1.5 GHz**						
	V_{OUT}	Differential High-Speed Output Mode (AC-Coupled)		380	650 @ 1.7 GHz 600 @ 2.1 GHz 580 @ 2.5 GHz 500@ 2.75 GHz	800	mVpp_se
	F_{out}<1.5 GHz						
	V_{OUT}	LVDS		400	450	500	mVpp_se
		LVPECL[1] 0.001 MHz <F_{out}<717.5 MHz		640	750	900	
		LVPECL 717.5 MHz < F_{out} < 1500 MHz		680	750	830	
Common Mode Voltage[1,4] (100 Ω load line-to-line)	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.20	1.30	V
			LVPECL	1.90	2.00	2.10	V
		V_{DDO} = 2.5 V	LVPECL LVDS	1.10	1.20	1.30	V
		V_{DDO} = 1.8 V	Sub-LVDS	0.80	0.90	1.0	V
Rise and Fall Times (20% to 80%)	t_R/t_F	Differential High-Speed Output Mode (AC-Coupled) F_{out}>1.5 GHz		—	70	110	ps
		Normal Mode F_{out}<1.5 GHz		—	90	120	

Note:

1. For normal mode, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. When in LVPECL mode and f_{OUT}>717.5 MHz note V_{OUT} may not meet standard LVPECL levels, but provides the greatest output voltage swing. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.
2. Max frequency using MultiSynth outputs is determined by the VCO frequency. Please use ClockBuilder Pro to determine the maximum output frequency for any given frequency plan.
3. High-speed outputs indicates no multiSynth is used (i.e., not fractional synthesis).



4. Not all combinations of voltage swing and common mode voltages settings are possible. See the reference manual for details.
5. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
6. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

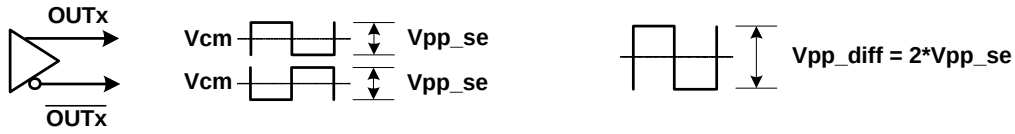
Table 5. Differential Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Output Impedance[4]	Z_O		—	100	—	Ω
Power Supply Noise Rejection[5]	PSRR	10 kHz sinusoidal noise	—	–101	—	dBc
		100 kHz sinusoidal noise	—	–96	—	
		500 kHz sinusoidal noise	—	–99	—	
		1 MHz sinusoidal noise	—	–97	—	
Output-output Cross-talk	XTALK	Measured spur from adjacent output[6]	—	–88	—	dBc

Note:

1. For normal mode, the amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The typical LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. When in LVPECL mode and f_{OUT}>717.5 MHz note V_{OUT} may not meet standard LVPECL levels, but provides the greatest output voltage swing. Also note that the output voltage swing specifications are given in peak-to-peak single-ended swing.
2. Max frequency using MultiSynth outputs is determined by the VCO frequency. Please use ClockBuilder Pro to determine the maximum output frequency for any given frequency plan.
3. High-speed outputs indicates no multiSynth is used (i.e., not fractional synthesis).



4. Not all combinations of voltage swing and common mode voltages settings are possible. See the reference manual for details.
5. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
6. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 6. LVCMOS Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		45	—	55	
Output-to-Output Skew	T_{SK}	Measured across outputs on same MultiSynth running at 156.25 MHz		—	30	140	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV = 3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV = 3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –5 mA		—	—	

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Family Reference Manual or contact Skyworks Solutions for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

AC Test Configuration

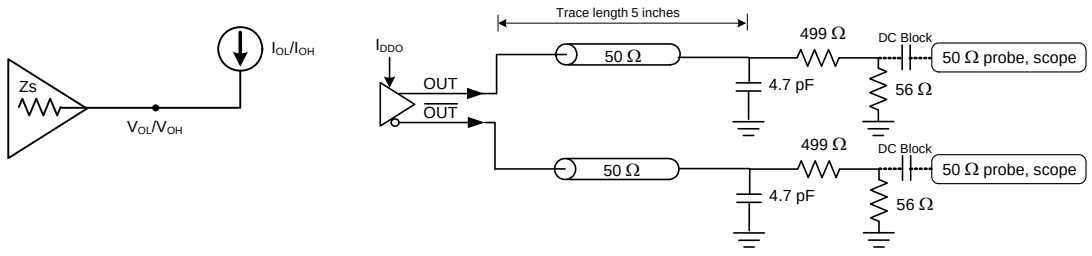


Table 6. LVCMOS Clock Output Specifications (Continued)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	f_{OUT} = 156.25 MHz CMOS_DRV = 3	VDDO = 3.3 V	—	400	600	ps
			VDDO = 2.5 V	—	450	600	ps
			VDDO = 1.8 V	—	550	750	ps

Notes:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Family Reference Manual or contact Skyworks Solutions for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

AC Test Configuration

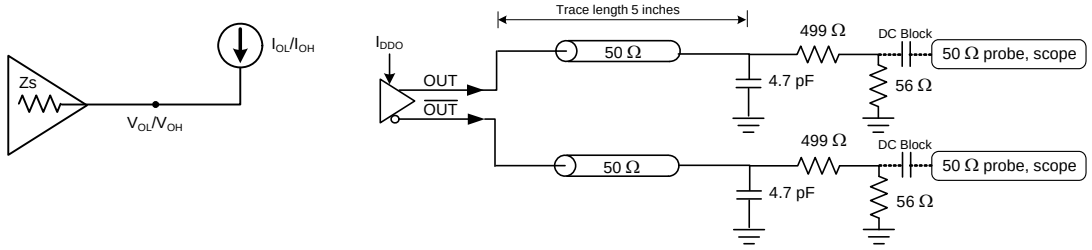


Table 7. Output Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5344H Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{INTR}}$, $\overline{\text{LOS\_XAXB}}$, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}* x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5342H Status Output Pins ($\overline{\text{LOL}}$, $\overline{\text{LOS0}}$, $\overline{\text{LOS1}}$, $\overline{\text{LOS\_XAXB}}$, $\overline{\text{INTR}}$, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. Note that the V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. VOL remains valid in all cases.
2. VDDIO is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Family Reference Manual for more details on the proper register settings.

Table 8. Performance Characteristics
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time[2]	t_{ACQ}	f_{IN} = 19.44 MHz	—	280	300	ms
Output Delay Adjustment	t_{DELAY_frac}	f_{VCO} = 14 GHz	—	0.28	—	ps
	t_{DELAY_int}		—	71.4	—	ps
	t_{RANGE}		—	±9.14	—	ns
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a Loop Bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1 and 2 Carrier Frequency = 2.103125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Only valid for a single automatic switch between two input clocks running at the same frequency	—	—	2.0	ns
		Only valid for a single manual switch between two input clocks running at the same frequency			1.3	
Pull-in Range	ω_P		—	500	—	ppm
Input-to-Output Delay Variation	$t_{IODELAY}$	Measured between a common 2 MHz input and 2 MHz output with different MultiSynths on the same part. DSPLL bandwidth = 4 kHz.	—	—	1.8	ns
		Measured between a common 2 MHz input and 2 MHz output with different MultiSynths between different parts. DSPLL bandwidth = 4 kHz.	—	—	2.0	ns

Table 8. Performance Characteristics (Continued)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RMS Phase Jitter[4]	J_{GEN}	Integer High-Speed Mode 1 MHz to 40 MHz	—	0.050	—	ps RMS
		Integer High-Speed Mode 12 kHz to 20 MHz	—	0.085	0.140	ps RMS
		Fractional MultiSynth Mode 12 kHz to 20 MHz	—	0.120	0.160	ps RMS

Notes:
1. Actual loop bandwidth might be lower; please refer to CBPro for actual value for your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths set to 100 Hz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Jitter generation test conditions:
   Integer High-Speed Mode: f_{IN} = 19.44 MHz, f_{OUT} = 2.104658 GHz diff. high-speed output, loop bandwidth = 100 Hz.
   Fractional MultiSynth (normal) Mode: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz.

Table 9. I²C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
			Standard Mode 100 kbps		Fast Mode 400 kbps		
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

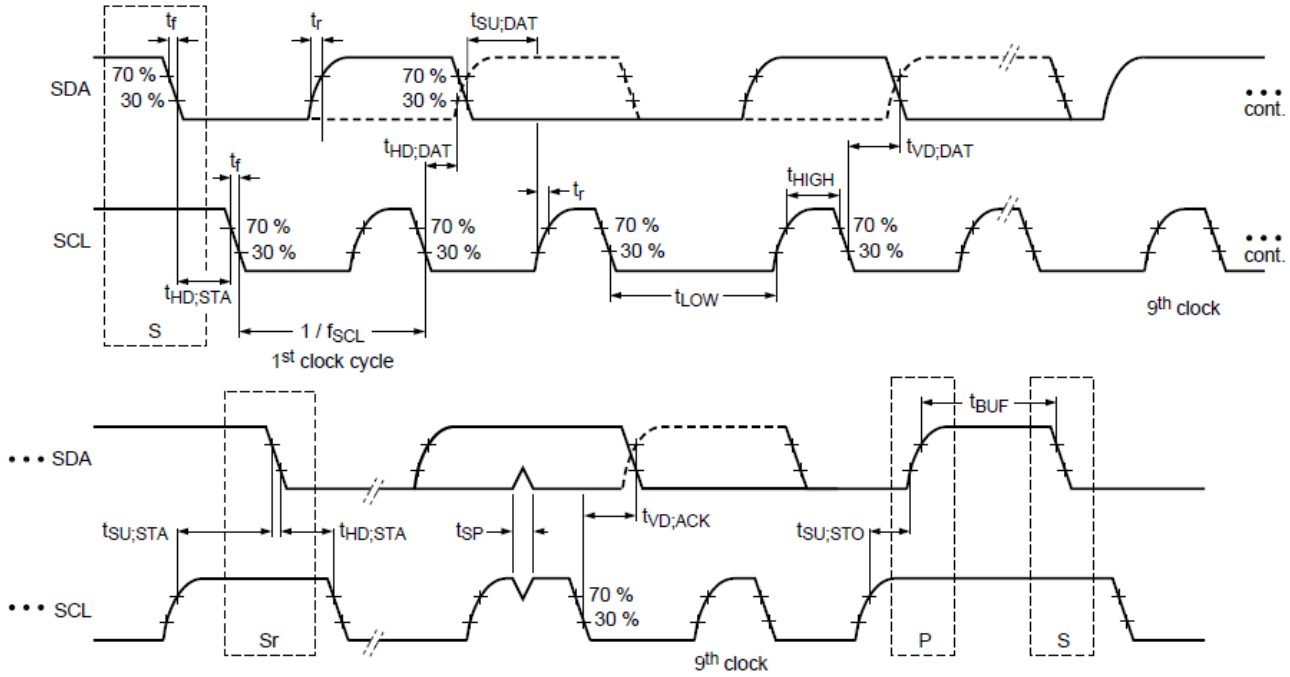


Figure 2. I²C Serial Port Timing Standard and Fast Modes

Table 10. SPI Timing Specifications (4-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to $\overline{CS}$	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

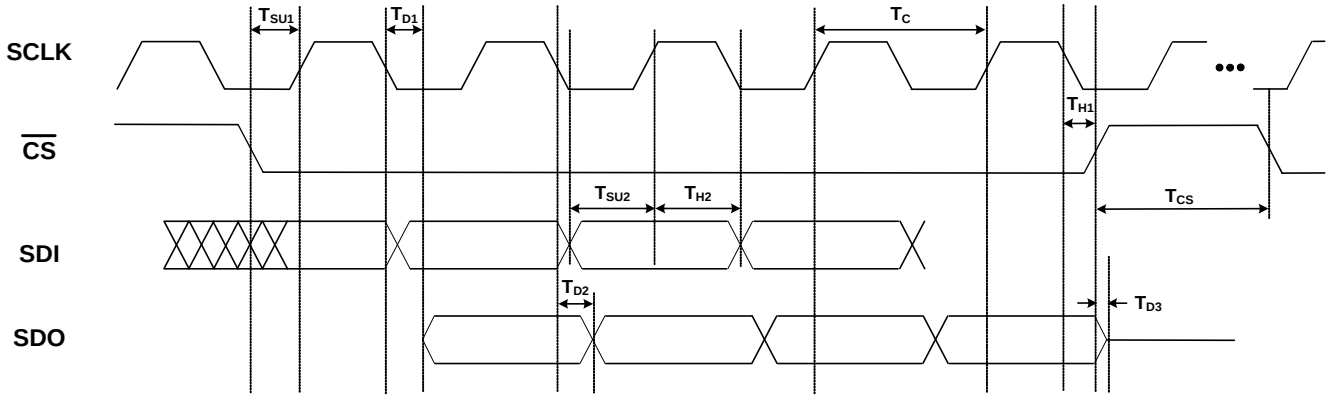


Figure 3. 4-Wire SPI Serial Interface Timing

Table 11. SPI Timing Specifications (3-Wire)
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, $\overline{CS}$ Rise to SDIO Tri-State	T_{D3}	—	10	15	ns
Setup Time, $\overline{CS}$ to SCLK	T_{SU1}	5	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Fall	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects ($\overline{CS}$)	T_{CS}	2	—	—	T_C

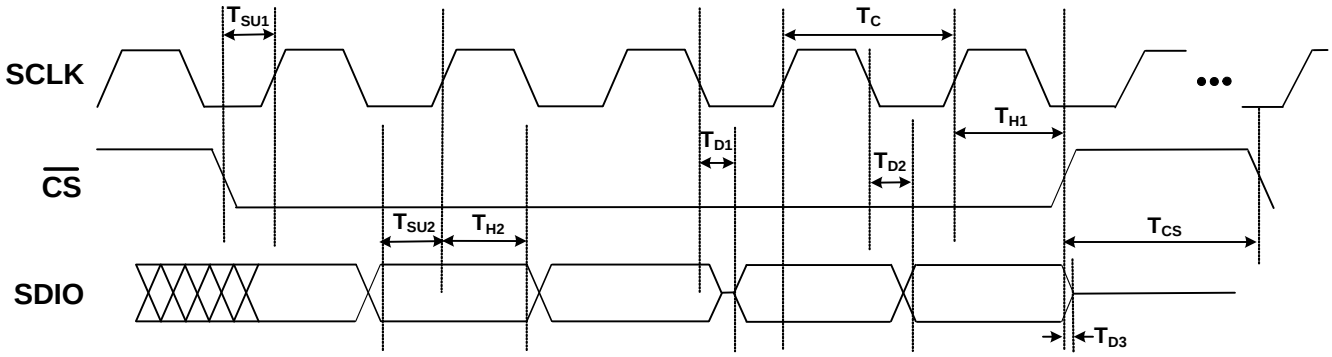


Figure 4. 3-Wire SPI Serial Interface Timing

Table 12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	$f_{XTAL\_48\text{-}54}$	Frequency range for best jitter performance	48	—	54	MHz
Load Capacitance	$C_{L\_48\text{-}54}$		—	8	—	pF
Crystal Drive Level	$d_{L\_48\text{-}54}$		—	—	200	µW
Equivalent Series Resistance Shunt Capacitance	$r_{ESR\_48\text{-}54}$ $C_{O\_48\text{-}54}$	Refer to the Family Reference Manual to determine ESR and shunt capacitance.				

Notes:
1. The Si5344H/42H is designed to work with crystals that meet the specifications in Table 12.
2. Refer to the Family Reference Manual or contact Skyworks Solutions for the recommended 48 to 54 MHz crystals.

Table 13. Thermal Characteristics

Parameter	Symbol	Test Condition*	Value	Units
Si5344H, Si5342H (44-pin QFN)				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

***Note:** Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.

Table 14. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}	IN0, IN1	–0.85 to 3.8	V
	V_{I2}	IN_SEL, $\overline{RST}$, $\overline{OE}$, I2C_SEL, SDI, SCLK, A0/$\overline{CS}$, A1, SDA/SDIO	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Maximum Junction Temperature During Operation	T_{JCT}		–55 to 125	°C
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20–40	s

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For more packaging information, including MSL rating, go to https://www.skyworksinc.com/support-ia.
4. The device is compliant with JEDEC J-STD-020.

3. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V, V_{DDA} = 3.3 V, V_{DDS} = 3.3 V, 1.8 V, and T_A = 25 °C.

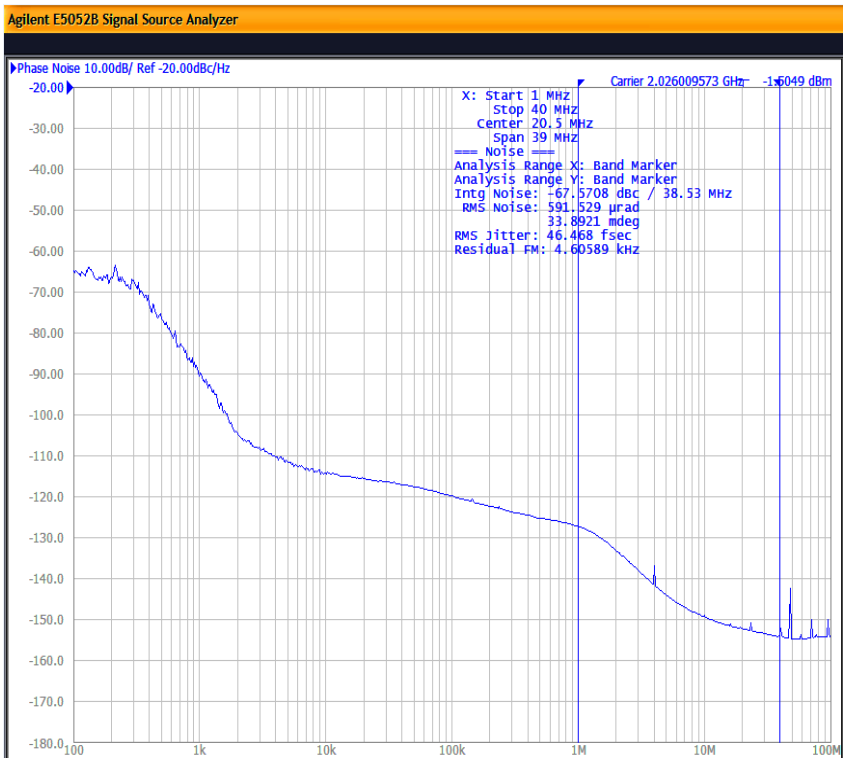


Figure 5. Input = 19.44 MHz; Output = 2.026 GHz, 3.3 V LVPECL

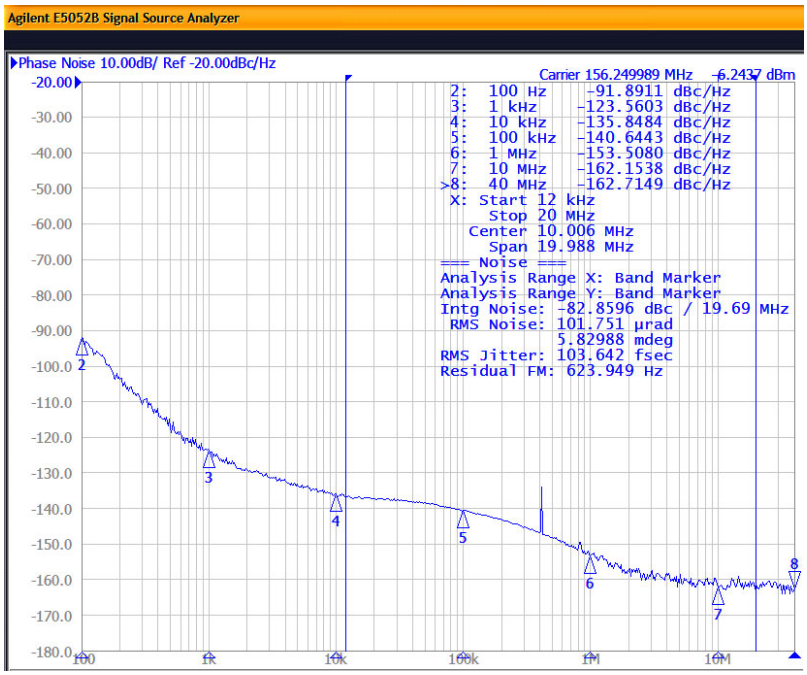


Figure 6. Input = 25 MHz; Output = 156.25 MHz, 3.3 V LVPECL

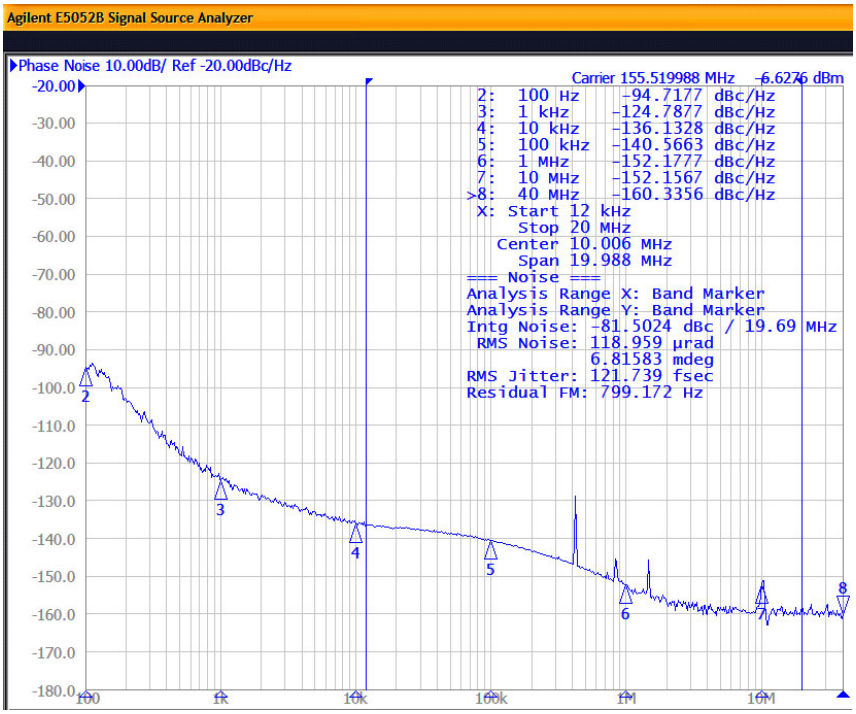


Figure 7. Input = 25 MHz; Output = 155.52 MHz, 3.3 V LVPECL

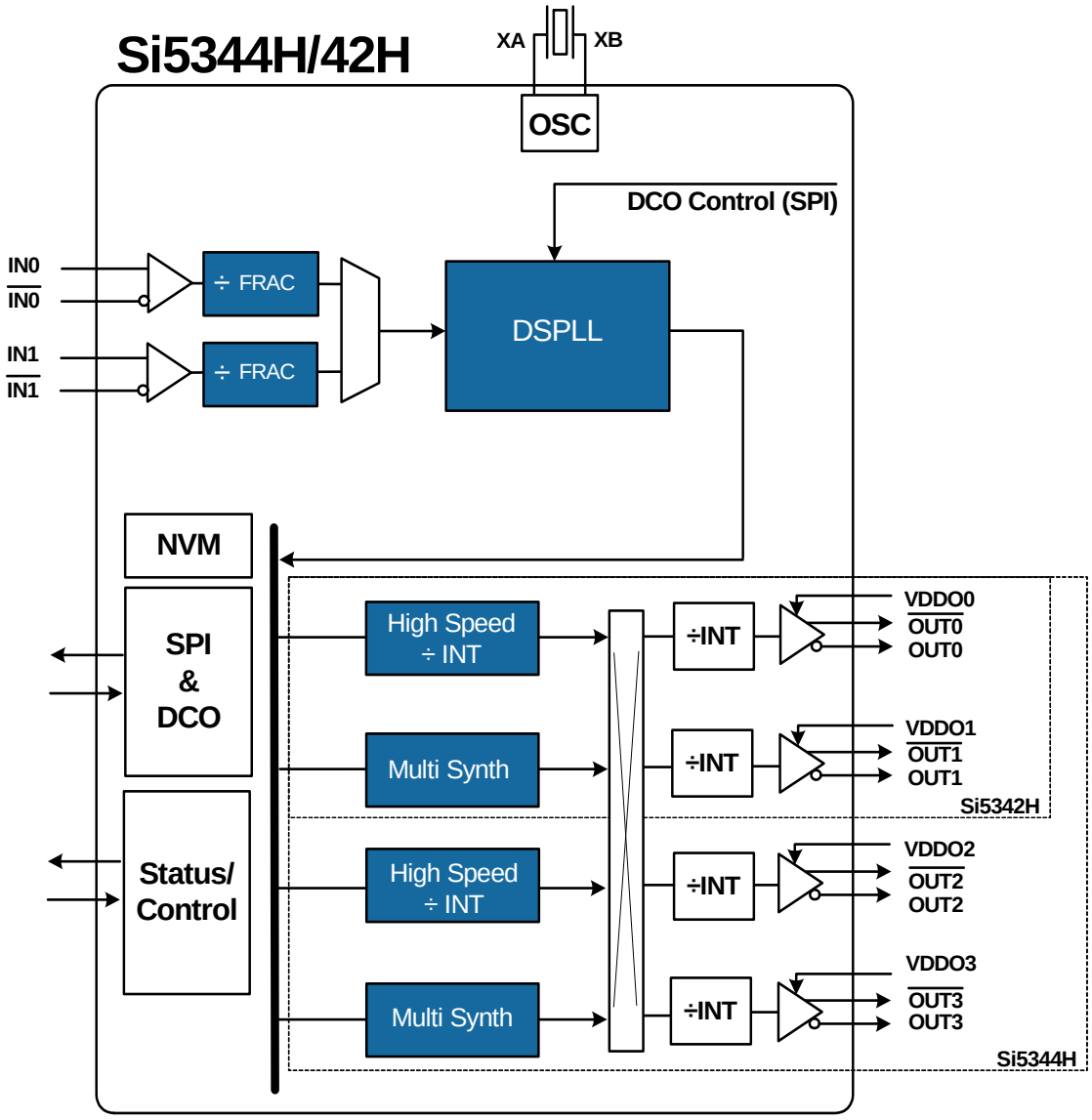


Figure 8. Si5344H/42H Block Diagram

4. Functional Description

The Si5344H/42H's internal DSPLL provides jitter attenuation and any-frequency multiplication of the selected input frequency. Fractional input dividers (P) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. The high-performance MultiSynth dividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency.

4.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

4.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

4.2.1. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

4.3. Modes of Operation

Once initialization is complete the DSPLL operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 9. The following sections describe each of these modes in greater detail.

4.3.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the $\overline{\text{RST}}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

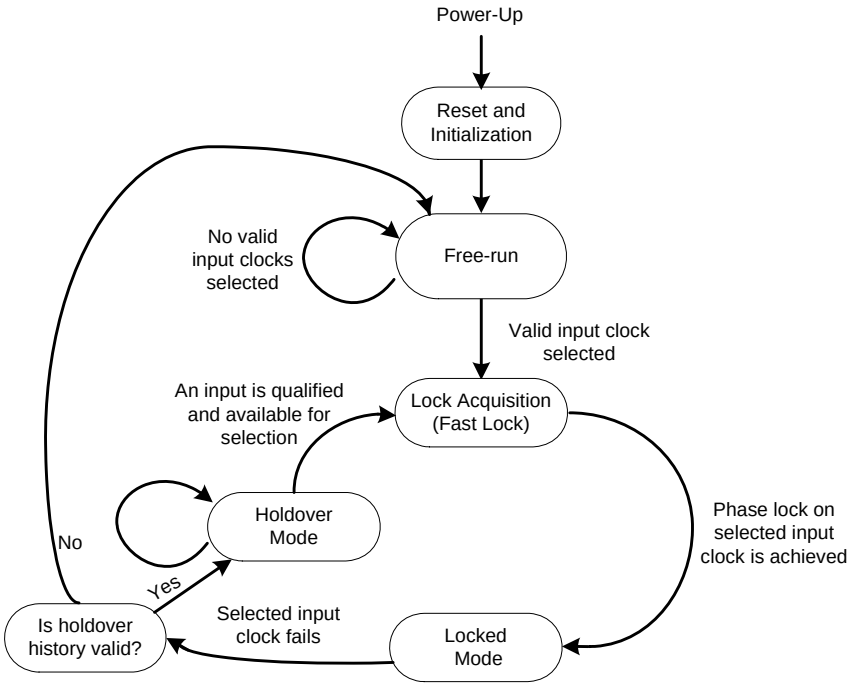


Figure 9. Modes of Operation

4.3.2. Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

4.3.3. Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.3.4. Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. A loss of lock pin ($\overline{\text{LOL}}$) and status bit indicate when lock is achieved. See section 4.7.4 for more details on the operation of the loss of lock circuit.

4.3.5. Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in Figure 10. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

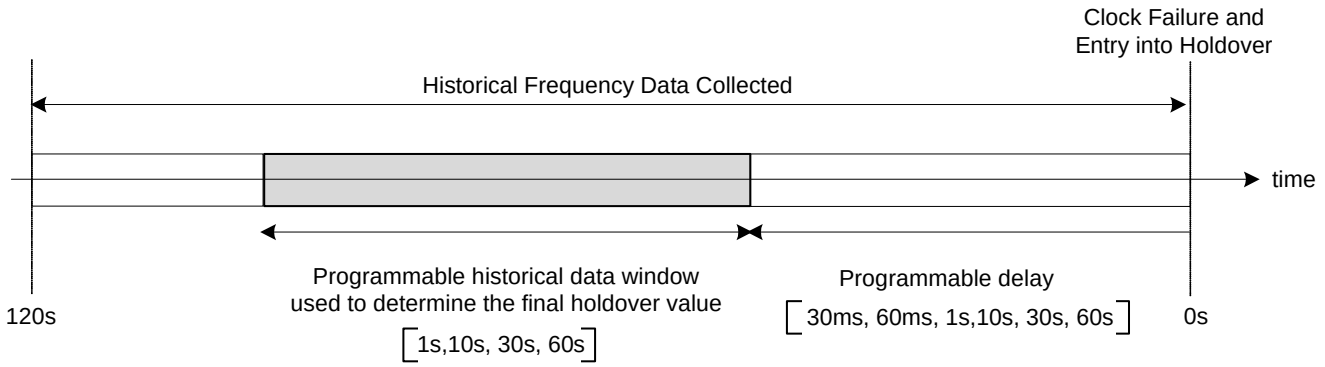


Figure 10. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

4.4. External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 11. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 12 for crystal specifications. A crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. Frequency offsets due to C_L mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

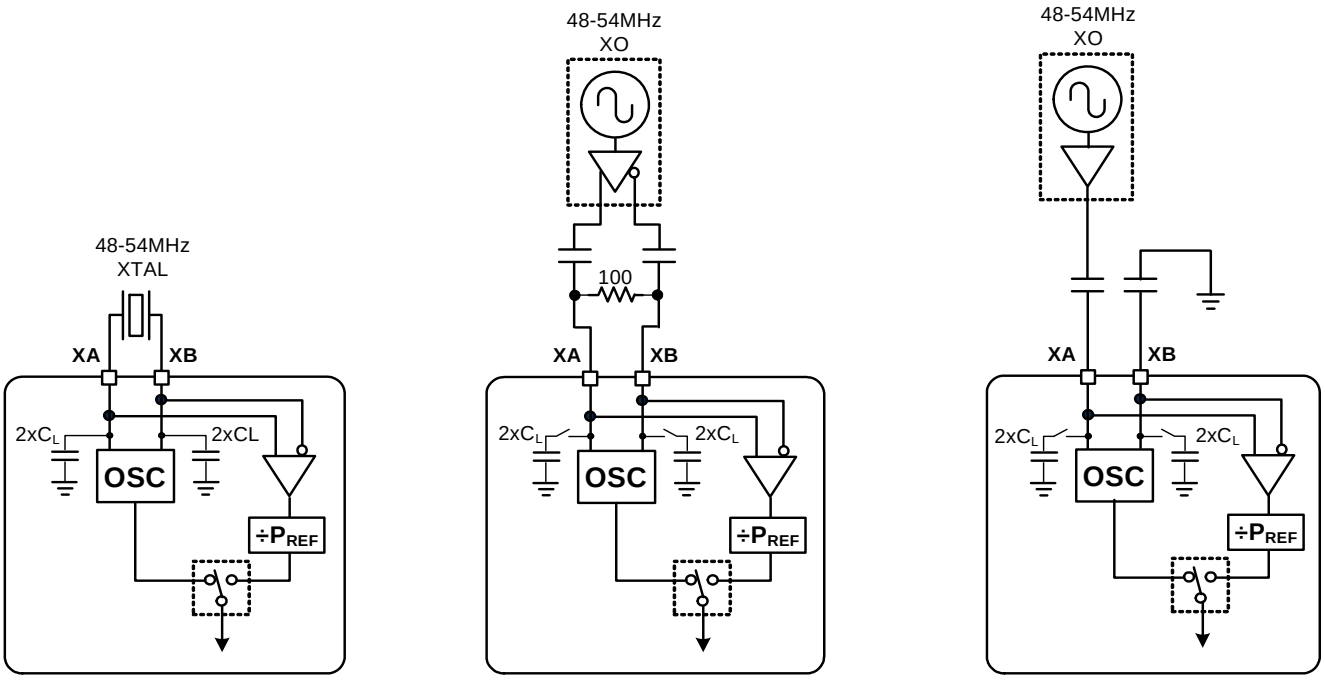
The device can also accommodate an external reference clock (REFCLK) instead of a crystal. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (C_L) are disabled in this mode. Refer to Table 3 for REFCLK requirements when using this mode. A P_{REF} divider is available to accommodate external clock frequencies higher than 54 MHz. Frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

4.5. Digitally Controlled Oscillator (DCO) Mode

The Si5344H/Si5342H supports DCO mode. In DCO mode, all outputs are controlled simultaneously. The DCO mode can be set up using the ClockBuilder Pro setup wizard.

Alternatively, DCO mode can be setup using the steps described in Si5344H/42H Family Reference Manual. DCO update rate is primarily limited by the SPI bus speed. Given a sufficient SPI bus rate, DCO update rate of 200 kHz or higher can be achieved.

In jitter attenuation mode, the device operates in dual-loop mode—the inner loop referenced to a crystal or XO tied to XA/XB pins and outer loop referenced to INx. In DCO mode, there is no INx input, and so the outer loop is disabled. The PLL inner loop feedback divider (MXAXB) can be externally controlled to produce the desired instantaneous output frequency. Fixing the MXAXB denominator and modulating only the numerator produces a linear frequency change across the full DCO range.



Crystal Resonator Connection

Differential XO Connection

Single-ended XO Connection

Figure 11. Crystal Resonator and External Reference Clock Connection Options

4.6. Inputs (IN0, IN1)

There are two inputs that can be used to synchronize the DSPLL. The inputs accept both differential and single-ended clocks. Input selection can be manual (pin or register controlled) or automatic with user definable priorities.

4.6.1. Manual Input Switching (IN0, IN1)

Input clock selection can be made manually using the IN_SEL pin or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pin are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode.

Table 15. Manual Input Selection Using IN_SEL Pin

IN_SEL	Selected Input
0	IN0
1	IN1

4.6.2. Automatic Input Selection (IN0, IN1)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

4.6.3. Hitless Input Switching

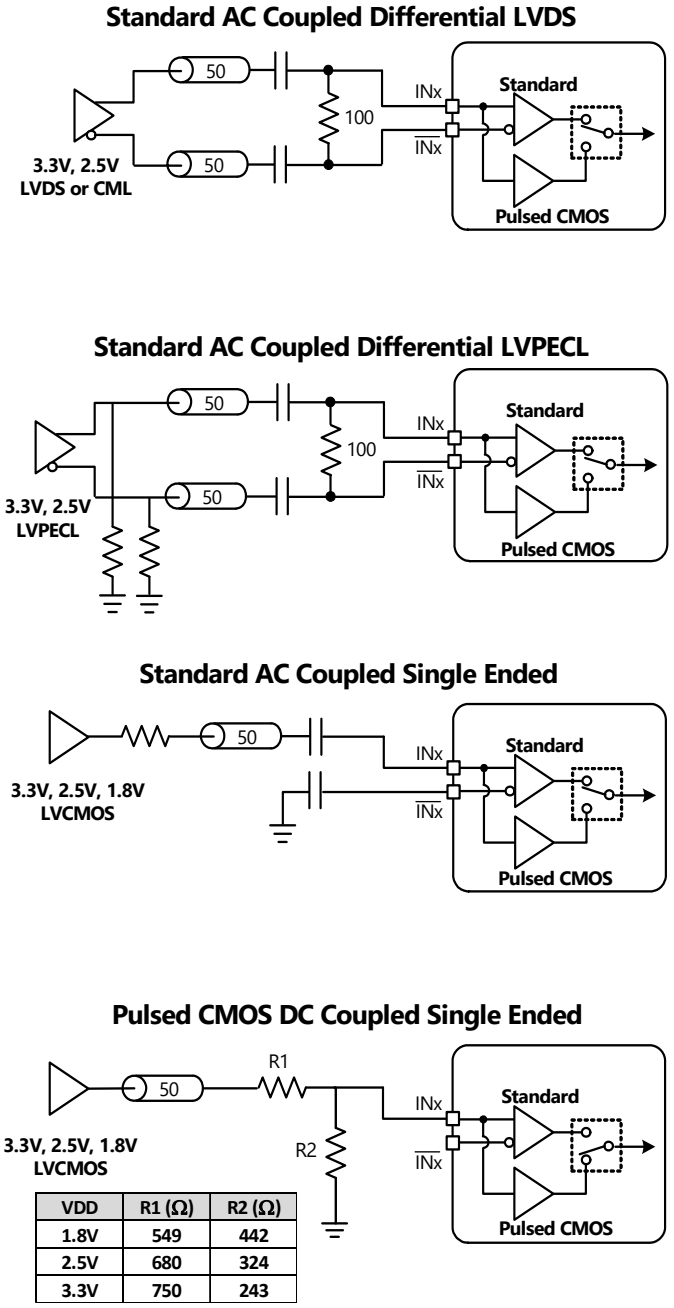
Hitless switching is a feature that prevents a phase transient from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz.

4.6.4. Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition.

4.6.5. Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in Figure 12. Differential signals must be ac-coupled, while single-ended LVCMOS signals can be ac or dc-coupled. Unused inputs can be disabled and left unconnected when not in use.



VDD	R1 (Ω)	R2 (Ω)
1.8V	549	442
2.5V	680	324
3.3V	750	243

Figure 12. Termination of Differential and LVCMOS Input Signals

4.6.6. Synchronizing to Gapped Input Clocks

The DSPLL supports locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in Figure 13. For more information on gapped clocks, see “AN561: Introduction to Gapped Clocks and PLLs”.

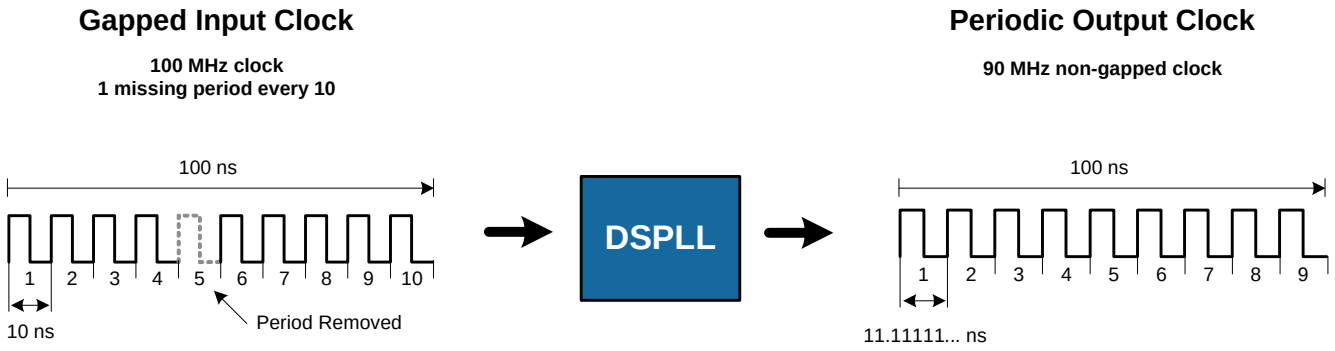


Figure 13. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every 8. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 8 when the switch occurs during a gap in either input clock.

4.7. Fault Monitoring

The input clocks (IN0, IN1) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in Figure 14. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss Of Lock (LOL) indicator which is asserted when the DSPLL loses synchronization.

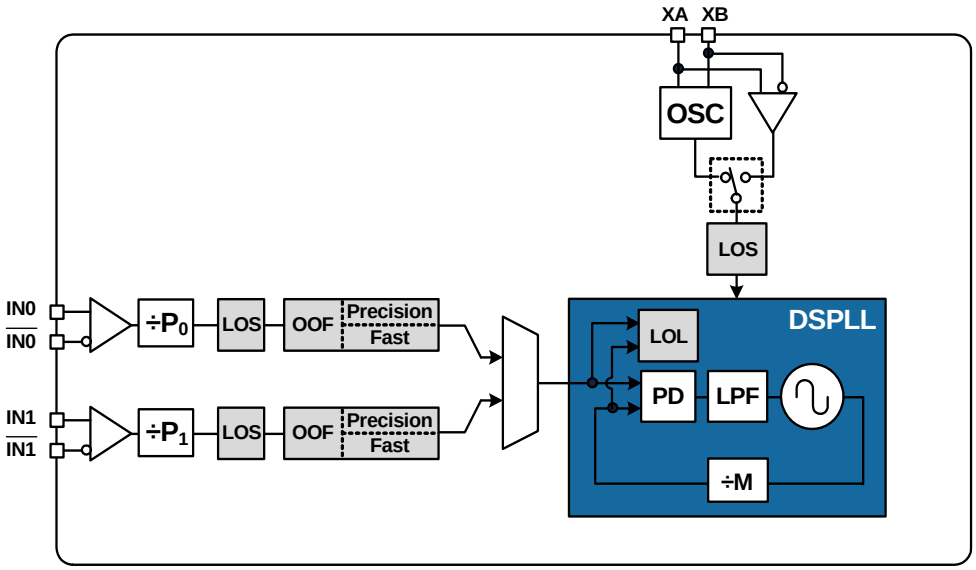


Figure 14. Fault Monitors

4.7.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

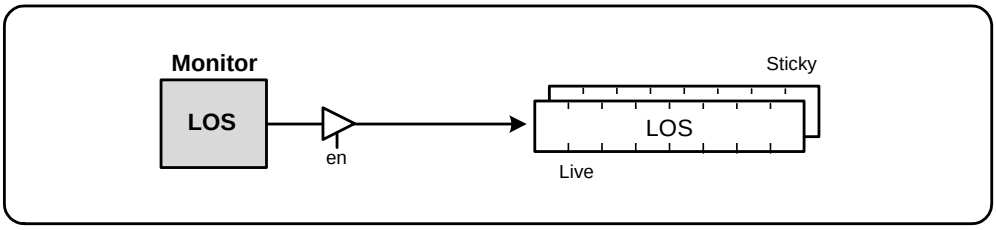


Figure 15. LOS Status Indicators

4.7.2. XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

4.7.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference.

This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in Figure 16. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

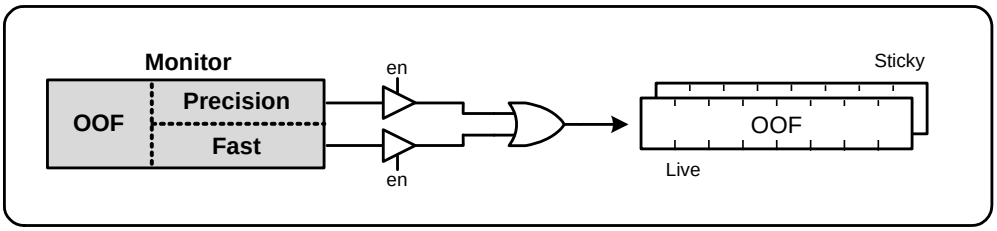


Figure 16. OOF Status Indicator

4.7.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable from ±2 ppm to ±500 ppm in steps of 2 ppm.

A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in Figure 17. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 - IN1) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

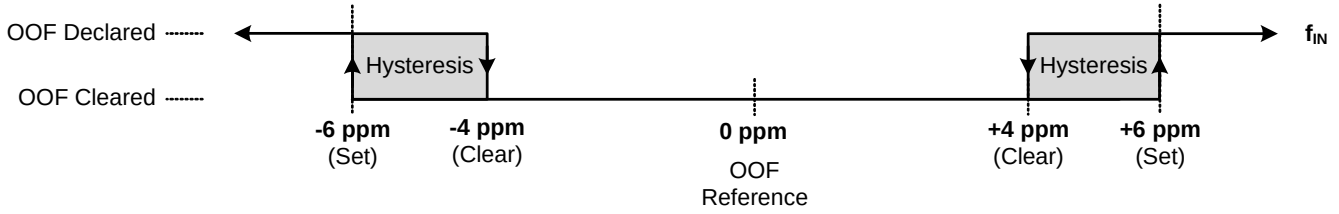


Figure 17. Example of Precise OOF Monitor Assertion and De-assertion Triggers

4.7.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

4.7.4. LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in Figure 18. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The $\overline{\text{LOL}}$ pin reflects the current state of the LOL monitor.

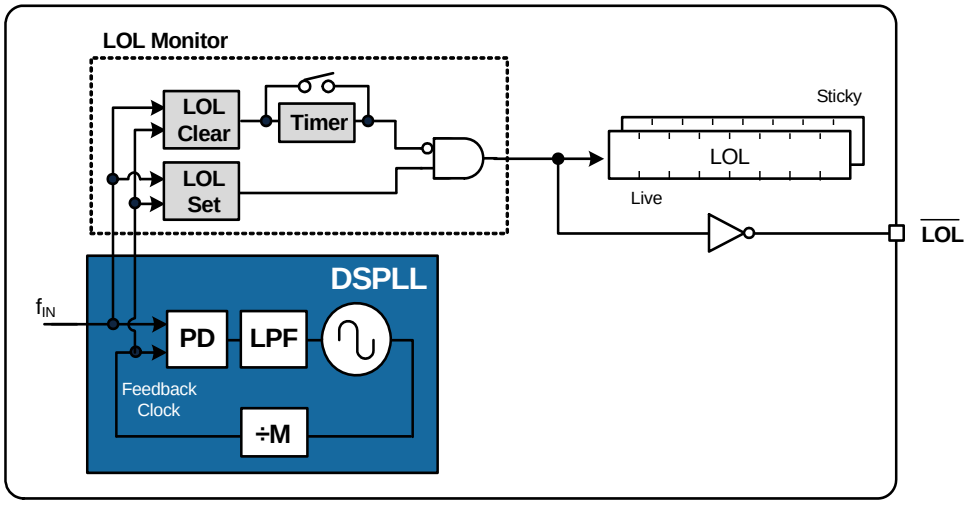


Figure 18. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.2 ppm to 20000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 2 ppm frequency difference is shown in Figure 19.

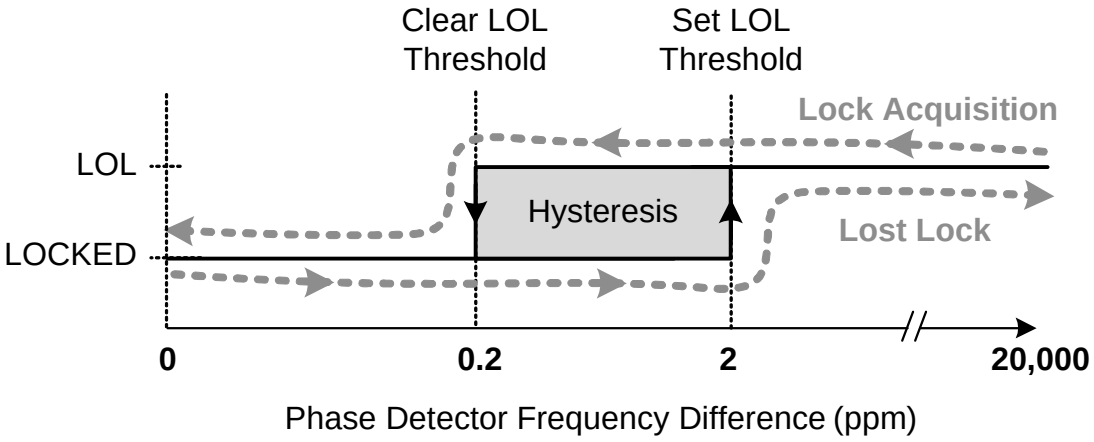


Figure 19. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

4.7.5. Interrupt pin ($\overline{\text{INTR}}$)

An interrupt pin ($\overline{\text{INTR}}$) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the $\overline{\text{INTR}}$ pin is reset by clearing the status register that caused the interrupt.

4.8. Outputs

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V).

4.8.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in Figure 20. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

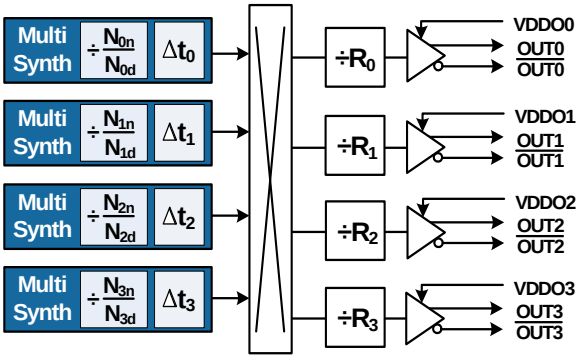


Figure 20. MultiSynth to Output Driver Crosspoint

4.8.2. Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 8 single-ended outputs, or any combination of differential and single-ended outputs.

4.8.3. Differential Output Terminations

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac coupled and dc coupled terminations as shown in Figure 21.

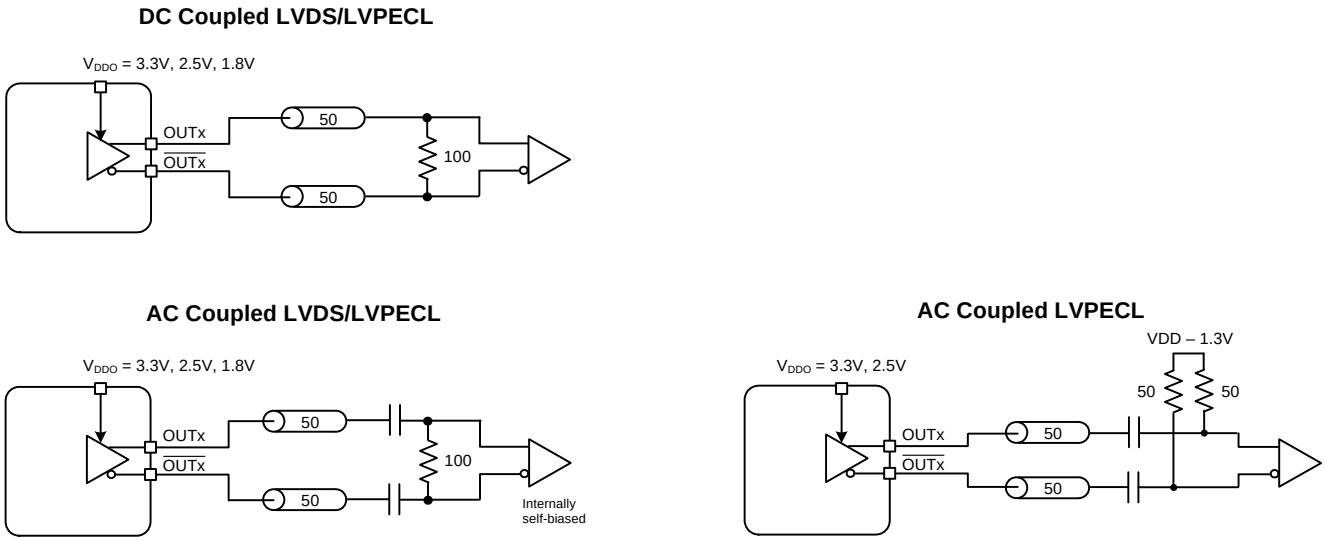


Figure 21. Supported Differential Output Terminations

4.8.4. LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in Figure 22.

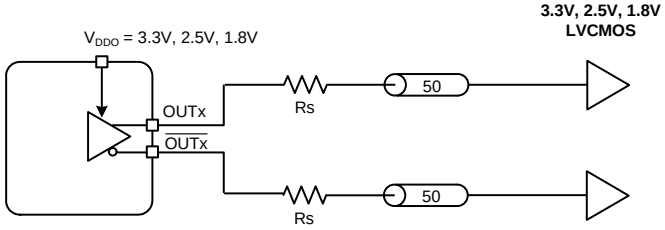


Figure 22. LVCMOS Output Terminations

4.8.5. LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances. A source termination resistor is recommended to help match the selected output impedance to the trace impedance, where Rs = Transmission line impedance – Z_O. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO options as shown in Table 16.

Table 16. Typical Output Impedance (Z_S)

	CMOS_DRIVE_Selection		
VDDO	**CMOS1**	**CMOS2**	**CMOS3**
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.8.6. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

4.8.7. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and $\overline{\text{OUTx}}$). By default the clock on the $\overline{\text{OUTx}}$ pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complementary clock generation and/or inverted polarity with respect to other output drivers.

4.8.8. Output Enable/Disable

The $\overline{OE}$ pin provides a convenient method of disabling or enabling the output drivers. When the $\overline{OE}$ pin is held high all outputs will be disabled. When held low, the outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

4.8.9. Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low, disable high, or disable high-impedance.

4.8.10. Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

4.8.11. Output Skew Control ($\Delta t_0 - \Delta t_3$)

The Si5344H/42H uses independent MultiSynth dividers (N_0 - N_3) to generate up to 4 unique frequencies to its 10 outputs through a crosspoint switch. By default all clocks are phase aligned. A delay path (Δt_0 - Δt_3) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation. The resolution of the phase adjustment is approximately 0.28 ps per step definable in a range of ±9.14 ns. Phase adjustments are register configurable. An example of generating two frequencies with unique configurable path delays is shown in Figure 23.

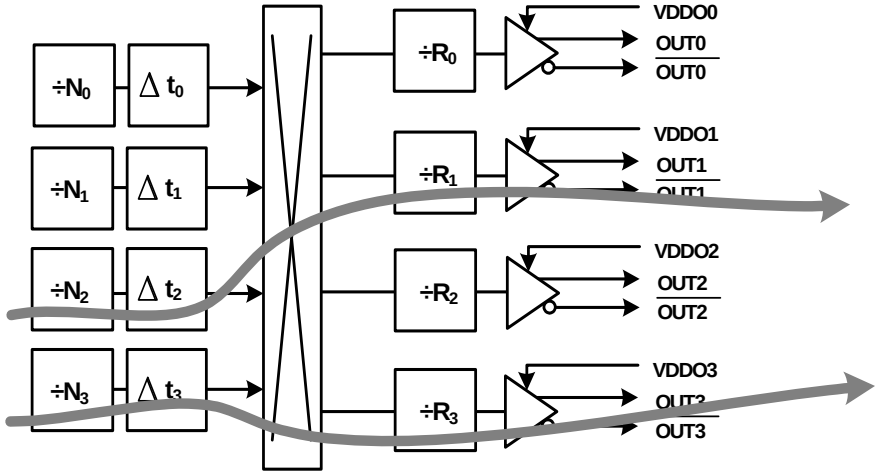


Figure 23. Example of Independently Configurable Path Delays

All phase delay values are restored to their default values after power-up, hard reset, or a reset using the $\overline{RST}$ pin. Phase delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the $\overline{RST}$ pin.

4.8.12. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the $\overline{RST}$ pin or asserting the hard reset bit will have the same result. Asserting the sync register bit provides another method of re-aligning the R dividers without resetting the device.

4.9. Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.10. In-Circuit Programming

The Si5344H/42H is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Family Reference Manual for a detailed procedure for writing registers to NVM.

4.11. Serial Interface

Configuration and operation of the Si5344H/42H is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Family Reference Manual for details.

4.12. Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. Use the ClockBuilder Pro custom part number wizard (ClockBuilder Pro) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks Solutions sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

4.13. Enabling Features and/or Configuration Settings Unavailable in ClockBuilder Pro for Factory Preprogrammed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continuously updated and enhanced. By registering at www.skyworksinc.com, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Family Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Skyworks Solutions applications engineer for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Skyworks Solutions applications engineer will email back your CBPro project file with your specific features and register settings enabled using what's referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in Table 17.

Table 17. Setting Overrides

Location	Customer Name	Engineering Name	Type	Target	Dec Value	Hex Value
0x0535[0]	FORCE_HOLD	OLB_HO_FORCE	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	OOF_DIV_CLK_DIS	User	OPN&EVB	0	0x00

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in Figure 24.

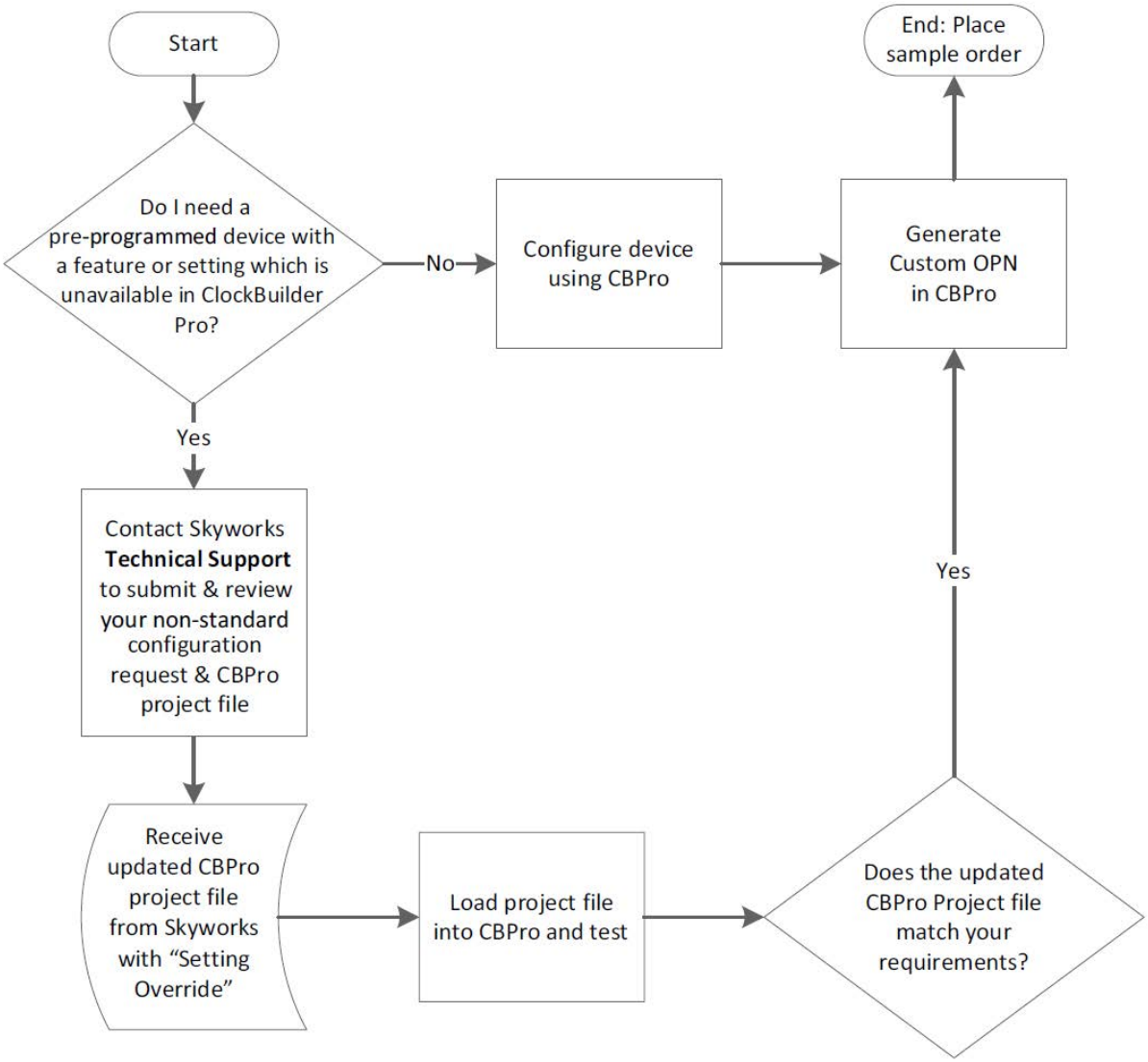


Figure 24. Process for Requesting Non-Standard CBPro Features

5. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in “5.2. High-Level Register Map” . Refer to the Family Reference Manual for a complete list of register descriptions and settings. Skyworks Solutions strongly recommends using ClockBuilder Pro to create and manage register settings.

5.1. Addressing Scheme

The device registers are accessible using a 16-bit address which consists of an 8-bit page address + 8-bit register address. By default the page address is set to 0x00. Changing to another page is accomplished by writing to the ‘Set Page Address’ byte located at address 0x01 of each page.

5.2. High-Level Register Map

Table 18. High-Level Register Map

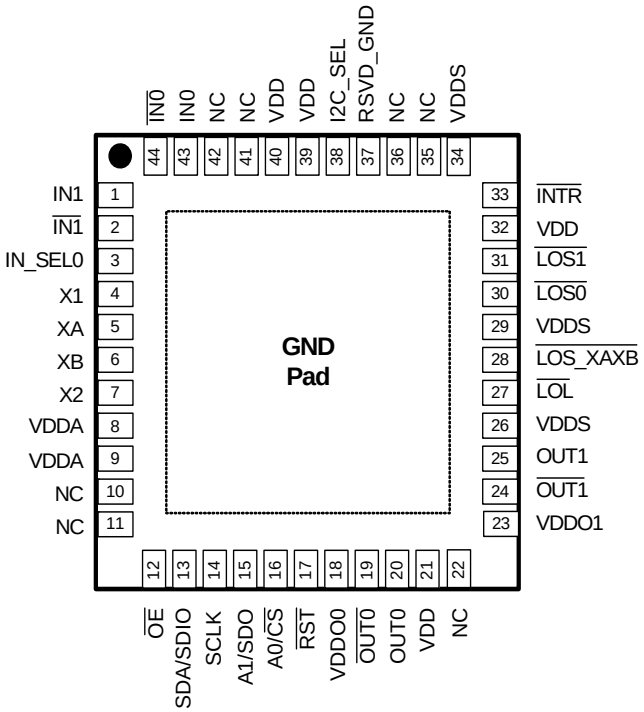
16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	2B	SPI (3-Wire vs 4-Wire)
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	12-2F	Output Driver Controls
	50-61	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–1B	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status

Table 18. High-Level Register Map (Continued)

16-Bit Address		Content
8-bit Page Address	**8-bit Register Address Range**	
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	59–60	Output Delay (Δt) Settings
	FE	Device Ready Status
05	0E - 14	Fast Lock Loop Bandwidth
	15–1F	Feedback Divider (M) Settings
	2A	Input Select Control
	2B	Fast Lock Control
	2C–35	Holdover Settings
	36	Input Clock Switching Mode Select
	38	Input Priority Settings
	3F	Holdover History Valid Data
06–08	00–FF	Reserved
09	01	Set Page Address
	43	Control I/O Voltage Select
	49	Input Settings
10–FF	00–FF	Reserved

6. Pin Descriptions

Si5342H 44QFN
Top View



Si5344H 44QFN
Top View

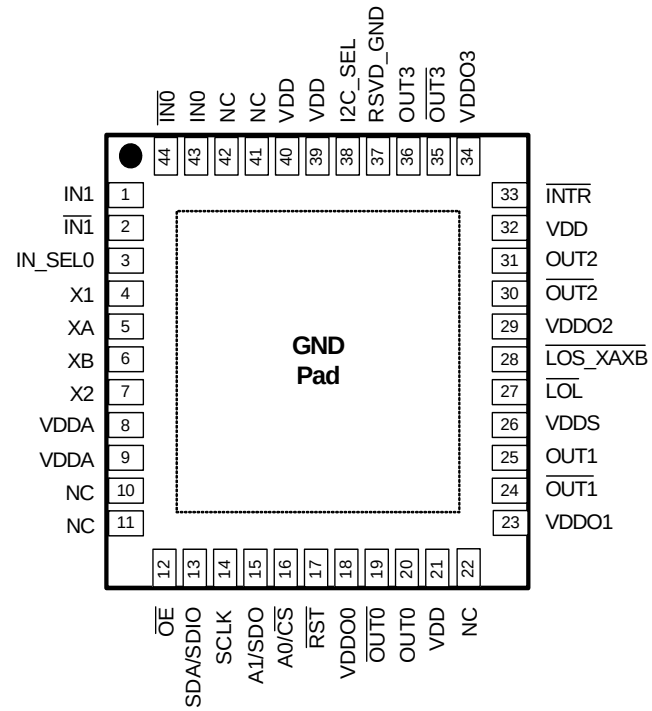


Table 19. Pin Descriptions Table

Pin Name	Si5342H Pin Number	Si5344H Pin Number	Pin Type[1]	Function
Inputs				
XA	5	5	I	**Crystal Input** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
XB	6	6	I	
X1	4	4	I	**XTAL Shield** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Contact Skyworks Solutions for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	7	7	I	
IN0	43	43	I	**Clock Inputs** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to "4.6.5. Input Configuration and Terminations" on page 29 for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
$\overline{\text{IN0}}$	44	44	I	
IN1	1	1	I	
$\overline{\text{IN1}}$	2	2	I	
Outputs				
OUT0	20	20	O	**Output Clocks** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in “4.8.3. Differential Output Terminations” . Unused outputs should be left unconnected.
$\overline{\text{OUT0}}$	19	19	O	
OUT1	25	25	O	
$\overline{\text{OUT1}}$	24	24	O	
OUT2	—	31	O	
$\overline{\text{OUT2}}$	—	30	O	
OUT3	—	36	O	
$\overline{\text{OUT3}}$	—	35	O	

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation. These pins are push-pull outputs and do not require an external pull-up resistor.

Table 19. Pin Descriptions Table

Pin Name	Si5342H Pin Number	Si5344H Pin Number	Pin Type[1]	Function
Serial Interface				
I2C_SEL	38	38	I	**I²C Select** This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high. Leave disconnected when unused. See Note 2.
SDA/SDIO	13	13	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I²C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. Tie low when unused. See Note 2.
A1/SDO	15	15	I/O	**Address Select 1/Serial Data Output** In I²C mode this pin functions as the A1 address input pin. In 4-wire SPI mode this is the serial data output (SDO) pin. Leave disconnected when unused. See Note 2.
SCLK	14	14	I	**Serial Clock Input** This pin functions as the serial clock input for both I²C and SPI modes. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused. See Note 2.
A0/$\overline{CS}$	16	16	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled address A0 in I²C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left unconnected when not in use. See Note 2.

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation. These pins are push-pull outputs and do not require an external pull-up resistor.

Table 19. Pin Descriptions Table

Pin Name	Si5342H Pin Number	Si5344H Pin Number	Pin Type[1]	Function
Control/Status				
$\overline{\text{INTR}}$	33	33	O	**Interrupt** This pin is asserted low when a change in device status has occurred. This pin must be pulled-up using an external resistor of at least 1 kΩ. It should be left unconnected when not in use. See Note [2].
$\overline{\text{RST}}$	17	17	I	**Device Reset** Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use. See Note [2].
$\overline{\text{OE}}$	12	12	I	**Output Enable** This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. See Note [2].
$\overline{\text{LOL}}$	27	27	O	**Loss Of Lock** This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use. See Note [3].
$\overline{\text{LOS0}}$	30	—	O	**Loss Of Signal for IN0 (Si5342H only)** This pin indicate a loss of clock at the IN0 pin when low. See Note [3].
$\overline{\text{LOS1}}$	31	—	O	**Loss Of Signal for IN1 (Si5342H only)** This pin indicate a loss of clock at the IN1 pin when low. See Note [3].
$\overline{\text{LOS\_XAXB}}$	28	28	O	**Loss Of Signal on XA/XB Pins** This pin indicates a loss of signal at the XA/XB pins when low. See Note [3].
IN_SEL	3	3	I	**Input Reference Select** The IN_SEL pin is used in manual pin controlled mode to select the active clock input as shown in Table 15 on page 29. These pins are internally pulled low. See Note [2].
RSVD_GND	37		—	**Reserved - Connect to Ground** This pin is connected to the die and must be connected to ground.

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation. These pins are push-pull outputs and do not require an external pull-up resistor.

Table 19. Pin Descriptions Table

Pin Name	Si5342H Pin Number	Si5344H Pin Number	Pin Type[1]	Function
NC	10	10	—	**No Connect** These pins are not connected to the die. Leave disconnected.
	11	11	—	
	22	22	—	
	35	—	—	
	36	—	—	
	41	—	—	
	42	—	—	

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation. These pins are push-pull outputs and do not require an external pull-up resistor.

Table 19. Pin Descriptions Table

Pin Name	Si5342H Pin Number	Si5344H Pin Number	Pin Type[1]	Function
Power				
VDD	21	21	P	**Core Supply Voltage** The device operates from a 1.8 V supply. A 0.1 µF bypass capacitor should be placed very close to this pin.
	32	32	P	
	39	39	P	
	40	40	P	
VDDA	8	8	P	**Core Supply Voltage 3.3 V** This core supply pin requires a 3.3 V power source. A 1 µF bypass capacitor should be placed very close to this pin.
	9	9	P	
VDDS	26	26	P	**Status Output Voltage** The voltage on these pins determines the V_{OL}/V_{OH} on some of the LOL and LOS status output pins. Connect to 3.3 V or 1.8 V. A 0.1 uF bypass capacitor should be placed very close to this pin.
	29	—	P	
	34	—	P	
VDDO0	18	18	P	**Output Clock Supply Voltage** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, $\overline{\text{OUTn}}$ outputs. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	23	23	P	
VDDO2	—	29	P	
VDDO3	—	34	P	
GND PAD	—		P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation.

Notes:
1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation. These pins are push-pull outputs and do not require an external pull-up resistor.

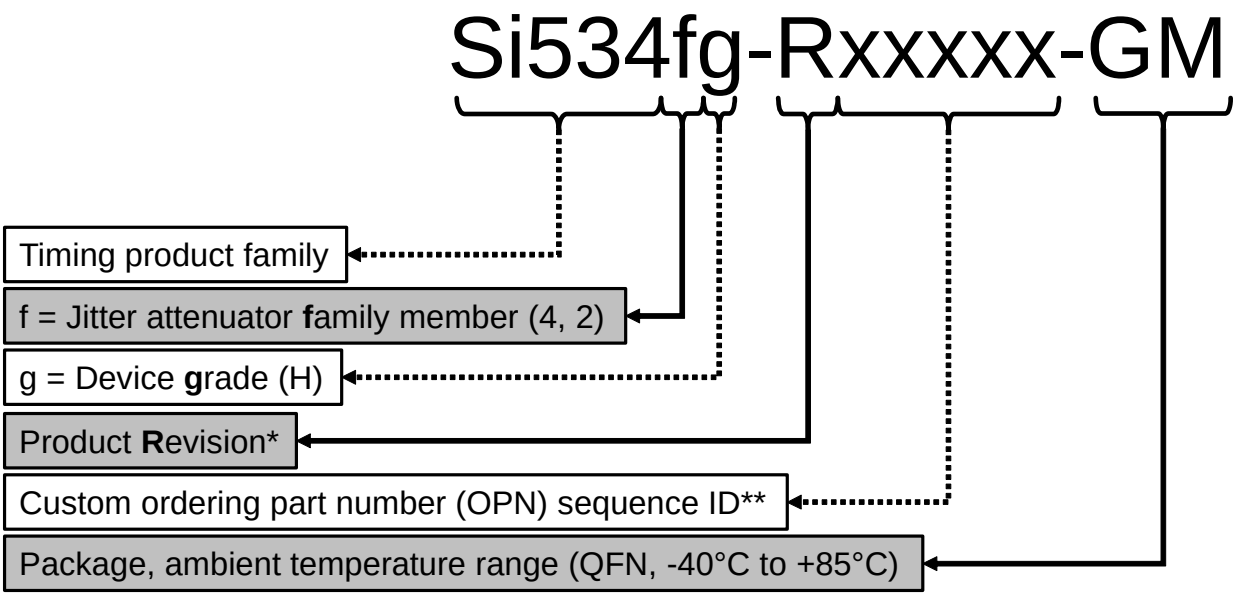
7. Ordering Guide

Ordering Part Number (OPN)	Number of Input/Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes (Typical Jitter)	Package	Temperature Range
Si5342H-D-GM[1,2]	2/2	Up to 717.5 MHz and Up to 2.75 GHz	Integer (50 fs) and Fractional (150 fs)	44-Lead 7x7 QFN	–40 to 85 °C
Si5344H-D-GM[1,2]	2/4	Up to 717.5 MHz and Up to 2.75 GHz	Integer (50 fs) and Fractional (150 fs)	44-Lead 7x7 QFN	–40 to 85 °C

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by Skyworks Solutions and the ClockBuilder Pro software utility.Custom part number format is: e.g. Si5342H-Dxxxxx-GM where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration and is assigned by the ClockBuilder Pro software.

7.1. Ordering Part Number Fields



*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

8. Package Outlines

8.1. 7x7 mm 44-QFN Package Diagram

Figure 25 illustrates the package details. Table 20 lists the values for the dimensions shown in the illustration.

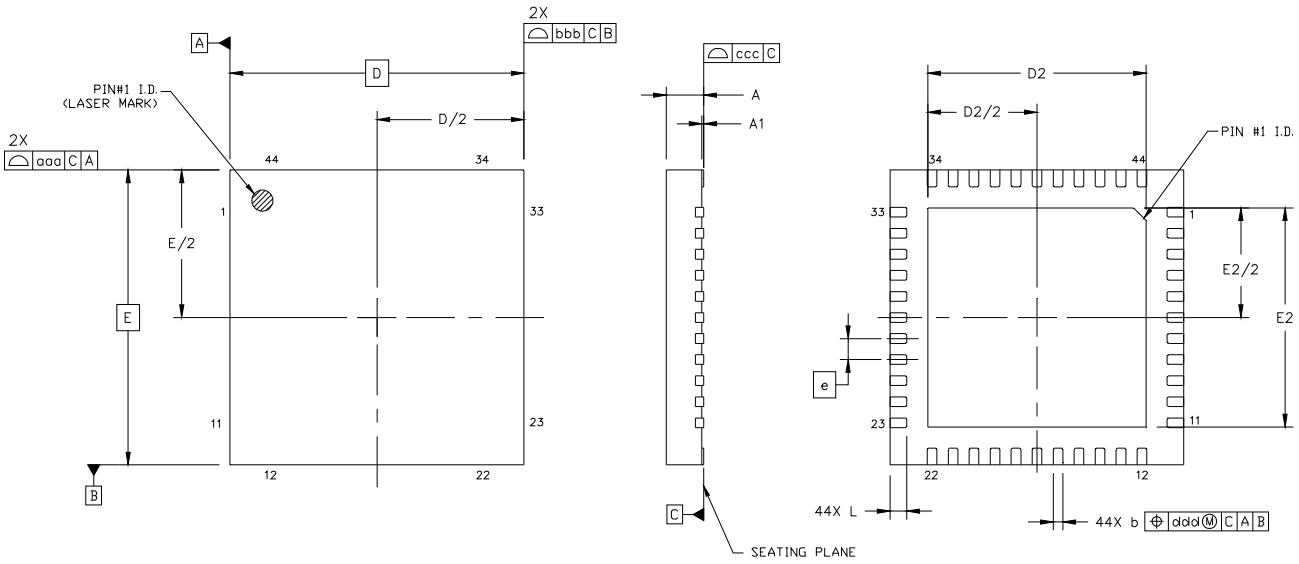


Figure 25. 44-Pin Quad Flat No-Lead (QFN)

Table 20. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. PCB Land Pattern

Figure 26 illustrates the PCB land pattern details for the devices. Table 21 lists the values for the dimensions shown in the illustration.

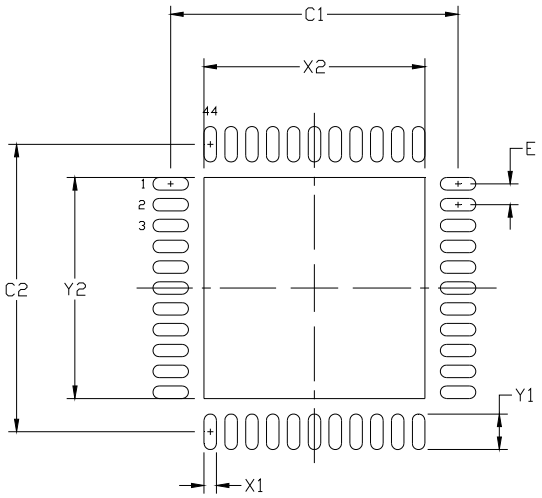


Figure 26. PCB Land Pattern

Table 21. PCB Land Pattern Dimensions

Dimension	Millimeters (Max)
C1	6.90
C2	6.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Top Marking

44-QFN

Line	Characters	Description
1	Si534fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): f = 4: 4-output Si5344H: 44-QFN f = 2: 2-output Si5342H: 44-QFN g = Device Grade (H). See “7. Ordering Guide” for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (Refer to “7. Ordering Guide” for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.4 mm diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; center-justified TW = Taiwan; Country of Origin (ISO Abbreviation)

11. Device Errata

Please log in or register at www.skyworksinc.com to access the device errata document.

Document Change List

Revision 0.91

- Initial data sheet released.

Revision 0.91 to Revision 0.96

- Updated and expanded output frequency range specification.
- Updated functional block diagram and description to allow MultiSynth or high-speed output on any output clock.
- Added typical application block diagram.
- AC/DC performance specification tables updated to support Revision C product.
- Updated ordering guide to support Revision C product.

Revision 0.96 to Revision 0.98

- Increased maximum output frequency from 2.38 GHz to 2.75 GHz.
- Expanded and improved output frequency ranges (see Table 5 on page 8).
- Updated description of Digitally Controlled Oscillator (DCO) mode (see page 27).
- AC/DC performance specification tables updated to support Revision D product.
- Updated ordering guide to support Revision D product.

Revision 0.98 to Revision 1.0

September 29, 2016

- Improved AC/DC performance specification. Tables updated to support Revision D product v1.0 product status.

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