



**THE DATASHEET OF
SI4114G-B-GM**



RF SYNTHESIZER WITH INTEGRATED VCOs FOR DIRECT CONVERSION GSM AND GPRS WIRELESS COMMUNICATIONS

Features

- RF synthesizers
 - 1710 to 1990 MHz
- Integrated VCOs, loop filters, varactors, and resonators
- Minimal (2) external components required
- Fast settling time: <140 μ s
- GPRS Class 12 compliant
- Low phase noise
- Programmable powerdown modes
- 1 μ A standby current
- Package: 5 x 5 mm 28-lead QFN

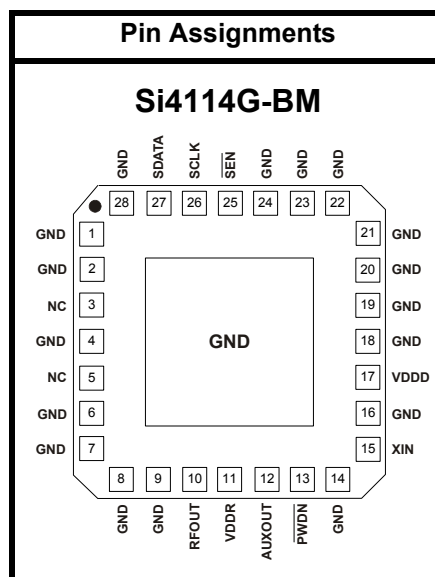
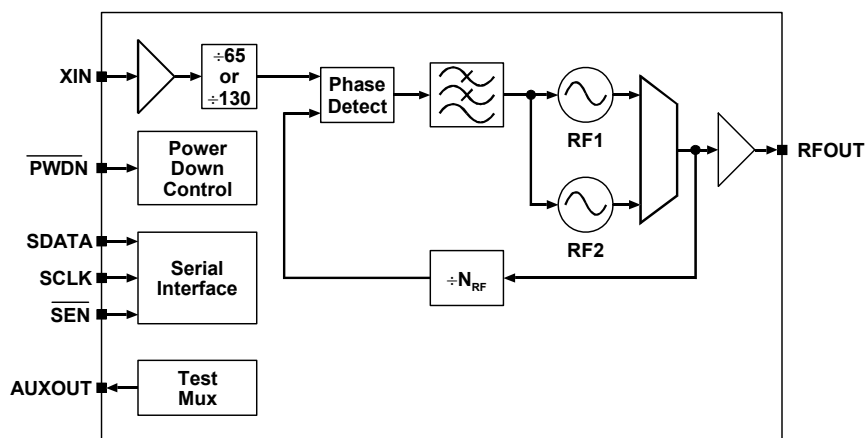
Applications

- E-GSM 900, DCS 1800, and PCS 1900 mobile handsets
- GPRS handsets and data terminals

Description

The Si4114G is a monolithic integrated circuit that performs RF synthesis for multi-band GSM and GPRS wireless communications applications. Optimized for use with direct conversion transceivers, the Si4114G includes two VCOs, loop filter, reference and VCO dividers, and phase detector. Divider and powerdown settings are programmable through a three-wire serial interface.

Functional Block Diagram



Patents pending

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Typical Application Circuit	13
3. Functional Description	14
3.1. Serial Interface	14
3.2. Self-Tuning Algorithm	14
3.3. Output Frequencies	14
3.4. PLL Loop Dynamics	15
3.5. RF Outputs (RFOUT)	15
3.6. Reference Frequency Amplifier	15
3.7. Powerdown Modes	15
3.8. Auxiliary Output (AUXOUT)	15
4. Control Registers	17
5. Pin Descriptions: Si4114G-BM	20
6. Ordering Guide	21
7. Package Outline: Si4114G-BM	22
Document Change List	23
Contact Information	24

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		-20	25	70	°C
Supply Voltage	V_{DD}		2.7	2.8	2.9	V
Supply Voltages Difference	V_{Δ}	$(V_{DDR} - V_{DDD}),$ $(V_{DDI} - V_{DDD})$	-0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 3.0 V and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings^{1,2}

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 4.0	V
Input Current ³	I_{IN}	±10	mA
Input Voltage ³	V_{IN}	-0.3 to $V_{DD}+0.3$	V
Storage Temperature Range	T_{STG}	-55 to 150	°C

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, \overline{SEN} , \overline{PWDN} , and XIN.

Table 3. DC Characteristics $(V_{DD} = 2.7 \text{ to } 2.9 \text{ V}, T_A = -20 \text{ to } 70 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 Mode Supply Current ¹		RF1 active	—	14	18	mA
RF2 Mode Supply Current ¹		RF2 active	—	13	18	mA
Standby Current		$\overline{\text{PWDN}} = 0$	—	1	—	μA
High Level Input Voltage ²	V_{IH}		$0.7 V_{DD}$	—	—	V
Low Level Input Voltage ²	V_{IL}		—	—	$0.3 V_{DD}$	V
High Level Input Current ²	I_{IH}	$V_{IH} = 3.6 \text{ V},$ $V_{DD} = 3.6 \text{ V}$	-10	—	10	μA
Low Level Input Current ²	I_{IL}	$V_{IL} = 0 \text{ V},$ $V_{DD} = 3.6 \text{ V}$	-10	—	10	μA
High Level Output Voltage ³	V_{OH}	$I_{OH} = -500 \mu\text{A}$	$V_{DD}-0.4$	—	—	V
Low Level Output Voltage ³	V_{OL}	$I_{OH} = 500 \mu\text{A}$	—	—	0.4	V

Notes:

1. RF1 = 1.92 GHz, RF2 = 1.78 GHz
2. For signals SCLK, SDATA, SEN, and $\overline{\text{PWDN}}$.
3. For signal AUXOUT.

Table 4. Serial Interface Timing

($V_{DD} = 2.7$ to 2.9 V, $T_A = -20$ to 70 °C)

Parameter ¹	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK \uparrow ²	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK \uparrow ²	t_{hold}	Figure 2	0	—	—	ns
$\overline{SEN}\downarrow$ to SCLK \uparrow Delay Time ²	t_{en1}	Figure 2	10	—	—	ns
SCLK \uparrow to $\overline{SEN}\uparrow$ Delay Time ²	t_{en2}	Figure 2	12	—	—	ns
$\overline{SEN}\uparrow$ to SCLK \uparrow Delay Time ²	t_{en3}	Figure 2	12	—	—	ns
\overline{SEN} Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:

1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of waveform. See Figure 2.

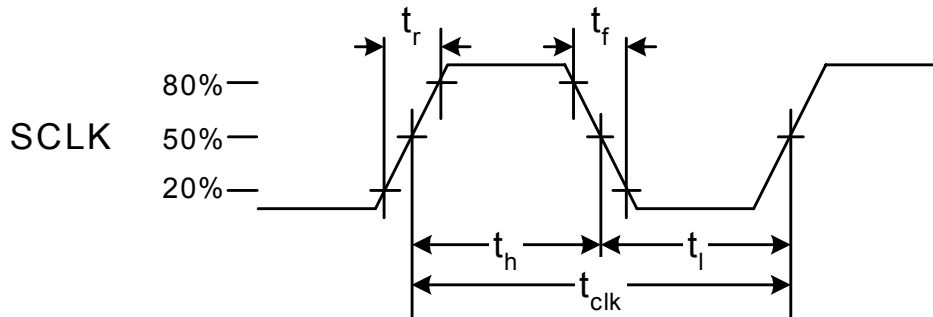


Figure 1. SCLK Timing Diagram

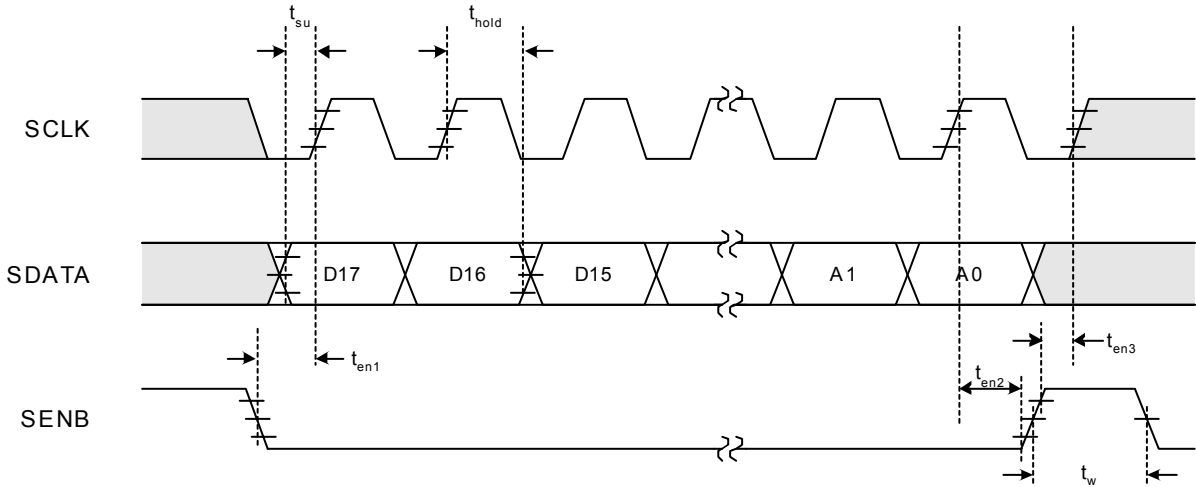


Figure 2. Serial Interface Timing Diagram

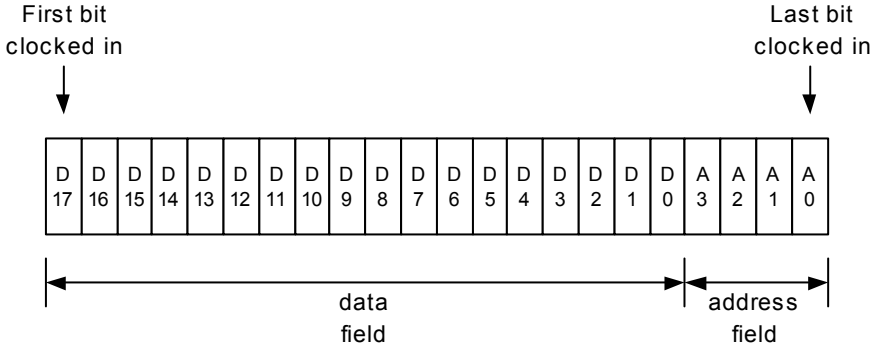


Figure 3. Serial Word Format

Table 5. RF Synthesizer Characteristics

($V_{DD} = 2.7$ to 2.9 V, $T_A = -20$ to 70 °C)

Parameter ¹	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		13	—	26	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	$V_{DD} + 0.3$	V_{PP}
Phase Detector Update Frequency	f_{ϕ}	$f_{\phi} = f_{REF}/R$	—	200	—	KHz
RF1 Tuning Range			1840	—	1990	MHz
RF2 Tuning Range			1710	—	1840	MHz
RF1 VCO Pushing		Open loop	—	500	—	kHz/V
RF2 VCO Pushing			—	400	—	kHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	400	—	kHz _{PP}
RF2 VCO Pulling			—	100	—	kHz _{PP}
RF1 Phase Noise ²		1 MHz offset	—	-132	-130.5	dBc/Hz
		1.6 MHz offset	—	-137	-135.5	dBc/Hz
		3 MHz offset	—	-142	-140.5	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 100 kHz	—	1.0	—	deg rms
RF2 Phase Noise ²		1 MHz offset	—	-134	-132	dBc/Hz
		1.6 MHz offset	—	-139	-137	dBc/Hz
		3 MHz offset	—	-144	-142	dBc/Hz
RF2 Integrated Phase Error		100 Hz to 100 kHz	—	0.8	—	deg rms
RF1 Harmonic Suppression		Second Harmonic	—	-26	—	dBc
RF2 Harmonic Suppression			—	-26	—	dBc
RFOUT Power Level ³		RF1 active, $Z_L = 50 \Omega$	-6	-2.4	0	dBm
RFOUT Power Level ³		RF2 active, $Z_L = 50 \Omega$	-6.5	-4	0	dBm
RF1 Reference Spurs ²		Offset = 200 kHz	—	-70	-63	dBc
		Offset = 400 kHz	—	-75	-67	dBc
		Offset = 600 kHz	—	-80	-70	dBc
RF2 Reference Spurs ²		Offset = 200 kHz	—	-67	-63	dBc
		Offset = 400 kHz	—	-71	-67	dBc
		Offset = 600 kHz	—	-75	-70	dBc
Powerup Request to Synthesizer Ready Time, RF1, RF2 ⁴	t_{pup}	Figures 4, 5	—	140	—	μ s
Powerdown Request to Synthesizer Off Time ⁵	t_{pdn}	Figures 4, 5	—	—	100	ns

Notes:

1. RF1 = 1.92 GHz, RF2 = 1.78 GHz for all parameters unless otherwise noted.
2. Maximum values guaranteed by design.
3. RF1 = 1.90 GHz, RF2 = 1.80 GHz, $T_A = -10$ to $+55$ °C.
4. From powerup request (\overline{PWDN} ↑ or \overline{SEN} ↑ during a write of 1 to bit PDRB in Register 2) to RF synthesizers ready (settled to within 0.1 ppm frequency error). Typical settling time to 5 degrees phase error is 120 μ s.
5. From powerdown request (\overline{PWDN} ↓, or \overline{SEN} ↑ during a write of 0 to bit PDRB in Register 2) to supply current equal to I_{PWDN} .

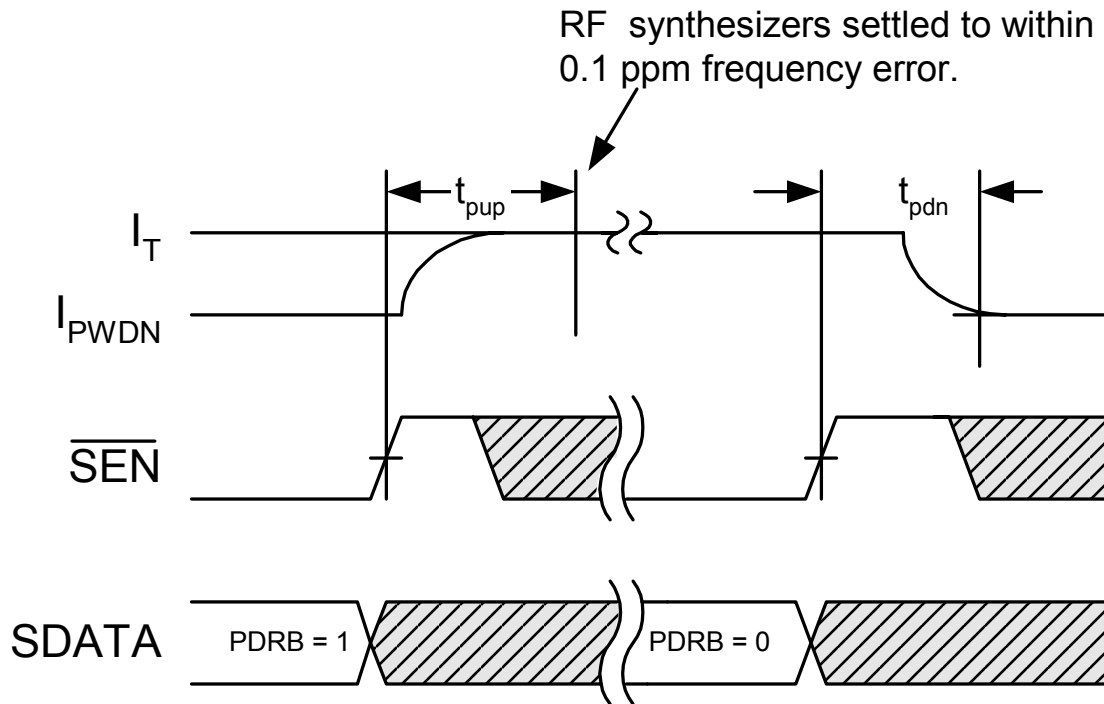


Figure 4. Software Power Management Timing Diagram

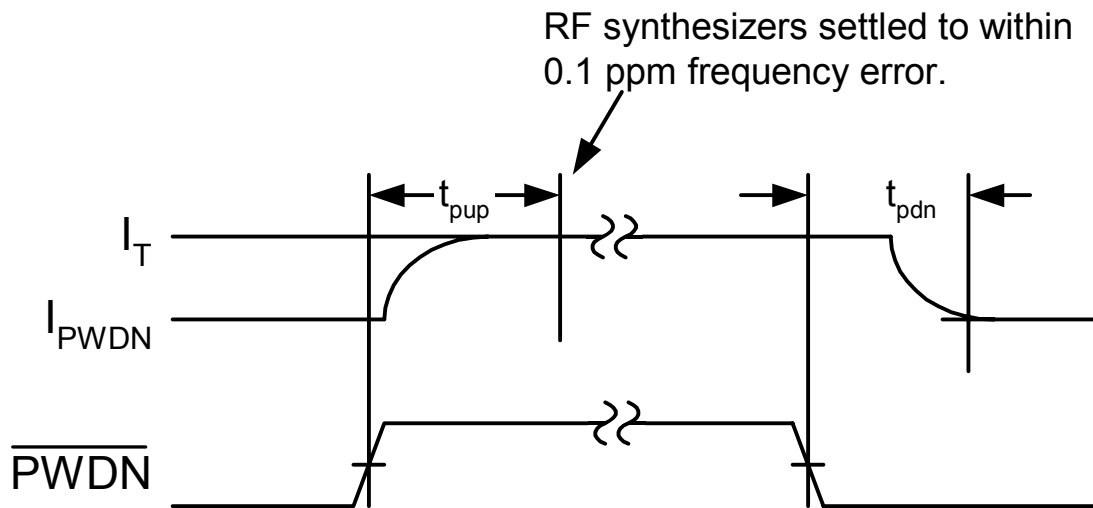


Figure 5. Hardware Power Management Timing Diagram

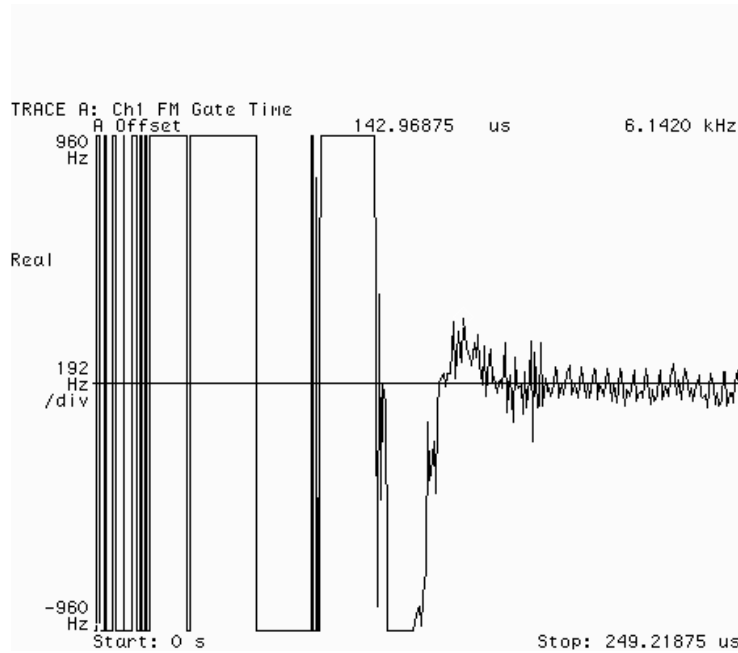


Figure 6. Typical Transient Response RF1 at 1.92 GHz with 200 kHz Phase Detector Update Frequency

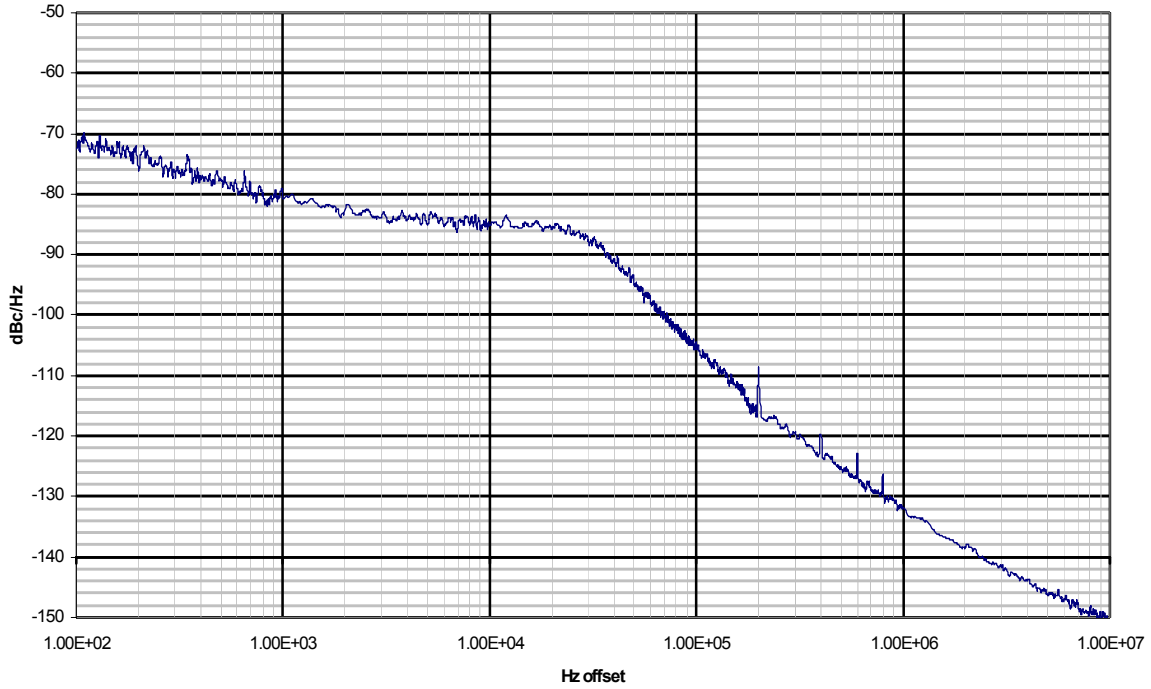


Figure 7. Typical RF1 Phase Noise at 1.92 GHz with 200 kHz Phase Detector Update Frequency

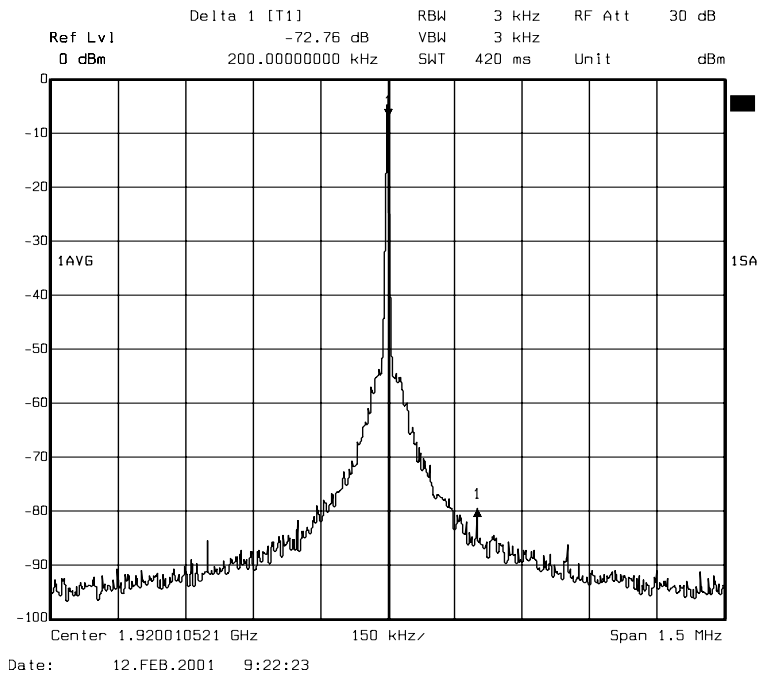


Figure 8. Typical RF1 Spurious Response at 1.92 GHz with 200 kHz Phase Detector Update Frequency

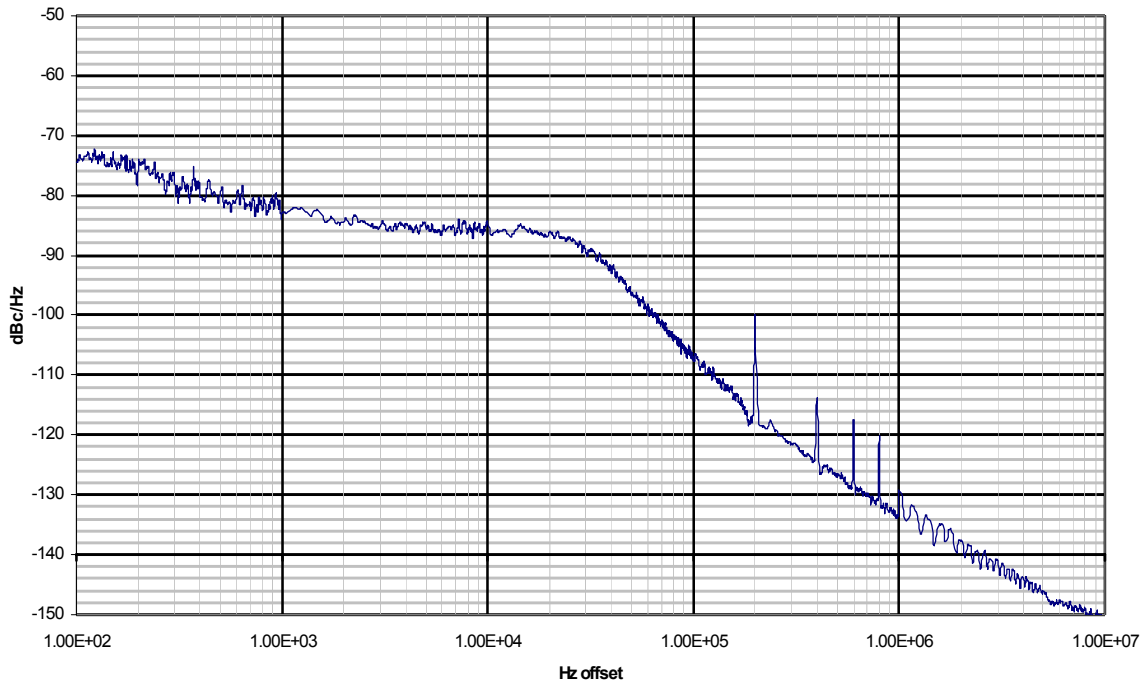


Figure 9. Typical RF2 Phase Noise at 1.78 GHz with 200 kHz Phase Detector Update Frequency

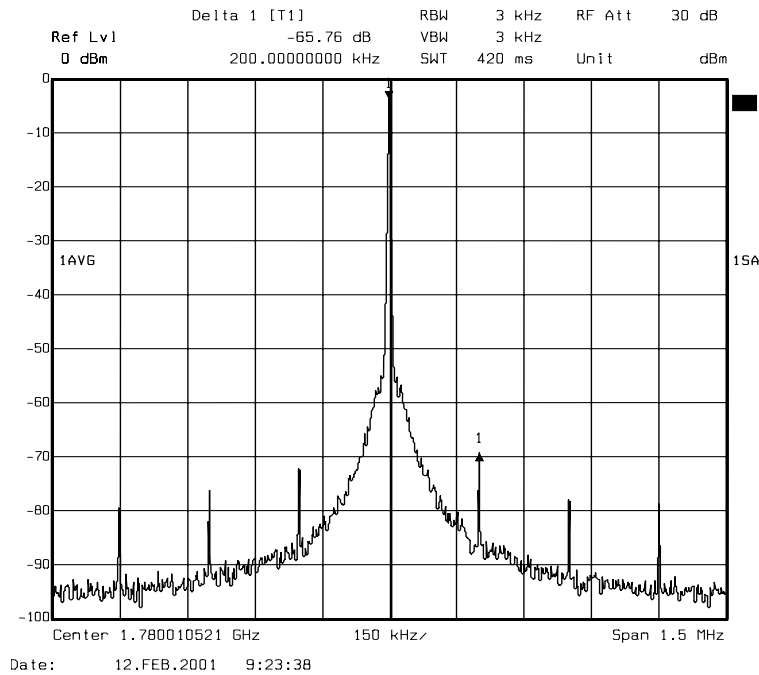
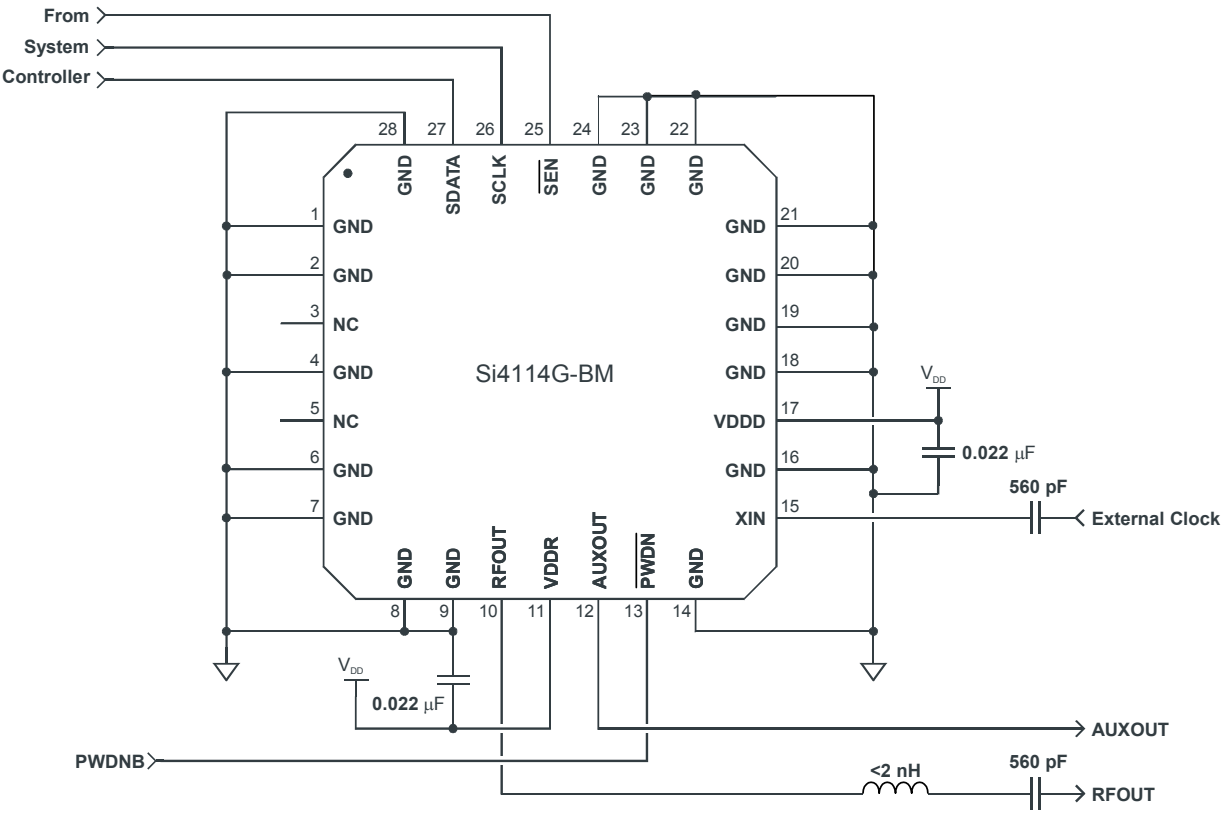


Figure 10. Typical RF2 Spurious Response at 1.78 GHz with 200 kHz Phase Detector Update Frequency

2. Typical Application Circuit



3. Functional Description

The Si4114G is a monolithic integrated circuit (IC) that performs multi-band RF synthesis for E-GSM 900, DCS 1800, and PCS 1900 applications. Its fast transient response also makes the Si4114G especially well suited to GPRS multislot applications where channel switching and settling times are critical. This IC, with a minimum number of external components, is all that is necessary to implement the frequency synthesis function.

The Si4114G has two complete phase-locked loops (PLLs) with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4114G suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference dividers. The IC is programmed through a three-wire serial interface.

Two RF PLLs are provided to cover the 1710–1990 MHz frequency span. RF1 covers 1840–1990 MHz; RF2 covers 1710–1840 MHz.

The center frequency of each VCO is set by an internal L-C tank circuit. Inaccuracies in this tank due to temperature or small manufacturing offsets are compensated for by the Si4114G's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered up (by either the $\overline{\text{PWDN}}$ pin or by software) and/or each time a new output frequency is programmed.

The unique PLL architecture used in the Si4114G produces a transient response that is superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

3.1. Serial Interface

A timing diagram for the serial interface is shown in Figure 2 on page 7. Figure 3 on page 7 shows the format of the serial word.

The Si4114G is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when $\overline{\text{SEN}}$ is low) data and address bits on the $\overline{\text{SDATA}}$ pin are clocked into an internal shift register on the rising edge of $\overline{\text{SCLK}}$. Data in the shift register is then transferred on the rising edge of $\overline{\text{SEN}}$ into the internal data register addressed in the address field. The serial interface is disabled when $\overline{\text{SEN}}$ is high.

Table 7 on page 17 summarizes the data register functions and addresses. The internal shift register will ignore any leading bits before the 22 required bits.

3.2. Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following powerup of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to coarse-tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for errors in the L-C tank circuit. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency lock, compensating for effects caused by temperature and supply voltage variations.

The Si4114G's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur AFTER self-tuning is limited. The PLL will be able to maintain lock for changes in temperature of approximately $\pm 30^\circ\text{C}$.

Applications such as GSM handsets where the PLL is regularly powered down or switched between channels eliminate the potential effects of temperature drift because the VCO is re-tuned when it is powered up or when a new frequency is programmed. In applications where the ambient temperature can drift substantially after self-tuning, it may be necessary to monitor the LDET $\overline{\text{B}}$ (lock-detect bar) signal on the AUXOUT pin to determine the locking state of the PLL. (See "3.8. Auxiliary Output (AUXOUT)" on page 15 for how to select LDET $\overline{\text{B}}$.)

The LDET $\overline{\text{B}}$ signal is normally low after self-tuning is completed but will rise when the PLL nears the limit of its compensation range (LDET $\overline{\text{B}}$ will also be high when either PLL is executing the self-tuning algorithm). The output frequency will still be locked when LDET $\overline{\text{B}}$ goes high, but the PLL will eventually lose lock if the temperature continues to drift in the same direction. Therefore, if LDET $\overline{\text{B}}$ goes high the RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

3.3. Output Frequencies

The RF output frequencies are set by programming the N-Divider registers. Each RF PLL has its own N register and can be programmed independently. Programming the N-Divider register for either RF1 or RF2

automatically selects the corresponding multiplexed output.

The reference frequency on the XIN pin is divided by R and this signal is the input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL works to make these frequencies equal after an initial transient:

$$\frac{f_{OUT}}{N} = \frac{f_{REF}}{R}$$

or

$$f_{OUT} = \frac{N}{R} \times f_{REF}$$

For XIN = 13 MHz or for XIN = 26 MHz and R = 65 or R = 130 respectively, this simplifies to the following:

$$f_{OUT} = N \times 200 \text{ kHz}$$

The integer N is set by programming the RF1 N-Divider register (Register 3) and the RF2 N-Divider register (Register 4).

Each N divider consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter. However, the calculation of these values is done automatically. Only the appropriate N value needs to be programmed.

The PLL R-divider option (Register 0, RDIV bit) can be programmed to either R = 65 or R = 130 to yield a 200 kHz phase detector update rate with either a 13 MHz or 26 MHz reference frequency, respectively.

3.4. PLL Loop Dynamics

The transient response for each PLL has been optimized for a GSM application. VCO gain, phase detector gain, and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period T_ϕ (T_ϕ equals $1/f_\phi$). For a GSM application with a 200 kHz phase detector update rate, the PLL is $T_\phi = 5 \mu\text{s}$. During the first 6.5 update periods, the Si4114G executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4114G PLLs, the time required to settle the output frequency to 0.1 ppm error is approximately 21 update periods. Thus, the total time after powerup or a change in programmed frequency until the synthesized frequency is well settled (including time for self-tuning) is around 28 update periods or 140 μs .

3.5. RF Outputs (RFOUT)

The RFOUT pin is driven by an amplifier that buffers the output pin from the RF VCOs, and must be coupled to

its load through an ac coupling capacitor. The amplifier is driven by either the RF1 or RF2 VCO, depending upon which N-Divider register was last written to. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

A matching network is recommended to maximize power delivered into a 50 Ω load. The network typically consists of a less than 2 nH series inductance, which may be realized with a PC board trace, connected between the RFOUT pin and the ac coupling capacitor. The network is made to provide an adequate match for both the RF1 and RF2 frequency bands, and also filters the output signal to reduce harmonic distortion. A 50 Ω load is not required for proper operation of the Si4114G. Depending on transceiver requirements, the matching network might not be needed. See Figure 11.

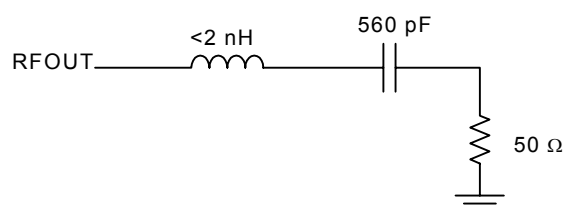


Figure 11. RFOUT 50 Ω Test Circuit

3.6. Reference Frequency Amplifier

The Si4114G provides a reference frequency amplifier. If the driving signal has CMOS levels it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be ac coupled to the XIN pin through a 560 pF capacitor.

3.7. Powerdown Modes

Table 6 summarizes the powerdown functionality. The Si4114G can be powered down by taking the $\overline{\text{PWDN}}$ pin low or by setting bits in the Powerdown register (Register 1). When the $\overline{\text{PWDN}}$ pin is low, the Si4114G will be powered down regardless of the Powerdown register settings. When the $\overline{\text{PWDN}}$ pin is high, power management is under control of the Powerdown register bits.

3.8. Auxiliary Output (AUXOUT)

The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (Register 0).

A lock detect (LDET) signal can be selected by setting the AUXSEL bits to 11. As discussed previously, this signal can be used to indicate that the PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned.

Table 6. Powerdown Configuration

$\overline{\text{PWDN}}$ Pin	PDRB	Reference Frequency Amplifier	RF Circuitry
$\overline{\text{PWDN}} = 0$	x	OFF	OFF
$\overline{\text{PWDN}} = 1$	0	OFF	OFF
	1	ON	ON

4. Control Registers

Table 7. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	0	0	0	0	AUXSEL [1:0]	0	0	0	0	0	0	RDIV	0	0	0	0	1	0
1	Reserved																		
2	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDRB
3	RF1 N Divider	N _{RF1} [17:0]																	
4	RF2 N Divider	0	N _{RF2} [16:0]																
5	Reserved																		
.																			
.																			
.																			
15	Reserved																		

Note: Registers 1 and 5–15 are reserved. Writes to these registers may result in unpredictable behavior. Any register not listed here is reserved and should not be written.

Si4114G

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	AUXSEL [1:0]		0	0	0	0	0	RDIV	0	0	0	0	1	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	AUXSEL[1:0]	Auxiliary Output Pin Definition. 00 = Reserved. 01 = Force output low. 10 = Reserved. 11 = Lock Detect (LDETb).
11:7	Reserved	Program to zero.
6	RDIV	R Divider Selector. 0 = ÷65. 1 = ÷130.
5:2	Reserved	Program to zero.
1	Reserved	Program to one.
0	Reserved	Program to zero.

Register 2. Powerdown Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDRB

Bit	Name	Function
17:1	Reserved	Program to zero.
0	PDRB	Powerdown RF Synthesizer. 0 = RF synthesizer powered down. 1 = RF synthesizer on.

Register 3. RF1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N _{RF1} [17:0]																	

Bit	Name	Function
17:0	N _{RF1} [17:0]	N Divider for RF1 Synthesizer. Note: N _{RF1} can be any value from 9201–9500 (1840.2–1990 MHz).

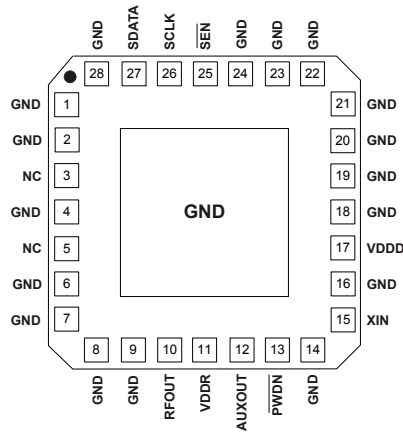
Register 4. RF2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	N _{RF2} [16:0]																

Bit	Name	Function
17	Reserved	Program to zero.
16:0	N _{RF2} [16:0]	N Divider for RF2 Synthesizer. Note: N _{RF2} can be any value from 8500–9200 (1710–1840 MHz).

Si4114G

5. Pin Descriptions: Si4114G-BM



Pin Number(s)	Name	Description
1, 2, 4, 6–9, 14, 16, 18–24, 28	GND	Common ground for RF analog and digital circuitry
3, 5	NC	No connect
10	RFOUT	Radio frequency (RF) output of the selected RF VCO
11	VDDR	Supply voltage for the RF analog circuitry
12	AUXOUT	Auxiliary output
13	PWDN	Powerdown input pin
15	XIN	Reference frequency amplifier input
17	VDDD	Supply voltage for digital circuitry
25	SEN	Serial port enable input
26	SCLK	Serial clock input
27	SDATA	Serial data input

6. Ordering Guide

Ordering Part Number	Description	Operating Temperature
Si4114G-BM	Dual RF Synthesizer	-20 to 70 °C
Si4114G-B-GM	Dual RF Synthesizer, Pb-free, QFN	-20 to 70 °C

7. Package Outline: Si4114G-BM

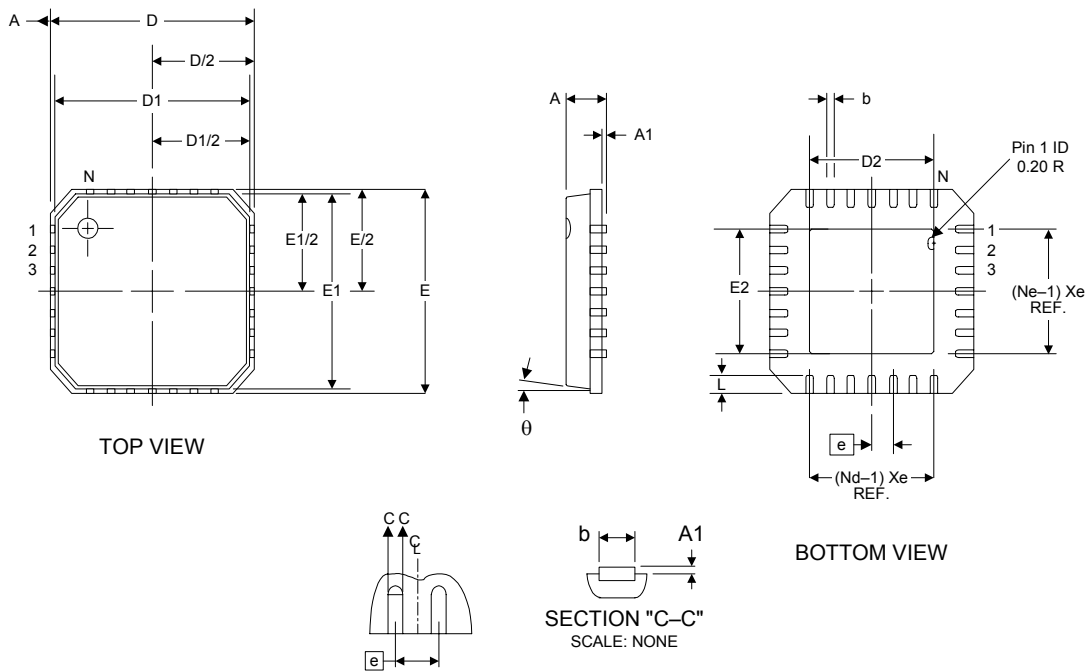


Figure 12. 28-Pin Quad Flat No-lead Package (QFN)

Table 8. Package Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.85	0.90
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D, E	5.00 BSC		
D1, E1	4.75 BSC		
D2	2.55	2.70	2.85
E2	2.55	2.70	2.85
N	28		
Nd	7		
Ne	7		
e	0.50 BSC		
L	0.50	0.60	0.75
θ			12°

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- Table 5 on page 8
 - Combined Notes and 3 and 4

Revision 1.0 to Revision 1.1

- Updated "6. Ordering Guide" on page 21.
- Changed all package type references of MLP to QFN.

CONTACT INFORMATION

Silicon Laboratories Inc.


400 West Cesar Chavez
Austin, Texas 78701
Tel: 1+ (512) 416-8500
Fax: 1+ (512) 416-9669
Toll Free: 1+ (877) 444-3032
Email: RFinfo@silabs.com
Internet: www.silabs.com

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