



**THE DATASHEET OF  
SI5367A-C-GQ**



## µP-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

### Features

- Not recommended for new designs. For alternatives, see the Si533x family of products.
- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 1.3 MHz)
- Four clock inputs with manual or automatically controlled switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- I<sup>2</sup>C or SPI programmable settings
- On-chip voltage regulator for 1.8 V ±5%, 2.5 V ±10%, or 3.5 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant



**Ordering Information:**  
See page 73.

### Applications

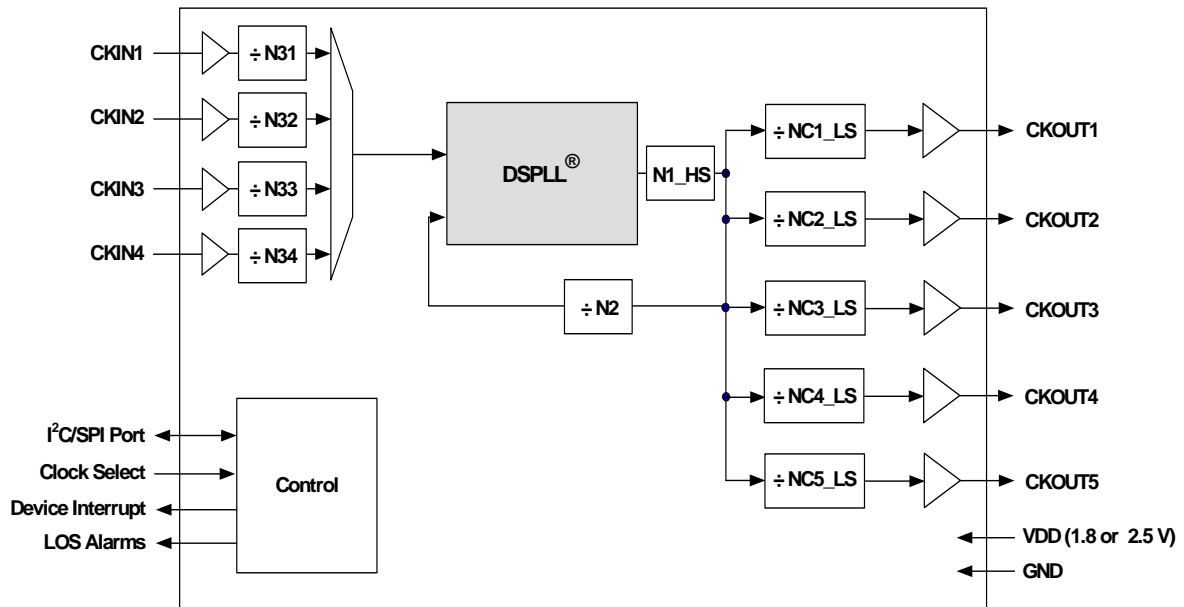
- SONET/SDH OC-48/OC-192 STM-16/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Wireless base stations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

### Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. The outputs are divided down separately from a common source. The Si5367 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface. The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL<sup>®</sup> technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.5 V supply, the Si5367 is ideal for providing clock multiplication in high performance timing applications.

# Si5367

## Functional Block Diagram



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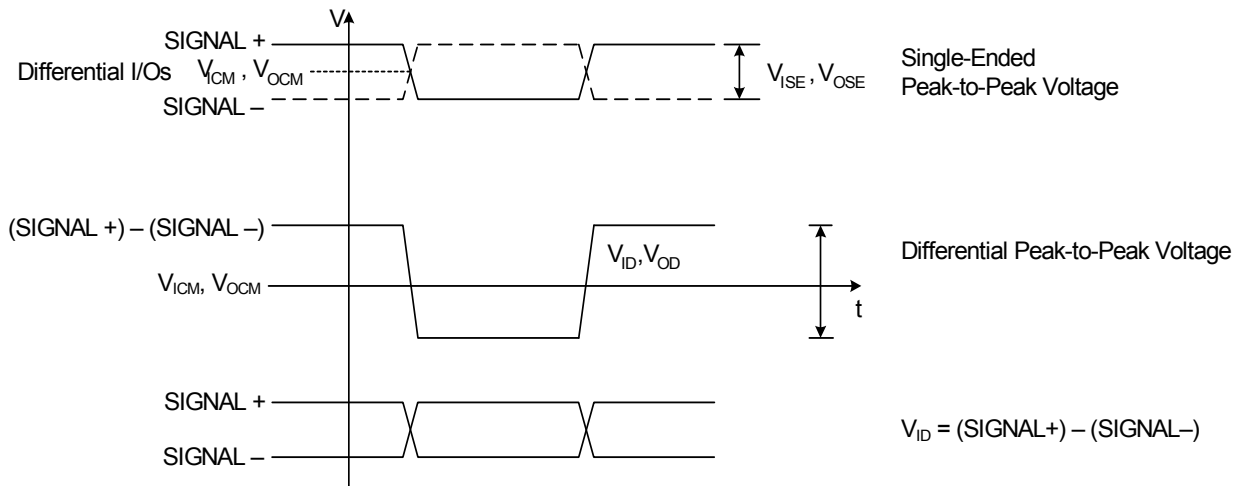
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## 1. Electrical Specifications

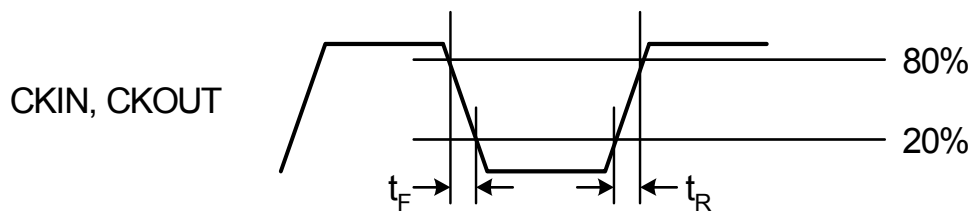
**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	$T_A$		-40	25	85	C
Supply Voltage during Normal Operation	$V_{DD}$	3.3 V Nominal	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V

**Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.



**Figure 1. Differential Voltage Characteristics**



**Figure 2. Rise/Fall Time Characteristics**

**Table 2. DC Characteristics** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current <sup>1,2</sup>	$I_{DD}$	LVPECL Format 622.08 MHz Out All CKOUTs Enabled	—	394	435	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	253	284	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	278	321	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	229	261	mA
		Disable Mode	—	165	—	mA
<b>CKINn Input Pins<sup>3</sup></b>						
Input Common Mode Voltage (Input Threshold Voltage)	$V_{ICM}$	1.8 V $\pm$ 5%	0.9	—	1.4	V
		2.5 V $\pm$ 10%	1	—	1.7	V
		3.3 V $\pm$ 10%	1.1	—	1.95	V
Input Resistance	$CKN_{RIN}$	Single-ended	20	40	60	k $\Omega$
Single-Ended Input Voltage Swing (See Absolute Specs)	$V_{ISE}$	$f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1.	0.2	—	—	$V_{PP}$
		$f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1.	0.25	—	—	$V_{PP}$
Differential Input Voltage Swing (See Absolute Specs)	$V_{ID}$	$f_{CKIN} < 212.5 \text{ MHz}$ See Figure 1.	0.2	—	—	$V_{PP}$
		$f_{CKIN} > 212.5 \text{ MHz}$ See Figure 1.	0.25	—	—	$V_{PP}$
<b>Output Clocks (CKOUTn)<sup>4,5</sup></b>						
<b>Notes:</b>						
1. Current draw is independent of supply voltage.						
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.						
3. No under- or overshoot is allowed.						
4. LVPECL outputs require nominal $V_{DD} \geq 2.5 \text{ V}$ .						
5. LVPECL, CML, LVDS and low-swing LVDS measured with $F_o = 622.08 \text{ MHz}$ .						
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						

**Table 2. DC Characteristics (Continued)** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode	$CKO_{V_{CM}}$	LVPECL 100 $\Omega$ load line-to-line	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
Differential Output Swing	$CKO_{V_D}$	LVPECL 100 $\Omega$ load line-to-line	1.1	—	1.9	$V_{PP}$
Single Ended Output Swing	$CKO_{V_{SE}}$	LVPECL 100 $\Omega$ load line-to-line	0.5	—	0.93	$V_{PP}$
Differential Output Voltage	$CKO_{V_D}$	CML 100 $\Omega$ load line-to-line	350	425	500	mV $_{PP}$
Common Mode Output Voltage	$CKO_{V_{CM}}$	CML 100 $\Omega$ load line-to-line	—	$V_{DD} - 0.36$	—	V
Differential Output Voltage	$CKO_{V_D}$	LVDS 100 $\Omega$ load line-to-line	500	700	900	mV $_{PP}$
		Low Swing LVDS 100 $\Omega$ load line-to-line	350	425	500	mV $_{PP}$
Common Mode Output Voltage	$CKO_{V_{CM}}$	LVDS 100 $\Omega$ load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	$CKO_{R_D}$	CML, LVPECL, LVDS	—	200	—	$\Omega$
Output Voltage Low	$CKO_{V_{OLLH}}$	CMOS	—	—	0.4	V
Output Voltage High	$CKO_{V_{OHLH}}$	$V_{DD} = 1.71 \text{ V}$ CMOS	$0.8 \times V_{DD}$	—	—	V

**Notes:**

1. Current draw is independent of supply voltage.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.
3. No under- or overshoot is allowed.
4. LVPECL outputs require nominal  $V_{DD} \geq 2.5 \text{ V}$ .
5. LVPECL, CML, LVDS and low-swing LVDS measured with  $F_o = 622.08 \text{ MHz}$ .
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.

**Table 2. DC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Drive Current (CMOS driving into CKO <sub>VOL</sub> for output low or CKO <sub>VOH</sub> for output high. CKOUT+ and CKOUT- shorted externally)	CKO <sub>IO</sub>	ICMOS[1:0] = 11 V <sub>DD</sub> = 1.8 V	—	7.5	—	mA
		ICMOS[1:0] = 10 V <sub>DD</sub> = 1.8 V	—	5.5	—	mA
		ICMOS[1:0] = 01 V <sub>DD</sub> = 1.8 V	—	3.5	—	mA
		ICMOS[1:0] = 00 V <sub>DD</sub> = 1.8 V	—	1.75	—	mA
		ICMOS[1:0] = 11 V <sub>DD</sub> = 3.3 V	—	32	—	mA
		ICMOS[1:0] = 10 V <sub>DD</sub> = 3.3 V	—	24	—	mA
		ICMOS[1:0] = 01 V <sub>DD</sub> = 3.3 V	—	16	—	mA
		ICMOS[1:0] = 00 V <sub>DD</sub> = 3.3 V	—	8	—	mA
<b>2-Level LVCMOS Input Pins</b>						
Input Voltage Low	V <sub>IL</sub>	V <sub>DD</sub> = 1.71 V	—	—	0.5	V
		V <sub>DD</sub> = 2.25 V	—	—	0.7	V
		V <sub>DD</sub> = 2.97 V	—	—	0.8	V
Input Voltage High	V <sub>IH</sub>	V <sub>DD</sub> = 1.89 V	1.4	—	—	V
		V <sub>DD</sub> = 2.25 V	1.8	—	—	V
		V <sub>DD</sub> = 3.63 V	2.5	—	—	V
<b>Notes:</b>						
1. Current draw is independent of supply voltage.						
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.						
3. No under- or overshoot is allowed.						
4. LVPECL outputs require nominal V <sub>DD</sub> ≥ 2.5 V.						
5. LVPECL, CML, LVDS and low-swing LVDS measured with F <sub>o</sub> = 622.08 MHz.						
6. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.						

**Table 2. DC Characteristics (Continued)** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>3-Level Input Pins<sup>6</sup></b>						
Input Voltage Low	$V_{ILL}$		—	—	$0.15 \times V_{DD}$	V
Input Voltage Mid	$V_{IMM}$		$0.45 \times V_{DD}$	—	$0.55 \times V_{DD}$	V
Input Voltage High	$V_{IHH}$		$0.85 \times V_{DD}$	—	—	V
Input Low Current	$I_{ILL}$	See Note 6	-20	—	—	$\mu\text{A}$
Input Mid Current	$I_{IMM}$	See Note 6	-2	—	+2	$\mu\text{A}$
Input High Current	$I_{IHH}$	See Note 6	—	—	20	$\mu\text{A}$
<b>LVC MOS Output Pins</b>						
Output Voltage Low	$V_{OL}$	$I_O = 2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$	—	—	0.4	V
Output Voltage Low		$I_O = 2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$	—	—	0.4	V
Output Voltage High	$V_{OH}$	$I_O = -2 \text{ mA}$ $V_{DD} = 1.71 \text{ V}$	$V_{DD} - 0.4$	—	—	V
Output Voltage High		$I_O = -2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$	$V_{DD} - 0.4$	—	—	V
Disabled Leakage Current	$I_{OZ}$	RSTb = 0	-100	—	100	$\mu\text{A}$
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>Current draw is independent of supply voltage.</li> <li>The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</li> <li>No under- or overshoot is allowed.</li> <li>LVPECL outputs require nominal <math>V_{DD} \geq 2.5 \text{ V}</math>.</li> <li>LVPECL, CML, LVDS and low-swing LVDS measured with <math>F_o = 622.08 \text{ MHz}</math>.</li> <li>This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.</li> </ol>						

**Table 3. AC Characteristics** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>CKINn Input Pins</b>						
Input Frequency	$CKN_F$		10	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	$CKN_{DC}$	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	$CKN_{CIN}$		—	—	3	pF
Input Rise/Fall Time	$CKN_{TRF}$	20–80% See Figure 2	—	—	11	ns
<b>CKOUTn Output Pins</b>						
(See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not config- ured for CMOS or Disabled)	$CKO_F$	$N1 \geq 6$	0.002	—	945	MHz
		$N1 = 5$	970	—	1134	MHz
		$N1 = 4$	1.213	—	1.4	GHz
Maximum Output Frequency in CMOS Format	$CKO_F$		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	$CKO_{TRF}$	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	$CKO_{TRF}$	CMOS Output $V_{DD} = 1.71$ $C_{LOAD} = 5 \text{ pF}$	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	$CKO_{TRF}$	CMOS Output $V_{DD} = 2.97$ $C_{LOAD} = 5 \text{ pF}$	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	$CKO_{DC}$	100 $\Omega$ Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps

**Table 3. AC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>LVC MOS Input Pins</b>						
Minimum Reset Pulse Width	t <sub>RSTMN</sub>		1	—	—	μs
Reset to Microprocessor Access Ready	t <sub>READY</sub>		—	—	10	ms
Input Capacitance	C <sub>in</sub>		—	—	3	pF
<b>LVC MOS Output Pins</b>						
Rise/Fall Times	t <sub>RF</sub>	C <sub>LOAD</sub> = 20 pF See Figure 2	—	25	—	ns
LOS <sub>n</sub> Trigger Window	LOS <sub>TRIG</sub>	From last CKIN <sub>n</sub> ↑ to ↓ Internal detection of LOS <sub>n</sub> N3 ≠ 1	—	—	4.5 x N3	T <sub>CKIN</sub>
Time to Clear LOL after LOS Cleared	t <sub>CLRLOL</sub>	↓LOS to ↓LOL Fold = Fnew Stable Xa/XB reference	—	10	—	ms
<b>Device Skew</b>						
Output Clock Skew	t <sub>SKEW</sub>	↑ of CKOUT <sub>n</sub> to ↑ of CKOUT <sub>m</sub> , CKOUT <sub>n</sub> and CKOUT <sub>m</sub> at same frequency and signal format <u>PHASEOFFSET</u> = 0 <u>CKOUT_ALWAYS_ON</u> = 1 <u>SQ_ICAL</u> = 1	—	—	100	ps
Phase Change due to Temperature Variation	t <sub>TEMP</sub>	Max phase changes from -40 to +85 °C	—	300	500	ps

**Table 3. AC Characteristics (Continued)** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>PLL Performance</b> ( $f_{in} = f_{out} = 622.08 \text{ MHz}$ ; $BW = 120 \text{ Hz}$ ; LVPECL)						
Lock Time	$t_{LOCKMP}$	Start of ICAL to ↓ of LOL	—	35	1200	ms
Closed Loop Jitter Peaking	$J_{PK}$		—	0.05	0.1	dB
Jitter Tolerance	$J_{TOL}$	Jitter Frequency $\geq$ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise $f_{out} = 622.08 \text{ MHz}$	$CKO_{PN}$	1 kHz Offset	—	-90	—	dBc/Hz
		10 kHz Offset	—	-113	—	dBc/Hz
		100 kHz Offset	—	-118	—	dBc/Hz
		1 MHz Offset	—	-132	—	dBc/Hz
Subharmonic Noise	$SP_{SUBH}$	Phase Noise @ 100 kHz Offset	—	-88	—	dBc
Spurious Noise	$SP_{SPUR}$	Max spur @ $n \times F3$ ( $n \geq 1, n \times F3 < 100 \text{ MHz}$ )	—	-93	—	dBc

**Table 4. Microprocessor Control** $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>I<sup>2</sup>C Bus Lines (SDA, SCL)</b>						
Input Voltage Low	$V_{IL_{I2C}}$		—	—	$0.25 \times V_{DD}$	V
Input Voltage High	$V_{IH_{I2C}}$		$0.7 \times V_{DD}$	—	$V_{DD}$	V
Hysteresis of Schmitt trigger inputs	$V_{HYS_{I2C}}$	$V_{DD} = 1.8 \text{ V}$	$0.1 \times V_{DD}$	—	—	V
		$V_{DD} = 2.5 \text{ or } 3.3 \text{ V}$	$0.05 \times V_{DD}$	—	—	V
Output Voltage Low	$V_{OL_{I2C}}$	$V_{DD} = 1.8 \text{ V}$ $I_O = 3 \text{ mA}$	—	—	$0.2 \times V_{DD}$	V
		$V_{DD} = 2.5 \text{ or } 3.3 \text{ V}$ $I_O = 3 \text{ mA}$	—	—	0.4	V

**Table 4. Microprocessor Control (Continued)**

( $V_{DD} = 1.8 \pm 5\%$ ,  $2.5 \pm 10\%$ , or  $3.3 V \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SPI Specifications</b>						
Duty Cycle, SCLK	$t_{DC}$	SCLK = 10 MHz	40	—	60	%
Cycle Time, SCLK	$t_c$		100	—	—	ns
Rise Time, SCLK	$t_r$	20–80%	—	—	25	ns
Fall Time, SCLK	$t_f$	20–80%	—	—	25	ns
Low Time, SCLK	$t_{lsc}$	20–20%	30	—	—	ns
High Time, SCLK	$t_{hsc}$	80–80%	30	—	—	ns
Delay Time, SCLK Fall to SDO Active	$t_{d1}$		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	$t_{d2}$		—	—	25	ns
Delay Time, SS Rise to SDO Tri-state	$t_{d3}$		—	—	25	ns
Setup Time, SS to SCLK Fall	$t_{su1}$		25	—	—	ns
Hold Time, SS to SCLK Rise	$t_{h1}$		20	—	—	ns
Setup Time, SDI to SCLK Rise	$t_{su2}$		25	—	—	ns
Hold Time, SDI to SCLK Rise	$t_{h2}$		20	—	—	ns
Delay Time between Slave Selects	$t_{cs}$		25	—	—	ns

Table 5. Jitter Generation

Parameter	Symbol	Test Condition*	Min	Typ	Max	Unit
		Measurement Filter				
Jitter Gen OC-192	JGEN	4–80 MHz	—	.23	—	ps <sub>rms</sub>
		0.05–80 MHz	—	.47	—	ps <sub>rms</sub>
Jitter Gen OC-48	JGEN	0.12–20 MHz	—	.48	—	ps <sub>rms</sub>

**\*Note:** Test conditions:

1.  $f_{IN} = f_{OUT} = 622.08$  MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 877 kHz
5. 114.285 MHz 3rd OT crystal used as XA/XB input
6.  $V_{DD} = 2.5$  V
7.  $T_A = 85$  °C

Table 6. Thermal Characteristics

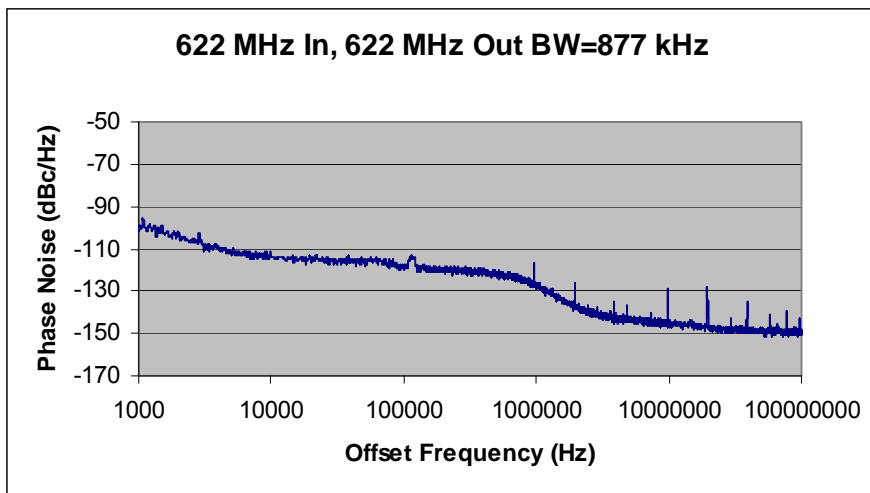
( $V_{DD} = 1.8 \pm 5\%$ ,  $2.5 \pm 10\%$ , or  $3.3$  V  $\pm 10\%$ ,  $T_A = -40$  to  $85$  °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still Air	40	C°/W

**Table 7. Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	-0.5 to 3.8	V
LVC MOS Input Voltage	$V_{DIG}$	-0.3 to ( $V_{DD} + 0.3$ )	V
CKINn Voltage Level Limits	$CKN_{VIN}$	0 to $V_{DD}$	V
XA/XB Voltage Level Limits	$XA_{VIN}$	0 to 1.2	V
Operating Junction Temperature	$T_{JCT}$	-55 to 150	C
Storage Temperature Range	$T_{STG}$	-55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN-		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN-		700	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN-		750	V
ESD MM Tolerance; CKIN+/CKIN-		100	V
Latch-Up Tolerance		JESD78 Compliant	

**Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

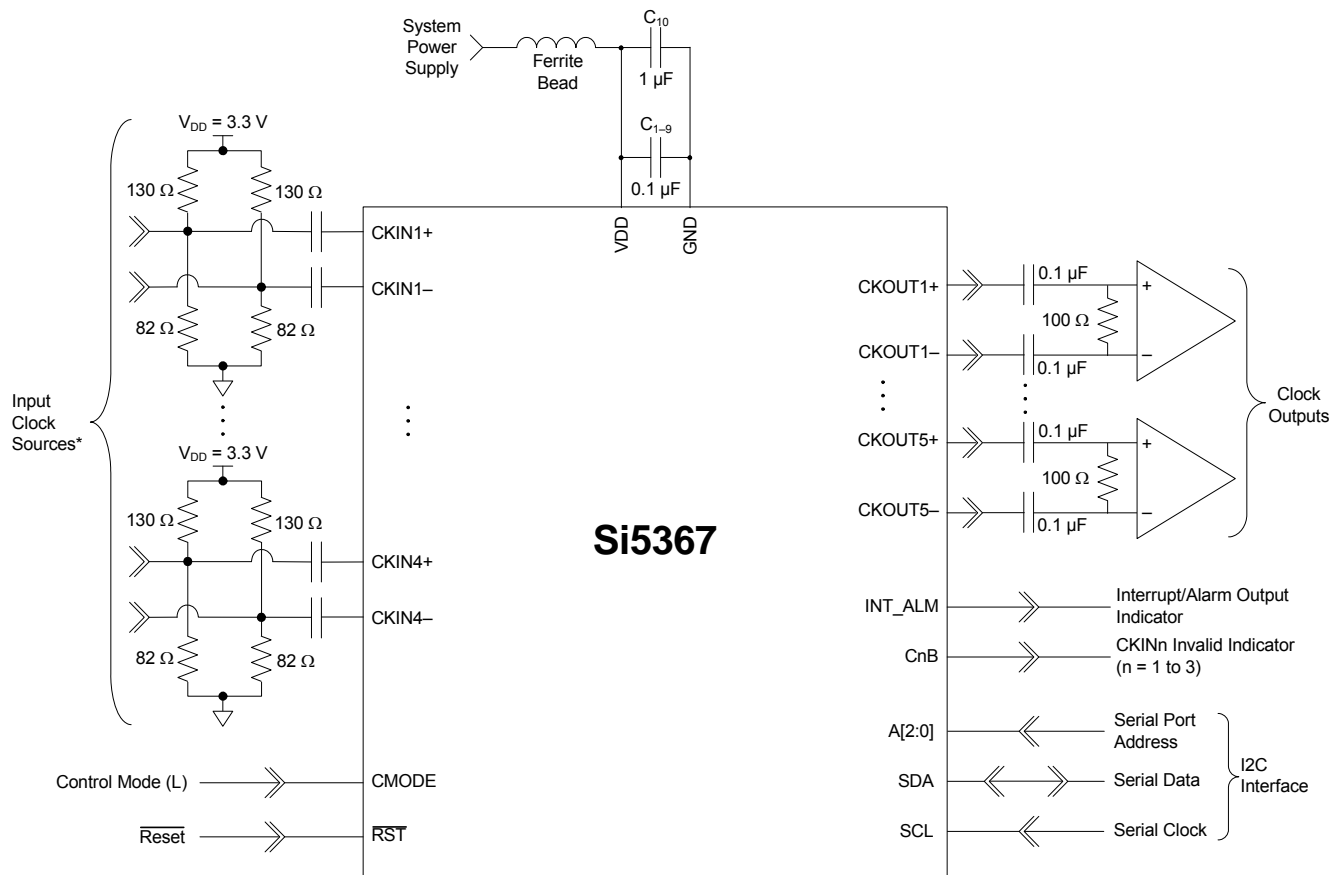


**Figure 3. Typical Phase Noise Plot**

**Table 8. Typical RMS Jitter Values**

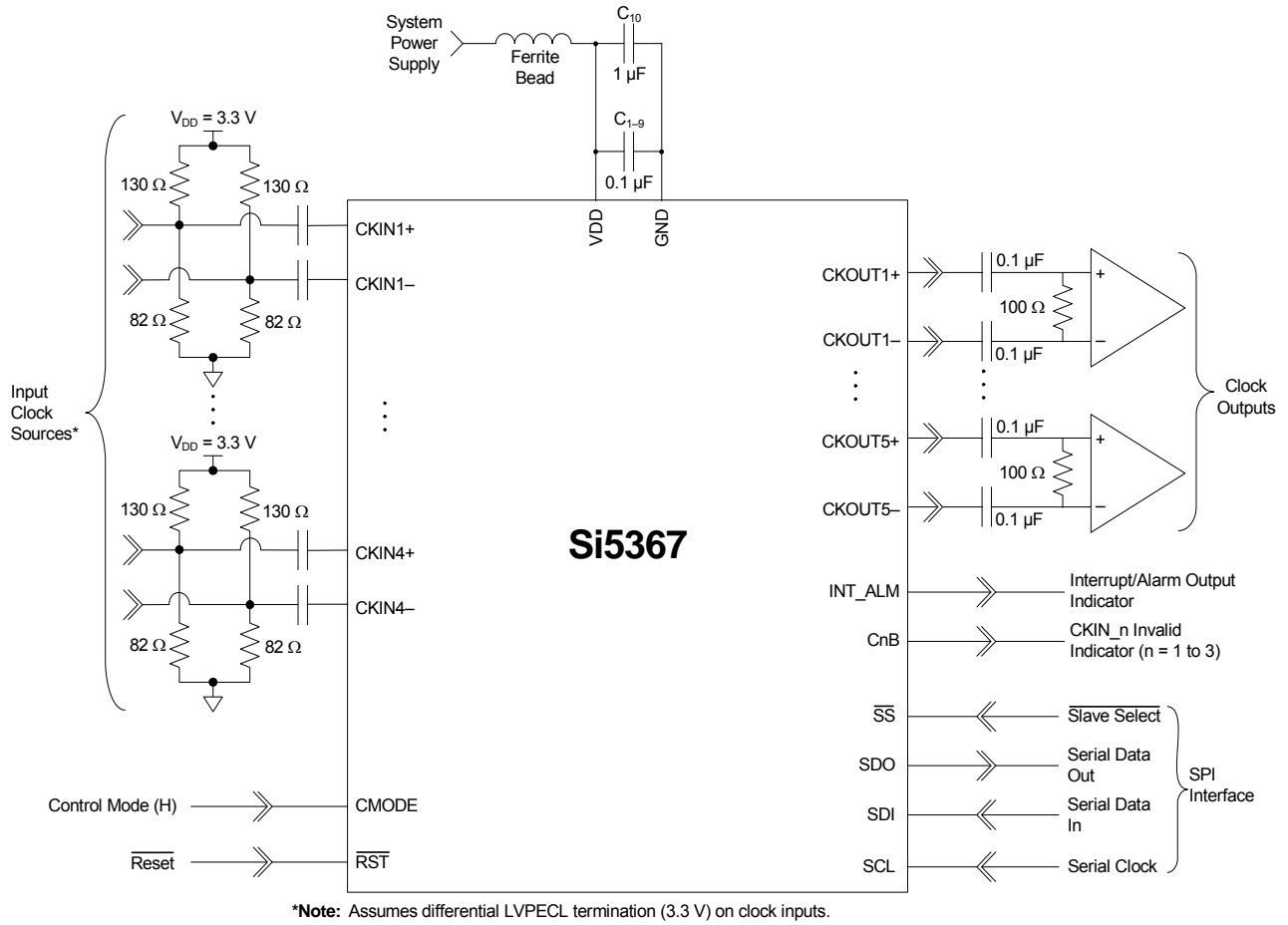
Jitter Bandwidth	RMS Jitter (fs)
OC-48, 12 kHz to 20 MHz	374
OC-192, 20 kHz to 80 MHz	388
OC-192, 4 MHz to 80 MHz	181
OC-192, 50 kHz to 80 MHz	377
Broadband, 800 Hz to 80 MHz	420

## 2. Typical Application Schematics



\*Note: Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 4. Si5367 Typical Application Circuit (I<sup>2</sup>C Control Mode)



**Figure 5. Si5367 Typical Application Circuit (SPI Control Mode)**

### 3. Functional Description

The Si5367 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5367 accepts four clock inputs ranging from 10 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides virtually any frequency translation combination across this operating range. Independent dividers are available for every input clock and output clock, so the Si5367 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5367 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface. Silicon Laboratories offers a PC-based software utility, *DSPLLsim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from <http://www.silabs.com/timing> (click on Documentation).

The Si5367 is based on Silicon Laboratories' 3rd-generation DSPLL<sup>®</sup> technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5367 PLL loop bandwidth is digitally programmable and supports a range from 150 kHz to 1.3 MHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5367 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on its inputs.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5367 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. In addition, the phase of each output clock may be adjusted in relation to the other output clocks. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the *DSPLLsim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8 or 2.5 V supply.

#### 3.1. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5367. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from <http://www.silabs.com/timing>; click on Documentation.

## 4. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0			CKOUT_ALWAYS_ON				BYPASS_REG	
1	CK_PRIOR4 [1:0]		CK_PRIOR3 [1:0]		CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
2	BWSEL_REG [3:0]							
3	CKSEL_REG [1:0]			SQ_ICAL				
4	AUTOSEL_REG [1:0]							
5	ICMOS [1:0]		SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
6			SFOUT4_REG [2:0]			SFOUT3_REG [2:0]		
7			SFOUT5_REG [2:0]			FOSREFSEL [2:0]		
8	HLOG_4 [1:0]		HLOG_3 [1:0]		HLOG_2 [1:0]		HLOG_1 [1:0]	
9							HLOG_5 [1:0]	
10			DSBL5_REG		DSBL4_REG	DSBL3_REG	DSBL2_REG	DSBL1_REG
11					PD_CK4	PD_CK3	PD_CK2	PD_CK1
19	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]				
20				CK3_BAD_PIN	CK2_BAD_PIN	CK1_BAD_PIN		INT_PIN
21				CK4_ACTV_PIN	CK3_ACTV_PIN	CK2_ACTV_PIN	CK1_ACTV_PIN	CKSEL_PIN
22					CK_ACTV_POL	CK_BAD_POL		INT_POL
23				LOS4_MSK	LOS3_MSK	LOS2_MSK	LOS1_MSK	
24				FOS4_MSK	FOS3_MSK	FOS2_MSK	FOS1_MSK	
25	N1_HS [2:0]				NC1_LS [19:16]			
26	NC1_LS [15:8]							
27	NC1_LS [7:0]							
28					NC2_LS [19:16]			
29	NC2_LS [15:8]							
30	NC2_LS [7:0]							
31					NC3_LS [19:16]			
32	NC3_LS [15:8]							
33	NC3_LS [7:0]							
34					NC4_LS [19:16]			
35	NC4_LS [15:8]							
36	NC4_LS [7:0]							
37					NC5_LS [19:16]			
38	NC5_LS [15:8]							

Register	D7	D6	D5	D4	D3	D2	D1	D0
39	NC5_LS [7:0]							
40	N2_LS [19:16]							
41	N2_LS [15:8]							
42	N2_LS [7:0]							
43	N31_ [18:16]							
44	N31_ [15:8]							
45	N31_ [7:0]							
46	N32_ [18:16]							
47	N31_ [15:8]							
48	N32_ [7:0]							
49	N33_ [18:16]							
50	N33_ [15:8]							
51	N33_ [7:0]							
52	N34_ [18:16]							
53	N34_ [15:8]							
54	N34_ [7:0]							
55	CLKIN2RATE_ [2:0]				CLKIN1RATE [2:0]			
56	CLKIN4RATE_ [2:0]				CLKIN3RATE [2:0]			
128					CK4_ACTV_REG	CK3_ACTV_REG	CK2_ACTV_REG	CK1_ACTV_REG
129	LOS4_INT				LOS3_INT	LOS2_INT	LOS1_INT	
130	FOS4_INT				FOS3_INT	FOS2_INT	FOS1_INT	
131	LOS4_FLG				LOS3_FLG	LOS2_FLG	LOS1_FLG	
132	FOS4_FLG			FOS3_FLG	FOS2_FLG	FOS1_FLG		
134	PARTNUM_RO [11:4]							
135	PARTNUM_RO [3:0]				REVID_RO [3:0]			
136	RST_REG	ICAL						
138					LOS4_EN [1:1]	LOS3_EN [1:1]	LOS2_EN [1:1]	LOS1_EN [1:1]
139	LOS4_EN [0:0]	LOS3_EN [0:0]	LOS2_EN [0:0]	LOS1_EN [0:0]	FOS4_EN	FOS3_EN	FOS2_EN	FOS1_EN
140	INDEPENDENTSKEW1 [7:0]							
141	INDEPENDENTSKEW2 [7:0]							
142	INDEPENDENTSKEW3 [7:0]							
143	INDEPENDENTSKEW4 [7:0]							
144	INDEPENDENTSKEW5 [7:0]							

## 5. Register Descriptions

### Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CKOUT_ALWAYS_ON				BYPASS_REG	
Type	R	R	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7:6	Reserved	
5	CKOUT_ALWAYS_ON	<p><b>CKOUT Always On.</b>            This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9.            0: Squelch output until part is calibrated (ICAL).            1: Provide an output. Note: The frequency may be significantly off until the part is calibrated.</p>
4:2	Reserved	
1	BYPASS_REG	<p><b>Bypass Register.</b>            This bit enables or disables the PLL bypass mode. Use is only valid when the part is in digital hold or before the first ICAL.            0: Normal operation            1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL. Bypass mode does not support CMOS clock outputs.</p>
0	Reserved	

**Register 1.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	CK_PRIOR4 [1:0]		CK_PRIOR3 [1:0]		CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
<b>Type</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 1110 0100

Bit	Name	Function
7:6	CK_PRIOR4 [1:0]	Selects which of the input clocks will be 4th priority in the autoselection state machine. 00: CKIN1 is 4th priority 01: CKIN2 is 4th priority 10: CKIN3 is 4th priority 11: CKIN4 is 4th priority
5:4	CK_PRIOR3 [1:0]	Selects which of the input clocks will be 3rd priority in the autoselection state machine. 00: CKIN1 is 3rd priority 01: CKIN2 is 3rd priority 10: CKIN3 is 3rd priority 11: CKIN4 is 3rd priority
3:2	CK_PRIOR2 [1:0]	<b>CK_PRIOR 2.</b> Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority 01: CKIN2 is 2nd priority 10: CKIN3 is 2nd priority 11: CKIN4 is 2nd priority
1:0	CK_PRIOR1 [1:0]	<b>CK_PRIOR 1.</b> Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority 01: CKIN2 is 1st priority 10: CKIN3 is 1st priority 11: CKIN4 is 1st priority

## Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]							
Type	R/W				R	R	R	R

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	<b>BWSEL_REG.</b> Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	

## Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CKSEL_REG [1:0]			SQ_ICAL				
Type	R/W		R	R/W	R	R	R	R

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	<b>CKSEL_REG.</b> If the device is operating in manual register-based clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1, the CKSEL[1:0] input pins continue to control clock selection and CKSEL_REG is of no consequence. 00: CKIN_1 selected. 01: CKIN_2 selected. 10: CKIN_3 selected. 11: CKIN_4 selected.
5	Reserved	
4	SQ_ICAL	<b>SQ_ICAL.</b> This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	

**Register 4.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	AUTOSEL_REG [1:0]							
<b>Type</b>	R/W		R	R	R	R	R	R

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_REG [1:0]	<b>AUTOSEL_REG [1:0].</b> Selects method of input clock selection to be used. 00: Manual (either register or pin controlled. See CKSEL_PIN). 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved
5:0	Reserved	

## Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	ICMOS [1:0]		SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
<b>Type</b>	R/W		R/W			R/W		

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	<p><b>ICMOS [1:0].</b>            When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-.</p> <p>00: 8 mA/2 mA            01: 16 mA/4 mA            10: 24 mA/6 mA            11: 32 mA (3.3 V operation)/8 mA (1.8 V operation)</p>
5:3	SFOUT2_REG [2:0]	<p><b>SFOUT2_REG [2:0].</b>            Controls output signal format and disable for CKOUT2 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved            001: Disable            010: CMOS (Bypass mode not supported.)            011: Low swing LVDS            100: Reserved            101: LVPECL            110: CML            111: LVDS</p>
2:0	SFOUT1_REG [2:0]	<p><b>SFOUT1_REG [2:0].</b>            Controls output signal format and disable for CKOUT1 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved            001: Disable            010: CMOS (Bypass mode not supported.)            011: Low swing LVDS            100: Reserved            101: LVPECL            110: CML            111: LVDS</p>

## Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>			SFOUT4_REG [2:0]			SFOUT3_REG [2:0]		
<b>Type</b>	R	R	R/W			R/W		

Reset value = 0010 1100

Bit	Name	Function
7:6	Reserved	
5:3	SFOUT4_REG [2:0]	<p><b>SFOUT4_REG [2:0].</b> Controls output signal format and disable for CKOUT4 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p>
2:0	SFOUT3_REG [2:0]	<p><b>SFOUT3_REG [2:0].</b> Controls output signal format and disable for CKOUT3 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved 001: Disable 010: CMOS (Bypass mode not supported.) 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS</p>

## Register 7.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			SFOUT5_REG [2:0]			FOSREFSEL [2:0]		
Type	R	R	R/W			R/W		

Reset value = 0010 1010

Bit	Name	Function
7:6	Reserved	
5:3	SFOUT5_REG [2:0]	<p><b>SFOUT5_REG [2:0]</b>            Controls output signal format and disable for CKOUT5 output buffer. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.</p> <p>000: Reserved            001: Disable            010: CMOS (Bypass mode not supported.)            011: Low swing LVDS            100: Reserved            101: LVPECL            110: CML            111: LVDS</p>
2:0	FOSREFSEL [2:0]	<p><b>FOSREFSEL [2:0].</b>            Selects which input clock is used as the reference frequency for Frequency Off-Set (FOS) alarms.</p> <p>000: XA/XB (External reference)            001: CKIN1            010: CKIN2            011: CKIN3            100: CKIN4            101: Reserved            110: Reserved            111: Reserved</p>

## Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HLOG_4[1:0]		HLOG_3[1:0]		HLOG_2[1:0]		HLOG_1[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_4 [1:0]	<p><b>HLOG_4 [1:0].</b>            00: Normal operation            01: Holds CKOUT4 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.            10: Holds CKOUT4 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.            11: Reserved</p>
5:4	HLOG_3 [1:0]	<p><b>HLOG_3 [1:0].</b>            00: Normal operation            01: Holds CKOUT3 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.            10: Holds CKOUT3 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.            11: Reserved.</p>
3:2	HLOG_2 [1:0]	<p><b>HLOG_2 [1:0].</b>            00: Normal operation            01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.            10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.            11: Reserved.</p>
1:0	HLOG_1 [1:0]	<p><b>HLOG_1 [1:0].</b>            00: Normal operation            01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.            10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.            11: Reserved</p>

---

**Register 9.**

---

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							HLOG_5 [1:0]	
Type	R	R	R	R	R	R	R/W	

Reset value = 1100 0000

Bit	Name	Function
7:2	Reserved	
1:0	HLOG_5 [1:0]	<b>HLOG_5 [1:0].</b> 00: Normal Operation 01: Holds CKOUT5 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT5 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved

## Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			DSBL5_REG		DSBL4_REG	DSBL3_REG	DSBL2_REG	DSBL1_REG
Type	R	R	R/W	R	R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5	DSBL5_REG	<b>DSBL5_REG.</b> This bit controls the powerdown and disable of the CKOUT5 output buffer. If disable mode is selected, the NC5_LS output divider is also powered down. 0: CKOUT5 enabled. 1: CKOUT5 disabled.
4	Reserved	
3	DSBL4_REG	<b>DSBL4_REG.</b> This bit controls the powerdown and disable of the CKOUT4 output buffer. If disable mode is selected, the NC4 output divider is also powered down. 0 = CKOUT4 enabled 1 = CKOUT4 disabled
2	DSBL3_REG	<b>DSBL3_REG.</b> This bit controls the powerdown and disable of the CKOUT3 output buffer. If disable mode is selected, the NC3 output divider is also powered down. 0: CKOUT3 enabled 1: CKOUT3 disabled
1	DSBL2_REG	<b>DSBL2_REG.</b> This bit controls the powerdown and disable of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
0	DSBL1_REG	<b>DSBL1_REG.</b> This bit controls the powerdown and disable of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled

## Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					PD_CK4	PD_CK3	PD_CK2	PD_CK1
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:4	Reserved	
3	PD_CK4	<b>PD_CK4.</b> This bit controls the powerdown of the CKIN4 input buffer. 0: CKIN4 enabled 1: CKIN4 disabled
2	PD_CK3	<b>PD_CK3.</b> This bit controls the powerdown of the CKIN3 input buffer. 0: CKIN3 enabled 1: CKIN3 disabled
1	PD_CK2	<b>PD_CK2.</b> This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	<b>PD_CK1.</b> This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

**Register 19.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]				
<b>Type</b>	R/W	R/W		R/W		R	R	R

Reset value = 0010 1100

Bit	Name	Function
7	FOS_EN	<b>FOS_EN.</b> Frequency offset enable globally disables FOS. See the individual FOS enables (FOS-x_EN, register 139). 00: FOS disable 01: FOS enabled by FOSx_EN
6:5	FOS_THR [1:0]	<b>FOS_THR [1:0].</b> Frequency Offset at which FOS is declared: 00: $\pm 11$ to 12 ppm Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK. 01: $\pm 48$ to 49 ppm (SMC). 10: $\pm 30$ ppm SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK. 11: $\pm 200$ ppm
4:3	VALTIME [1:0]	<b>VALTIME [1:0].</b> Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 s
2:0	Reserved	

## Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CK3_BAD_PIN	CK2_BAD_PIN	CK1_BAD_PIN		INT_PIN
Type	R	R	R	R/W	R/W	R/W	R	R/W

Reset value = 0011 1100

Bit	Name	Function
7:5	Reserved	
4	CK3_BAD_PIN	<b>CK3_BAD_PIN.</b> The CK3_BAD status can be reflected on the C3B output pin. 0: C3B output pin tristated 1: C3B status reflected to output pin
3	CK2_BAD_PIN	<b>CK2_BAD_PIN.</b> The CK2_BAD status can be reflected on the C2B output pin. 0: C2B output pin tristated 1: C2B status reflected to output pin
2	CK1_BAD_PIN	<b>CK1_BAD_PIN.</b> The CK1_BAD status can be reflected on the C1B output pin. 0: C1B output pin tristated 1: C1B status reflected to output pin
1	Reserved	
0	INT_PIN	<b>INT_PIN.</b> Reflects the interrupt status on the INT output pin. 0: Interrupt status not displayed on INT output pin. If ALRMOUT_PIN = 0, output pin is tristated. 1: Interrupt status reflected to output pin. ALRMOUT_PIN ignored.

**Register 21.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CK4_ACTV_PIN*	CK3_ACTV_PIN*	CK2_ACTV_PIN*	CK1_ACTV_PIN*	CKSEL_PIN*
Type	R	Force 1	R	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:5	Reserved	
4	CK4_ACTV_PIN	<p><b>CK4_ACTV_PIN.</b></p> <p>If the CKSEL[1]/CK4_ACTV pin is functioning as the CK4_ACTV output (see CKSEL[1]/CK4_ACTV pin description on CK4_ACTV), the CK4_ACTV_REG status bit can be reflected to the CK4_ACTV output pin using the CK4_ACTV_PIN enable function.</p> <p>0: CK4_ACTV output pin tristated 1: CK4_ACTV status reflected to output pin.</p>
3	CK3_ACTV_PIN	<p><b>CK3_ACTV_PIN.</b></p> <p>If the CKSEL[0]/CK3_ACTV pin is functioning as the CK3_ACTV output (see CKSEL[0]/CK3_ACTV pin description on CK3_ACTV), the CK3_ACTV_REG status bit can be reflected to the CK3_ACTV output pin using the CK3_ACTV_PIN enable function.</p> <p>0: CK3_ACTV output pin tristated. 1: CK3_ACTV status reflected to output pin.</p>
2	CK2_ACTV_PIN	<p><b>CK2_ACTV_PIN.</b></p> <p>The CK2_ACTV_REG status bit can be reflected to the CK2_ACTV output pin using the CK2_ACTV_PIN enable function.</p> <p>0: CK2_ACTV output pin tristated. 1: CK2_ACTV status reflected to output pin.</p>
1	CK1_ACTV_PIN	<p><b>CK1_ACTV_PIN.</b></p> <p>The CK1_ACTV_REG status bit can be reflected to the CK1_ACTV output pin using the CK1_ACTV_PIN enable function.</p> <p>0: CK1_ACTV output pin tristated. 1: CK1_ACTV status reflected to output pin.</p>
0	CKSEL_PIN	<p><b>CKSEL_PIN.</b></p> <p>If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CKSEL[1:0] input pins.</p> <p>0: CKSEL pins ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CKSEL[1:0] input pins controls clock selection.</p>
<p><b>*Note:</b> The CKx_ACTV_PIN bits in this register are of consequence only when CKSEL_PIN is 0.</p>		

## Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FSYNCOU_T_POL	CK_ACTV_POL	CK_BAD_POL		INT_POL
Type	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:5	Reserved	
4	FSYNCOU_T_POL	<b>FSYNCOU_T_POL.</b> Controls active polarity of FSYNCOU_T. 0: Active low 1: Active high
3	CK_ACTV_POL	<b>CK_ACTV_POL.</b> Sets the active polarity for the CK1_ACTV, CK2_ACTV, CK3_ACTV, and CK4_ACTV signals when reflected on an output pin. 0: Active low 1: Active high
2	CK_BAD_POL	<b>CK_BAD_POL.</b> Sets the active polarity for the C1B, C2B, C3B, and ALRMOUT signals when reflected on output pins. 0: Active low 1: Active high
1	Reserved	
0	INT_POL	<b>INT_POL.</b> Sets the active polarity for the interrupt status when reflected on the INT_ALM output pin. 0: Active low 1: Active high

**Register 23.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_MSK	LOS3_MSK	LOS2_MSK	LOS1_MSK	
Type	R	R	R	R/W	R/W	R/W	R/W	R

Reset value = 0001 1111

Bit	Name	Function
7:5	Reserved	
4	LOS4_MSK	<b>LOS4_MSK.</b> Determines if a LOS on CKIN4 (LOS4_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS4_FLG register. 0: LOS4 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS4_FLG ignored in generating interrupt output.
3	LOS3_MSK	<b>LOS3_MSK.</b> Determines if a LOS on CKIN3 (LOS3_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS3_FLG register. 0: LOS3 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS3_FLG ignored in generating interrupt output.
2	LOS2_MSK	<b>LOS2_MSK.</b> Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	<b>LOS1_MSK.</b> Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.
0	Reserved	

## Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FOS4_MSK	FOS3_MSK	FOS2_MSK	FOS1_MSK	
Type	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value = 0011 1111

Bit	Name	Function
7:5	Reserved	
4	FOS4_MSK	<p><b>FOS4_MSK.</b> Determines if the FOS4_FLG is used to in the generation of an interrupt. Writes to this register do not change the value held in the FOS4_FLG register. 0: FOS4 alarm triggers active interrupt on INToutput (if INT_PIN=1). 1: FOS4_FLG ignored in generating interrupt output.</p>
3	FOS3_MSK	<p><b>FOS3_MSK.</b> Determines if the FOS3_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS3_FLG register. 0: FOS3 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: FOS3_FLG ignored in generating interrupt output.</p>
2	FOS2_MSK	<p><b>FOS2_MSK.</b> Determines if the FOS2_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register. 0: FOS2 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: FOS2_FLG ignored in generating interrupt output.</p>
1	FOS1_MSK	<p><b>FOS1_MSK.</b> Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register. 0: FOS1 alarm triggers active interrupt on INT output (if INT_PIN=1). 1: FOS1_FLG ignored in generating interrupt output.</p>
0	Reserved	

**Register 25.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N1_HS [2:0]				NC1_LS [19:16]			
<b>Type</b>	R/W			R	R/W			

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	<p><b>N1_HS [2:0].</b> Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 4) low-speed divider. 000: N1 = 4 Note: Changing the coarse skew via the INC pin is disabled for this value. 001: N1 = 5 010: N1 = 6 011: N1 = 7 100: N1 = 8 101: N1 = 9 110: N1 = 10 111: N1 = 11</p>
4	Reserved	
3:0	NC1_LS [19:16]	<p><b>NC1_LS [19:16].</b> Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2<sup>20</sup> Valid divider values=[1, 2, 4, 6, ..., 2<sup>20</sup>].</p>

**Register 26.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC1_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	<p><b>NC1_LS [15:8].</b> See Register 25.</p>

## Register 27.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [7:0]	<b>NC1_LS [7:0].</b> See Register 25.

## Register 28.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC2_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC1_LS [19:16]	<b>NC2_LS [19:16].</b> Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = $2^{20}$ Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ]

**Register 29.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC2_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	<b>NC2_LS [15:8].</b> See Register 28.

**Register 30.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC2_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	<b>NC2_LS [7:0].</b> See Register 28.

## Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					NC3_LS [19:16]			
Type	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC3_LS [19:16]	<p><b>NC3_LS [19:16].</b>  Sets value for NC3 low-speed divider, which drives CKOUT3 output. Must be 0 or odd.  00000000000000000000 = 1  00000000000000000001 = 2  00000000000000000011 = 4  00000000000000000101 = 6  ...  11111111111111111111 = <math>2^{20}</math>  Valid divider values = [1, 2, 4, 6, ..., <math>2^{20}</math>].</p>

## Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC3_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC3_LS [15:8]	<p><b>NC3_LS [15:8].</b>  See Register 31.</p>

**Register 33.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC3_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC3_LS [7:0]	<b>NC3_LS [7:0].</b> See Register 31.

**Register 34.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>					NC4_LS [19:16]			
<b>Type</b>	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC4_LS [19:16]	<b>NC4_LS [19:16].</b> Sets value for NC4 low-speed divider, which drives CKOUT4 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = $2^{20}$ Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ].

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**Register 35.**

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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC4_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC4_LS [15:8]	<b>NC4_LS [15:8].</b> See Register 34.

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**Register 36.**

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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC4_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC4_LS [7:0]	<b>NC4_LS [7:0].</b> See Register 34.

**Register 37.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>					NC5_LS [19:16]			
<b>Type</b>	R	R	R	R	R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	NC5_LS [19:16]	<p><b>NC5_LS [19:16].</b> Sets value for NC5 low-speed divider, which drives CKOUT5 output. Must be 0 or odd. When CK_CONFIG = 0: 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111 = 2<sup>20</sup></p> <p>Valid divider values = [1, 2, 4, 6, ..., 2<sup>20</sup>]. When CK_CONFIG = 1, maximum value limited to 2<sup>19</sup>.: 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 01111111111111111111 = 2<sup>19</sup> Valid divider values = [1, 2, 4, 6, ..., 2<sup>19</sup>].</p>

**Register 38.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC5_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC5_LS [15:8]	<p><b>NC5_LS [15:8].</b> See Register 37.</p>

## Register 39.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	NC5_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC5_LS [7:0]	<b>NC5_LS [7:0].</b> See Register 37.

## Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>					N2_LS [19:16]			
<b>Type</b>	R	R	R	R	R/W			

Reset value = 1100 0000

Bit	Name	Function
7:4	Reserved	
3:0	N2_LS [19:16]	<b>NC2_LS [19:0].</b> Sets value for N2 low-speed divider, which drives phase detector. 000000000000000100000 = 2 0000000000000001000010 = 4 0000000000000001000100 = 6 ... 00000000001000000000 = 512 Valid divider values = [32,34,36, ...512].

**Register 41.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N2_LS [15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	<b>N2_LS [15:8].</b> See Register 40.

**Register 42.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N2_LS [7:0]							
<b>Type</b>	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	<b>N2_LS [7:0].</b> See Register 40.

## Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N31 [18:16]		
Type	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N31 [18:16]	<b>N31 [18:0].</b> Sets value for input divider for CKIN1. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values = [1, 2, 3, ..., $2^{19}$ ].

## Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31 [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31 [15:8]	<b>N31 [15:8].</b> See Register 43.

**Register 45.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N31 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31 [7:0]	<b>N31 [7:0].</b> See Register 43.

**Register 46.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>						N32_[18:16]		
<b>Type</b>	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N32_[18:16]	<b>N32_[18:0].</b> Sets value for input divider for CKIN2. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = 2 <sup>19</sup> Valid divider values=[1, 2, 3, ..., 2 <sup>19</sup> ].

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**Register 47.**

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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	<b>N32_[15:8].</b> See Register 46.

---

**Register 48.**

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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	<b>N32_[7:0].</b> See Register 46.

**Register 49.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N33_[18:16]							
<b>Type</b>	R	R	R	R	R		R/W	

Reset value = 0000 0000

Bit	Name	Function
18:0	N33_[18:16]	<b>N33_[18:16].</b> Sets value for input divider for CKIN3. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = $2^{19}$ Valid divider values=[1, 2, 3, ..., $2^{19}$ ]

**Register 50.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N33_[15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N33_[15:8]	<b>N33_[15:8].</b> See Register 49.

## Register 51.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N33_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N33_[7:0]	<b>N33_[7:0].</b> See Register 49.

## Register 52.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							N34_[18:16]	
Type	R	R	R	R	R		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:0	N34_[18:16]	<b>N34_[18:0].</b> Sets value for input divider for CKIN4. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000010 = 3 ... 11111111111111111111 = 2 <sup>19</sup> Valid divider values = [1, 2, 3, ..., 2 <sup>19</sup> ].

**Register 53.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N34_[15:8]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N34_[15:8]	<b>N34_[15:8].</b> See Register 52.

**Register 54.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	N34_[7:0]							
<b>Type</b>	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N34_[15:8]	<b>N34_[7:0].</b> See Register 52.

## Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLKIN2RATE_[5:3]			CLKIN1RATE[2:0]		
Type	R	R	R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5:3	CLKIN2RATE[5:3]	<b>CLKIN2RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved
2:0	CLKIN1RATE [2:0]	<b>CLKIN1RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved

## Register 56.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLKIN4RATE_[5:3]			CLKIN3RATE[2:0]		
Type	R	R	R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	
5:3	CLKIN4RATE[5:3]	<b>CLKIN4RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved
2:0	CLKIN3RATE [2:0]	<b>CLKIN3RATE[2:0].</b> CKINn frequency selection for FOS alarm monitoring. 000: 10–27 MHz 001: 25–54 MHz 002: 50–105 MHz 003: 95–215 MHz 004: 190–435 MHz 005: 375–710 MHz 006: Reserved 007: Reserved

## Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CK4_ACTV_REG	CK3_ACTV_REG	CK2_ACTV_REG	CK1_ACTV_REG
Type	R	R	R	R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:4	Reserved	
3	CK4_ACTV_REG	<b>CK4_ACTV_REG.</b> Indicates if CKIN4 is currently the active clock for the PLL input. 0: CKIN4 is not the active input clock. Either it is not selected or LOS4_INT is 1. 1: CKIN_4 is the active input clock.
2	CK3_ACTV_REG	<b>CK3_ACTV_REG.</b> Indicates if CKIN3 is currently the active clock for the PLL input. 0: CKIN3 is not the active input clock - either it is not selected or LOS3_INT is 1. 1: CKIN3 is the active input clock.
1	CK2_ACTV_REG	<b>CK2_ACTV_REG.</b> Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	<b>CK1_ACTV_REG.</b> Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.

## Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_INT	LOS3_INT	LOS2_INT	LOS1_INT	
Type	R	R	R	R	R	R	R	R

Reset value = 0001 1110

Bit	Name	Function
7:5	Reserved	
4	LOS4_INT	<b>LOS4_INT.</b> Indicates the LOS status on CKIN4. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN4 input.
3	LOS3_INT	<b>LOS3_INT.</b> Indicates the LOS status on CKIN3. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN3 input.
2	LOS2_INT	<b>LOS2_INT.</b> Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	<b>LOS1_INT.</b> Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	Reserved	

## Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FOS4_INT	FOS3_INT	FOS2_INT	FOS1_INT	
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0001

Bit	Name	Function
7:5	Reserved	
4	FOS4_INT	<b>FOS4_INT.</b> CKIN4 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN4 input.
3	FOS3_INT	<b>FOS3_INT.</b> CKIN3 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN3 input.
2	FOS2_INT	<b>FOS2_INT.</b> CKIN2 Frequency Offset Status. 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input.
1	FOS1_INT	<b>FOS1_INT.</b> <b>CKIN1 Frequency Offset Status.</b> 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input.
0	Reserved	

## Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS4_FLG	LOS3_FLG	LOS2_FLG	LOS1_FLG	
Type	R	R	R	R/W	R/W	R/W	R/W	R

Reset value = 0001 1111

Bit	Name	Function
7:5	Reserved	
4	LOS4_FLG	<p><b>LOS4_FLG.</b> CKIN4 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by LOS4_MSK bit. Flag cleared by writing location to 0.</p>
3	LOS3_FLG	<p><b>LOS3_FLG.</b> CKIN3 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS3_MSK bit. Flag cleared by writing location to 0.</p>
2	LOS2_FLG	<p><b>LOS2_FLG.</b> CKIN2 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing location to 0.</p>
1	LOS1_FLG	<p><b>LOS1_FLG.</b> CKIN1 Loss-of-Signal Flag. 0: Normal operation. 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing location to 0.</p>
0	Reserved	

## Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			FOS4_FLG	FOS3_FLG	FOS2_FLG	FOS1_FLG		
Type	R	R	R/W	R/W	R/W	R/W	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:6	Reserved	
5	FOS4_FLG	<p><b>FOS4_FLG.</b> CLKIN_4 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS4_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS4_MSK bit. Flag cleared by writing location to 0.</p>
4	FOS3_FLG	<p><b>FOS3_FLG.</b> CLKIN_3 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS3_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN=1) and if not masked by FOS3_MSK bit. Flag cleared by writing location to 0.</p>
3	FOS2_FLG	<p><b>FOS2_FLG.</b> CLKIN_2 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing location to 0.</p>
2	FOS1_FLG	<p><b>FOS1_FLG.</b> CLKIN_1 Frequency Offset Flag. 0: Normal operation. 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing location to 0.</p>
1:0	Reserved	

**Register 134.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	PARTNUM_RO [11:4]							
<b>Type</b>	R							

Reset value = 0000 0100

Bit	Name	Function
7:0	PARTNUM_RO [11:4]	<b>PARTNUM_RO [11:4].</b> Device ID: 0000 0100 0011'b = Si5367

**Register 135.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	PARTNUM_RO [3:0]				REVID_RO [3:0]			
<b>Type</b>	R				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	PARTNUM_RO [7:4]	<b>PARTNUM_RO [3:0].</b> See Register 134.
3:0	REVID_RO [3:0]	<b>REVID_RO [3:0].</b> Indicates revision number of device. 0000: Revision A 0001: Revision B 0010: Revision C Other codes: Reserved

## Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL						
Type	R/W	R/W	R	R	R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	<p><b>RST_REG.</b> Internal Reset. 0: Normal operation. 1: Reset of all internal logic. Outputs tristated or disabled during reset.</p>
6	ICAL	<p><b>ICAL.</b> Start an Internal Calibration Sequence. For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. <b>Note:</b> Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. Changes in SFOUTn_REG, PD_CKn, or DSBLn_REG will cause a random change in skew until an ICAL is completed. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, ICAL is internally reset to zero.</p>
5:0	Reserved	

## Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					LOS4_EN[1:1]	LOS3_EN[1:1]	LOS2_EN[1:1]	LOS1_EN [1:1]
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:4	Reserved	
3	LOS4_EN [1:0]	<p><b>LOS4_EN [1:0].</b>  <b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring.            01: Reserved.            10: Enable LOSA monitoring.            11: Enable LOS monitoring.            LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p>
2	LOS3_EN [1:0]	<p><b>LOS3_EN [1:0].</b>  <b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring.            01: Reserved.            10: Enable LOSA monitoring.            11: Enable LOS monitoring.            LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p>
1	LOS2_EN [1:0]	<p><b>LOS2_EN [1:0].</b>  <b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring.            01: Reserved.            10: Enable LOSA monitoring.            11: Enable LOS monitoring.            LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p>
0	LOS1_EN [1:0]	<p><b>LOS1_EN [1:0].</b>  <b>Note:</b> LOS1_EN is split between two registers.            00: Disable LOS monitoring.            01: Reserved.            10: Enable LOSA monitoring.            11: Enable LOS monitoring.            LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.</p>

## Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	LOS4_EN [0:0]	LOS3_EN [0:0]	LOS2_EN [0:0]	LOS1_EN [0:0]	FOS4_EN	FOS3_EN	FOS2_EN	FOS1_EN
<b>Type</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7	LOS4_EN [0:0]	<p><b>LOS4_EN [0:0].</b>  <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b>  <b>Note:</b> LOS1_EN is split between two registers.                      00: Disable LOS monitoring.                      01: Reserved.                      10: Enable LOSA monitoring.                      11: Enable LOS monitoring.                      LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p>
6	LOS3_EN [0:0]	<p><b>LOS3_EN [0:0].</b>  <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b>  <b>Note:</b> LOS1_EN is split between two registers.                      00: Disable LOS monitoring.                      01: Reserved.                      10: Enable LOSA monitoring.                      11: Enable LOS monitoring.                      LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p>
5	LOS2_EN [0:0]	<p><b>LOS2_EN.</b>  <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b>  <b>Note:</b> LOS1_EN is split between two registers.                      00: Disable LOS monitoring.                      01: Reserved.                      10: Enable LOSA monitoring.                      11: Enable LOS monitoring.                      LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p>
4	LOS1_EN [0:0]	<p><b>LOS1_EN [0:0].</b>  <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b>  <b>Note:</b> LOS1_EN is split between two registers.                      00: Disable LOS monitoring.                      01: Reserved.                      10: Enable LOSA monitoring.                      11: Enable LOS monitoring.                      LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.</p>

Bit	Name	Function
3	FOS4_EN	<b>FOS4_EN.</b> <b>Enables FOS on a Per Channel Basis.</b> 0: Disable FOS monitoring. 1: Enable FOS monitoring.
2	FOS3_EN	<b>FOS3_EN.</b> <b>Enables FOS on a Per Channel Basis.</b> 0: Disable FOS monitoring. 1: Enable FOS monitoring.
1	FOS2_EN	<b>FOS2_EN.</b> <b>Enables FOS on a Per Channel Basis.</b> 0: Disable FOS monitoring. 1: Enable FOS monitoring.
0	FOS1_EN	<b>FOS1_EN.</b> <b>Enables FOS on a Per Channel Basis.</b> 0: Disable FOS monitoring. 1: Enable FOS monitoring.

**Register 140.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW1 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW1 [7:0]	<b>INDEPENDENTSKEW1 [7:0].</b> 8-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider.

## Register 141.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW2 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	INDEPEND-ENTSKEW2 [7:0]	<b>INDEPENDENTSKEW2 [7:0].</b> 8-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider.

## Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW3 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW3 [7:0]	<b>INDEPENDENTSKEW3 [7:0].</b> 8-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider.

## Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW4 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW4 [7:0]	<b>INDEPENDENTSKEW4 [7:0].</b> 8-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider.

**Register 144.**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	INDEPENDENTSKEW5 [7:0]							
<b>Type</b>	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW5 [7:0]	<b>INDEPENDENTSKEW5 [7:0].</b> 8-bit field that represents a 2s complement of the phase offset in terms of clocks from the high speed output divider when CK_CONFIG = 0.

**Table 9. CKOUT\_ALWAYS\_ON and SQICAL Truth Table**

CKOUT_ALWAYS_ON	SQICAL	Results	Output to Output Skew Preserved?
0	0	CKOUT OFF until after the first ICAL	N
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)	Y
1	0	CKOUT always ON, including during an ICAL	N
1	1	CKOUT always ON, including during an ICAL	Y

Table 10 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 10. Register Locations Requiring ICAL

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
1	CK_PRIOR4
1	CK_PRIOR3
1	CK_PRIOR2
1	CK_PRIOR1
2	BWSEL_REG
5	ICMOS
7	FOSREFSEL
10	DSBL5_REG
10	DSBL4_REG
10	DSBL3_REG
10	DSBL2_REG
10	DSBL1_REG
11	PD_CK2
11	PD_CK1
19	FOS_EN
19	FOS_THR
19	VALTIME
25	N1_HS
26	NC1_LS
28	NC2_LS
31	NC3_LS
34	NC4_LS
37	NC5_LS
40	N2_HS
40	N2_LS
43	N31
46	N32
49	N33
51	N34
55	CLKIN2RATE
55	CLKIN1RATE
56	CLKIN4RATE
56	CLKIN3RATE

## 6. Pin Descriptions: Si5367

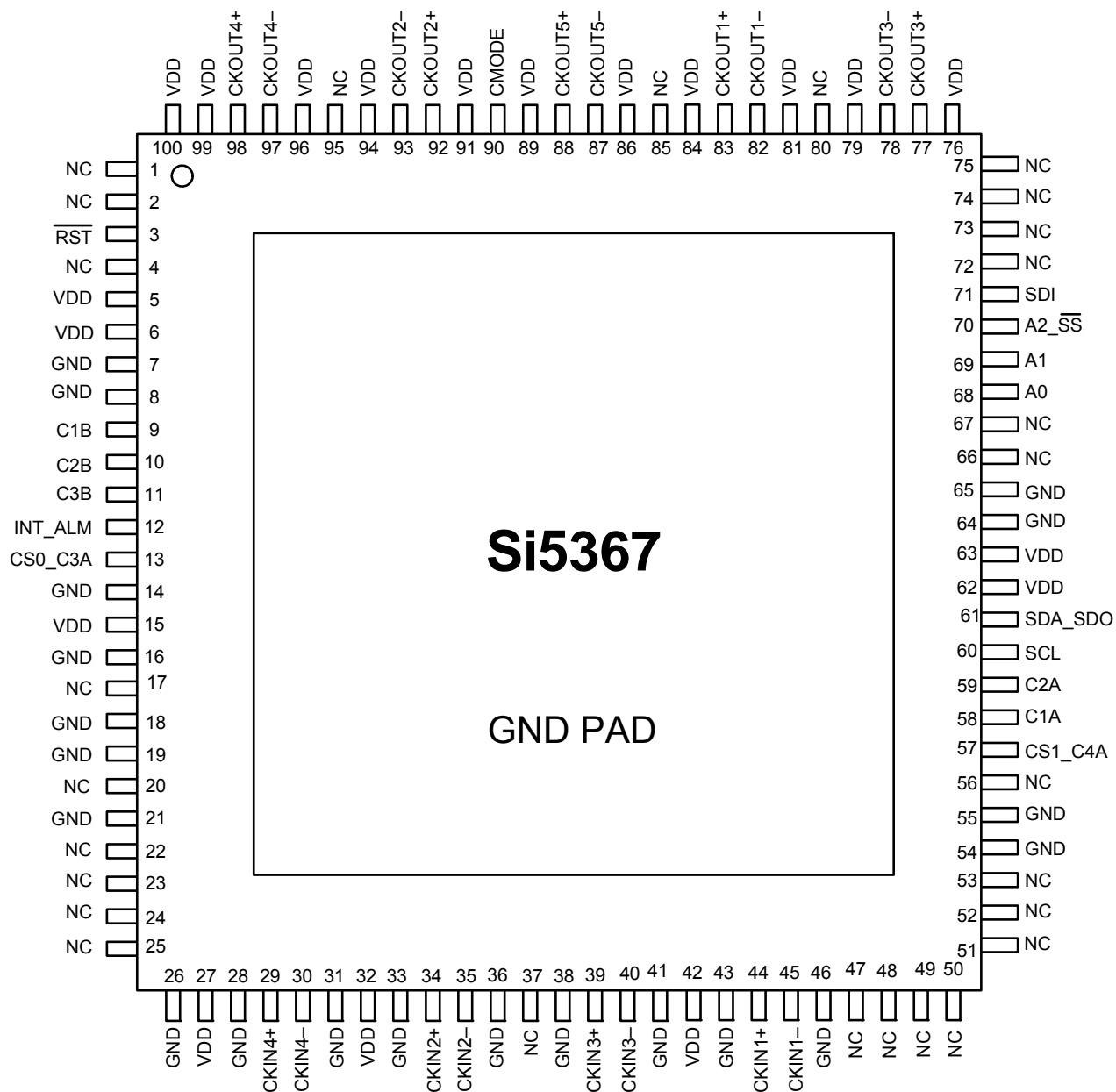


Table 11. Si5367 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description																				
1, 2, 4, 17, 20, 22, 23, 24, 25, 37, 47, 48, 49, 50, 51, 52, 53, 56, 66, 67, 72, 73, 74, 75, 80, 85, 95	NC			<b>No Connect.</b> These pins must be left unconnected for normal operation.																				
3	$\overline{\text{RST}}$	I	LVC MOS	<b>External Reset.</b> Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up.																				
5, 6, 15, 27, 32, 42, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V <sub>DD</sub>	Vdd	Supply	<b>V<sub>DD</sub>.</b> The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V <sub>DD</sub> pins: <table border="0"> <tr> <td>Pins</td> <td>Bypass Cap</td> </tr> <tr> <td>5, 6</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>15</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>27</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>62, 63</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>76, 79</td> <td>1.0 <math>\mu\text{F}</math></td> </tr> <tr> <td>81, 84</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>86, 89</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>91, 94</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> <tr> <td>96, 99, 100</td> <td>0.1 <math>\mu\text{F}</math></td> </tr> </table>	Pins	Bypass Cap	5, 6	0.1 $\mu\text{F}$	15	0.1 $\mu\text{F}$	27	0.1 $\mu\text{F}$	62, 63	0.1 $\mu\text{F}$	76, 79	1.0 $\mu\text{F}$	81, 84	0.1 $\mu\text{F}$	86, 89	0.1 $\mu\text{F}$	91, 94	0.1 $\mu\text{F}$	96, 99, 100	0.1 $\mu\text{F}$
Pins	Bypass Cap																							
5, 6	0.1 $\mu\text{F}$																							
15	0.1 $\mu\text{F}$																							
27	0.1 $\mu\text{F}$																							
62, 63	0.1 $\mu\text{F}$																							
76, 79	1.0 $\mu\text{F}$																							
81, 84	0.1 $\mu\text{F}$																							
86, 89	0.1 $\mu\text{F}$																							
91, 94	0.1 $\mu\text{F}$																							
96, 99, 100	0.1 $\mu\text{F}$																							
7, 8, 14, 16, 18, 19, 21, 26, 28, 31, 33, 36, 38, 41, 43, 46, 54, 55, 64, 65	GND	GND	Supply	<b>Ground.</b> This pin must be connected to system ground. Minimize the ground path impedance for optimal performance.																				
9	C1B	O	LVC MOS	<b>CKIN1 Invalid Indicator.</b> This pin performs the <u>CK1_BAD</u> function if <u>CK1_BAD_PIN</u> = 1 and is tristated if <u>CK1_BAD_PIN</u> = 0. Active polarity is controlled by <u>CK_BAD_POL</u> . 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.																				
10	C2B	O	LVC MOS	<b>CKIN2 Invalid Indicator.</b> This pin performs the <u>CK2_BAD</u> function if <u>CK2_BAD_PIN</u> = 1 and is tristated if <u>CK2_BAD_PIN</u> = 0. Active polarity is controlled by <u>CK_BAD_POL</u> . 0 = No alarm on CKIN2. 1 = Alarm on CKIN2.																				

**Note:** Internal register names are indicated by underlined italics, e.g. INT\_PIN. See Si5368 Register Map.

Table 11. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description										
11	C3B	O	LVC MOS	<p><b>CKIN3 Invalid Indicator.</b> This pin performs the <u>CK3_BAD</u> function if <u>CK3_BAD_PIN</u> = 1 and is tristated if <u>CK3_BAD_PIN</u> = 0. Active polarity is controlled by <u>CK_BAD_POL</u>. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.</p>										
12	INT_ALM	O	LVC MOS	<p><b>Interrupt/Alarm Output Indicator.</b> This pin functions as a maskable interrupt output with active polarity controlled by the <u>INT_POL</u> register bit. The INT output function can be turned off by setting <u>INT_PIN</u> = 0. If the ALRMOUT function is desired instead on this pin, set <u>ALRMOUT_PIN</u> = 1 and <u>INT_PIN</u> = 0. 0 = ALRMOUT not active. 1 = ALRMOUT active. The active polarity is controlled by <u>CK_BAD_POL</u>. If no function is selected, the pin tristates.</p>										
13 57	CS0_C3A CS1_C4A	I/O	LVC MOS	<p><b>Input Clock Select/CKIN3 or CKIN4 Active Clock Indicator.</b> <b>Input:</b> If manual clock selection is chosen, and if <u>CKSEL_PIN</u> = 1, the CKSEL pins control clock selection and the <u>CKSEL_REG</u> bits are ignored.</p> <table border="1"> <thead> <tr> <th>CS[1:0]</th> <th>Active Input Clock</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>CKIN1</td> </tr> <tr> <td>01</td> <td>CKIN2</td> </tr> <tr> <td>10</td> <td>CKIN3</td> </tr> <tr> <td>11</td> <td>CKIN4</td> </tr> </tbody> </table> <p>If configured as inputs, these pins must not float.</p> <p><b>Output:</b> If <u>CKSEL_PIN</u> = 0, the <u>CKSEL_REG</u> register bits control this function. If auto clock selection is enabled, then they serve as the CKIN_n active clock indicator. 0 = CKIN3 (CKIN4) is not the active input clock 1 = CKIN3 (CKIN4) is currently the active input to the PLL The <u>CKn_ACTV_REG</u> bit always reflects the active clock status for CKIN_n. If <u>CKn_ACTV_PIN</u> = 1, this status will also be reflected on the CnA pin with active polarity controlled by the <u>CK_ACTV_POL</u> bit. If <u>CKn_ACTV_PIN</u> = 0, this output tristates.</p>	CS[1:0]	Active Input Clock	00	CKIN1	01	CKIN2	10	CKIN3	11	CKIN4
CS[1:0]	Active Input Clock													
00	CKIN1													
01	CKIN2													
10	CKIN3													
11	CKIN4													

**Note:** Internal register names are indicated by underlined italics, e.g. INT\_PIN. See Si5368 Register Map.

Table 11. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
29 30	CKIN4+ CKIN4–	I	MULTI	<b>Clock Input 4.</b> Differential clock input. This input can also be driven with a single-ended signal. CKIN4 serves as the frame sync input associated with the CKIN2 clock when <u>CK_CONFIG_REG</u> = 1.
34 35	CKIN2+ CKIN2–	I	MULTI	<b>Clock Input 2.</b> Differential input clock. This input can also be driven with a single-ended signal.
39 40	CKIN3+ CKIN3–	I	MULTI	<b>Clock Input 3.</b> Differential clock input. This input can also be driven with a single-ended signal. CKIN3 serves as the frame sync input associated with the CKIN1 clock when <u>CK_CONFIG_REG</u> = 1.
44 45	CKIN1+ CKIN1–	I	MULTI	<b>Clock Input 1.</b> Differential clock input. This input can also be driven with a single-ended signal.
58	C1A	O	LVC MOS	<b>CKIN1 Active Clock Indicator.</b> This pin serves as the CKIN1 active clock indicator. The <u>CK1_ACTV_REG</u> bit always reflects the active clock status for CKIN1. If <u>CK1_ACTV_PIN</u> = 1, this status will also be reflected on the C1A pin with active polarity controlled by the <u>CK_ACTV_POL</u> bit. If <u>CK1_ACTV_PIN</u> = 0, this output tristates.
59	C2A	O	LVC MOS	<b>CKIN2 Active Clock Indicator.</b> This pin serves as the CKIN2 active clock indicator. The <u>CK2_ACTV_REG</u> bit always reflects the active clock status for CKIN_2. If <u>CK2_ACTV_PIN</u> = 1, this status will also be reflected on the C2A pin with active polarity controlled by the <u>CK_ACTV_POL</u> bit. If <u>CK2_ACTV_PIN</u> = 0, this output tristates.
60	SCL	I	LVC MOS	<b>Serial Clock.</b> This pin functions as the serial port clock input for both SPI and I <sup>2</sup> C modes. This pin has a weak pull-down.
61	SDA_SDO	I/O	LVC MOS	<b>Serial Data.</b> In I <sup>2</sup> C microprocessor control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data output.
68 69	A0 A1	I	LVC MOS	<b>Serial Port Address.</b> In I <sup>2</sup> C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I <sup>2</sup> C address is 1101 [A2][A1][A0.] In SPI control mode (CMODE = 1), these pins are ignored. This pin has a weak pull-down.
<b>Note:</b> Internal register names are indicated by underlined italics, e.g. <u>INT_PIN</u> . See Si5368 Register Map.				

Table 11. Si5367 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
70	A2_SS	I	LVC MOS	<b>Serial Port Address/Slave Select.</b> In I <sup>2</sup> C microprocessor control mode (CMODE = 0), this pin functions as a hardware controlled address bit. The I <sup>2</sup> C address is 1101 [A2][A1][A0.] In SPI microprocessor control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pull-down.
71	SDI	I	LVC MOS	<b>Serial Data In.</b> In SPI microprocessor control mode (CMODE = 1), this pin functions as the serial data input. In I <sup>2</sup> C microprocessor control mode (CMODE = 0), this pin is ignored. This pin has a weak pull-down.
77 78	CKOUT3+ CKOUT3-	O	MULTI	<b>Clock Output 3.</b> Differential clock output. Output signal format is selected by <u>SFOUT3_REG</u> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
82 83	CKOUT1- CKOUT1+	O	MULTI	<b>Clock Output 1.</b> Differential clock output. Output signal format is selected by <u>SFOUT1_REG</u> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
87 88	CKOUT5- CKOUT5+	O	MULTI	<b>Clock Output 5.</b> Differential clock output. Output signal format is selected by <u>SFOUT5_REG</u> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
90	CMODE	I	LVC MOS	<b>Control Mode.</b> Selects I <sup>2</sup> C or SPI control mode for the device. 0 = I <sup>2</sup> C Control Mode. 1 = SPI Control Mode. This pin must be tied high or low.
92 93	CKOUT2+ CKOUT2-	O	MULTI	<b>Clock Output 2.</b> Differential clock output. Output signal format is selected by <u>SFOUT2_REG</u> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

**Note:** Internal register names are indicated by underlined italics, e.g. *INT PIN*. See Si5368 Register Map.

**Table 11. Si5367 Pin Descriptions (Continued)**

Pin #	Pin Name	I/O	Signal Level	Description
97 98	CKOUT4– CKOUT4+	O	MULTI	<b>Clock Output 4.</b> Differential clock output. Output signal format is selected by <u>SFOUT4_REG</u> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND PAD	GND	Supply	<b>Ground Pad.</b> The ground pad must provide a low thermal and electrical impedance to a ground plane.

**Note:** Internal register names are indicated by underlined italics, e.g. INT\_PIN. See Si5368 Register Map.

## 7. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5367A-C-GQ*	.002–945 MHz 970–1134 MHz 1.213–1.4 GHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Si5367B-C-GQ*	.002–808 MHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
Si5367C-C-GQ*	.002–346 MHz	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C

**\*Note:** Not recommended for new designs. For alternatives, see the Si533x family.

## 8. Package Outline: 100-Pin TQFP

Figure 6 illustrates the package details for the Si5367. Table 12 lists the values for the dimensions shown in the illustration.

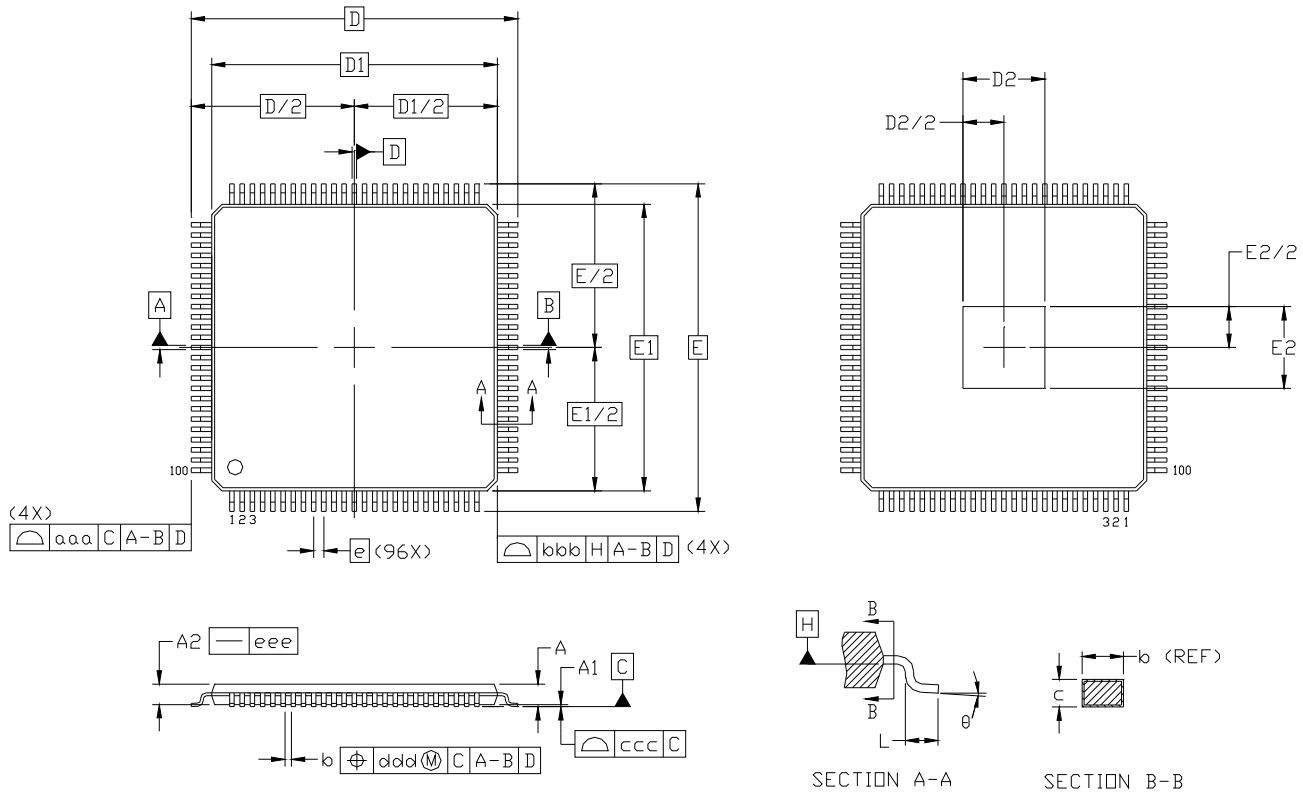


Figure 6. 100-Pin Thin Quad Flat Package (TQFP)

Table 12. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E	16.00 BSC		
A1	0.05	—	0.15	E1	14.00 BSC		
A2	0.95	1.00	1.05	E2	3.85	4.00	4.15
b	0.17	0.22	0.27	L	0.45	0.60	0.75
c	0.09	—	0.20	aaa	—	—	0.20
D	16.00 BSC			bbb	—	—	0.20
D1	14.00 BSC			ccc	—	—	0.08
D2	3.85	4.00	4.15	ddd	—	—	0.08
e	0.50 BSC			θ	0°	3.5°	7°

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. PCB Land Pattern

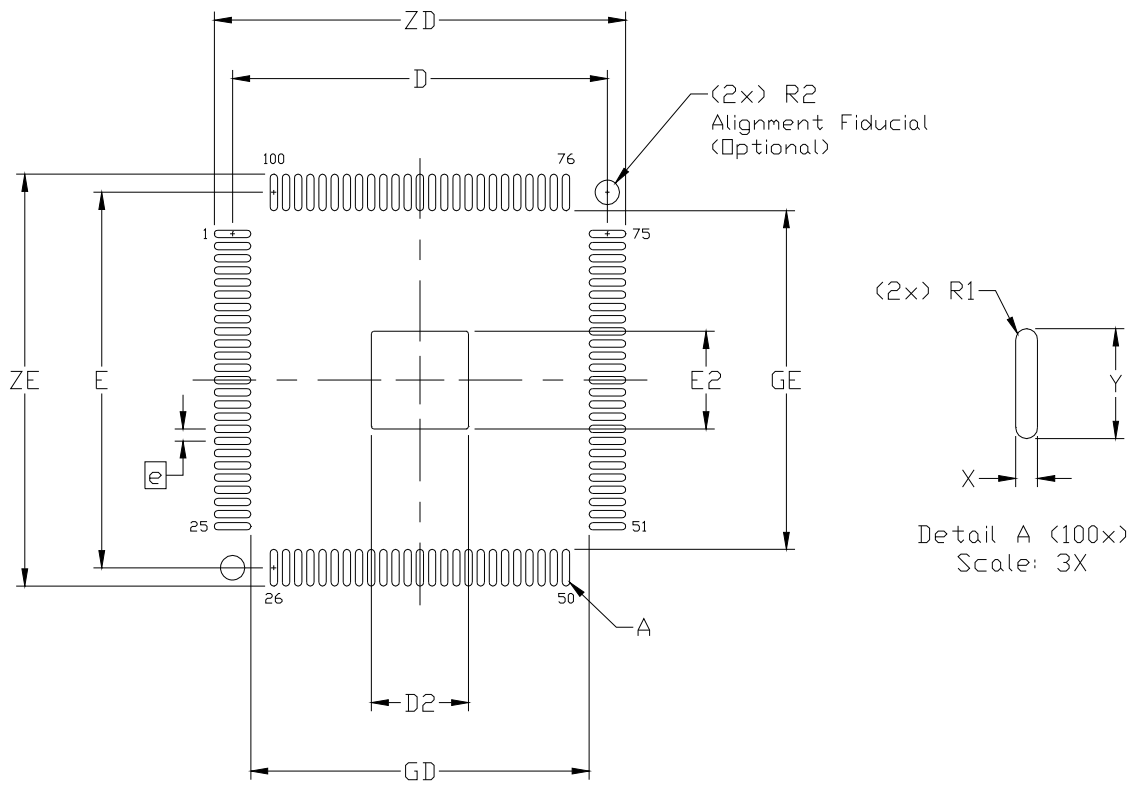


Figure 7. PCB Land Pattern Diagram

Table 13. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

**Notes:****General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

**Card Assembly**

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 10. Top Marking

### 10.1. Si5367 Top Marking



### 10.2. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Logo Size:</b>	9.2 x 3.1 mm Center-Justified	
<b>Font Size:</b>	3.0 Point (1.07 mm) Right-Justified	
<b>Line 1 Marking:</b>	Device Part Number Si5367x-C-GQ	X = Speed Grade See "7. Ordering Guide" on page 73.
<b>Line 2 Marking:</b>	YY = Year WW = Workweek	Assigned by the Assembly Supplier. Corresponds to the year and work-week of the mold date.
	R = Die Revision	
	TTTTT = Mfg Code	Manufacturing Code
<b>Line 3 Marking:</b>	Circle = 1.8 mm Diameter Center-Justified	"e3" Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	

## DOCUMENT CHANGE LIST

### Revision 0.1 to Revision 0.2

- Changed LVTTTL to LVCMOS in Absolute Maximum Ratings table.
- Updated "6. Pin Descriptions: Si5367".
  - Changed FSOUT (pins 87 and 88) to CLKOUT5.
  - Changed FS\_ALIGN (pin 21) control pin to GND.
  - Changed pin 16 to ground.

### Revision 0.2 to Revision 0.3

- Removed references to latency control, INC, and DEC pins.
- Updated block diagram on page 1.
- Added Figure 3, "Typical Phase Noise Plot," on page 14.
- Updated "6. Pin Descriptions: Si5367".
  - Changed font of register names to underlined italics.
- Updated "7. Ordering Guide" on page 73.
- Added "9. PCB Land Pattern".

### Revision 0.3 to Revision 0.4

- Changed 1.8 V operating range to  $\pm 5\%$ .
- Clarified "6. Pin Descriptions: Si5367" on page 67.
- Updated "8. Package Outline: 100-Pin TQFP" on page 74.

### Revision 0.4 to Revision 0.5

- Changed "any-rate" to "any-frequency" throughout.
- Expanded and reordered electrical specification Tables 1 through 7.
- Added "4. Register Map" on page 18.
- Added "5. Register Descriptions" on page 20.
- Added "10. Top Marking" on page 77.
- Updated Table 5, "Jitter Generation," on page 13.
- Updated "7. Ordering Guide" on page 73.
- "3. Pin Descriptions: Si5322" on page 14.

### Revision 0.5 to Revision 1.0

- Updated logo.
- Transitioned to full production.

NOTES:



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