



**THE DATASHEET OF
SI5332DD08839-GM2R**



Si5332 Data Sheet

6/8/12-Output Any-Frequency Clock Generator

Based on Skyworks' proprietary MultiSynth™ flexible frequency synthesis technology, the Si5332 generates any combination of output frequencies with excellent jitter performance (190 fs rms). The device's highly flexible architecture enables a single device to generate a wide range of integer and non-integer related frequencies on up to 12 differential clock outputs with 0 ppm frequency synthesis error. The device offers multiple banks of outputs that can each be tied to independent voltages, enabling usage in mixed-supply applications. Further, the signal format of each clock output is user-configurable. Given its frequency, format, and supply voltage flexibility, the Si5332 is ideally suited to replace multiple clock ICs and oscillators with a single device.

The Si5332 is quickly and easily configured using ClockBuilder Pro™ software. ClockBuilder Pro assigns a custom part number for each unique configuration. Devices ordered with custom part numbers are factory-programmed free of charge, making it easy to get a custom clock uniquely tailored for each application. Using the Si5332's I²C interface, the device may be user-configured at power-up or internally-configured NVM programmed with new configuration using the ClockBuilder Pro Field Programmer.

Applications:

- Servers, Storage, Search Acceleration
- Ethernet Switches, Routers
- Small Cells, Mobile Backhaul/Fronthaul
- Print Imaging
- Communications
- Broadcast Video
- Test and Measurement
- Industrial, Embedded Computing

KEY FEATURES

- Any-Frequency 6/8/12-output programmable clock generators
- Offered in three different package sizes, supporting different combinations of output clocks and user configurable hardware input pins
 - 32-pin, up to 6 outputs
 - 40-pin, up to 8 outputs
 - 48-pin, up to 12 outputs
- MultiSynth technology enables any-frequency synthesis on any output up to 250 MHz
- Highly configurable output path featuring a cross point mux
 - Up to three independent fractional synthesis output paths
 - Up to five independent integer dividers
- Embedded 50 MHz crystal option
- Input frequency range:
 - External crystal: 16 to 50 MHz
 - Differential clock: 10 to 250 MHz
 - LVCMOS clock: 10 to 170 MHz
- Output frequency range:
 - Differential: 5 to 333.33 MHz
 - LVCMOS: 5 to 170 MHz
- PCIe Gen 1/2/3/4/5/6 compliant
- User-configurable clock output signal format per output: LVDS, LVPECL, HCSL, LVCMOS
- Multi-profile configuration support
- Temperature range: -40 to +85 °C
- Down and center spread spectrum
- RoHS-6 compliant
- [Si5332 Family Reference Manual](#)

Table of Contents

| | |
|---|-----------|
| 1. Features List | 4 |
| 2. Ordering Guide | 5 |
| 3. Functional Description | 6 |
| 3.1 Functional Block Diagrams | 7 |
| 3.2 Modes of Operation | 9 |
| 3.2.1 Initialization | 9 |
| 3.3 Frequency Configuration | 9 |
| 3.4 Inputs | 10 |
| 3.4.1 External Reference Input (XA/XB) | 10 |
| 3.4.2 Input Clocks | 10 |
| 3.4.3 Input Selection | 10 |
| 3.5 Outputs | 11 |
| 3.5.1 Output Signal Format | 11 |
| 3.5.2 Differential Output Terminations | 12 |
| 3.5.3 LVCMOS Output Terminations | 16 |
| 3.5.4 LVCMOS Output Signal Swing | 17 |
| 3.5.5 LVCMOS Output Polarity | 17 |
| 3.5.6 Output Enable/Disable | 17 |
| 3.5.7 Differential Output Configurable Skew Settings | 17 |
| 3.5.8 Synchronous Output Disable Feature | 17 |
| 3.6 Spread Spectrum | 18 |
| 3.7 Universal Hardware Input Pins | 18 |
| 3.8 Custom Factory Preprogrammed Parts | 19 |
| 3.9 I ² C Serial Interface | 20 |
| 3.10 In-Circuit Programming | 20 |
| 4. Register Map | 21 |
| 5. Electrical Specifications | 22 |
| 6. Pin Descriptions | 38 |
| 6.1 Pin Descriptions (48-Pin) | 38 |
| 6.2 Pin Descriptions (40-Pin) | 43 |
| 6.3 Pin Descriptions (32-Pin) | 48 |
| 7. Package Outline | 52 |
| 7.1 Si5332 6x6 mm 48-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D) | 52 |
| 7.2 Si5332 6x6 mm 40-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D) | 54 |
| 7.3 Si5332 5x5 mm 32-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D) | 55 |
| 7.4 Si5332 6x6 mm 48-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L) | 57 |
| 7.5 Si5332 6x6 mm 40-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L) | 59 |

| | |
|---|-----------|
| 7.6 Si5332 5x5 mm 32-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L) . . . | .61 |
| 8. PCB Land Pattern | 62 |
| 8.1 Si5332A/B/C/D 48-QFN Land Pattern | .62 |
| 8.2 Si5332A/B/C/D 40-QFN Land Pattern | .64 |
| 8.3 Si5332A/B/C/D 32-QFN Land Pattern | .66 |
| 8.4 Si5332E/F/G/H/L 48-LGA Land Pattern. | .68 |
| 8.5 Si5332E/F/G/H/L 40-LGA Land Pattern. | .70 |
| 8.6 Si5332E/F/G/H/L 32-LGA Land Pattern. | .72 |
| 9. Top Marking. | 74 |
| 10. Revision History. | 75 |

1. Features List

- Any-Frequency 6/8/12-output programmable clock generators
- Offered in three different package sizes, supporting different combinations of output clocks and user configurable hardware input pins
 - 32-pin, up to 6 outputs
 - 40-pin, up to 8 outputs
 - 48-pin, up to 12 outputs
- MultiSynth™ technology enables any-frequency synthesis on any output up to 250 MHz
- Integer output frequencies up to 333.33 MHz
- Embedded 50 MHz crystal option (E/F/G/H/L grades)
- Highly configurable output path featuring a cross point mux
 - Two independent fractional synthesis output paths
 - Up to five independent integer dividers
- Ordering options for embedded 50 MHz reference crystal
- Input frequency range:
 - External crystal: 16 to 50 MHz
 - Differential clock: 10 to 250 MHz
 - LVCMOS clock: 10 to 170 MHz
- Output frequency range:
 - Differential: 5 to 333.33 MHz
 - LVCMOS: 5 to 170 MHz
- User-configurable clock output signal format per output: LVDS, LVPECL, HCSSL, LVCMOS
- Low phase jitter:
 - 175 fs RMS (embedded crystal)
 - 190 fs RMS (external crystal)
- PCIe Gen1/2/3/4/5/6, SRIS compliant
- 1.8 V, 2.5 V, 3.3 V core VDD
- Adjustable output-output delay
- Multi-profile configuration support:
 - Store up to 16 input/output configurations in the same custom part number
- Independent glitchless on-the-fly output frequency changes
- Very low power consumption
- Independent output supply pins for each bank of outputs:
 - 1.8 V, 2.5 V, or 3.3 V differential
 - 1.5 V, 1.8 V, 2.5 V, 3.3 V LVCMOS
- Programmable spread spectrum
 - Down and center spread from 0.1% to 2.5% in 0.01% steps at 30 to 33 kHz
- Integrated power supply filtering
- Serial interface: I²C
- ClockBuilder Pro software utility simplifies device configuration and assigns custom part numbers
- Operating temperature range: –40 to +85 °C
- RoHS-6 compliant

2. Ordering Guide

Blank Devices, In-System Programmable



Preprogrammed Devices Using a ClockBuilder Pro Configuration File



Figure 2.1. Orderable Part Number Guide

3. Functional Description

The Si5332 is a high-performance, low-jitter clock generator capable of synthesizing up to twelve user-programmable clock frequencies up to 333.33 MHz. The device supports free run operation using an external or embedded crystal, or it can lock to an external clock signal. The output drivers support up to twelve differential clocks or twenty four LVCMOS clocks, or a combination of both. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, and LVCMOS. VDDO pins are provided for versatility, which can be set to 3.3 V, 2.5 V, 1.8 V or 1.5 V (CMOS only) to power the multi-format output drivers. The core voltage supply (VDD) accepts 3.3 V, 2.5 V, or 1.8 V and is independent from the output supplies (VDDOxs). Using its two-stage synthesis architecture and patented high-resolution low-jitter MultiSynth technology, the Si5332 can generate an entire clock tree from a single device.

The Si5332 combines a wideband PLL with next generation MultiSynth technology to offer the industry's highest output count high performance programmable clock generator, with attainable jitter performance below 200 fs RMS. The PLL locks to either an external 16-50 MHz crystal or an embedded 50 MHz crystal for generating free-running clocks or to an external clock (CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#) for generating synchronous clocks. In free-run mode, the oscillator frequency is multiplied by the PLL and then divided down either by an integer divider or MultiSynth for fractional synthesis.

The Si5332 features user-defined universal hardware input pins which can be configured in the ClockBuilder Pro software utility. Universal hardware pins can be used for OE, spread spectrum enable, input clock selection, output frequency selection, or I²C address select.

The device provides the option of storing a user-defined clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up. To enable in-system programming, a power up mode is available through OTP which powers up the chip in an OTP defined default mode but with no outputs enabled. This allows a host processor to first write a user defined subset of the registers and then restart the power-up sequence to activate the newly programmed configuration without re-downloading the OTP.

3.1 Functional Block Diagrams

Si5332-GM3: 12-Output, 48-QFN/LGA



Figure 3.1. Block Diagram for 12-Output Si5332 in 48-QFN/LGA

The Si5332-GM3 features:

- Up to twelve differential clock outputs, with six VDDO pins.
- Seven user-configurable HW input pins, defined using ClockBuilder Pro.

Si5332-GM2: 8-Output, 40-QFN/LGA



Figure 3.2. Block Diagram for 8-Output Si5332 in 40-QFN/LGA

The Si5332-GM2 features:

- Up to eight differential clock outputs, with six VDDO pins.
- Seven user-configurable HW input pins, defined using ClockBuilder Pro.

Si5332-GM1: 6-Output, 32-QFN/LGA



Figure 3.3. Block Diagram for 6-Output Si5332 in 32-QFN/LGA

The Si5332-GM1 features:

- Up to six differential clock outputs with individual VDDO.
- Five user-configurable HW input pins, defined using ClockBuilder Pro.

3.2 Modes of Operation

The Si5332 supports both free-run and synchronous modes of operation. The default mode selection is set in ClockBuilder Pro. Alternatively, two universal hardware input pins can be defined as CLKIN_SEL[1:0] to select between a crystal or clock input. There is also the option to select the input source via the serial interface by writing to the input select register.

3.2.1 Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. The clock outputs will be squelched until the device initialization is done.

3.3 Frequency Configuration

The phase-locked loop is fully integrated and does not require external loop filter components. Its function is to phase lock to the selected input and provide a common synchronous reference to the high-performance MultiSynth fractional or integer dividers.

A cross point mux connects any of the MultiSynth divided frequencies or INT divided frequencies to individual output drivers or banks of output drivers. Additional output integer dividers provide further frequency division by an even integer from 1 to 63. The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (M_n/M_d), the MultiSynth fractional dividers (N_n/N_d), and the output integer dividers (R). Skyworks' Clockbuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan.

3.4 Inputs

The Si5332 requires an external 16-50 MHz crystal at its XIN/XOUT pins or the embedded 50 MHz crystal to operate in free-run mode, or an external input clock (CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#) for synchronous operation. An external crystal is not required in synchronous mode.

3.4.1 External Reference Input (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) on Si5332A/B/C/D to produce a low jitter reference for the PLL when operating in the free-run mode. The Si5332 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to [Table 5.4 External Crystal Input Specification \(A/B/C/D Grades\)](#) on page 25 for crystal specifications.

For free-running operation, the internal oscillator can operate from a low-frequency fundamental mode crystal (XTAL) with a resonant frequency of 16 to 50 MHz. A crystal can easily be connected to pins XA and XB without external components, as shown in the figure below. Internal loading capacitance (CL) values from 2.5 pF to 21.5 pF can be selected via register settings. Alternatively, an external CL can be used along with the internal CL.



Figure 3.4. External Reference Input (XA/XB)

The Si5332E/F/G/H/L options feature an embedded 50 MHz reference crystal that is used in the free run mode.

3.4.2 Input Clocks

An input clock is available to synchronize the PLL when operating in synchronous mode. This input can be configured as LVPECL, LVDS or HCSL differential, or LVCMOS. The recommended input termination schemes are shown in the [Si5332 Family Reference Manual](#). Differential signals must be AC coupled. Unused inputs can be disabled by register configuration.

3.4.3 Input Selection

The active clock input is selected by register control, or by defining two universal input pins as CLKIN_SEL[1:0] in ClockBuilder Pro. A register bit determines input selection as pin or register selectable. If there is no clock signal on the selected input at power up, the device will not generate output clocks.

In a typical application, the Si5332 reference input is configured immediately after power-up and initialization. If the device is switched to another input more than ± 1000 ppm offset from the initial input, the device must be recalibrated manually to the new frequency, temporarily turning off the clock outputs. After the VCO is recalibrated, the device will resume producing clock outputs. If the selected inputs are within ± 1000 ppm, any phase error difference will propagate through the device at a rate determined by the PLL bandwidth. Hitless switching and phase build-out are not supported by the Si5332.

3.5 Outputs

The Si5332 supports up to 12 differential output drivers. Each output can be independently configured as a differential pair or as dual LVCMOS outputs. The 8-output and 12-output devices feature banks of outputs, with each bank sharing a common VDDO.

Table 3.1. Clock Outputs

| Device/Package | Maximum Outputs |
|---------------------|----------------------------|
| Si5332-GM1 (32-Pin) | 6 Differential, 12 LVCMOS |
| Si5332-GM2 (40-Pin) | 8 Differential, 16 LVCMOS |
| Si5332-GM3 (48-Pin) | 12 Differential, 24 LVCMOS |

The output stage is different for each of the three versions of Si5332.

- The 6-output device features individual VDDO pins for each clock output. Each clock output can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point MUX.
- The 8-output device includes four clock outputs with dedicated VDDO pins, each of which can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point MUX. The remaining four clock outputs are divided into Bank A and Bank B. Each Bank of outputs can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point MUX. The outputs within each of the two Banks share a common VDDO pin.
- The 12-output device includes two clock outputs with dedicated VDDO pins, each of which can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point MUX. The remaining ten clock outputs are divided into Bank A, Bank B, Bank C, and Bank D. Each Bank of outputs can be sourced from MultiSynth0, MultiSynth1, the input reference clock, or one of the five INT dividers through the cross point MUX. The outputs within each of the four Banks share a common VDDO pin.

Utilizing the reference clock enables a fan-out buffer function from an input clock source to any bank of outputs.

Individual output Integer output dividers (R) allow the generation of additional synchronous frequencies. These integer dividers are configurable as divide by 1 (default) through 63.

3.5.1 Output Signal Format

The differential output swing and common mode voltage are compatible with a wide variety of signal formats including HCSL, LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS drivers, enabling the device to support both differential and single-ended clock outputs. Output formats can be defined in ClockBuilder Pro or via the serial interface.

3.5.2 Differential Output Terminations

LVDS Driver Termination

For a general LVDS interface, the recommended value for the differential termination impedance (Z_T) is between 90 Ω and 132 Ω . The actual value should be selected to match the differential impedance (Z_0) of the transmission line. A typical point-to-point LVDS design uses a 100 Ω parallel resistor at the receiver and a 100 Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard LVDS termination schematic as shown in [Figure 3.5 Standard LVDS Termination on page 12](#) can be used with either type of output structure. [Figure 3.6 Optional LVDS Termination on page 12](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 0.01 to 0.1 μF . If using a non-standard termination, please contact Skyworks to confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

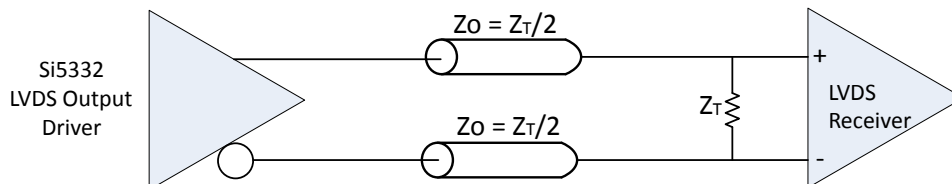


Figure 3.5. Standard LVDS Termination

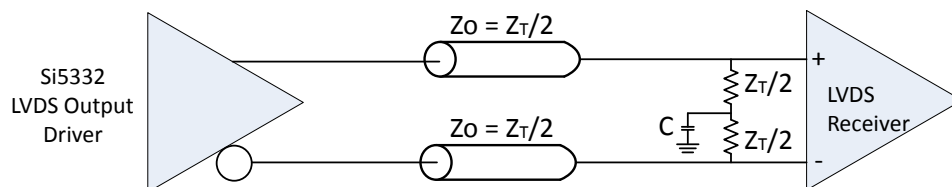


Figure 3.6. Optional LVDS Termination

Termination for 3.3 V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. [Figure 3.7 3.3 V LVPECL Output Termination, Option 1 on page 13](#) and [Figure 3.8 3.3 V LVPECL Output Termination, Option 2 on page 13](#) show two different layouts. Other suitable clock layouts may exist, and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



Figure 3.7. 3.3 V LVPECL Output Termination, Option 1



Figure 3.8. 3.3 V LVPECL Output Termination, Option 2

Termination for 2.5 V LVPECL Outputs

Figure 3.9 2.5 V LVPECL Termination Example, Option 1 on page 14 and Figure 3.10 2.5 V LVPECL Termination Example, Option 2 on page 14 show examples of termination for the 2.5 V LVPECL driver option. These terminations are equivalent to terminating 50 Ω to VDDO – 2 V. For VDDO = 2.5 V, the VDDO – 2 V is very close to ground level. The R3 in Figure 3.10 2.5 V LVPECL Termination Example, Option 2 on page 14 can be optionally eliminated using the termination shown in Figure 3.9 2.5 V LVPECL Termination Example, Option 1 on page 14.



Figure 3.9. 2.5 V LVPECL Termination Example, Option 1



Figure 3.10. 2.5 V LVPECL Termination Example, Option 2

Termination for HCSL Outputs

The Si5332 HCSL driver option integrated termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100 Ω and 85 Ω transmission line options. This configuration option may be specified using ClockBuilder Pro or via the device I²C interface.



Figure 3.11. HCSL Internal Termination Mode



Figure 3.12. HCSL External Termination Mode

3.5.3 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.



Figure 3.13. LVCMOS Output Termination Example, Option 1



Figure 3.14. LVCMOS Output Termination Example, Option 2

The Si5332 output drivers natively support 3.3, 2.5, 1.8 V, and 1.5 V CMOS. 1.2 V CMOS signals can be obtained using a two-resistor network as shown in the following figure and tables below. Place R1 and R2 as close to the device output as possible.



Figure 3.15. 1.2 V CMOS Signals Obtained Using a Two-Resistor Network

Table 3.2. R1 and R2 Values for 50 Ω Driver

| Si5332 LVCMOS Output Termination w/50 Ω Driver for Interfacing to 1.2 V Receivers | | |
|---|-----------------------------|-----------------------------|
| VDDO _x | 1.2 V LVCMOS | |
| | R _s ¹ | R _p ¹ |
| 1.8 V | 23.2 | 150 |
| 2.5 V | 57.6 | 95.3 |
| 3.3 V | 95.3 | 78.7 |

Note:
1. 1% resistor values shown.

Table 3.3. R1 and R2 Values for 25 Ω Driver

| Si5332 LVCMOS Output Termination w/25 Ω Driver for Interfacing to 1.2 V Receivers | | |
|---|-----------------------------|-----------------------------|
| VDDO _x | 1.2 V LVCMOS | |
| | R _s ¹ | R _p ¹ |
| 1.8 V | 12.1 | 75 |
| 2.5 V | 29.4 | 48.7 |
| 3.3 V | 46.4 | 39.2 |

Note:
1. 1% resistor values shown.

3.5.4 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

3.5.5 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUT_x and OUT_{xb}). By default, the clock on the OUT_{xb} pin is generated in phase with the clock on the OUT_x pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

3.5.6 Output Enable/Disable

The universal hardware input pins can be programmed to operate as output enable (OEB), controlling one or more outputs. Pin assignment is done using ClockBuilder Pro. An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high all designated outputs will be disabled. When held low, the designated outputs will be enabled.

3.5.7 Differential Output Configurable Skew Settings

Skew on the differential outputs can be independently configured. The skew is adjustable in 35 ps steps across a range of 245 ps.

3.5.8 Synchronous Output Disable Feature

Output clocks are always enabled and disabled synchronously. The output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output.

3.6 Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5332 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The Si5332 implements spread spectrum using its patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude. Spread spectrum can be enabled through I²C, or by configuring one of the universal hardware input pins using ClockBuilder Pro.

The Si5332 features both center and down spread spectrum modulation capability, from 0.1% to 2.5%. Each MultiSynth is capable of generating an independent spread spectrum clock. The feature is enabled using a user-defined universal hardware input pin or via the device I²C interface. Spread spectrum can be applied to any output clock derived from a MultiSynth fractional divider, with any clock frequency up to 250 MHz. Since the spread spectrum clock generation is performed in the MultiSynth fractional dividers, the spread spectrum waveform is highly consistent across process, voltage and temperature. The Si5332 features two independent MultiSynth dividers, enabling the device to provide two independent spread profiles simultaneously to the clock output banks.

Spread spectrum is commonly used for 100 MHz PCI Express clock outputs. To comply with the spread spectrum specifications for PCI Express, the spreading frequency should be set to a maximum of 33 kHz and –0.5% down spread. A universal hardware input pin can be configured to toggle spread spectrum on/off.

3.7 Universal Hardware Input Pins

Universal hardware input pins are user configurable control input pins that can have one or more of the functions listed below assigned to them using ClockBuilder Pro.

Universal hardware input pins can be utilized for the following functions:

Table 3.4. Universal Hardware Input Pins

| Description | Function |
|---------------------------------|---|
| SSEN_EN0 | Spread spectrum enable on MultiSynth0 (N0). |
| SSEN_EN1 | Spread spectrum enable on MultiSynth0 (N1). |
| FS_INTx | Used to switch an integer output divider frequency from frequency A to frequency B. |
| FS_MSx | Used to switch a MultiSynth output divider output from frequency and/or change spread spectrum profile. |
| OE | Output enable for one or more outputs. |
| I ² C address select | Sets the LSB of the I ² C address to either 0 or 1. |
| CLKIN_SEL[1:0] | Selects between crystal or clock inputs. |
| PROFILE_SEL[x] | Selects which device profile to load on power-up. See Multi-Profile description below. |

Assigning a universal hardware input pin to control a specific function overrides the register bit control via I²C for that same function. For example, if a universal hardware pin is assigned as an output enable, it will take precedence over the output enable register bits, rendering it inoperative.

Spread Spectrum Enable Pins (SSEN[1:0])

Spread_EN[1:0] pins are active pins that enable/disable spread spectrum on all outputs that correspond to MultiSynth0 or MultiSynth1, respectively. The change in frequency or spread spectrum will be instantaneous and may not be glitch free.

Table 3.5. SSEN_EN Pin Selection Table

| SSEN_ENx | |
|----------|---|
| 0 | Spread Spectrum disabled on MultiSynthx |
| 1 | Spread Spectrum enabled on MultiSynthx |

Output Frequency Select Pins

There are five integer dividers, one corresponding to each of the five output banks. Using ClockBuilder Pro, a universal hardware input pin can be assigned for each integer divider, providing capability to select between two different pre-programmed divide values. Divider values of every integer from 8 to 255 are available in ClockBuilder Pro for each integer divider.

Table 3.6. F_S_INT Pin Selection Table

| F _S _INT _x | Output Frequency from INT _x |
|----------------------------------|---|
| 0 | Frequency A, as defined in ClockBuilder Pro |
| 1 | Frequency B, as defined in ClockBuilder Pro |

Output Enable

A universal hardware input pin can be defined to control output enable of a differential output, a bank of differential outputs, or as a global output enable pin controlling all outputs. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 μs for the output to have a clean clock.

Output enabled/disabled for LVCMOS are done in pairs. Each differential buffer True and Compliment output can generate an LVCMOS clock and the OE pin associated with the True and Compliment output buffer will control the respective LVCMOS pair.

For example: If DIFF0 is configured to be SE1 and DIFF0# is configured to be SE2 and OE1 is the associated OE pin, de-asserting the OE1 pin will disable both SE1 and SE2 outputs. The disable and enable of the outputs to a known state is glitch free.

I²C Address Pin

This pin sets the LSB of the I²C address. For example, if the I²C address is the device default of 0x6A, setting this pin high will set the I²C address to 0x6B.

CLKIN_SEL[0:1] Pins

These pins are used to set the input source clock between the input clock channels (Crystal, CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#). Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

Multi-Profile

Si5332 has the ability to store multiple unique configurations in the same custom part number by enabling multi-profile support in ClockBuilder Pro after selecting the desired Si5332 device. The ClockBuilder Pro wizard guides users to enter the input/output/feature set needed for each individual profile configuration, then compiles them together and assigns the necessary number of universal hardware pins based on the number of profiles entered.

The actual number of profiles supported in a particular design is limited by overall design complexity and NVM size. ClockBuilder Pro automatically determines the NVM size required for your multi-profile design and will warn if the maximum limit is exceeded.

3.8 Custom Factory Preprogrammed Parts

Custom pre-programmed parts can be ordered corresponding to a specific configuration file generated using the ClockBuilder Pro software utility. Skyworks writes the configuration file into the device prior to shipping. Use the [ClockBuilder Pro](#) custom part number wizard to quickly and easily generate a custom part number for your ClockBuilder Pro configuration file. A factory pre-programmed part will generate clocks at power-up.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your pre-programmed device will ship within two weeks.

3.9 I²C Serial Interface

The Si5332 is compatible with Rev 6 of the I²C specification, including Standard, Fast, and Fast+ modes.

Configuration and operation of the Si5332 can be controlled by reading and writing registers using the I²C . Communication with a 1.8 V to 3.3 V host is supported. See the *Si5332 Family Reference Manual* for details.

3.10 In-Circuit Programming

The Si5332 is in-system configurable using the I²C interface by the following two methods:

- *In-circuit configuration of device registers after power-up.* With this method changes to volatile register memory can be done as required to produce the desired outputs. This does not alter internal NVM; therefore, register memory changes are lost at power-down. Refer to the *Si5332 Family Reference Manual* available on our web site for details.
- *In-circuit re-configuration of internal NVM.* Writing to internal NVM requires the use of the CBPro Field Programmer (CBPROG-DON-GL) and CBPro software. See *UG286: ClockBuilderPro Field Programmer Kit* user's guide available on our web site for more information. (One important note: The Si5332 core VDDs (VDD_DIG, VDDA, and VDD_XTAL) must be powered by 3.3 V during in-circuit NVM programming.)
- VDD core voltages (VDD_DIG, VDDA, VDD_XTAL) must be 3.3 V for in-circuit programming. Using VDD core voltage lower than 3.3 V (i.e., 2.5 V or 1.8 V) will not support reliable in-circuit NVM programming.

4. Register Map

Refer to the [Si5332 Family Reference Manual](#) for a complete list of registers descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

($V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+10\%/-5\%$, $V_{DDO} = 1.8\text{ V } \pm 5\%$, $2.5\text{ V } \pm 5\%$, or $3.3\text{ V } \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|------------------------------|--------------------------------------|----------------|------|-----|-------|------------------|
| Ambient Temperature | T_A | | -40 | 25 | 85 | $^\circ\text{C}$ |
| Junction Temperature | T_{JMAX} | | — | — | 125 | $^\circ\text{C}$ |
| Core Supply Voltage | $V_{DDA}, V_{DD_DIG}, V_{DD_xtal}$ | | 1.71 | — | 3.63 | V |
| Output Driver Supply Voltage | V_{DDO} | | 1.71 | — | 3.465 | V |

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of $25\text{ }^\circ\text{C}$ unless otherwise noted.
2. All core voltages (V_{DD_DIG} , V_{DDA} , V_{DD_XTAL}) must be connected to the same voltage.

Table 5.2. DC Characteristics

($V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+10\%/-5\%$, $V_{DDO} = 1.8\text{ V } \pm 5\%$, $2.5\text{ V } \pm 5\%$, or $3.3\text{ V } \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|------------------------------|------------|--|------------|-----|-----|-----|-------|
| Core Supply Current | I_{DD} | | | — | 45 | 70 | mA |
| Output Buffer Supply Current | I_{DDOx} | LVPECL Output ³ @ 156.25 MHz | | — | 33 | 35 | mA |
| | | HCSL Output ³ @ 100 MHz | | — | 20 | 22 | mA |
| | | LVDS Output ³ @ 156.25 MHz | | — | 11 | 13 | mA |
| | | 3.3 V VDDO LVCMOS ⁴ output @ 170 MHz | | — | 16 | 19 | mA |
| | | 2.5 V VDDO LVCMOS ⁴ output @ 170 MHz | | — | 9 | 11 | mA |
| | | 1.8 V VDDO LVCMOS ⁴ output @ 170 MHz | | — | 7.5 | 8.5 | mA |
| Total Power Dissipation | P_d | 48-pin | Notes 5 | — | 590 | — | mW |
| | | 40-pin | Note 1, 5 | — | 320 | — | mW |
| | | 32-pin | Notes 2, 5 | — | 270 | — | mW |

Notes:

- Si5332 40-pin test configuration: $V_{DDO} = V_{DDA} = V_{DDI} = 1.8\text{ V}$, 4 × 2.5 V LVDS outputs enabled @ 156.25 MHz, 2 × 1.8 V HCSL outputs enabled @ 100 MHz, 2x 3.3 V LVCMOS outputs enabled @ 25 MHz. . Excludes power in termination resistors.
- Si5332 32-pin test configuration: $V_{DDO} = V_{DDA} = V_{DDI} = 1.8\text{ V}$, 2 × 2.5 V LVDS outputs enabled @ 156.25 MHz, 2 × 1.8 V HCSL outputs enabled @ 100 MHz. 2x 3.3 V LVCMOS outputs enabled @ 25 MHz. Excludes power in termination resistors.
- Differential outputs terminated into a 100 Ω load.
- LVCMOS outputs measured into a 5 inch 50 Ω PCB trace with 4 pF load.



- Detailed power consumption for any configuration can be estimated using [ClockBuilderPro](#) when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 5.3. Clock Input Specifications

($V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+10\%/ -5\%$, $V_{DDO} = 1.8\text{ V } \pm 5\%$, $2.5\text{ V } \pm 5\%$, or $3.3\text{ V } \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|------------------|--------------------------------------|---------------------|-----|---------------------|-----------------|
| Input Clock (AC-Coupled Differential Input Clock on CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#) | | | | | | |
| Frequency | F_{IN} | Differential | 10 | — | 250 | MHz |
| Voltage Swing | $V_{PP_DIFF}^3$ | Differential AC-coupled < 250 MHz | 0.5 | — | 1.8 | V_{PP_diff} |
| Slew Rate | SR/SF | 20-80% | 0.75 | — | — | V/ns |
| Duty Cycle | DC | | 40 | — | 60 | % |
| Input Impedance | R_{IN} | | 10 | — | — | k Ω |
| Input Capacitance | C_{IN} | | 2 | 3.5 | 6 | pF |
| Input Clock (AC or DC Coupled LVCMOS Input Clock on CLKIN_2 or CLKIN_3) | | | | | | |
| Frequency | F_{IN} | | 10 | — | 170 | MHz |
| Input High Voltage | V_{IH} | | $0.8 \times V_{DD}$ | — | — | V |
| Input Low Voltage | V_{IL} | | — | — | $0.2 \times V_{DD}$ | V |
| Slew Rate ^{1,2} | SR/SF | 20-80% | 0.75 | — | — | V/ns |
| Duty Cycle | DC | | 40 | — | 60 | % |
| Input Capacitance | C_{IN} | | 2 | 3.5 | 6 | pF |
| Input Clock (AC-Coupled Input Clock on XA) | | | | | | |
| Frequency | F_{IN} | | 10 | — | 170 | MHz |
| Voltage Swing | | | | — | 1 | V _{pp} |
| Input Low Voltage | V_{IL} | | — | — | $0.2 \times V_{DD}$ | V |
| Slew Rate ^{1, 2} | SR/SF | 20–80% | 0.75 | — | — | V/ns |
| Duty Cycle | DC | | 40 | — | 60 | % |
| Input Capacitance | C_{IN} | | 2 | 3.5 | 6 | pF |
| Notes: | | | | | | |
| 1. Imposed for jitter performance. | | | | | | |
| 2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80-20} = ((0.8 - 0.2) \times V_{IN_Vpp_se}) / SR$. | | | | | | |
| 3. $V_{PP_DIFF} = 2 \times V_{PP_SINGLE-ENDED}$ | | | | | | |

Table 5.4. External Crystal Input Specification (A/B/C/D Grades)(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--------------------------------|-------------------|--------------------------------|-------|-----|-----|-------|
| Crystal Frequency | F _{xtal} | | 16-50 | | | MHz |
| Load Capacitance | C _L | 16 - 30 MHz | 6 | 12 | 20 | pF |
| | | 31 - 50 MHz | | | 10 | pF |
| Shunt Capacitance | C _O | 16 - 30 MHz | — | — | 7 | pF |
| | | 31 - 50 MHz | — | — | 2 | pF |
| ESR | | 16 - 30 MHz | — | — | 50 | Ω |
| | | 31 - 50 MHz | — | — | 50 | Ω |
| Crystal Drive Level | d _L | | | — | 250 | μW |
| Input Capacitance ¹ | C _{IN} | Internal cap disabled | — | 2.5 | — | pF |
| | | Internal cap enabled (per pad) | 5 | — | 43 | pF |
| Input Voltage | V _{XIN} | | -0.3 | — | 1.3 | V |

Notes:

- Internal capacitance on the xtal input pads is programmable or can be disabled. Please reference section 5.3.1 for more detailed information.

Table 5.5. Embedded Crystal Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|----------------|--|-----|-----|-----|-------|
| Initial Accuracy (E/F/G/H/L Grades) ¹ | f _i | Measured at +25 °C at time of shipping | — | ±10 | — | ppm |
| Total Stability (E/F/G/H/L Grades) | | -40 °C to +85 °C | -50 | — | 50 | ppm |
| Total Stability (L-Grade Only) | | +25 °C to +85 °C | -30 | — | 30 | ppm |
| Temperature Stability (E/F/G/H/L Grades) ² | | -40 °C to +85 °C | -30 | — | 30 | ppm |
| Temperature Stability (L-Grade Only) ² | | +25 °C to +85 °C | -25 | — | 25 | ppm |

Note:

- Internal crystal loading capacitance is set at factory during device frequency calibration and can not be changed.
- Temperature stability is inclusive of initial accuracy.

Table 5.6. Control Pins

($V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V } +10\%/-5\%$, or $3.3\text{ V } \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|----------|----------------|-----------------------|-----|-----------------------|------------|
| Si5332 Control Input Pins (Inputx) | | | | | | |
| Input Voltage | V_{IL} | | -0.1 | — | $0.3 \times V_{DD}^1$ | V |
| | V_{IH} | | $0.7 \times V_{DD}^1$ | — | $1.1 \times V_{DD}$ | V |
| Input Capacitance | C_{IN} | | — | — | 4 | pF |
| Pull-up/down Resistance | R_{IN} | | — | 50 | — | k Ω |
| Note: | | | | | | |
| 1. V_{DD} indicates all core voltages V_{DD_DIG} , V_{DDA} , and V_{DD_XTAL} which are required to all be using same nominal voltage. | | | | | | |

Table 5.7. Differential Clock Output Specifications(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|-------------------------------------|--------------------------------|---------------------------|----------------|------------------------|-----------------------|------------------------|-----------------|
| Output Frequency | f _{OUT} | Integer synthesis mode | | 5 | — | 333.33 ²⁰ | MHz |
| | | Fractional synthesis mode | | 5 | — | 250 | MHz |
| Duty Cycle | DC | | | 48 | — | 52 | % |
| Output-Output Skew | T _{SK} | Within the same bank | | — | — | 30 | ps |
| | | Across banks | | — | — | 80 | ps |
| Output Voltage Swing | V _{SEPP} | LVPECL | | 0.6 | 0.75 | 0.85 | V _{PP} |
| | | LVDS | 1.8/2.5/3.3 V | 0.3 | 0.375 | 0.45 | V _{PP} |
| | | HCSL | | 0.7 | 0.8 | 0.9 | V _{PP} |
| Common Mode Voltage | V _{CM} | LVPECL | | — | V _{DDO} -1.4 | — | V |
| | | LVDS | 2.5/3.3 V | 1.125 | 1.2 | 1.275 | V |
| | | LVDS | 1.8 V | 0.75 | 0.8 | 0.85 | V |
| | | HCSL | | 0.35 | 0.4 | 0.45 | V |
| HCSL Edge Rate | Edgr | Notes 12,14,18 | | 1 | — | 4.5 | V/ns |
| HCSL Delta Tr | D _{tr} | Notes 14, 17, 18 | | — | — | 135 | ps |
| HCSL Delta Tf | D _{tf} | Notes 14, 17, 18 | | — | — | 125 | ps |
| HCSL Vcross Abs | V _{xa} | Notes 11, 13, 14, 17 | | 250 | — | 550 | mV |
| HCSL Delta Vcross | D _{vcrs} | Notes 14, 17 | | — | — | 140 | mV |
| HCSL Vovs | V _{ovs} | Notes 14, 17 | | — | — | V _{HIGH} +300 | mV |
| HCSL Vuds | V _{uds} | Notes 14, 17 | | — | — | V _{LOW} -300 | mV |
| HCSL Vrng | V _{rng} | Notes 14, 17 | | V _{HIGH} -200 | — | V _{LOW} +200 | mV |
| Rise and Fall Times (20% to 80%) | t _R /t _F | LVDS (fast mode) | 3.3 V or 2.5 V | 150 | 200 | 350 | ps |
| | | LVDS (slow mode) | 3.3 V or 2.5 V | 350 | 530 | 620 | ps |
| | | | 1.8 V | 150 | 225 | 350 | ps |
| Rise and Fall Times (20% to 80%) | t _R /t _F | LVPECL | | 150 | — | 320 | ps |
| | | HCSL | | — | — | 420 | ps |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|--------|----------------|-----|-----|-----|-------|
| Notes: | | | | | | |
| 1. For best jitter performance, keep the midpoint differential input slew rate faster than 0.3 V/ns. | | | | | | |
| 2. Not in PLL bypass mode. | | | | | | |
| 3. For best jitter performance, keep the midpoint input single ended slew rate faster than 1 V/ns. | | | | | | |
| 4. On chip termination resistance can be programmed on (100ohm) or off (high impedance). | | | | | | |
| 5. Not including R divider. | | | | | | |
| 6. Input capacitance on crystal pins targets 23 pf each plus 1 pf external trace capacitance to provide 12 pf series equivalent crystal load capacitance. | | | | | | |
| 7. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#. | | | | | | |
| 8. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150mV to +150mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall. | | | | | | |
| 9. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. | | | | | | |
| 10. Test configuration is $R_s=33.2 \Omega$, $R_p=49.9$, 2 pF. | | | | | | |
| 11. $V_{cross(rel)}$ Min and Max are derived using the following, $V_{cross(rel)} \text{ Min} = 0.250 + 0.5 (V_{havg} - 0.700)$, $V_{cross(rel)} \text{ Max} = 0.550 - 0.5 (0.700 - V_{havg})$. | | | | | | |
| 12. Measurement taken from Single Ended waveform. | | | | | | |
| 13. Measurement taken from differential waveform VLow Math function. | | | | | | |
| 14. Overshoot is defined as the absolute value of the maximum voltage. | | | | | | |
| 15. Undershoot is defined as the absolute value of the minimum voltage. | | | | | | |
| 16. The crossing point must meet the absolute and relative crossing point specifications simultaneously. | | | | | | |
| 17. ΔV_{cross} is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in V_{cross} for any particular system. | | | | | | |
| 18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max. | | | | | | |
| | | | | | | |
| 19. LVDS swing levels for 50 Ω transmission lines. | | | | | | |
| 20. Actually 333 + 1/3 MHz. | | | | | | |

Table 5.8. LVCMOS Clock Output Specifications(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|--------------------------------|-------------------------------------|-----------------------|------|--------|-------|
| Frequency | f _{out} | 1.8-3.3 V CMOS | 5 | — | 170 | MHz |
| | | 1.5 V CMOS | 5 | — | 133.33 | MHz |
| Rise/Fall Time, 3.3 V (20-80%) | t _R /t _F | 50 Ω impedance, 5" trace, CL = 4 pf | — | 0.5 | 0.8 | ns |
| Rise/Fall Time, 2.5 V (20-80%) | t _R /t _F | 50 Ω impedance, 5" trace CL = 4 pf | — | 0.6 | 0.95 | ns |
| Rise/Fall Time, 1.8 V (20-80%) | t _R /t _F | 50 Ω impedance, 5" trace CL = 4 pf | — | 0.75 | 1.3 | ns |
| Rise/Fall Time, 1.5 V (20-80%) | t _R /t _F | 50 Ω impedance, 5" trace CL = 4 pf | — | 0.9 | 1.3 | ns |
| CMOS Output Resistance (Single Strength) | | 3.3 V | — | 46 | — | Ω |
| | | 2.5 V | — | 48 | — | Ω |
| | | 1.8 V | — | 53 | — | Ω |
| | | 1.5 V | — | 58 | — | Ω |
| CMOS Output Resistance (Double Strength) | | 3.3 V | — | 23 | — | Ω |
| | | 2.5 V | — | 24 | — | Ω |
| | | 1.8 V | — | 27 | — | Ω |
| | | 1.5 V | — | 29 | — | Ω |
| CMOS Output Voltage | V _{OH} | -4 mA load | V _{DDO} -0.3 | — | — | V |
| | V _{OL} | 4 mA load | — | — | 0.3 | V |
| Duty Cycle | DC | XO and PLL mode | 45 | — | 55 | % |

Table 5.9. Performance Characteristics(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|-----------------------------|--|-----|------|-----|-------|
| Power Ramp | t _{VDD} | 0 V to V _{DDmin} | 0.1 | — | 10 | ms |
| Initialization Time ¹ | t _{initialization} | Time for I ² C to become operational after core supply exceeds V _{DDmin} | — | — | 15 | ms |
| Clock Stabilization from Power-up | t _{STABLE} | Time for clock outputs to appear after POR | — | 15 | 25 | ms |
| Input to Output Propagation Delay | t _{PROP} | Buffer mode (PLL Bypass) | — | 2.5 | 4 | ns |
| Spread Spectrum PP Frequency Deviation ² | SSPKDEV | MultiSynth Output < 250 MHz | 0.1 | — | 2.5 | % |
| 0.5% Spread Frequency Deviation ² | SSDEV | MultiSynth Output < 250 MHz | 0.4 | 0.45 | 0.5 | % |
| Spread Spectrum Modulation Rate ^{2, 3} | SSMOD | MultiSynth Output < 250 MHz | 30 | 31.5 | 33 | kHz |

Notes:

1. Update rate via I²C is also limited by the time it takes to perform a write operation.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and 250 MHz.
3. Default value is ~31.5 kHz.

Table 5.10. Jitter Performance Specifications(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Typ | Max | Units |
|--|------------------|---|------|-----|----------|
| Jitter Generation, Locked to External 25 MHz Clock | J _{GEN} | INT Mode 12 kHz – 20 MHz ^{1,2} | 210 | 280 | fs RMS |
| | | FRAC/DCO Mode 12 kHz – 20 MHz ^{3,5} | 250 | | fs RMS |
| | J _{PER} | Derived from integrated phase noise at a BER of 1e-12 | 3.3 | | ps Pk-Pk |
| | J _{CC} | | 3.1 | | ps Pk |
| | J _{PER} | N = 10, 000 cycles Integer or Fractional Mode. ^{2,3} Measured in the time domain. Performance is limited by the noise floor of the equipment. | 12 | | ps Pk-Pk |
| | J _{CC} | | 11 | | ps Pk |
| Jitter Generation, Locked to External 25 MHz Crystal | J _{GEN} | INT Mode 12 kHz – 20 MHz ^{1,2} | 190 | 240 | fs RMS |
| | | FRAC/DCO Mode 12 kHz – 20 MHz ^{3,5} | 250 | | fs RMS |
| | J _{PER} | Derived from integrated phase noise at a BER of 1e-12 | 3.5 | | ps Pk-Pk |
| | J _{CC} | | 3.1 | | ps Pk |
| | J _{PER} | N = 10, 000 cycles Integer or Fractional Mode. ^{2,3} Measured in the time domain. Performance is limited by the noise floor of the equipment. | 12 | | ps Pk-Pk |
| | J _{CC} | | 11 | | ps Pk |
| Jitter Generation, Locked to Embedded 50 MHz Crystal | J _{GEN} | INT Mode 12 kHz – 20 MHz ^{1,2} | 175 | 215 | fs RMS |
| | | FRAC/DCO Mode 12 kHz – 20 MHz ^{3,5} | 250 | | fs RMS |
| | J _{PER} | Derived from integrated phase noise at a BER of 1e-1 | 3.2 | | ps Pk-Pk |
| | J _{CC} | | 2.8 | | ps Pk |
| | J _{PER} | N = 10, 000 cycles Integer or Fractional Mode. ^{2,3} Measured in the time domain. Performance is limited by the noise floor of the equipment. | 12 | | ps Pk-Pk |
| | J _{CC} | | 11 | | ps Pk |
| Power Supply Noise Rejection ⁶ | PSNR | 25 kHz | -100 | — | dBc |
| | | 50 kHz | -97 | — | |
| | | 100 kHz | -72 | — | |
| | | 500 kHz | -83 | — | |
| | | 1 MHz | -91 | — | |

| Parameter | Symbol | Test Condition | Typ | Max | Units |
|--|--------|----------------|-----|-----|-------|
| Notes: | | | | | |
| 1. INT jitter generation test conditions $f_{OUT} = 156.25$ MHz LVPECL. | | | | | |
| 2. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value. | | | | | |
| 3. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer. | | | | | |
| 4. All jitter data in this table is based upon all output formats being differential. When LVCMOS outputs are used, there is the potential that the output jitter may increase due to the nature of LVCMOS outputs. If your configuration implements any LVCMOS output and any output is required to have jitter less than 3 ps RMS, contact Skyworks for support to validate your configuration and ensure the best jitter performance. | | | | | |
| 5. FRAC jitter generation test conditions $f_{OUT} = 150$ MHz LVPECL. | | | | | |
| 6. Measured at 156.25 MHz carrier frequency. Carrier power of -1.5 dBm. 100 mVpp sine wave noise added and noise spur amplitude measured.. | | | | | |

Table 5.11. PCI-Express Clock Outputs (100 MHz HCSL)¹

($V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8\text{ V to }3.3\text{ V }+10\%/ -5\%$, $V_{DDO} = 1.8\text{ V } \pm 5\%$, $2.5\text{ V } \pm 5\%$, or $3.3\text{ V } \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Test Condition | SSC On/Off | Typ | Max | Units |
|---------------------------|--|------------|-------|-------|--------|
| PCIe Gen 1.1 | Includes PLL BW 1.5–22 MHz, Peaking = 3 dB, Td = 10 ns, Ftrk = 1.5 MHz with BER = $1\text{E-}12$ ² | Off | 11 | 19 | ps RMS |
| | | On | 22 | 30 | ps RMS |
| PCIe Gen 2.1 | Includes PLL BW 5 MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, Low Band, $F < 1.5\text{ MHz}$ | Off | 0.02 | 0.026 | ps RMS |
| | | On | 0.12 | 0.21 | ps RMS |
| | Includes PLL BW 5 MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, High Band, $1.5\text{ MHz} < F < \text{Nyquist}$ ² | Off | 0.2 | 0.31 | ps RMS |
| | | On | 0.8 | 1.3 | ps RMS |
| PCIe Gen 3.0 Common Clock | Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2dB and 1dB, Td=12 ns, CDR = 10 MHz ^{2, 3} | Off | 0.06 | 0.1 | ps RMS |
| | | On | 0.26 | 0.36 | ps RMS |
| PCIe Gen 3.0 SRIS | Includes PLL BW 4 MHz Peaking = 2 dB and 1 dB, Td = 12 ns CDR = 10 MHz ^{2, 3} | On | 0.31 | 0.36 | ps RMS |
| PCIe Gen 4.0 Common Clock | Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1 dB, Td=12 ns, CDR = 10 MHz ^{2, 3} | Off | 0.05 | 0.1 | ps RMS |
| | | On | 0.26 | 0.36 | ps RMS |
| PCIe Gen 4.0 SRIS | Includes PLL BW 4 MHz Peaking = 2 dB and 1 dB, Td = 12 ns CDR = 10 MHz ^{2, 3} | On | 0.31 | 0.36 | ps RMS |
| PCIe Gen 5.0 Common Clock | Includes PLL BW 500 kHz to 1.8 MHz, CDR = 20 MHz ^{2, 3} | Off | 0.025 | 0.04 | ps RMS |
| | | On | 0.1 | 0.15 | ps RMS |
| PCIe Gen 5.0 SRIS | Includes PLL BW 500 kHz to 1.8 MHz, CDR = 20 MHz ^{2, 3} | On | 0.08 | 0.1 | ps RMS |
| PCIe Gen 6.0 Common Clock | Includes PLL BW 500 kHz to 1.0 MHz, CDR = 10 MHz ^{2, 3} | Off | 0.013 | 0.022 | ps RMS |
| | | On | 0.043 | 0.077 | ps RMS |
| PCIe Gen 6.0 SRIS | Includes PLL BW 500 kHz to 1.0 MHz, CDR = 10 MHz ^{2, 3} | On | 0.062 | 0.087 | ps RMS |

Notes:

- All jitter data in this table is based upon all output formats being differential. When LVCMOS outputs are used, there is the potential that the output jitter may increase due to the nature of LVCMOS outputs. If your configuration implements any LVCMOS output and any output is required to have jitter less than 3 ps RMS, contact Skyworks for support to validate your configuration and ensure the best jitter performance.
- All output clocks 100 MHz HCSL format. Jitter data taken from Clock Jitter Tool.
- Excludes oscilloscope sampling noise.

Table 5.12. Fanout Mode Additive Jitter Performance Specifications(V_{DD} = V_{D_{DDA}} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C)

| Parameter | Symbol | Test Condition | Typ | Max | Units |
|------------------------------------|--------|---|-----------------|-----|--------|
| Additive Phase Jitter | | 156.25 MHz, 12 kHz–20 MHz ¹ , LVDS (slow mode) | 130 (LVDS slow) | 170 | fs RMS |
| | | 156.25 MHz, 12 kHz–20 MHz, LVDS (fast mode) | 120 | 150 | fs RMS |
| | | 156.25 MHz, 12 kHz–20 MHz, LVPECL ¹ | 110 | 140 | fs RMS |
| | | 156.25 MHz, 12 kHz–20 MHz, HCSL ₁ | 120 | 150 | fs RMS |
| PCIe Gen 3/4 Additive Phase Jitter | | 100 MHz HCSL input/outputs Includes PLL BW 2–4 MHz, CDR = 10 MHz ^{2, 3, 4, 5} | 28 | 36 | fs RMS |
| PCIe Gen 5.0 Additive Phase Jitter | | Includes PLL BW 500 kHz to 1.8 MHz, CDR = 20 MHz ^{2, 3, 4, 5} | 21 | 27 | fs RMS |
| PCIe Gen 6.0 Additive Phase Jitter | | Includes PLL BW 500 kHz to 1.0 MHz, CDR = 10 MHz ^{2, 3, 4, 5} | 13 | 17 | fs RMS |

Note:

1. Measured with differential input on CLKIN_2, bypassing the PLL to any output.
2. Skyworks' PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = $\sqrt{\text{output jitter}^2 - \text{input jitter}^2}$. Input used is 100 MHz from Si5340.
3. Measurements on 100 MHz output use the template file in the PCIe Clock Jitter Tool.
4. For complete PCIe specifications, visit www.pcisig.com.
5. Input clock slew rate of 3.0 V/ns used for jitter measurements.

Table 5.13. QFN Thermal Characteristics (Si5332A/B/C/D Only)

| Parameter | Symbol | Test Condition ¹ | Value | Units |
|--|---------------|-----------------------------|-------|-------|
| Si5332 — 48 QFN | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 27.2 | °C/W |
| | | Air Flow 1 m/s | 22.7 | |
| | | Air Flow 2 m/s | 21.8 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 14 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 11.3 | |
| | ψ_{JB} | Still Air | 9.5 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.4 | |
| Si5332 — 40 QFN | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 23.1 | °C/W |
| | | Air Flow 1 m/s | 17.5 | |
| | | Air Flow 2 m/s | 16.5 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 14.1 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 11.4 | |
| | ψ_{JB} | Still Air | 3.4 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.4 | |
| Si5332 — 32 QFN | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 28.4 | °C/W |
| | | Air Flow 1 m/s | 24 | |
| | | Air Flow 2 m/s | 23 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 18.5 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 15.1 | |
| | ψ_{JB} | Still Air | 7 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.5 | |
| Note: | | | | |
| 1. Based on JEDEC standard 4-layer PCB. | | | | |

Table 5.14. LGA Thermal Characteristics (Si5332E/F/G/H/L Only)

| Parameter | Symbol | Test Condition ¹ | Value | Units |
|--|---------------|-----------------------------|-------|-------|
| Si5332 — 48 LGA | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 31.5 | °C/W |
| | | Air Flow 1 m/s | 28.5 | |
| | | Air Flow 2 m/s | 27.4 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 19.4 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 20.2 | |
| | ψ_{JB} | Still Air | 20.2 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.4 | |
| Si5332 — 40 LGA | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 29.9 | °C/W |
| | | Air Flow 1 m/s | 26.5 | |
| | | Air Flow 2 m/s | 25.3 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 19.6 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 18.9 | |
| | ψ_{JB} | Still Air | 18.9 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.4 | |
| Si5332 — 32 LGA | | | | |
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still Air | 35.21 | °C/W |
| | | Air Flow 1 m/s | 32.9 | |
| | | Air Flow 2 m/s | 31.7 | |
| Thermal Resistance, Junction to Case | θ_{JC} | | 19.8 | |
| Thermal Resistance, Junction to Board | θ_{JB} | | 24.3 | |
| | ψ_{JB} | Still Air | 24.3 | |
| Thermal Resistance, Junction to Top Center | ψ_{JT} | | 0.5 | |
| Note: | | | | |
| 1. Based on Si5332 CEVB, see Si5332 Reference Manual for layout information. | | | | |

Table 5.15. Absolute Maximum Ratings ^{1,2,3}

| Parameter | Symbol | Test Condition | Value | Units |
|--|-----------------|------------------------|------------------|-------|
| Storage Temperature Range | T_{STG} | | -55 to +150 | °C |
| DC Supply Voltage | V_{DD} | | -0.5 to 3.8 | V |
| | V_{DDA} | | -0.5 to 3.8 | V |
| | $V_{DD_{xtal}}$ | | -0.5 to 3.8 | V |
| | V_{DDO} | | -0.5 to 3.8 | V |
| Input Voltage Range | V_I | XIN/XOUT | -0.3 to 1.3 | V |
| Latch-up Tolerance | LU | | JESD78 Compliant | |
| ESD Tolerance | HBM | 100 pF, 1.5 k Ω | 2.0 | kV |
| Junction Temperature | T_{JCT} | | -55 to 125 | °C |
| Soldering Temperature | T_{PEAK} | | 260 | °C |
| Soldering Temperature Time at T_{PEAK} | T_P | | 20 to 40 | sec |

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to https://www.skyworksinc.com/product_certificate.aspx.
3. The device is compliant with JEDEC J-STD-020.

6. Pin Descriptions

6.1 Pin Descriptions (48-Pin)



Figure 6.1. 48-QFN

Table 6.1. Si5332 Pin Descriptions (48-Pin)

| Pin Number | Pin Name | Pin Type | Function |
|------------|-----------|----------|---|
| 1 | VDD_DIG | P | Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL. |
| 2 | CLKIN_2 | I | These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| 3 | CLKIN_2b | I | |
| 4 | VDD_XTAL | P | Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG. |
| 5 | XA/CLKIN1 | I or P | Si5332A/B/C/D: |
| 6 | XB | I or P | These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Refer to Section 5. Electrical Specifications for recommended crystal specifications. Si5332E/F/G/H/L (Embedded Crystal) No Connect. Do not connect pins 5 or 6 to anything. |
| 7 | CLKIN_3 | I | These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_3 and CLKIN_3b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| 8 | CLKIN_3b | I | |
| 9 | VDDA | P | Core Supply Voltage. Connect to 1.8–3.3 V. See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL. |
| 10 | INPUT1 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 11 | INPUT2 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 12 | INPUT3 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 13 | SCLK | I | Serial Clock Input This pin functions as the serial clock input for I ² C. SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I ² C bus pull-up) to same voltage as VDD_DIG. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 14 | SDA | I/O | <p>Serial Data Interface</p> <p>This is the bidirectional data pin (SDA) for the I²C mode.</p> <p>SDA is a digital open-drain bi-directional internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I²C bus pull-up) to same voltage as VDD_DIG.</p> |
| 15 | OUT0b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 16 | OUT0 | O | |
| 17 | VDDO0 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 18 | OUT1b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 19 | OUT1 | O | |
| 20 | VDDO1 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1 and OUT2</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 21 | OUT2b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 22 | OUT2 | O | |
| 23 | INPUT4 | I | <p>Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.</p> |
| 24 | VDDO2 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT3, OUT4, and OUT5</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|--|
| 25 | OUT3b | O | Output Clock |
| 26 | OUT3 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 27 | OUT4b | O | Output Clock |
| 28 | OUT4 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 29 | OUT5b | O | Output Clock |
| 30 | OUT5 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 31 | OUT6b | O | Output Clock |
| 32 | OUT6 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 33 | OUT7b | O | Output Clock |
| 34 | OUT7 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 35 | OUT8b | O | Output Clock |
| 36 | OUT8 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 37 | VDDO3 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6, OUT7, and OUT8 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 38 | INPUT5 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 39 | VDDO4 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT9</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 40 | OUT9b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 41 | OUT9 | O | |
| 42 | INPUT6 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 43 | INPUT7 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 44 | VDDO5 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT10 and OUT11</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 45 | OUT10b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 46 | OUT10 | O | |
| 47 | OUT11b | O | <p>Output Clock</p> <p>These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.</p> |
| 48 | OUT11 | O | |
| 49 | GND PAD | P | <p>Ground Pad</p> <p>This pad provides electrical and thermal connection to ground and must be connected for proper operation.</p> |

6.2 Pin Descriptions (40-Pin)



Figure 6.2. 40-QFN

Table 6.2. Si5332 Pin Descriptions (40-Pin)

| Pin Number | Pin Name | Pin Type | Function |
|------------|-----------|----------|---|
| 1 | VDD_DIG | P | Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL. |
| 2 | CLKIN_2 | I | These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| 3 | CLKIN_2b | I | |
| 4 | VDD_XTAL | P | Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG. |
| 5 | XA/CLKIN1 | I or P | Si5332A/B/C/D: |
| 6 | XB | I or P | These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Refer to Section 5. Electrical Specifications for recommended crystal specifications. Si5332E/F/G/H/L (Embedded Crystal) No Connect. Do not connect pins 5 or 6 to anything. |
| 7 | CLKIN_3 | I | These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_3 and CLKIN_3b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| 8 | CLKIN_3b | I | |
| 9 | VDDA | P | Core Supply Voltage. Connect to 1.8–3.3 V. See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL. |
| 10 | INPUT1 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 11 | SCLK | I | Serial Clock Input This pin functions as the serial clock input for I ² C. SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I ² C bus pull-up) to same voltage as VDD_DIG. |
| 12 | SDA | I/O | Serial Data Interface This is the bidirectional data pin (SDA) for the I ² C mode. SDA is a digital open-drain bi-directional internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I ² C bus pull-up) to same voltage as VDD_DIG. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 13 | OUT0b | O | Output Clock |
| 14 | OUT0 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 15 | VDDO0 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 16 | OUT1b | O | Output Clock |
| 17 | OUT1 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 18 | VDDO1 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 19 | INPUT2 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 20 | INPUT3 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 21 | OUT2b | O | Output Clock |
| 22 | OUT2 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 23 | OUT3b | O | Output Clock |
| 24 | OUT3 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 25 | VDDO2 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT2 and OUT3 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 26 | OUT4b | O | Output Clock |
| 27 | OUT4 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 28 | VDDO3 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT4 and OUT5 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 29 | OUT5b | O | Output Clock |
| 30 | OUT5 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 31 | INPUT4 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 32 | INPUT5 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 33 | VDDO4 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 34 | OUT6b | O | Output Clock |
| 35 | OUT6 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 36 | INPUT6 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 37 | INPUT7 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 38 | OUT7b | O | Output Clock |
| 39 | OUT7 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 40 | VDDO5 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT7</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 41 | GND PAD | P | <p>Ground Pad</p> <p>This pad provides electrical and thermal connection to ground and must be connected for proper operation.</p> |

6.3 Pin Descriptions (32-Pin)



Figure 6.3. 32-QFN

Table 6.3. Si5332 Pin Descriptions (32-Pin)

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 1 | VDD_DIG | P | Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL. |
| 2 | CLKIN_2 | I | These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are un-used and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused". |
| 3 | CLKIN_2b | I | |
| 4 | VDD_XTAL | P | Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG." |

| Pin Number | Pin Name | Pin Type | Function |
|------------|-----------|----------|---|
| 5 | XA/CLKIN1 | I or P | Si5332A/B/C/D |
| 6 | XB | I or P | <p>These pins are used for an optional XTAL input when operating the device in asynchronous mode (i.e. free-run mode). Refer to Section 5. Electrical Specifications for recommended crystal specifications.</p> <p>Si5332E/F/G/H/L (Embedded Crystal)</p> <p>No Connect. Do not connect these pins 5 or 6 to anything.</p> |
| 7 | VDDA | P | <p>Core Supply Voltage. Connect to 1.8–3.3 V.</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Must be connected to same voltage as VDD_DIG and VDD_XTAL.</p> |
| 8 | INPUT1 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 9 | SCLK | I | <p>Serial Clock Input</p> <p>This pin functions as the serial clock input for I²C.</p> <p>SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I²C bus pull-up) to same voltage as VDD_DIG.</p> |
| 10 | SDA | I/O | <p>Serial Data Interface</p> <p>This is the bidirectional data pin (SDA) for the I²C mode.</p> <p>SDA is a digital open-drain bi-directional internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I²C bus pull-up) to same voltage as VDD_DIG.</p> |
| 11 | OUT0b | O | Output Clock |
| 12 | OUT0 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 13 | VDDO0 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |
| 14 | OUT1b | O | Output Clock |
| 15 | OUT1 | O | These output clocks support a programmable signal swing & common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 16 | VDDO1 | P | <p>Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1</p> <p>See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations.</p> <p>Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.</p> |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|---|
| 17 | INPUT2 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 18 | OUT2b | O | Output Clock These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 19 | OUT2 | O | |
| 20 | VDDO2 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT2 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 21 | OUT3b | O | Output Clock These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 22 | OUT3 | O | |
| 23 | VDDO3 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT3 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 24 | INPUT3 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 25 | VDDO4 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT4 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 26 | OUT4b | O | Output Clock These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 27 | OUT4 | O | |
| 28 | INPUT4 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |
| 29 | INPUT5 | I | Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for. |

| Pin Number | Pin Name | Pin Type | Function |
|------------|----------|----------|--|
| 30 | OUT5b | O | Output Clock |
| 31 | OUT5 | O | These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.5.2 Differential Output Terminations and 3.5.3 LVCMOS Output Terminations . Unused outputs should be left unconnected. |
| 32 | VDDO5 | P | Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT5 See the <i>Si5332 Family Reference Manual</i> for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption. |
| 33 | GND PAD | P | Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation. |

7. Package Outline

7.1 Si5332 6x6 mm 48-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D)

The figure below illustrates the package details for the Si5332A/B/C/D in 48-QFN. The table below lists the values for the dimensions shown in the illustration.



Figure 7.1. 48-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.00 BSC | | |
| D2 | 3.5 | 3.6 | 3.7 |
| e | 0.40 BSC | | |
| E | 6.00 BSC | | |
| E2 | 3.5 | 3.6 | 3.7 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |

| Dimension | Min | Nom | Max |
|--|-----|-----|-----|
| Notes: <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.3. This drawing conforms to the JEDEC Solid State Outline MO-220.4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | | |

7.2 Si5332 6x6 mm 40-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D)

The figure below illustrates the package details for the Si5332A/B/C/D in 40-QFN. The table below lists the values for the dimensions shown in the illustration.



Figure 7.2. 40-Pin Quad Flat No-Lead (QFN)

Table 7.2. Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.00 BSC | | |
| D2 | 4.35 | 4.50 | 4.65 |
| e | 0.50 BSC | | |
| E | 6.00 BSC | | |
| E2 | 4.35 | 4.50 | 4.65 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

7.3 Si5332 5x5 mm 32-QFN Package Diagram, External Crystal Versions (Si5332A/B/C/D)

The figure below illustrates the package details for the Si5332A/B/C/D 32-QFN option. The table below lists the values for the dimensions shown in the illustration.



Figure 7.3. 32-Pin Quad Flat No-Lead (QFN)

Table 7.3. Package Dimensions

| Dimension | MIN | NOM | MAX |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D/E | 4.90 | 5.00 | 5.10 |
| D2/E2 | 3.40 | 3.50 | 3.60 |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | --- | --- |
| R | 0.09 | --- | 0.14 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |

| Dimension | MIN | NOM | MAX |
|-----------|-----|------|-----|
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.4 Si5332 6x6 mm 48-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L)

The figure below illustrates the package details for the Si5332E/F/G/H/L in 48-LGA. The table lists the values for the dimensions shown in the illustration.

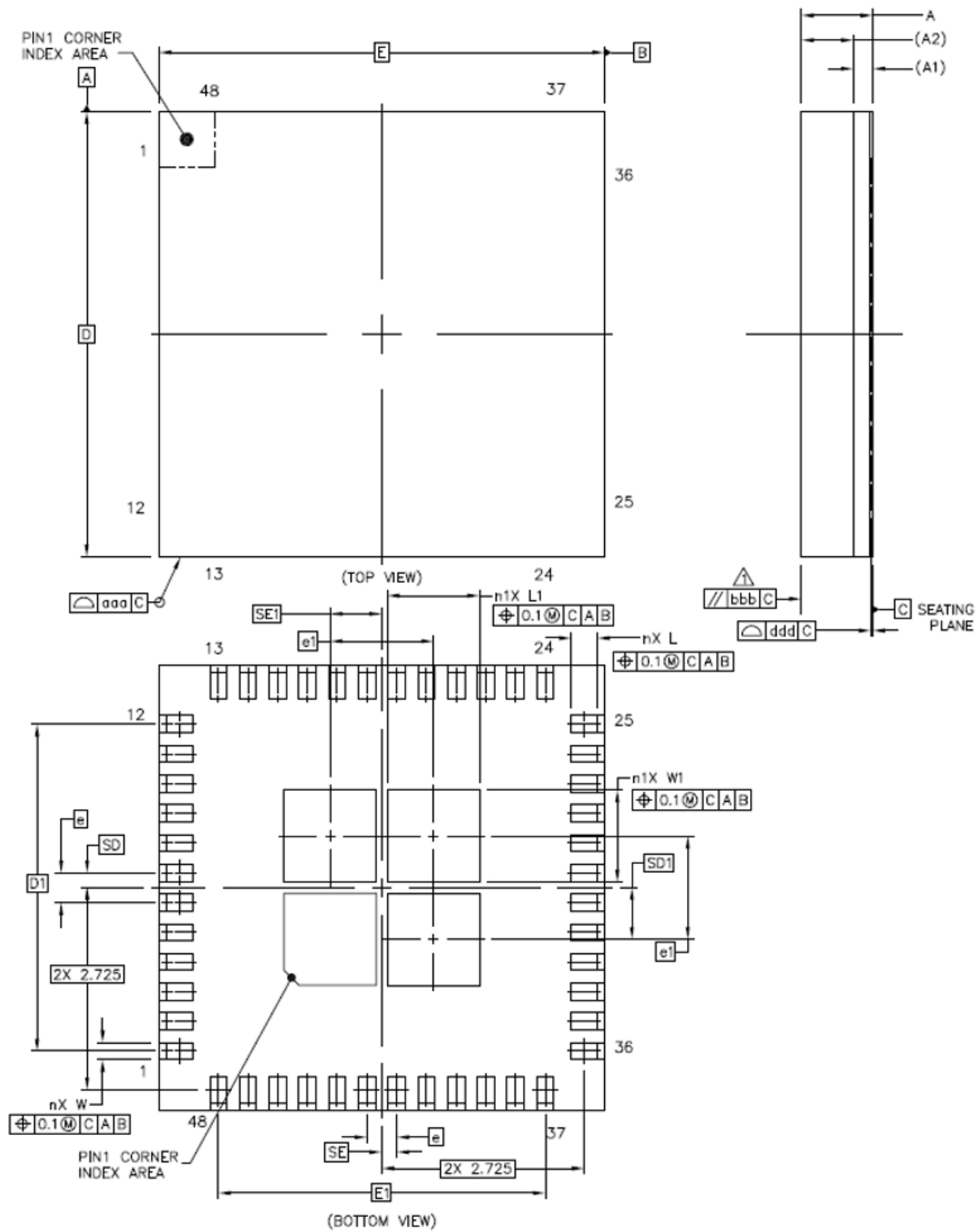


Figure 7.4. 48-Pin LGA

Table 7.4. Package Dimensions

| Dimension | Minimum | Nominal | Maximum |
|-----------|-----------|---------|---------|
| A | — | — | 1.1 |
| A1 | 0.26 REF | | |
| A2 | 0.7 REF | | |
| D | 6 BSC | | |
| E | 6 BSC | | |
| W | 0.18 | 0.23 | 0.28 |
| L | 0.3 | 0.35 | 0.4 |
| e | 0.4 BSC | | |
| n | 48 | | |
| D1 | 4.4 BSC | | |
| E1 | 4.4 BSC | | |
| SD | 0.2 BSC | | |
| SE | 0.2 BSC | | |
| SD1 | 0.695 BSC | | |
| SE1 | 0.695 BSC | | |
| W1 | 1.19 | 1.24 | 1.29 |
| L1 | 1.19 | 1.24 | 1.29 |
| e1 | 1.39 | | |
| n1 | 4 | | |
| aaa | 0.1 | | |
| bbb | 0.1 | | |
| ddd | 0.08 | | |
| eee | — | | |
| fff | — | | |

Note:

1. Dimensions in parentheses are reference.
2. All dimensions are in millimeters (mm).
3. Dimensioning and Tolerances per ANSI Y14.5M-1994.

7.5 Si5332 6x6 mm 40-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L)

The figure below illustrates the package details for the Si5332E/F/G/H/L in 40-LGA. The table below lists the values for the dimensions shown in the illustration.



Figure 7.5. 40-Pin LGA

Table 7.5. Package Dimensions

| | Symbol | Dimensions | | |
|-----------------------------|--------|------------|------|------|
| | | Min | Typ | Max |
| Total Thickness | A | 0.9 | 1 | 1.1 |
| Substrate Thickness | A1 | 0.26 REF | | |
| Mold Thickness | A2 | 0.7 REF | | |
| Body Size | D | 6 BSC | | |
| | E | 6 BSC | | |
| Lead Width | W | 0.18 | 0.23 | 0.28 |
| Lead Length | L | 0.3 | 0.35 | 0.4 |
| Lead Pitch | e | 0.5 BSC | | |
| Edge Ball Center to Center | D1 | 4.5 BSC | | |
| | E1 | 4.5 BSC | | |
| Body Center to Contact Ball | SD | 0.25 BSC | | |
| | SE | 0.25 BSC | | |
| | SD1 | 0.695 BSC | | |
| | SE1 | 0.695 BSC | | |
| EP Width | W1 | 1.19 | 1.24 | 1.29 |
| EP Length | L1 | 1.19 | 1.24 | 1.29 |
| EP Pitch | e1 | 1.39 BSC | | |
| EP Count | n1 | 4 | | |
| Package Edge Tolerance | aaa | 0.1 | | |
| Mold Flatness | bbb | 0.1 | | |
| Coplanarity | ddd | 0.08 | | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.6 Si5332 5x5 mm 32-LGA Package Diagram, Embedded Crystal Versions (Si5332E/F/G/H/L)

The figure below illustrates the package details for the Si5332E/F/G/H/L 32-LGA option. The table below lists the values for the dimensions shown in the illustration.



Figure 7.6. 32-Pin LGA

Table 7.6. Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.90 | 1.0 | 1.1 |
| A1 | 0.26 REF | | |
| A2 | 0.70 REF | | |
| b | 0.2 | 0.25 | 0.30 |
| D | 5.00 BSC | | |
| D2 | 2.1 REF | | |
| E | 5.00 BSC | | |
| E2 | 2.1 REF | | |
| e | 0.50 BSC | | |
| L | 0.32 | 0.37 | 0.42 |
| L1 | 0.10 REF | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.08 | | |
| ddd | 0.10 | | |
| eee | 0.08 | | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1 Si5332A/B/C/D 48-QFN Land Pattern



Figure 8.1. 48-QFN Land Pattern

Table 8.1. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 5.90 |
| C2 | 5.90 |
| e | 0.40 BSC |
| X1 | 0.20 |
| Y1 | 0.85 |
| X2 | 3.60 |
| Y2 | 3.60 |

| Dimension | mm |
|--|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none"> 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none"> 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads. 4. The stencil aperture to center land pads size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none"> 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8.2 Si5332A/B/C/D 40-QFN Land Pattern



Figure 8.2. 40-QFN Land Pattern

Table 8.2. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 5.90 |
| C2 | 5.90 |
| e | 0.50 BSC |
| X1 | 0.30 |
| Y1 | 0.85 |
| X2 | 4.65 |
| Y2 | 4.65 |

| Dimension | mm |
|--|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.4. The stencil aperture to center land pad size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8.3 Si5332A/B/C/D 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for Si5332 in 32-QFN package. The table below lists the values for the dimensions shown in the illustration.



Figure 8.3. 32-QFN Land Pattern

Table 8.3. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 4.90 |
| C2 | 4.90 |
| e | 0.50 BSC |
| X1 | 0.30 |
| Y1 | 0.85 |
| X2 | 3.60 |
| Y2 | 3.60 |

| Dimension | mm |
|--|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.4. The stencil aperture to center land pad size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8.4 Si5332E/F/G/H/L 48-LGA Land Pattern



Figure 8.4. 48-LGA Land Pattern

Table 8.4. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 5.52 |
| C2 | 5.52 |
| e | 0.40 BSC |
| X1 | 0.20 |
| Y1 | 0.50 |
| X2 | 2.60 |
| Y2 | 2.60 |

| Dimension | mm |
|---|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none"> 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none"> 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads. 4. The package e-pad is partitioned as a 2x2 array. The stencil aperture to land pad size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none"> 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8.5 Si5332E/F/G/H/L 40-LGA Land Pattern



Figure 8.5. 40-LGA Land Pattern

Table 8.5. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 5.52 |
| C2 | 5.52 |
| e | 0.50 BSC |
| X1 | 0.30 |
| Y1 | 0.50 |
| X2 | 2.60 |
| Y2 | 2.60 |

| Dimension | mm |
|---|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none"> 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none"> 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads. 4. The package e-pad is partitioned as a 2x2 array. The stencil aperture to land pad size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none"> 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8.6 Si5332E/F/G/H/L 32-LGA Land Pattern

The figure below illustrates the PCB land pattern details for Si5332 in 32-LGA package. The table below lists the values for the dimensions shown in the illustration.



Figure 8.6. 32-LGA Land Pattern

Table 8.6. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|----------|
| C1 | 4.50 |
| C2 | 4.50 |
| e | 0.50 BSC |
| X1 | 0.30 |
| Y1 | 0.45 |
| X2 | 2.20 |
| Y2 | 2.20 |

| Dimension | mm |
|---|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.4. The stencil aperture to land pad size recommendation is 70% paste coverage. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

9. Top Marking



Figure 9.1. Si5332 Top Marking

Table 9.1. Top Marking Explanation

| Line | Characters | Description |
|------|------------|--|
| 1 | Si5332g | Base part number and device grade g = Device Grade (A, B, C, D, E, F, G, H, L) |
| 2 | R-GMp | R = Product revision (see Ordering Guide for current revision) - = Dash character GM = Package (QFN/LGA) and temperature range (-40 to +85C) p = Package Size <ul style="list-style-type: none"> • 1 = 6-output, 32-pin • 2 = 8-output, 40-pin • 3 = 12-output, 48-pin |
| | Rxxxx | R = Product revision (see ordering guide for current revision) xxxxx = Customer specific NVM sequence number. NVM code assigned for custom, factory pre-programmed devices using ClockBuilder Pro. See Ordering Guide for more information. |
| 3 | TTTTTT | Manufacturing trace code. |
| 4 | YYWW | Year (YY) and work week (WW) of package assembly |

10. Revision History

Revision 206453A

January, 2023

- Changed decimal-based revision number to alphanumeric code.
- Added “PCIe Gen1/2/3/4/5/6 compliant” to Key Features on front page.
- Added note stating that temp stability is inclusive of initial accuracy in [Table 5.5 Embedded Crystal Specifications on page 25](#).
- Updated PSNR units from dB to dBc in [Table 5.10 Jitter Performance Specifications on page 31](#).
- Updated [7.4 Si5332 6x6 mm 48-LGA Package Diagram, Embedded Crystal Versions \(Si5332E/F/G/H/L\)](#).
- Added PCIe Gen 6.0 specs in [Table 5.11 PCI-Express Clock Outputs \(100 MHz HCSL\)¹ on page 33](#).
- Added PCIe Gen 6.0 specs in [Table 5.12 Fanout Mode Additive Jitter Performance Specifications on page 34](#).

Revision 1.3

March, 2020

- Updated 48-LGA and 40-LGA package outline drawings.
- Updated stencil design notes in PCB land pattern diagram sections for all QFN and LGA packages.
- Added L-grade ordering option.

Revision 1.2

February, 2019

- Modified some values in various Electrical Specifications tables.
- Removed reference to QFN and/or added LGA.
- Added LGA Thermal Characteristics table in the Electrical Specifications section.

Revision 1.1

August, 2018

- Updated RMS phase jitter specifications in clock generator and buffer modes
- Added PCIe additive phase jitter specifications in buffer mode
- Separated LVDS Tr/Tf, common mode, and swing specifications into slow and fast mode
- Updated HCSL Tr/Tf max specification from 400 ps to 420 ps
- Increased max output frequency range to 333.33 MHz
- Added package thermal characteristics table for E/F/G/H embedded crystal grade devices

Revision 1.0

February, 2018

- Updated Si5332 5x5 mm 32-QFN package diagram for external crystal versions
- Updated Si5332 32-QFN land pattern
- Updated jitter specifications for embedded crystal reference ([Table 5.7 Differential Clock Output Specifications on page 27](#))

Revision 0.7

September, 2017

- Initial release.



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