THE DATASHEET OF

SI5335D-B08168-GM

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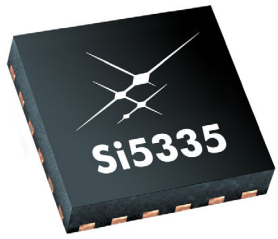
Si5335

Web-Customizable, Any-Frequency, Any-Output Quad Clock Generator/Buffer

Features

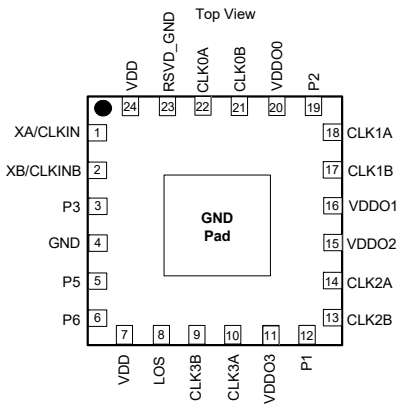
- Low power MultiSynth™ technology enables independent, any-frequency synthesis of four frequencies
- Configurable as a clock generator or clock buffer device
- Three independent, user-assignable, pin-selectable device configurations
- Highly-configurable output drivers with up to four differential outputs, eight single-ended clock outputs, or a combination of both
- Low phase jitter of 0.7 ps RMS
- Flexible input reference:
  - External crystal: 25 or 27 MHz
  - CMOS input: 10 to 200 MHz
  - SSTL/HSTL input: 10 to 350 MHz
  - Differential input: 10 to 350 MHz
- Independently configurable outputs support any frequency or format:
  - LVPECL/LVDS/CML: 1 to 350 MHz
  - HCSL: 1 to 250 MHz
  - CMOS: 1 to 200 MHz
  - SSTL/HSTL: 1 to 350 MHz
- Independent output voltage per driver: 1.5, 1.8, 2.5, or 3.3 V
- Single supply core with excellent PSRR: 1.8, 2.5, 3.3 V
- Up to five user-assignable pin functions simplify system design: SSENB (spread spectrum control), RESET, Master OEB or OEB per pin, and Frequency plan select (FS1, FS0)
- Loss of signal alarm
- PCIe Gen 1/2/3/4 common clock compliant
- PCIe Gen 3 SRNS Compliant
- Two selectable loop bandwidth settings: 1.6 MHz or 475 kHz
- Easy to customize with web-based utility
- Small size: 4 x 4 mm, 24-QFN
- Low power (core):
  - 45 mA (PLL mode)
  - 12 mA (Buffer mode)
- Wide temperature range: –40 to +85 °C



Ordering Information:

See page 41.

Pin Assignments



Applications

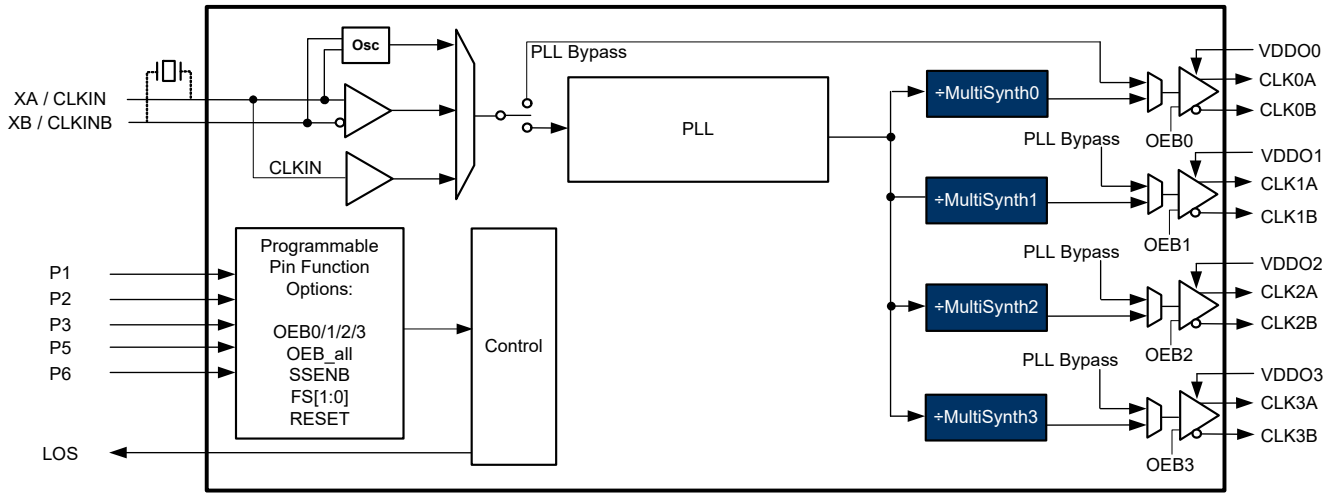
- Ethernet switch/router
- PCI Express Gen 1/2/3/4
- PCIe jitter attenuation
- DSL jitter attenuation
- Broadcast video/audio timing
- Processor and FPGA clocking
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Description

The Si5335 is a highly flexible clock generator capable of synthesizing four completely non-integer-related frequencies up to 350 MHz. The device has four banks of outputs with each bank supporting one differential pair or two single-ended outputs. Using Skyworks Solutions' patented MultiSynth fractional divider technology, all outputs are guaranteed to have 0 ppm frequency synthesis error regardless of configuration, enabling the replacement of multiple clock ICs and crystal oscillators with a single device. The Si5335 supports up to three independent, pin-selectable device configurations, enabling one device to replace three separate clock generators or buffer ICs. To ease system design, up to five user-assignable and pin-selectable control pins are provided, supporting PCIe-compliant spread spectrum control, master and/or individual output enables, frequency plan selection, and device reset. Two selectable PLL loop bandwidths support jitter attenuation in applications, such as PCIe and DSL. Through its flexible ClockBuilder Pro web configuration utility, factory-customized, pin-controlled devices are available in two weeks without minimum order quantity restrictions.

Measuring PCIe clock jitter is quick and easy with the Skyworks Solutions PCIe Clock Jitter Tool. Download it for free at https://www.skyworksinc.com/en/Application-Pages/PCI-Express-Learning-Center.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current (Clock Generator Mode)	I_{DDCG}	100 MHz on all outputs, 25 MHz refclk, clock generator mode	—	45	60	mA
Core Supply Current (Buffer Mode)	I_{DDB}	50 MHz refclk	—	12	—	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 350 MHz	—	—	30	mA
		CML, 350 MHz	—	12	—	mA
		LVDS, 350 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load	—	—	20	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load[1]	—	6	9	mA
		CMOS, 200 MHz[1,2] 3.3 V VDD0	—	13	18	mA
		CMOS, 200 MHz[1,2] 2.5 V	—	10	14	mA
		CMOS, 200 MHz[1,2] 1.8 V	—	7	10	mA
		HSTL, 350 MHz	—	—	19	mA

Notes:
1. Single CMOS driver active.
2. Measured into a 5” 50 Ω trace with 2 pF load.

Table 3. Performance Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Acquisition Time	t_{ACQ}	1.6 MHz loop bandwidth	—	—	25	ms
PLL Tracking Range	f_{TRACK}	475 kHz or 1.6 MHz loop bandwidth	5000	20000	—	ppm
PLL Loop Bandwidth	f_{BW1}	High bandwidth option	—	1.6	—	MHz
	f_{BW2}	Low bandwidth option	—	475	—	kHz
MultiSynth Frequency Synthesis Resolution	f_{RES}	Output frequency ≤ Fvco/8	0	0	1	ppb
CLKIN Loss of Signal Detect Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Release Time	t_{LOSRLS}		0.01	0.2	1	µs
POR to Output Clock Valid	t_{RDY}		—	—	2	ms
Input-to-Output Propagation Delay	t_{PROP}	Buffer Mode (PLL Bypass)	—	2.5	4	ns
Reset Minimum Pulse Width	t_{RESET}		—	—	200	ns
Output-Output Skew[1]	t_{DSKEW}	F_{OUT} ≥ 5 MHz	—	—	100	ps
Spread Spectrum PP Frequency Deviation[2]	SS_{DEV}	F_{OUT} = 100 MHz	—	–0.45	–0.5	%
Spread Spectrum Modulation Rate[3]	SS_{DEV}	F_{OUT} = 100 MHz	30	31.5	33	kHz

Notes:
1. Outputs at integer-related frequencies and using the same driver format.
2. Default value is 0.5% down spread.
3. Default value is 31.5 kHz for PCI compliance.

Table 4. Input and Output Clock Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock (AC Coupled Differential Input Clocks on Pins 1 and 2)[1]						
Frequency	f_{IN}	LVDS, LVPECL, HCSL, CML	10[2]	—	350	MHz
Differential Voltage Swing	V_{PP}	350 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time[3]	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle[3]	DC (PLL mode)	< 1 ns t_R/t_F	40	—	60	%
	DC (PLL bypass mode)	< 1 ns t_R/t_F	45	—	55	%
Input Impedance[1]	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (AC-Coupled Single-Ended Input Clock on Pin 1)						
Frequency	f_{IN}	CMOS, HSTL, SSTL	10[2]	—	200	MHz
CMOS Input Voltage Swing	V_I	200 MHz	0.8	—	1.2	Vpp
CMOS Rise/Fall Time	t_R/t_F	10%–90%	—	—	4	ns
CMOS Rise/Fall Time	t_R/t_F	20%–80%	—	—	2.3	ns
HSTL/SSTL Input Voltage	$V_{I(HSTL/SSTL)}$	200 MHz	0.4	—	1.2	V_{PP}
HSTL/SSTL Rise/Fall Time	t_R/t_F	10%–90%	—	—	1.4	ns

Notes:

1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "3.4.2. Differential Input Clocks" on page 19.
2. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
3. Applies to differential inputs. For best jitter performance, keep the midpoint peak-to-peak differential input slew rate on pins 1 and 2 faster than 0.3 V/ns.
4. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver. See "3.10.6. CML Outputs" on page 31.
5. Includes effect of internal series 22 Ω resistor.

Table 4. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Duty Cycle	DC (PLL mode)	< 1 ns t_R/t_F	40	—	60	%
	DC (PLL bypass mode)	< 1 ns t_R/t_F	45	—	55	%
Input Capacitance	C_{IN}		—	3.5	—	pF
Output Clocks (Differential)						
Frequency	f_{OUT}	LVPECL, LVDS, CML	1	—	350	MHz
		HCSL	1	—	250	MHz
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO}– 1.45 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{SEPP}	peak-to-peak single-ended swing	0.575	0.725	0.85	V_{PP}
CML Output Voltage	V_{OC}	Common Mode	—	See Note [4]	—	V
	V_{SEPP}	Peak-to-Peak Single-ended Swing	0.67	0.860	1.07	V_{PP}
Rise/Fall Time	t_R/t_F	20% to 80% LVPECL, LVDS, HCSL, CML	—	—	450	ps

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "3.4.2. Differential Input Clocks" on page 19.
2. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
3. Applies to differential inputs. For best jitter performance, keep the midpoint peak-to-peak differential input slew rate on pins 1 and 2 faster than 0.3 V/ns.
4. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver. See "3.10.6. CML Outputs" on page 31.
5. Includes effect of internal series 22 Ω resistor.

Table 4. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Duty Cycle	DC	LVPECL, LVDS, HCSL, CML	45	—	55	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	1	—	200	MHz
		SSTL, HSTL	1	—	350	MHz
CMOS 20%–80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%–80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	2.0	ns
CMOS Output Voltage[5]	V_{OH}	4 mA load	VDDO – 0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
CMOS Output Resistance[5]			—	50	—	Ω
HSTL, SSTL 20%–80% Rise/Fall Time	t_R/t_F	See Figure 16.	—	0.35	—	ns
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO+0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO –0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO–0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V
HSTL, SSTL Output Resistance			—	50	—	Ω
Duty Cycle	DC		45	—	55	%

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "3.4.2. Differential Input Clocks" on page 19.
2. Minimum input frequency in clock buffer mode (PLL bypass) is 5 MHz. Operation to 1 MHz is also supported in buffer mode, but loss-of-signal (LOS) status is not functional.
3. Applies to differential inputs. For best jitter performance, keep the midpoint peak-to-peak differential input slew rate on pins 1 and 2 faster than 0.3 V/ns.
4. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver. See "3.10.6. CML Outputs" on page 31.
5. Includes effect of internal series 22 Ω resistor.

Table 5. Control Pins*

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Control Pins (P1, P2, P3, P5*, P6*)						
Input Voltage Low	V_{IL}	Pins P1, P2, P3	–0.1	—	0.3 x V_{DD}	V
		Pins P5 and P6	—	—	0.3	V
Input Voltage High	V_{IH}	Pins P1, P2, P3	0.7 x V_{DD}	—	3.73	V
		Pins P5* and P6*	0.85	—	1.2	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Output Control Pins (LOS, Pin 8)						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up = 1 kΩ	—	—	10	ns
***Note:** For more information, see "3.6.1. P5 and P6 Input Control" on page 24.						

Table 6. Crystal Specifications for 25 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	25	—	MHz
Load Capacitance (on-chip differential)	c_L	—	18	—	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	100	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

Table 7. Crystal Specifications for 27 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	27	—	MHz
Load Capacitance (on-chip differential)	c_L	—	18	—	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	75	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

Table 8. Jitter Specifications, Clock Generator Mode (Loop Bandwidth = 1.6 MHz)[1,2,3]
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GbE Random Jitter (12 kHz–20 MHz)[4]	J_{GbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.7	1	ps RMS
GbE Random Jitter (1.875–20 MHz)	R_{JGbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.38	0.79	ps RMS
OC-12 Random Jitter (12 kHz–5 MHz)	J_{OC12}	CLKIN = 19.44 MHz All CLKn at 155.52 MHz[5]	—	0.7	1	ps RMS
PCI Express 1.1 Common Clocked (with spread spectrum)		Total Jitter[6]	—	20.1	33.6	ps pk-pk
PCI Express 2.1 Common Clocked (no spread spectrum)		RMS Jitter[6], 10 kHz to 1.5 MHz	—	0.15	1.47	ps RMS
		RMS Jitter[6], 1.5 MHz to 50 MHz	—	0.58	0.75	ps RMS
PCI Express 3.0 Common Clocked (no spread spectrum)		RMS Jitter[6]	—	0.15	0.45	ps RMS
PCIe Gen 3 Separate Reference No Spread, SRNS		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.11	0.32	ps RMS
PCIe Gen 4, Common Clock		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.15	0.45	ps RMS
Period Jitter	J_{PER}	N = 10,000 cycles[7]	—	10	30	ps pk-pk

Notes:
1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 2 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
3. For best jitter performance, keep the single-ended clock input slew rates at pins 1 and 2 greater that 1.0 V/ns and the differential clock input slew rates greater than 0.3 V/ns.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is mesured with the Intel Clock Jitter Tool, Ver.1.6.4.
7. For any output frequency ≥ 10 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
10. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
11. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/PCI-Express-Learning-Center.

Table 8. Jitter Specifications, Clock Generator Mode (Loop Bandwidth = 1.6 MHz)[1,2,3] (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-Cycle Jitter	J_{CC}	N = 10,000 cycles Output MultiSynth operated in integer or fractional mode[7]	—	9	29	ps pk[8]
Random Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in integer or fractional mode[7]	—	0.7	1.5	ps RMS
Deterministic Jitter	D_J	Output MultiSynth operated in fractional mode[7]	—	3	15	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	2	10	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J+14xR_J$ (See Note [9])	Output MultiSynth operated in fractional mode[7]	—	13	36	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	12	20	ps pk-pk

Notes:
1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 2 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
3. For best jitter performance, keep the single-ended clock input slew rates at pins 1 and 2 greater that 1.0 V/ns and the differential clock input slew rates greater than 0.3 V/ns.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is mesured with the Intel Clock Jitter Tool, Ver.1.6.4.
7. For any output frequency ≥ 10 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
10. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
11. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/PCI-Express-Learning-Center.

Table 9. Jitter Specifications, Clock Generator Mode (Loop Bandwidth = 475 kHz)[1,2]
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DSL Random Jitter (10 kHz–400 kHz)	R_{JDSL1}	CLKIN = 70.656 MHz All CLKn at 70.656 MHz[4]	—	0.8	2	ps RMS
DSL Random Jitter (100 kHz–10 MHz)	R_{JDSL2}	CLKIN = 70.656 MHz All CLKn at 70.656 MHz[4]	—	0.9	2	ps RMS
DSL Random Jitter (10 Hz–30 MHz)	R_{JDSL3}	CLKIN = 70.656 MHz All CLKn at 70.656 MHz[4]	—	1.95	2.2	ps RMS
PCI Express 1.1 Common Clocked (with spread spectrum)		Total Jitter[5]	—	20	34	ps pk-pk
PCI Express 2.1 Common Clocked (no spread spectrum)		RMS Jitter[5], 10 kHz to 1.5 MHz	—	0.3	0.5	ps RMS
		RMS Jitter[5], 1.5 MHz to 50 MHz	—	0.5	1.0	ps RMS
PCI Express 3.0 Common Clocked (no spread spectrum)		RMS Jitter[5]	—	0.15	0.45	ps RMS
PCIe Gen 3 Separate Reference No Spread, SRNS		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.11	0.32	ps RMS
PCIe Gen 4, Common Clock		PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.15	0.45	ps RMS
Period Jitter	J_{PER}	N = 10,000 cycles[6]	—	10	30	ps pk-pk

Notes:
1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 2 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
3. D_J for PCI and GbE is < 5 ps pp
4. Output MultiSynth in Integer mode.
5. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is mesured with the Intel Clock Jitter Tool, Ver.1.6.4.
6. For any output frequency ≥ 5 MHz.
7. Measured in accordance with JEDEC standard 65.
8. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
9. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
10. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/PCI-Express-Learning-Center.

Table 9. Jitter Specifications, Clock Generator Mode (Loop Bandwidth = 475 kHz)[1,2] (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-Cycle Jitter	J_{CC}	N = 10,000 cycles Output MultiSynth operated in integer or fractional mode[6]	—	9	29	ps pk[7]
Random Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in integer or fractional mode[6]	—	1	2.5	ps RMS
Deterministic Jitter	D_J	Output MultiSynth operated in fractional mode[6]	—	3	15	ps pk-pk
		Output MultiSynth operated in integer mode[6]	—	2	10	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J+14xR_J$ (See Note [8])	Output MultiSynth operated in fractional mode[6]	—	13	36	ps pk-pk
		Output MultiSynth operated in integer mode[6]	—	15	30	ps pk-pk

Notes:
1. All jitter measurements apply for LVDS/HCSL/LVPECL/CML output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 2 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
3. D_J for PCI and GbE is < 5 ps pp
4. Output MultiSynth in Integer mode.
5. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is mesured with the Intel Clock Jitter Tool, Ver.1.6.4.
6. For any output frequency ≥ 5 MHz.
7. Measured in accordance with JEDEC standard 65.
8. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.
9. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
10. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/PCI-Express-Learning-Center.

Table 10. itter Specifications, Clock Buffer Mode (PLL Bypass)*

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additive Phase Jitter (12 kHz–20 MHz)	t_{RPHASE}	0.7 V pk-pk differential input clock at 350 MHz with 70 ps rise/fall time	—	0.165	—	ps RMS
Additive Phase Jitter (50 kHz–80 MHz)	$t_{RPHASEWB}$	0.7 V pk-pk differential input clock at 350 MHz with 70 ps rise/fall time	—	0.225	—	ps RMS
***Note:** All outputs are in Clock Buffer mode (PLL Bypass).						

Table 11. Typical Phase Noise Performance

Offset Frequency	Loop Bandwidth	25 MHz XTAL to 156.25 MHz	27 MHz Ref In to 148.3517 MHz	19.44 MHz Ref In to 155.52 MHz	100 MHz Ref In to 100 MHz	Units
100 Hz	1.6 MHz	–90	–87	–110	–115	dBc/Hz
	475 kHz	N/A*	–91	–91	–113	dBc/Hz
1 kHz	1.6 MHz	–120	–117	–116	–122	dBc/Hz
	475 kHz	N/A*	–112	–111	–122	dBc/Hz
10 kHz	1.6 MHz	–126	–123	–123	–128	dBc/Hz
	475 kHz	N/A*	–124	–122	–127	dBc/Hz
100 kHz	1.6 MHz	–132	–130	–128	–136	dBc/Hz
	475 kHz	N/A*	–122	–121	–124	dBc/Hz
1 MHz	1.6 MHz	–132	–132	–128	–136	dBc/Hz
	475 kHz	N/A*	–133	–131	–135	dBc/Hz
10 MHz	1.6 MHz	–145	–145	–145	–152	dBc/Hz
	475 kHz	N/A*	–152	–153	–152	dBc/Hz
***Note:** XTAL input mode does not support the 475 kHz loop bandwidth setting.						

Table 12. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

Table 13. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Input Voltage	V_{IN}	Pins: XA/CLKIN, XB/CLKINB, P5, P6	–0.5 to 1.3	V
		Pins: P1, P2, P3	–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	
Junction Temperature	T_J		150	°C
Peak Soldering Reflow Temperature[2]			260	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Refer to JEDEC J-STD-020 standard for more information.

2. Typical PCIe System Diagram

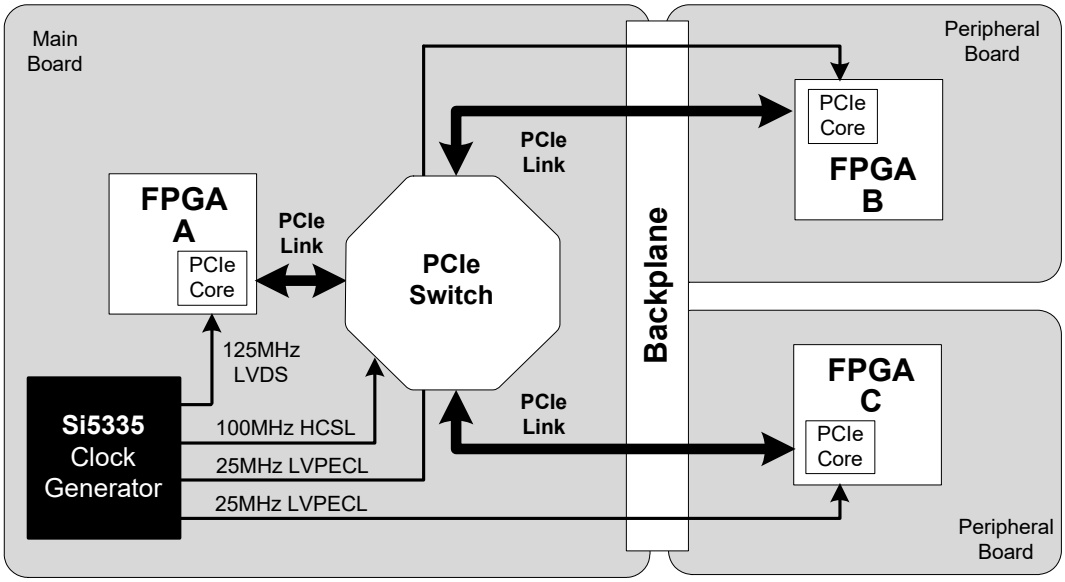


Figure 1. PCI Express Switching Application Example

Figure 1 shows the Si5335 in a PCI Express application using the common clock topology. The Si5335 provides reference clocks to the three FPGAs, each of which requires a different clock signaling format (LVDS, LVPECL), I/O voltage (1.8, 2.5, 3.3 V), or frequency (25, 100, 125 MHz). In addition, the Si5335 provides a PCIe compliant, 100 MHz HCSL reference clock to the PCIe switch.

3. Functional Description

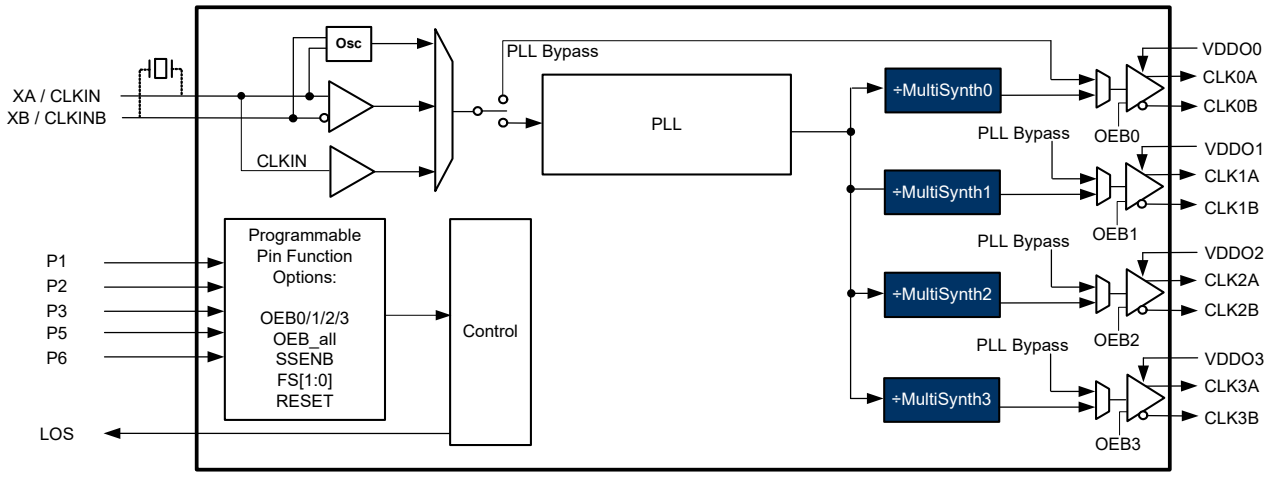


Figure 2. Si5335 Functional Block Diagram

3.1. Overview

The Si5335 is a high-performance, low-jitter clock generator or buffer capable of synthesizing four independent user-programmable clock frequencies up to 350 MHz. The device supports free-run operation using an external 25 or 27 MHz crystal, or it can lock to an external clock for generating synchronous clocks. The output drivers support four differential clocks or eight single-ended clocks or a combination of both. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, CML, CMOS, HSTL, and SSTL. Separate output supply pins allow supply voltages of 3.3, 2.5, 1.8, and 1.5 V to support the multi-format output driver. The core voltage supply accepts 3.3, 2.5, or 1.8 V and is independent from the output supplies. Using its two-stage synthesis architecture and patented high-resolution MultiSynth technology, the Si5335 can generate four independent frequencies from a single input frequency. In addition to clock generation, the inputs can bypass the synthesis stage enabling the Si5335 to be used as a high-performance clock buffer.

Spread spectrum* is available on each of the clock outputs for EMI-sensitive applications, such as PCI Express. The device includes an interrupt pin that monitors for both loss of PLL lock (LOL) and loss of input signal (LOS) conditions while configured in clock generator mode. In clock generator mode, the LOS pin is asserted whenever LOL or LOS is true. In clock buffer mode (i.e., when the PLL is bypassed), the LOS pin is asserted whenever the input clock is lost. The LOL condition does not apply in clock buffer mode.

***Note:** See " Document Change List" on page 46 for more information.

3.2. MultiSynth Technology

Next-generation timing architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using a combination of single PLL ICs, 4-PLL ICs and discrete XOs, often at the expense of BOM complexity and power. The Si5335 uses patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 phase-locked loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions. Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high-frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high-speed fractional divider with Skyworks Solutions' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, the output of each MultiSynth can produce any frequency from 1 to 350 MHz.

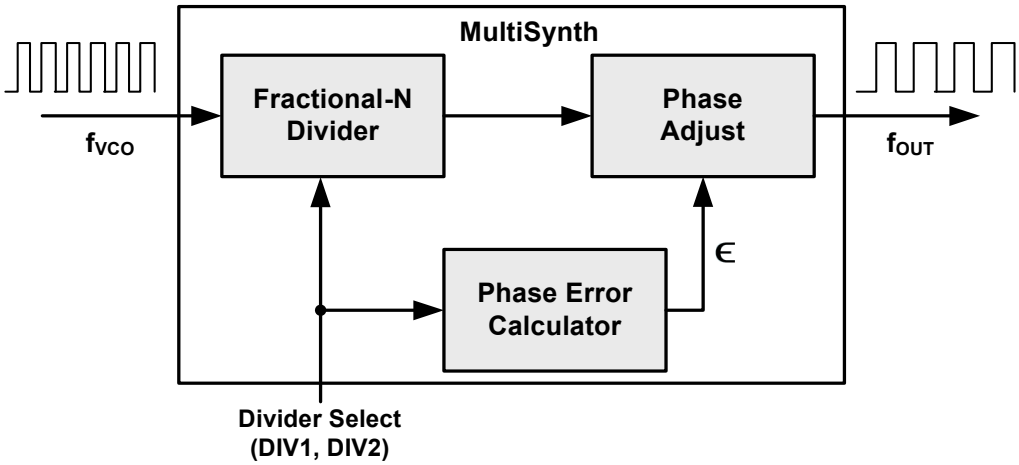


Figure 3. Skyworks Solutions' MultiSynth Technology

3.3. ClockBuilder Web-Customization Utility

ClockBuilder is a web-based utility available at https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software that allows hardware designers to tailor the Si5335's flexible clock architecture to meet any application-specific requirements and order custom clock samples. Through a simple point-and-click interface, users can specify any combination of input frequency and output frequencies and generate a custom part number for each application-specific configuration. There are no minimum order quantity restrictions.

ClockBuilder enables mass customization of clock generators. This allows a broader range of applications to take advantage of using application-specific pin controlled clocks, simplifying design while eliminating the firmware development required by traditional I^2C-programmable clock generators.

Based on Skyworks Solutions' patented MultiSynth technology, the device PLL output frequency is constant and all clock output frequencies are synthesized by the four MultiSynth fractional dividers. All PLL parameters, including divider settings, VCO frequency, loop bandwidth, charge pump current, and phase margin are internally set by the device during the configuration process. This ensures optimized jitter performance and loop stability while simplifying design.

3.4. Input Configuration

The Si5335 input can be driven from either an external crystal or a reference clock. Reference selection is made when the device configuration is specified using the ClockBuilder™ web-based utility available at https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software.

3.4.1. Crystal Input

If the crystal input option is used, the Si5335 operates as a free-running clock generator. In this mode of operation the device requires a low-cost 25 or 27 MHz fundamental mode crystal connected across XA and XB as shown in Figure 4. Given the Si5335's frequency flexibility, the same 25 or 27 MHz crystal can be reused to generate any combination of output frequencies. Custom frequency crystals are not required. The Si5335 integrates the crystal load capacitors on-chip to reduce external component count. The crystal should be placed very close to the device to minimize stray capacitance. To ensure stable oscillation, the recommended crystal specifications provided in Tables 6 and 7 must be followed. See AN360 for additional details regarding crystal recommendations.

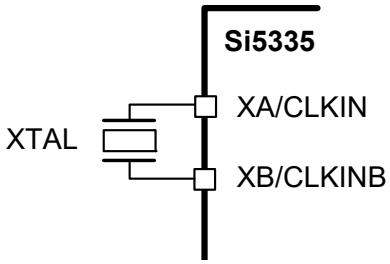


Figure 4. Connecting an XTAL to the Si5335

3.4.2. Differential Input Clocks

The multi-format differential clock inputs of the Si5335 will interface with today's most common differential signals, such as LVDS, LVPECL, CML, and HCSL. The differential inputs are internally self-biased *and must be ac-coupled externally with a 0.1 µF capacitor*. The receiver will accept a signal with a voltage swing between 400 mV and 2.4 V_{PP} differential. Each half of the differential signal must not exceed 1.2 V_{PP} at the input to the Si5335 or else the 1.3 V dc voltage limit may be exceeded.

3.4.2.1. LVDS Inputs

When interfacing the Si5335 device to an LVDS signal, a 100 Ω termination is required at the input along with the required dc blocking capacitors as shown in Figure 5.

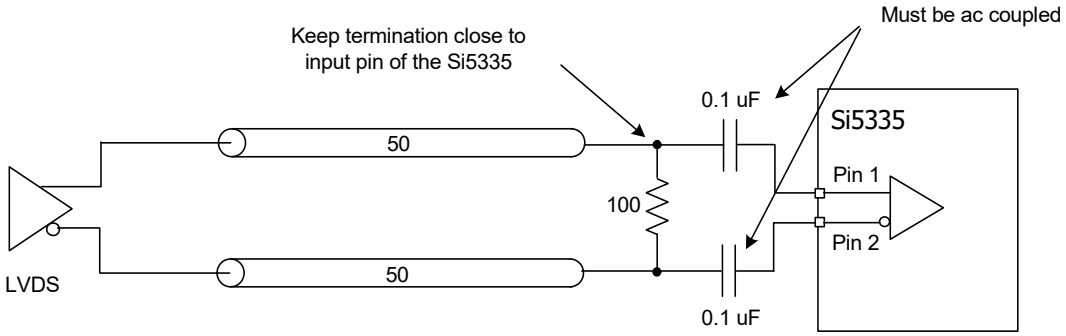


Figure 5. LVDS Input Signal

3.4.2.2. LVPECL Input Clocks

Recommended configurations for interfacing an LVPECL input signal to the Si5335 are shown in Figure 6. Typical values for the bias resistors (Rb) range between 120 and 200 Ω depending on the LVPECL driver. The 100 Ω resistor provides line termination. Because the receiver is internally self-biased, no additional external bias is required.

Another solution is to terminate the LVPECL driver with a Thevenin configuration as shown in Figure 6b. The values for R_1 and R_2 are calculated to provide a 50Ω termination to V_{DD}-2V. Given this, the recommended resistor values are R_1 = 127 Ω and R_2 = 82.5 Ω for V_{DD} = 3.3 V, and R_1 = 250 Ω and R_2 = 62.5 Ω for V_{DD} = 2.5 V.

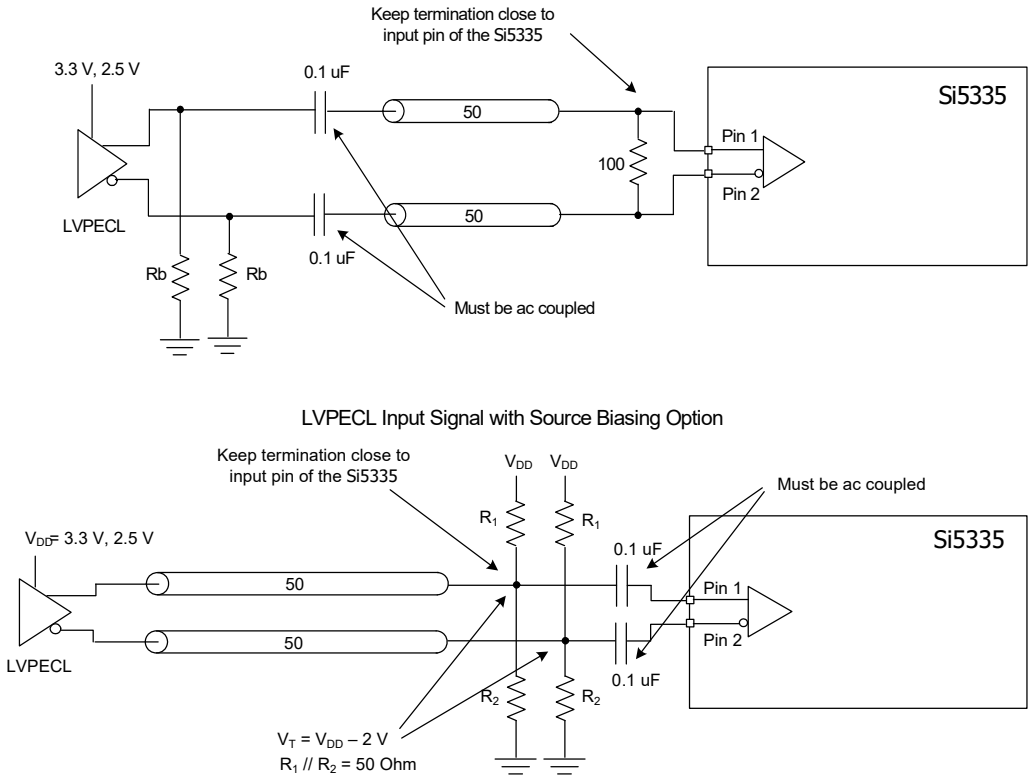
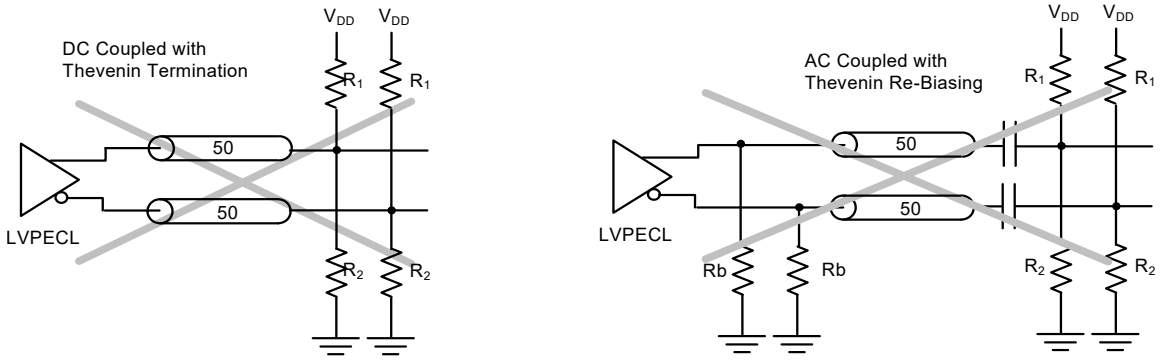


Figure 6. Recommended Options for Interfacing to an LVPECL Input Signal

Since the differential receiver of the Si5335 is internally self biased, an LVPECL signal may not be dc-coupled to the device. Figure 7 shows some common LVPECL connections that should not be used because of the dc levels they present at the receiver's input.



Not Recommended

Figure 7. Common LVPECL Connections that May be Destructive to the Si5335 Input

3.4.2.3. CML Input Clocks

CML signals may be applied to the differential inputs of the Si5335. Since the Si5335 differential inputs are internally self-biased, a CML signal may not be dc-coupled to the device.

The recommended configurations for interfacing a CML input signal to the Si5335 are shown in Figure 8. The 100 Ω resistor provides line termination, and, since the receiver is internally-biased, no additional external biasing components are required.

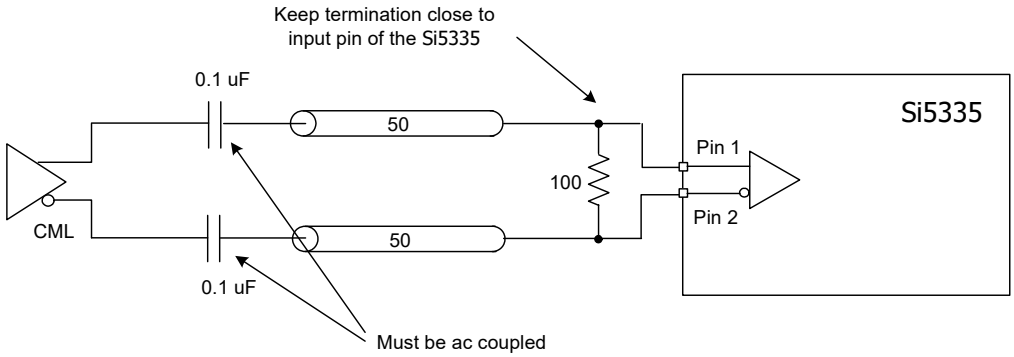


Figure 8. CML Input Signal

3.4.2.4. HCSL Input Clocks

A typical HCSL driver has an open source output, which requires an external series resistor and a resistor to ground. The values of these resistors depend on the driver but are typically equal to 33 Ω (Rs) and 50 Ω (Rt). Note that the HCSL driver in the Si5335 requires neither Rs nor Rt resistors. Other than two ac-coupling capacitors, no additional external components are necessary when interfacing an HCSL signal to the Si5335.

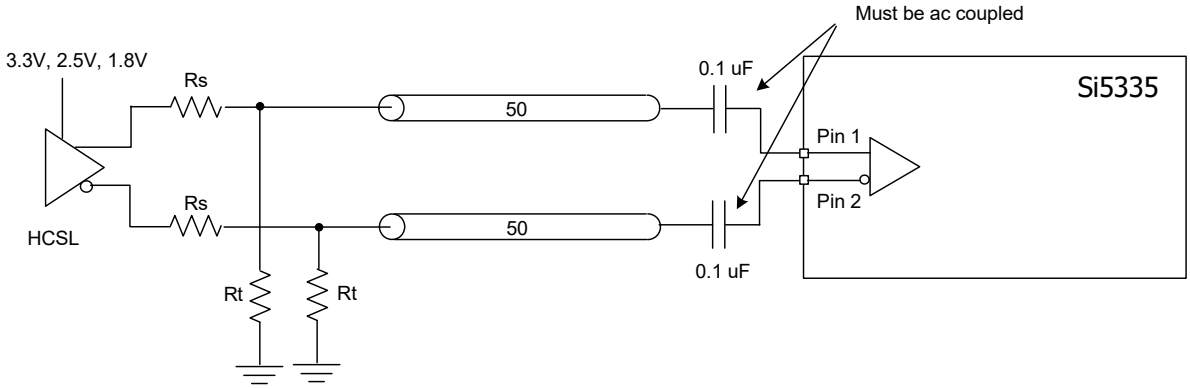


Figure 9. HCSL Input Signal to Si5335

3.4.3. Single-Ended CMOS Input Clocks

For synchronous timing applications, the Si5335 can lock to a 10 to 200 MHz CMOS reference clock. A typical interface circuit is shown in Figure 10. A series termination resistor may be required if the CMOS driver impedance does not match the trace impedance.

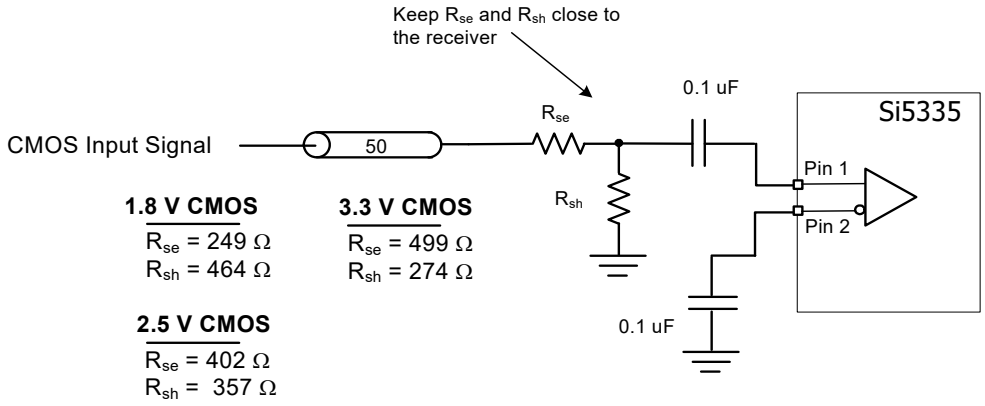


Figure 10. Interfacing CMOS Reference Clocks to the Si5335

3.4.4. Single-Ended SSTL and HSTL Input Clocks

HSTL and SSTL single-ended inputs can be input to the differential inputs, pins 1 and 2, of the Si5335 with the circuit shown in Figure 11.

Some drivers may require a series 25 Ω resistor. If the SSTL/HSTL input is being driven by another Si5335 device, the 25 Ω series resistor is not required as this is integrated on-chip. The maximum recommended input frequency in this case is 350 MHz.

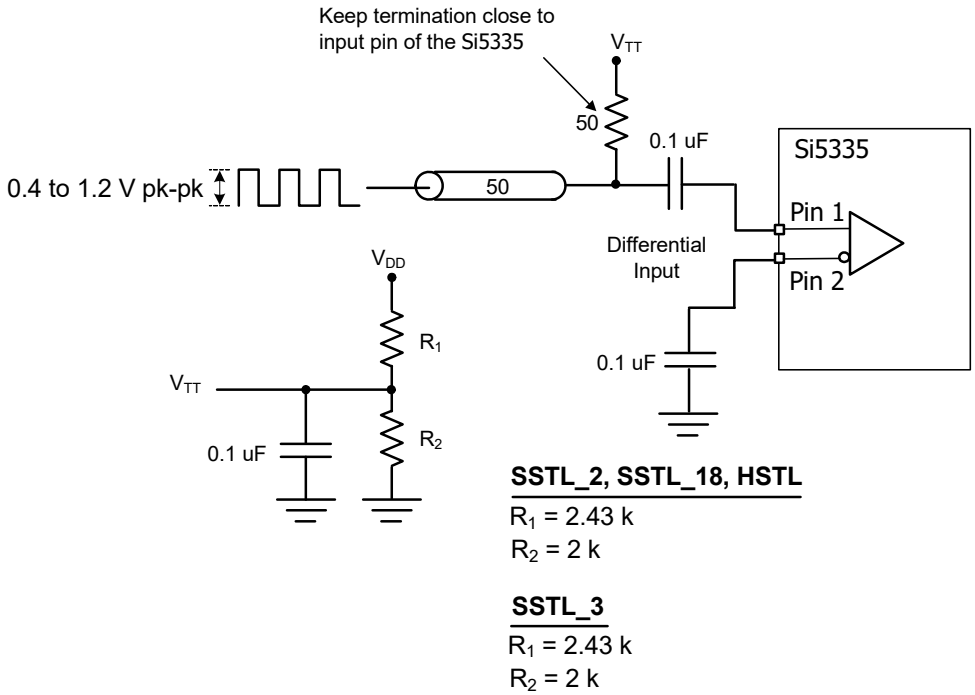


Figure 11. Single-Ended SSTL/HSTL Input Clocks to the Si5335

3.4.5. Applying a Single-Ended Clock to the Differential Input Clock Pins

It is possible to interface any single-ended clock signal to the differential input pins (XA/CLKIN, XB/CLKINB). The recommended interface for a signal that requires a 50 Ω load is shown in Figure 12. On these inputs, it is important that the signal level be less than 1.2 V_{PP} SE and greater than 0.4 V_{PP} SE. The maximum recommended input frequency in this case is 350 MHz.

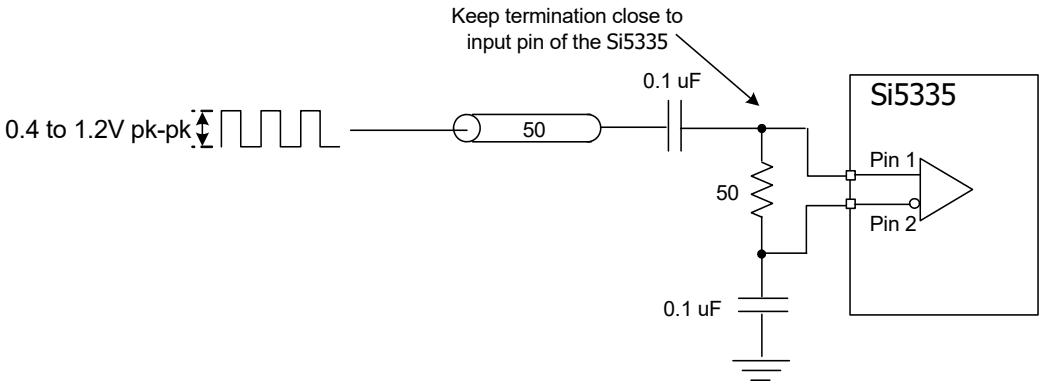


Figure 12. Single-Ended Input Signal with 50 Ω Termination

3.5. Input and Output Frequency Configuration

The Si5335 utilizes a single PLL-based architecture, four independent MultiSynth fractional output dividers, and a MultiSynth fractional feedback divider such that a single device provides the clock generation capability of 4 independent PLLs. Unlike competitive multi-PLL solutions, the Si5335 can generate four unique non-integer related output frequencies with 0 ppm frequency error for any combination of output frequencies. In addition, any combination of output frequencies can be generated from a single reference frequency without having to change the crystal or reference clock frequency between frequency configurations.

The Si5335 frequency configuration is set when the device configuration is specified using the ClockBuilder Pro web-based utility. Any combination of output frequencies ranging from 1 to 350 MHz can be configured on each of the device outputs. Up to three unique device configurations can be specified in a single device, enabling the Si5335 to replace 3 different clock generators or clock buffers.

3.6. Multi-Function Control Inputs

The Si5335 supports five user-defined input pins (pins 3, 5, 6, 12, 19) that are customizable to support the functions listed below. The pinout of each device is customized using the ClockBuilder utility. This enables the device to be custom tailored to a specific application. Each of the different functions is described in further detail below.

Table 14. Multi-Function Control Inputs

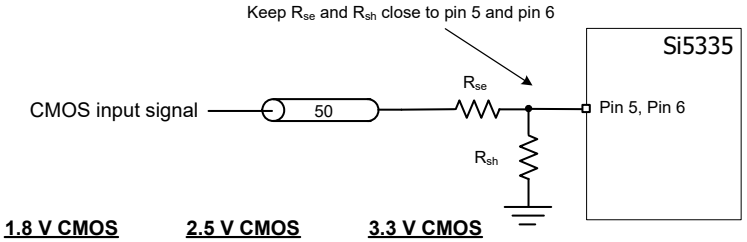
Pin Function	Description	Assignable Pin Name
OEB_all	**Output Enable All.** All outputs enabled when low.	P1, P2, P3, P5*, P6*
OEB0	**Output Enable Bank 0.** CLK0A/0B enabled when low.	P1, P2, P3, P5*, P6*
OEB1	**Output Enable Bank 1.** CLK1A/1B enabled when low.	P1, P2, P3, P5*, P6*
OEB2	**Output Enable Bank 2.** CLK2A/2B enabled when low.	P1, P2, P3, P5*, P6*
OEB3	**Output Enable Bank 3.** CLK3A/3B enabled when low.	P1, P2, P3, P5*, P6*

Table 14. Multi-Function Control Inputs (Continued)

FS0	**Frequency Select.** Selects active device frequency plan from factory-configured profiles. See “3.8. Frequency Select/Device Reset” for more information.	P1
FS1	**Frequency Select.** Selects active device frequency plan from factory-configured profiles. See “3.8. Frequency Select/Device Reset” for more information.	P1 (for 2-plan devices) P2 (for 3-plan devices)
RESET	**Reset.** Asserting this pin (driving high) is required to change FS1,FS0 pin setting. Reset is not required if FS1,FS0 pins are unassigned.	P1, P2, P3
SSENB	**Spread Spectrum Enable.** Enables PCI-compliant spread spectrum clocking on all 100 MHz clock outputs when low.	P1, P2, P3, P5*, P6*
***Note:** See “3.6.1. P5 and P6 Input Control” for recommended termination circuits for these pins.		

3.6.1. P5 and P6 Input Control

Control input signals to P5 and P6 cannot exceed 1.2 V. When these inputs are driven from CMOS sources, a resistive attenuator is required for pins 5 and 6, as shown in Figure 13.



1.8 V CMOS	2.5 V CMOS	3.3 V CMOS
R_{se} = 1 kΩ	1.96 kΩ	3.09 kΩ
R_{sh} = 1.58 kΩ	1.58 kΩ	1.58 kΩ

Figure 13. P5, P6 Control Pin Termination

3.7. Output Enable

Each of the device’s four banks of clock outputs can be individually disabled using OEB0, OEB1, OEB2 and OEB3, respectively. Alternatively, all clock outputs can be disabled using the master output enable OEB_all. When a Si5335 clock output bank is disabled, the output disable state is determined by the configuration specified in the ClockBuilder web utility. When one or more banks of clock outputs are enabled or disabled, clock start and stop transitions are handled glitchlessly.

3.8. Frequency Select/Device Reset

The device frequency plan is customized using the ClockBuilder web utility. The Si5335 optionally supports up to three unique, pin-selectable configurations per device, enabling one device to replace up to three separate clock ICs. To select a particular frequency plan, set the FS pins as outlined below:

For custom Si5335 devices configured to support two frequency plans, the FS1 pin should be set as follows:

FS1	Profile

0	1
1	2

For custom Si5335 devices configured to support three frequency plans, the FS1 and FS0 pins should be set as follows:

FS1	FS0	Profile
0	0	Reserved
0	1	1
1	0	2
1	1	3

If a change is made to the FS pin settings, the device reset pin (RESET) must be held high for the minimum pulse width specified in Table 3 on page 5 to change the device configuration. The output clocks will be momentarily squelched until the device begins operation with the new frequency plan.

If the RESET pin is not selected in ClockBuilder as one of the five programmable pins, a power-on reset must be applied for an FS pin change to take effect.

3.9. Loss-of-Signal Alarm

The Si5335 supports a loss of signal (LOS) output indicator for monitoring the condition of the crystal/clock reference input. The LOS condition occurs when there is no input clock to the device or the PLL has lost lock (in clock generator mode). When an input clock is removed, the LOS pin will assert and the output clocks may drift up to 5% (in clock generator mode). When the input clock with an appropriate frequency is reapplied, the LOS pin will deassert. In clock buffer mode, LOS is driven high when the input clock is lost.

LOS Output State	Description
0	Input clock present and PLL is locked
1	Input clock not present and PLL is not locked

3.10. Output Stage

The output stage consists of programmable output drivers as shown in Figure 14.

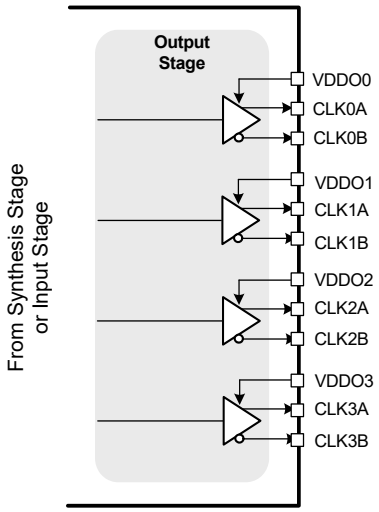


Figure 14. Output Stage

The Si5335 devices provide four outputs that can be differential or single-ended. When configured as single-ended, the driver generates two signals that can be configured as in-phase or complementary. Each of the outputs has its own output supply pin, allowing the device to be used in mixed supply applications without the need for external level translators. The CML output driver generates a similar output swing as the LVPECL driver but consumes half the current. CML outputs must be ac-coupled.

3.10.1. CMOS/LVTTL Outputs

The CMOS output driver has a controlled impedance of about 50 Ω, which includes an internal series resistor of approximately 22 Ω. For this reason, an external Rs series resistor is not recommended when driving 50 Ω traces. If the trace impedance is higher than 50 Ω, a series resistor, Rs, should be used. A typical configuration is shown in Figure 15. A CMOS output driver can be configured with ClockBuilder as a single- or dual-output driver. Dual otuput configurations support in-phase or complementary outputs. The output supports 3.3, 2.5, and 1.8 V CMOS signal levels when the appropriate voltage is supplied to the external VDDO pin and the device is configured accordingly.

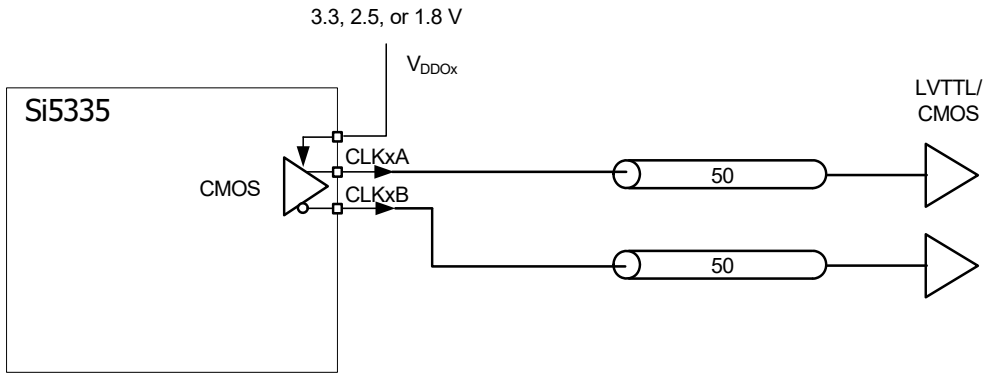


Figure 15. Interfacing to a CMOS Receiver

3.10.2. SSTL and HSTL Outputs

The Si5335 supports both SSTL and HSTL outputs, which can be single-ended or differential. The recommended termination scheme for SSTL is shown in Figure 16. The V_{TT} supply can be generated using a simple voltage divider as shown below (note that Rt = 50 Ω).

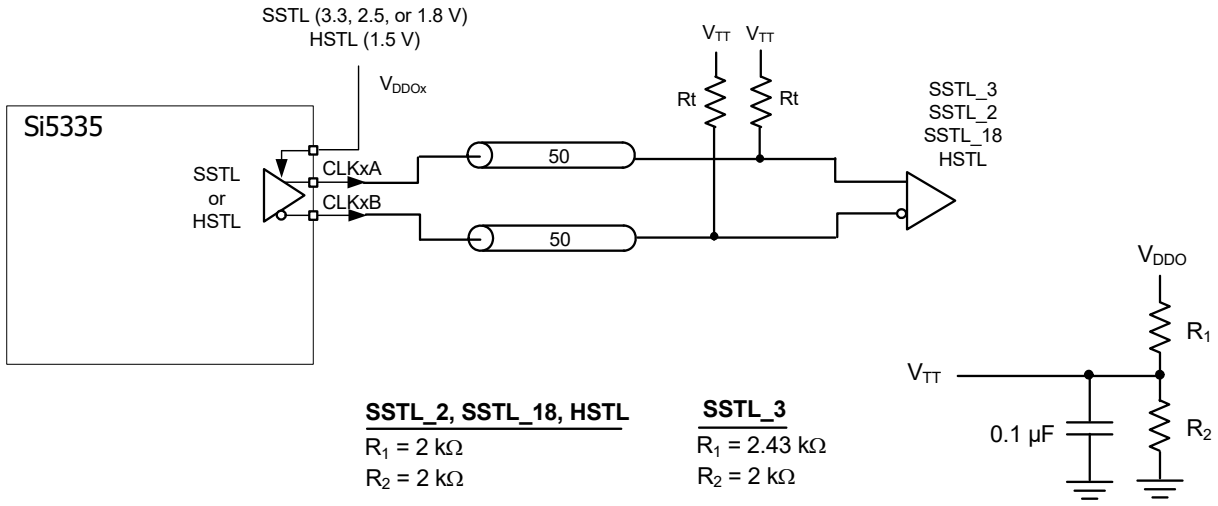


Figure 16. Interfacing the Si5335 to an SSTL or HSTL Receiver

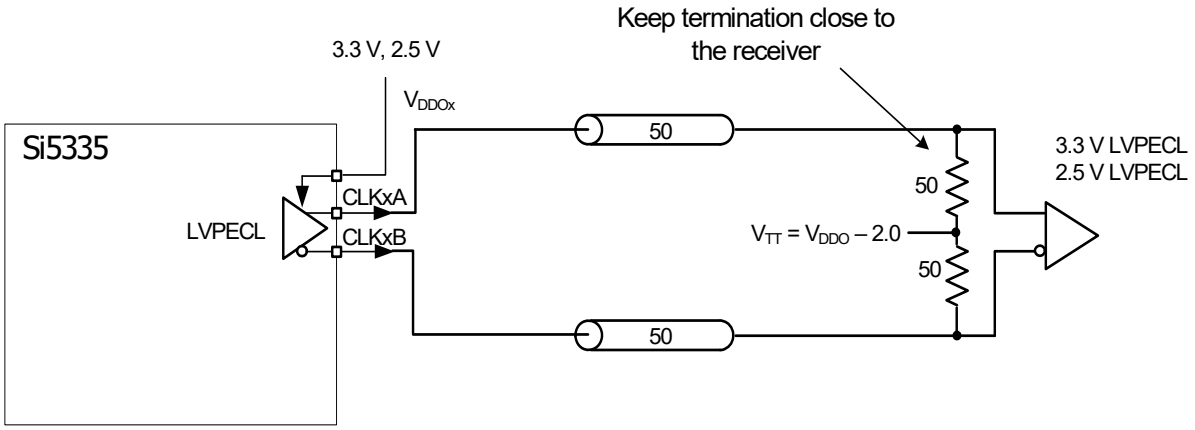
3.10.3. LVPECL Outputs

The LVPECL driver is configurable in both 3.3 V or 2.5 V standard LVPECL modes. The output driver can be ac-coupled or dc-coupled to the receiver.

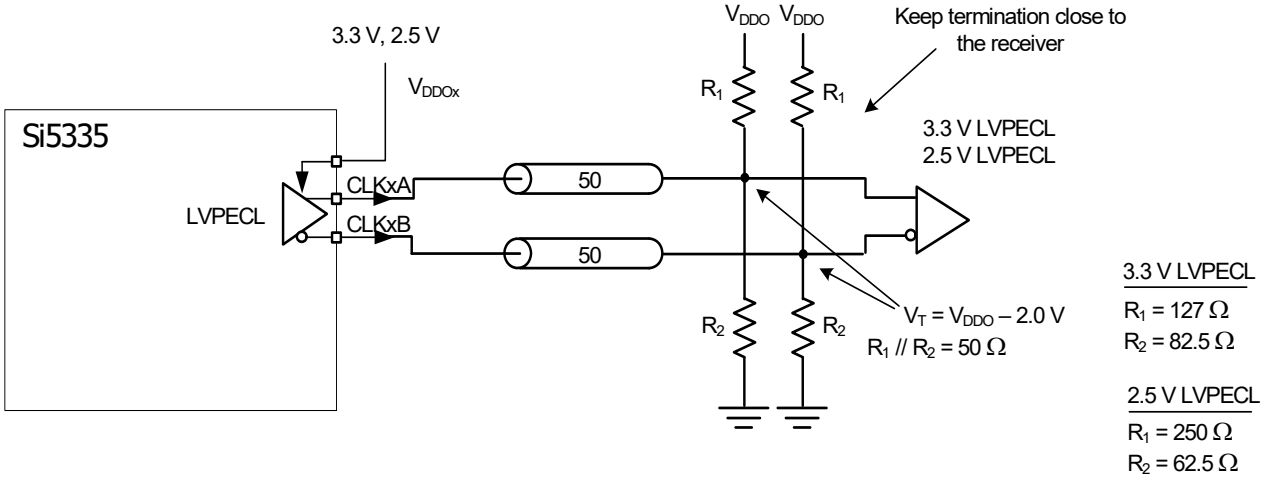
3.10.3.1. DC-Coupled LVPECL Outputs

The standard LVPECL driver supports two commonly used dc-coupled configurations. Both of these are shown in Figure 17a and Figure 17b. LVPECL drivers were designed to be terminated with 50 Ω to VDD–2 V, which is illustrated in Figure 17a. V_{TT} can be supplied with a simple voltage divider as shown.

An alternative method of terminating LVPECL is shown in Figure 17b, which is the Thevenin equivalent to the termination in Figure 17a. It provides a 50 Ω load terminated to V_{DD}–2.0 V. For 3.3 V LVPECL, use R_1 = 127 Ω and R_2 = 82.5 Ω; for 2.5 V LVPECL, use R_1 = 250 Ω and R_2 = 62.5 Ω. The only disadvantage to this type of termination is that the Thevenin circuit consumes additional power from the V_{DDO} supply.



a. DC-Coupled Termination of 50 Ω to V_{DDO} – 2.0 V

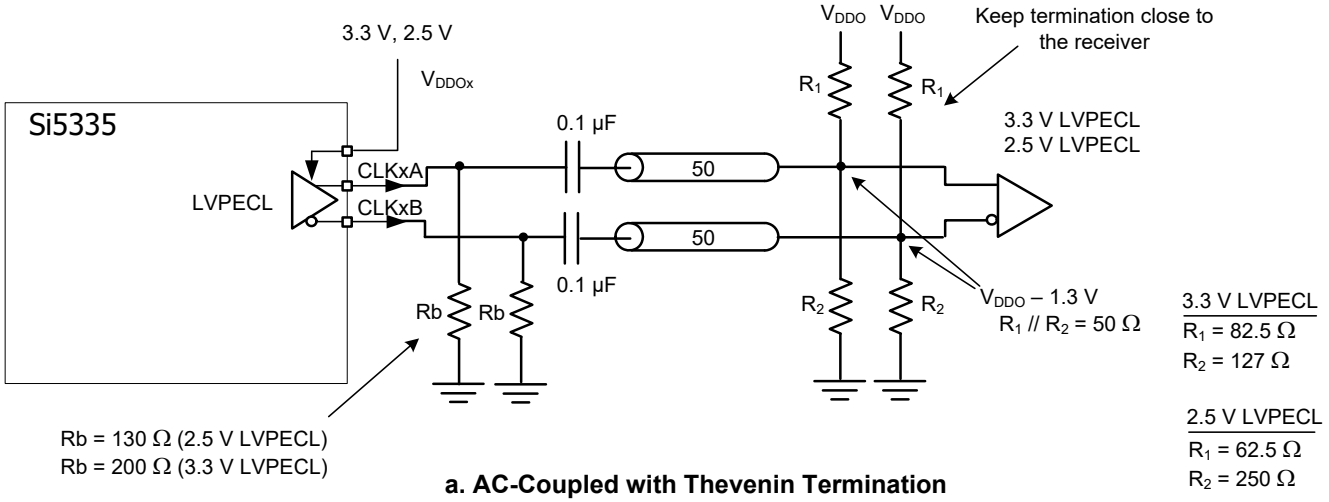


b. DC-Coupled with Thevenin Termination

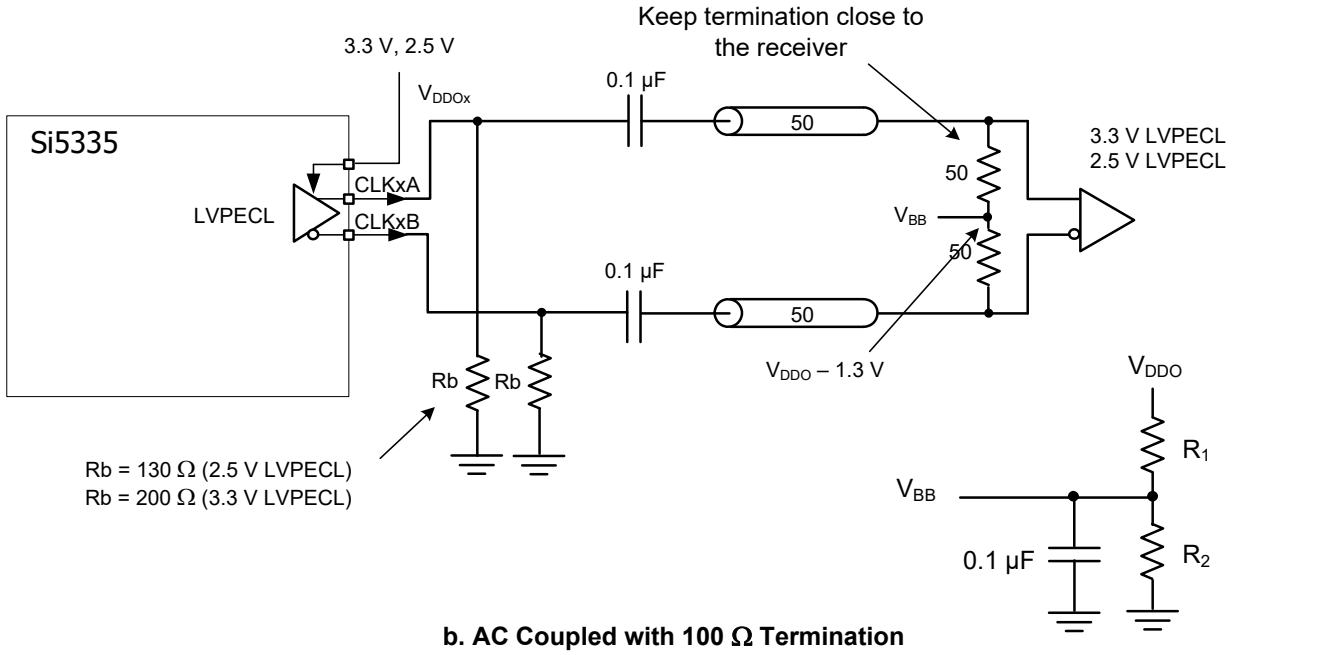
Figure 17. Interfacing the Si5335 to an LVPECL Receiver Using DC Coupling

3.10.3.2. AC Coupled LVPECL Outputs

AC coupling is necessary when a receiver and a driver have compatible voltage swings but different common-mode voltages. AC coupling works well for dc-balanced signals, such as for 50% duty cycle clocks. Figure 18 describes two methods for ac coupling the standard LVPECL driver. The Thevenin termination shown in Figure 18a is a convenient and common approach when a V_{BB} (V_{DD} – 1.3 V) supply is not available; however, it does consume additional power. The termination method shown in Figure 18b consumes less power. A V_{BB} supply can be generated from a simple voltage divider circuit as shown in Figure 18b.



a. AC-Coupled with Thevenin Termination



b. AC Coupled with 100 Ω Termination

Figure 18. Interfacing to an LVPECL Receiver Using AC Coupling

3.10.4. LVDS Outputs

The LVDS output option provides a very simple and power-efficient interface that requires no external biasing when connected to an LVDS receiver. An ac-coupled LVDS driver is often useful as a CML driver. The LVDS driver may be dc-coupled or ac-coupled to the receiver in 3.3 V or 2.5 V output mode.

3.10.4.1. AC-Coupled LVDS Outputs

The Si5335 LVDS output can drive an ac-coupled load. The ac coupling capacitors may be placed at either the driver or receiver end, as long as they are placed prior to the 100 Ω termination resistor. Keep the 100 Ω termination resistor as close to the receiver as possible, as shown in Figure 19. When a 1.8 V output supply voltage is used, the LVDS output of the Si5335 produces a common-mode voltage of ~0.875 V, which does not support the LVDS standard. In this case, it is best to ac-couple the output to the load.

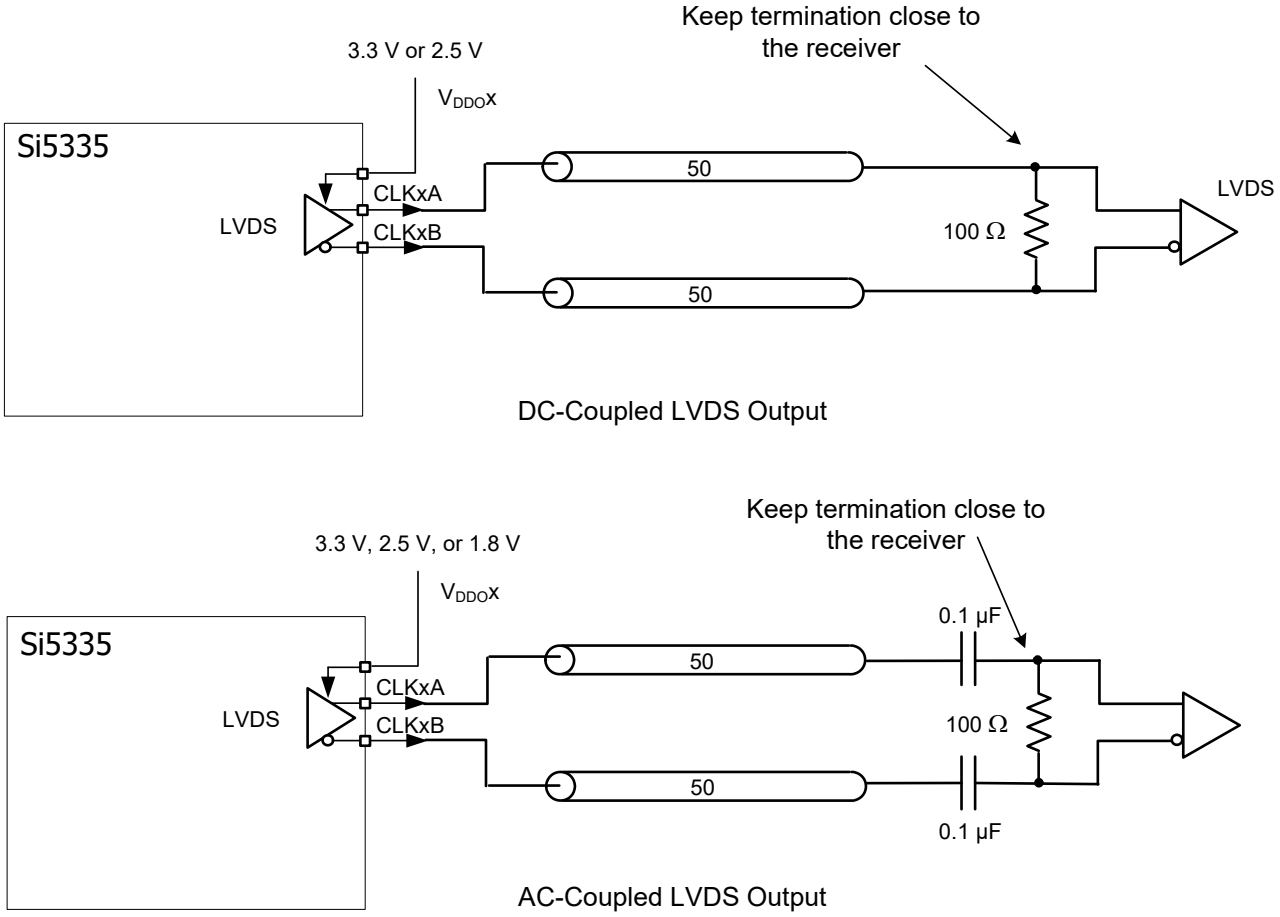


Figure 19. Interfacing to an LVDS Receiver

3.10.5. HCSL Outputs

Host clock signal level (HCSL) outputs are commonly used in PCI Express applications. A typical HCSL driver has an open source output that requires an external series resistor and a resistor to ground. The Si5335 HCSL driver has integrated these resistors to simplify the interface to an HCSL receiver. No external components are necessary when connecting the Si5335 HCSL driver to an HCSL receiver.

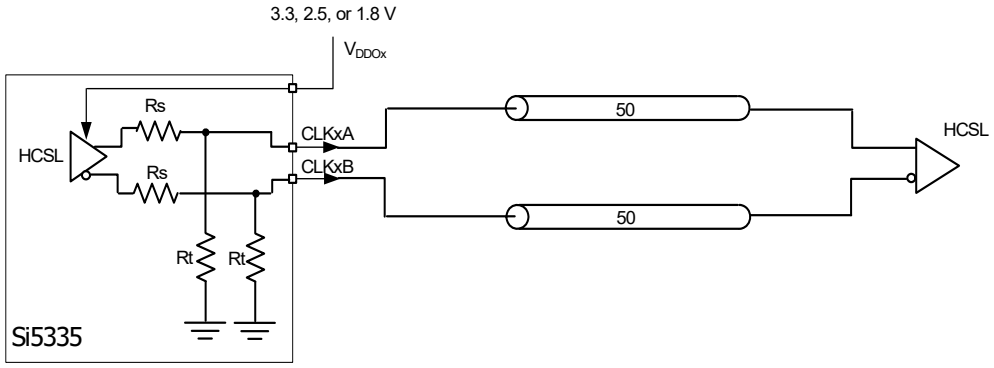
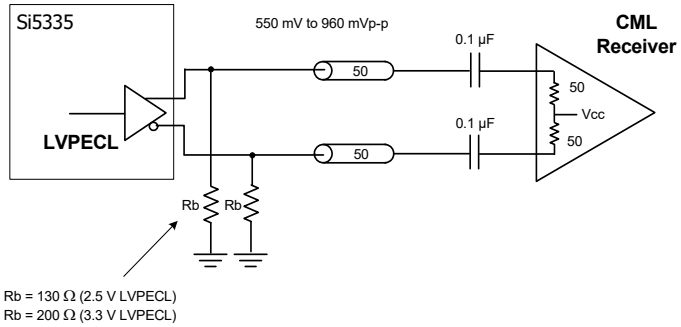


Figure 20. Interfacing the Si5335 to an HCSL Receiver

3.10.6. CML Outputs

Current mode logic (CML) is transmitted differentially and terminated to 50 Ω to Vcc as shown in Figure 20. A CML receiver can be driven with either an LVPECL, CML, or LVDS output. To drive a CML receiver, an Si5335 output configured in LVPECL or CML mode generates a single-ended output swing of 550 mV to 960 mV. However, to reduce power consumption by approximately 15 mA per output driver pair (compared to an LVPECL-configured output), the Si5335's CML output mode can be selected without affecting the output voltage swing. For even lower power consumption, depending on the input signal swing required, CML receivers can be driven with an Si5335 output configured in LVDS mode. CML output format is not available when the Si5335 is in PLL bypass (clock buffer) mode.

Driving a CML Receiver Using the LVPECL Output



Driving a CML Receiver Using the CML or LVDS Output

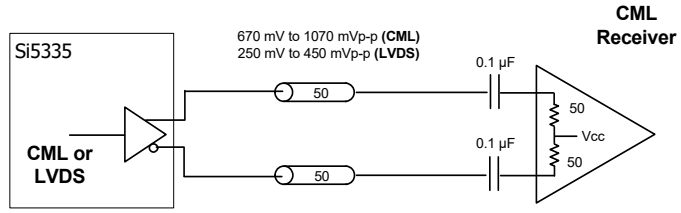


Figure 21. Terminating an LVPECL or an LVDS Output to a CML Receiver

4. Power Consumption

In clock generator mode, the Si5335 Power consumption is a function of the following:

- Supply voltage
- Frequency of output Clocks
- Number of output Clocks
- Format of output Clocks

Because of internal voltage regulation, the current from the core V_{DD} is independent of the V_{DD} voltage and hence the plot shown in Figure 5 can be used to estimate the V_{DD} core (pins 7 and 24) current.

The current from the output supply voltages can be estimated from the values provided in Table 2, “DC Characteristics,” on page 4. To get the most accurate value for V_{DD} currents, the Si5338-EVB with ClockBuilder Desktop software should be used.

To do this, go to the “Power” tab of ClockBuilder Desktop and press “Measure”. In this manner, a specific configuration can be implemented on the EVB and the actual current for each supply voltage measured. When doing this it is critical that the output drivers have the proper load impedance for the selected format.

When testing for output driver current with HSTL and SSTL, it is required to have load circuitry as shown in "3.10.2. SSTL and HSTL Outputs" on page 27. The Si5338 EVB has layout pads that can be used for this purpose. When testing for output driver current with LVPECL the same layout pads can be used to implement the LVPECL bias resistor of 130 Ω (2.5 V VDDx) or 200 Ω (3.3 V VDDx). See the schematic in the Si5338-EVB data sheet and AN408 for additional information.

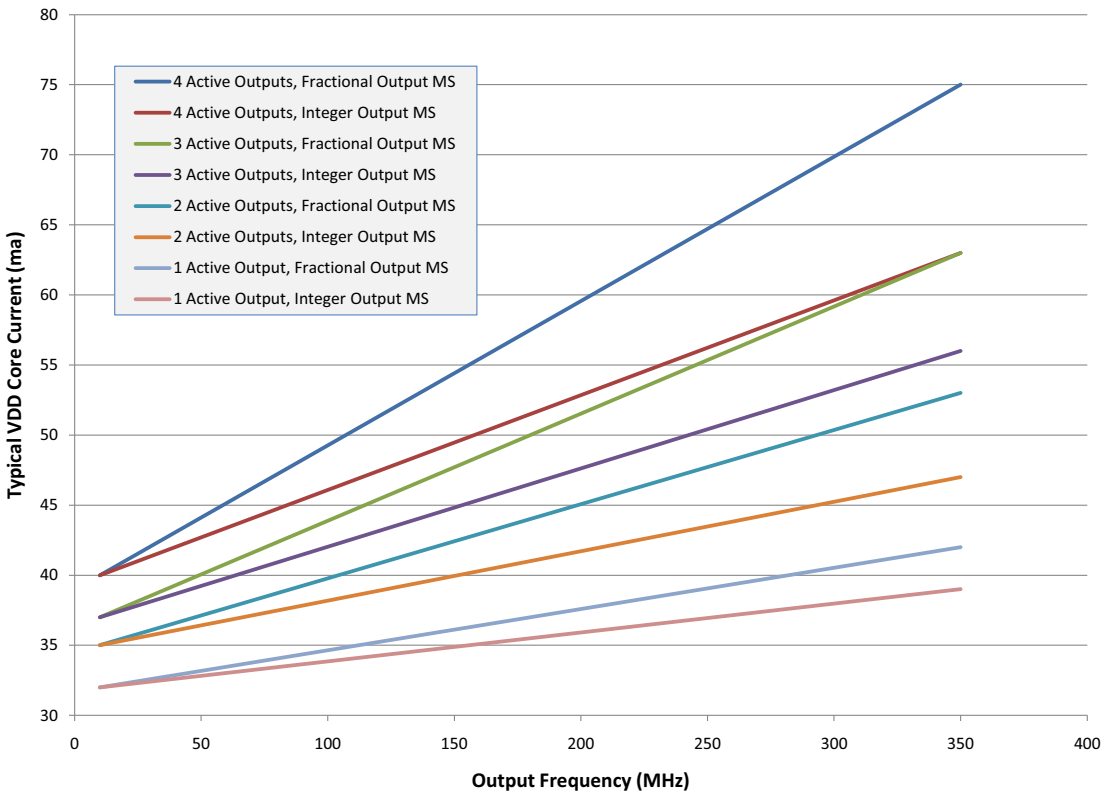


Figure 22. Core VDD Supply Average Current vs Output Frequency

5. Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5335 supports spread spectrum modulation in clock generator mode only. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. Spread spectrum modulation is generated digitally in the output MultiSynth dividers, which means that the spread spectrum parameters are virtually independent of process, voltage, and temperature variations.

If the SSENB function is assigned to a pin in ClockBuilder and asserted (driven low), PCIe-compliant spread spectrum is applied to all 100 MHz output clocks with a default spreading rate of 31.5 kHz and 0.5% down spread. If no 100 MHz output clocks are defined but the SSENB is assigned and asserted, none of the output clocks will have spread spectrum clocking applied. Some custom spread-spectrum clocking profiles are available. If the Si5335's default PCIe spread spectrum profile is not suitable for your application, submit your custom spread spectrum requirements for review by visiting the Skyworks Solutions Technical Support web page at at https://www.skyworksinc.com/support-ia, or contact your local Skyworks Solutions sales representative for more information.

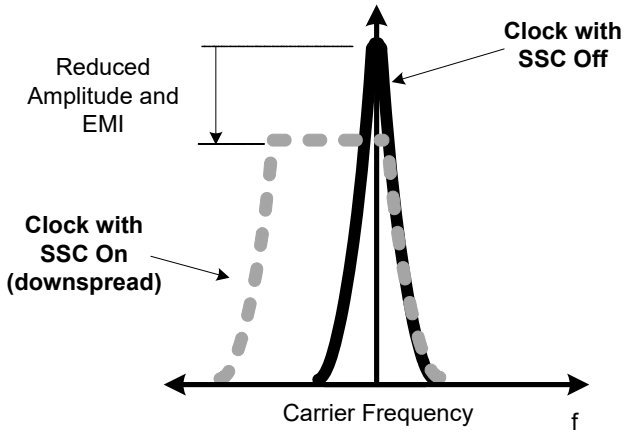


Figure 23. Spread Spectrum Clocking Impact on Output Power Spectrum

6. Jitter Performance

The Si5335 provides consistently low jitter for any combination of output frequencies. The device leverages a low phase noise single PLL architecture and Skyworks Solutions' patented MultiSynth fractional output divider technology to deliver period jitter of 10 ps pk-pk (typ). The Si5335 provides superior performance to conventional multi-PLL solutions which may suffer from degraded jitter performance depending on frequency plan and the number of active PLLs.

7. Power Supply Considerations

The Si5335 has 2 core supply voltage pins (V_{DD}) and 4 clock output bank supply voltage pins (V_{DDO0}–V_{DDO3}), enabling the device to be used in mixed supply applications. The Si5335 does not typically require ferrite beads for power supply filtering. The device has extensive on-chip power supply regulation to minimize the impact of power supply noise on output jitter. Figure 24 shows that the additive jitter created when a significant amount of noise is applied to the device power supply is very low.

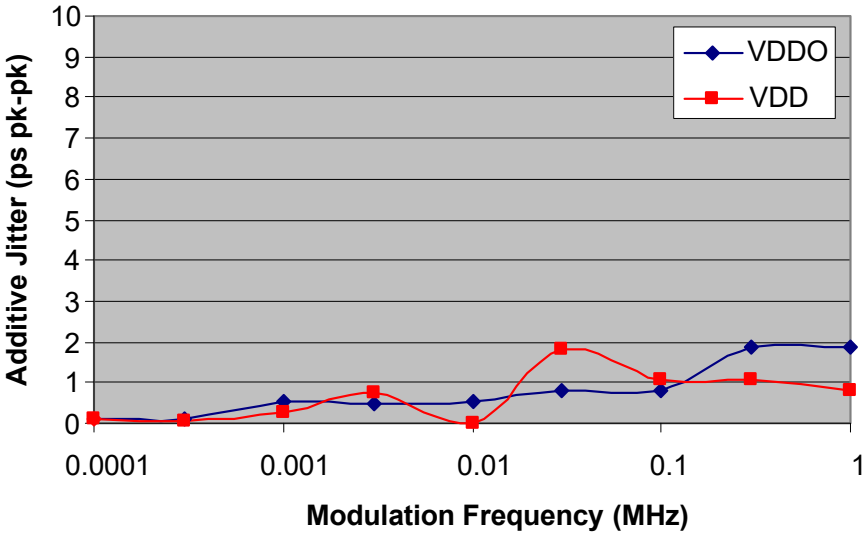


Figure 24. Peak-to-Peak Additive Jitter from 100 mV Sine Wave on Supply

8. Loop Bandwidth Considerations

For synchronous reference clock applications, two user-selectable loop bandwidth settings (1.6 MHz and 475 kHz) are available to allow designers to optimize their timing system to support jitter attenuation of the reference clock. In general, the 1.6 MHz setting provides the lowest output jitter and should be selected for most applications. The 1.6 MHz option provides faster PLL tracking of the input clock but less jitter attenuation of the input clock than the 475 kHz loop bandwidth option. The 1.6 MHz loop bandwidth option must be selected for all applications which use a crystal reference input on the XA/XB pins (pins 1 and 2) and for all applications which provide a low jitter input clock reference to the Si5335.

The 475 kHz setting reduces the clock generator's loop bandwidth, which has the benefit of attenuating some of jitter that would normally pass through the 1.6 MHz setting. As the PLL loop bandwidth decreases, the intrinsic jitter of the device increases and is reflected in higher jitter generation specifications, but total output jitter is the best measure of system performance. Total output jitter includes both the generated jitter as well as the transferred jitter.

This lower loop bandwidth option can be useful in some applications, such as PCIe, DSL or other systems which may utilize backplane distributed reference clocks. In these systems, the input clock may have appreciable low frequency jitter (e.g., < 1.6 MHz). The source of the reference clock jitter can arise from suboptimal PCB trace layouts, impedance mismatches and connectors. Input clock jitter may also be generated from an IC which has poor power supply rejection performance, resulting in switching power supply noise and jitter coupling onto the clock input of the Si5335. In these applications, designers may opt to use the 475 kHz loop bandwidth to help attenuate the input clock jitter. Proper selection of PLL loop bandwidth involves a number of application-specific considerations. Refer to “AN513: Jitter Attenuation—Choosing the Right Phase-Locked Loop Bandwidth” for more information.

Please also refer to “AN624: Si5335 Solves Timing Challenges in PCI Express, Computing, Communications and FPGA-Based Systems”.

9. Applications of the Si5335

Because of its flexible architecture, the Si5335 can be configured to serve several functions in the timing path. The following sections describe some common applications.

9.1. Free-Running Clock Generator

Using the internal oscillator (Osc) and an inexpensive external crystal (XTAL), the Si5335 can be configured as a free-running clock generator for replacing high-end and long-lead-time crystal oscillators found on many printed circuit boards (PCBs). Replacing several crystal oscillators with a single IC solution helps consolidate the bill of materials (BOM), reduces the number of suppliers, and reduces the number of long-lead-time components on the PCB. In addition, since crystal oscillators tend to be the least reliable aspect of many systems, the overall failure-in-time (FIT) rate improves with the elimination of each oscillator.

Up to four independent clock frequencies can be generated at any rate within its supported frequency range and with any of supported output types. Figure 25 shows the Si5335 configured as a free-running clock generator.

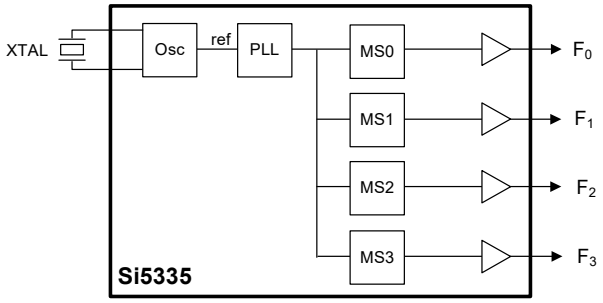


Figure 25. Si5335 as a Free-Running Clock Generator

9.2. Synchronous Frequency Translation

In other cases, it is useful to generate an output frequency that is synchronous (or phase-locked) to another clock frequency. The Si5335 is the ideal choice for generating up to four clocks with different frequencies with a fixed phase relationship to an input reference. Because of its highly precise frequency synthesis, the Si5335 can generate all four output frequencies with 0 ppm error to the input reference. The Si5335 is an ideal choice for applications that have traditionally required multiple stages of frequency synthesis to achieve complex frequency translations. Examples are in broadcast video (e.g., 148.5 MHz to 148.3516483 MHz), WAN/LAN applications (e.g. 155.52 MHz to 156.25 MHz), and Forward Error Correction (FEC) applications (e.g., 156.25 MHz to 161.1328125 MHz). Figure 26 shows the Si5335 configured as a synchronous clock generator. Frequencies may be entered into the ClockBuilder Web utility with up to seven decimal points to ensure that the exact frequencies can be achieved.

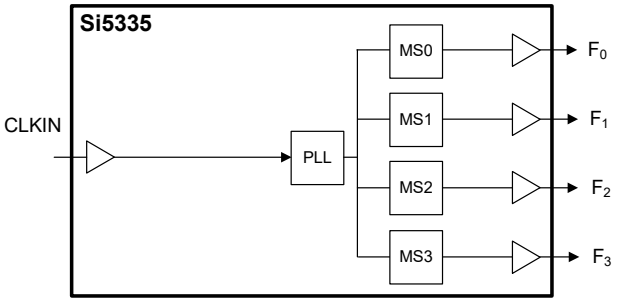


Figure 26. Si5335 as a Synchronous Clock Generator or Frequency Translator

9.3. Configurable Universal Buffer and Level Translator

Using the ClockBuilder web utility, the synthesis stage can be entirely bypassed allowing the Si5335 to act as a configurable clock buffer with level translation. Because of its highly selectable configuration, virtually any output format and I/O voltage combination is possible. The configurable output drivers allow four differential outputs, eight single-ended outputs, or a combination of both. Figure 27 shows the Si5335 configured as a flexible clock buffer supporting mixed I/O supplies.

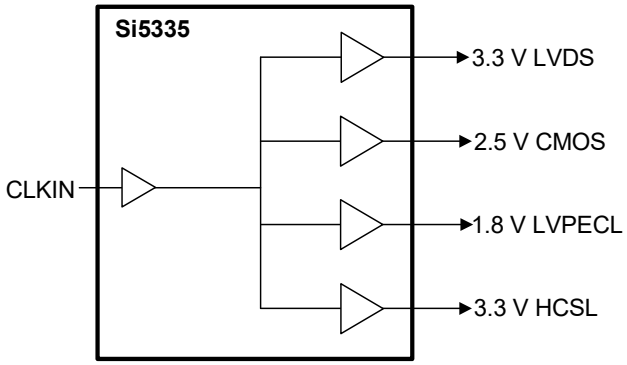
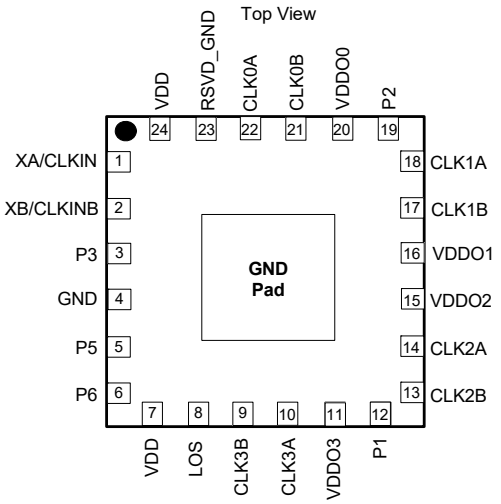


Figure 27. Si5335 as a Configurable Clock Buffer with Level Translation

10. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 15. Si5335 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1,2	XA/CLKIN, XB/CLKINB	I	Multi	**XA/CLKIN, XB/CLKINB.** These pins are used as the main differential or single-ended clock input or as the XTAL input. See "3.4. Input Configuration" on page 19 and Figures 10, 11, and 12 for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal. The single-ended input voltage swing must be limited to 1.2 Vpp.
3	P3	I	Multi	**Multi-Function Input. 3.3 V tolerant.** This pin functions as a multi-function input pin. The pin function (OEB_all, OEB0, OEB1, OEB2, OEB3, SSENB, or RESET) is user-selectable at time of configuration using the ClockBuilder web configuration utility.
4	GND	GND	GND	**Ground.** Must be connected to system ground for proper device operation.
5,6	P5, P6	I	Multi	**Multi-Function Input.** These pins function as multi-function input pins. The pin functions (OEB_all, OEB0, OEB1, OEB2, OEB3, or SSENB) are user-selectable at time of configuration using the ClockBuilder configuration utility. A resistor voltage divider is required when driven by a signal greater than 1.2 V. See "3.6.1. P5 and P6 Input Control" on page 24 for details.
7	VDD	VDD	Supply	**Core Supply Voltage.** This is the core supply voltage, which can operate from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.

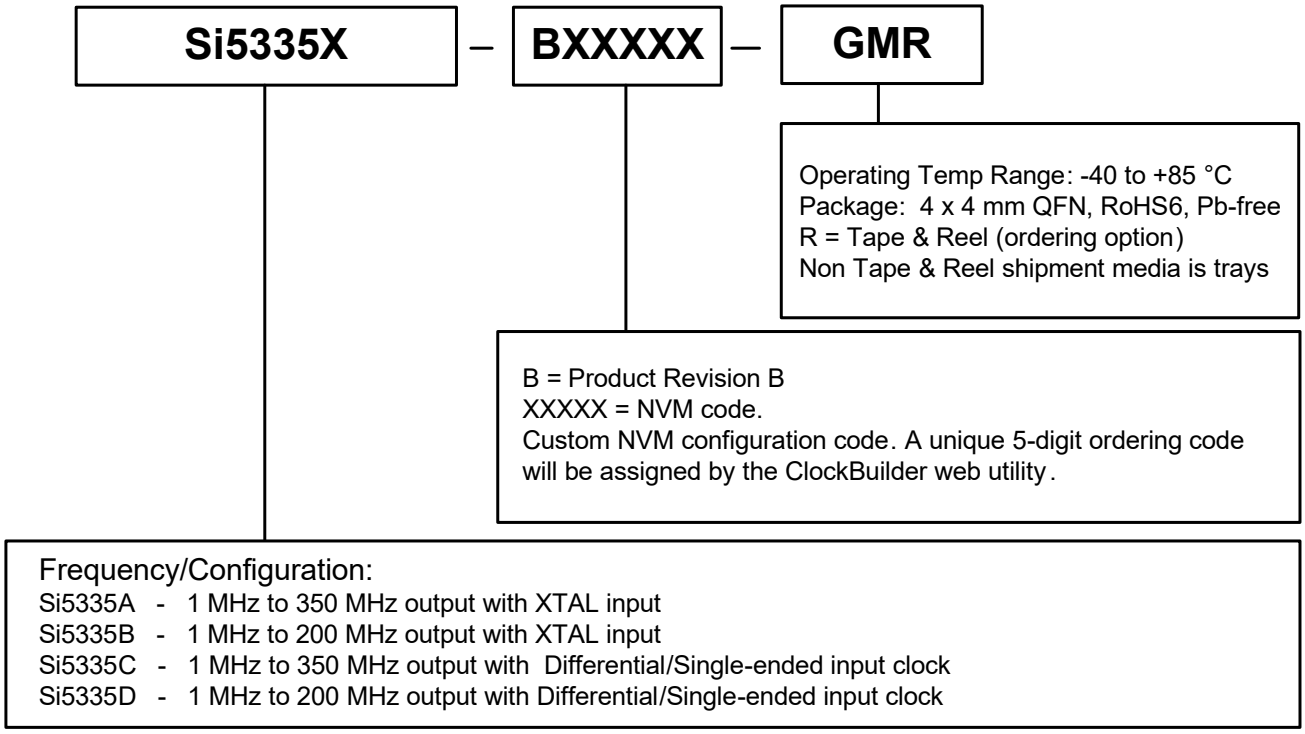
Table 15. Si5335 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
8	LOS	O	Open Drain	**Loss of Signal.** A typical pullup resistor of 1–4 kΩ is used on this pin. This pin can be pulled up to a supply voltage as high as 3.6 V regardless of the other supply voltages on pins 7, 11, 15, 16, 20, and 24. The LOS condition allows the pull up resistor to pull the output up to the supply voltage. See "3.9. Loss-of-Signal Alarm" on page 25. This pin functions as an input clock loss-of-signal and PLL lock status pin in clock generator mode: 0 = Input clock present and PLL locked. 1 = Input clock not present or PLL not locked. In clock buffer mode, LOS is asserted when the input clock is not present.
9	CLK3B	O	Multi	**Output Clock B for Channel 3.** May be a single-ended output or half of a differential output with CLK3A being the other differential half. If unused, leave this pin floating.
10	CLK3A	O	Multi	**Output Clock A for Channel 3.** May be a single-ended output or half of a differential output with CLK3B being the other differential half. If unused, leave this pin floating.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK3A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK3 is not used, this pin must be tied to VDD (pin 7, 24).
12	P1	I	Multi	**Multi-Function Input. 3.3 V tolerant.** This pin functions as a multi-function input pin. The pin function (OEB_all, OEB0, OEB1, OEB2, OEB3, SSENB, FS0, FS1, or RESET) is user-selectable at time of configuration using the ClockBuilder web configuration utility
13	CLK2B	O	Multi	**Output Clock B for Channel 2.** May be a single-ended output or half of a differential output with CLK2A being the other differential half. If unused, leave this pin floating.
14	CLK2A	O	Multi	**Output Clock A for Channel 2.** May be a single-ended output or half of a differential output with CLK2B being the other differential half. If unused, leave this pin floating.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK2A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK2 is not used, this pin must be tied to VDD (pin 7, 24).
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK1A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK1 is not used, this pin must be tied to VDD (pin 7, 24).

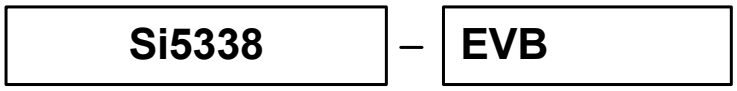
Table 15. Si5335 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
17	CLK1B	O	Multi	**Output Clock B for Channel 1.** May be a single-ended output or half of a differential output with CLK1A being the other differential half. If unused, leave this pin floating.
18	CLK1A	O	Multi	**Output Clock A for Channel 1.** May be a single-ended output or half of a differential output with CLK1B being the other differential half. If unused, leave this pin floating.
19	P2	I	Multi	**Multi-Function Input. 3.3 V tolerant.** This pin functions as a multi-function input pin. The pin function (OEB_all, OEB0, OEB1, OEB2, OEB3, SSENB, FS1, or RESET) is user-selectable at time of configuration using the ClockBuilder web configuration utility.
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK0A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK0 is not used, this pin must be tied to VDD (pin 7, 24).
21	CLK0B	O	Multi	**Output Clock B for Channel 0.** May be a single-ended output or half of a differential output with CLK0A being the other differential half. If unused, leave this pin floating.
22	CLK0A	O	Multi	**Output Clock A for Channel 0.** May be a single-ended output or half of a differential output with CLK0B being the other differential half. If unused, leave this pin floating.
23	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	GND	**Ground Pad.** This is the large pad in the center of the package. The device will not function unless the ground pad is properly connected to a ground plane on the PCB. See Table 17, “PCB Land Pattern,” on page 43 for ground via requirements.

11. Ordering Information



Evaluation Boards



Si5335 Evaluation Board

The Si5338-EVB with ClockBuilder Desktop software includes the ability to evaluate Si5335 output frequency and format configurations. The EVB does not currently include the ability to control the programmable function pins (P1, P2, P3, P5, and P6).

12. Package Outline: 24-Lead QFN

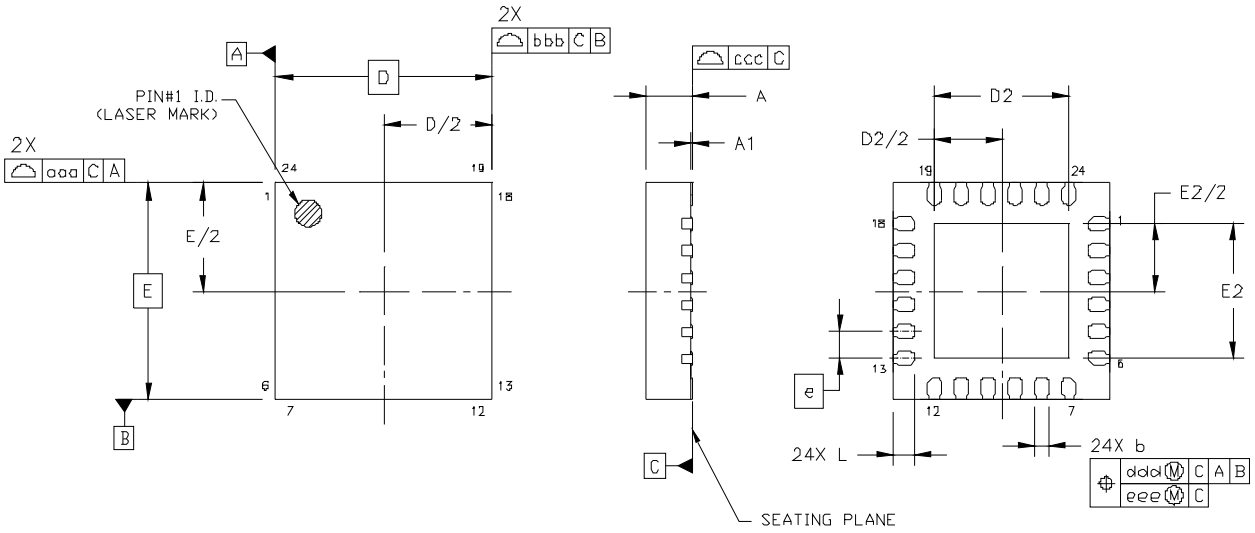


Figure 28. 24-Lead Quad Flat No-lead (QFN)

Table 16. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Terminal base alloy: Cu
6. Terminal plating/grid array material: Au/NiPd.
7. Visit https://www.skyworksinc.com/support-ia for more information.

13. Recommended PCB Land Pattern

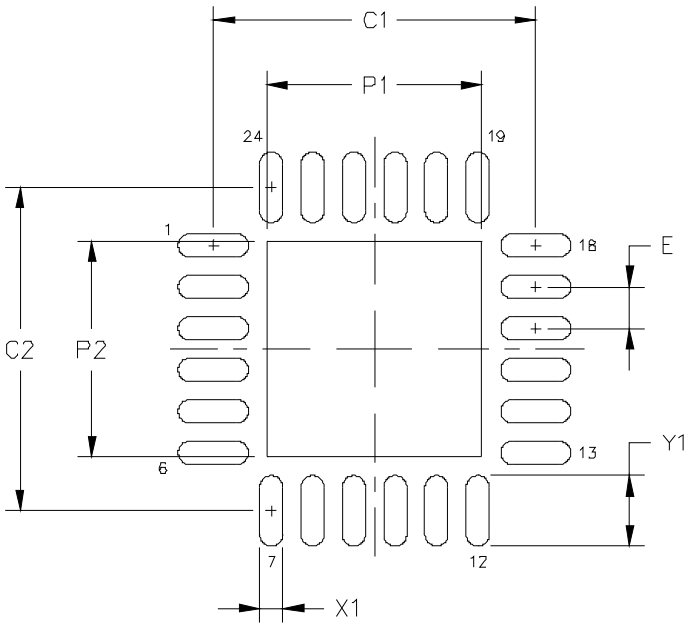


Table 17. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias. These 5 vias should have a length of no more than 20 mils to the ground plane. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design:

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

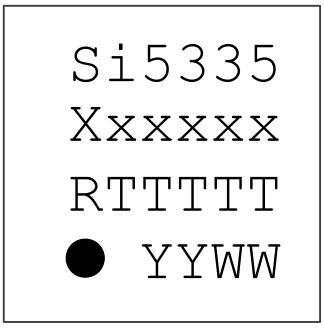
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly:

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

14. Top Marking

14.1. Si5335 Top Marking



14.2. Top Marking Explanation

Line	Characters	Description
Line 1	Si5335	Base part number.
Line 2	Xxxxxx	X = Frequency and configuration code. See "11. Ordering Information" on page 41 for more information. xxxxx = NVM code assigned by ClockBuilder web utility. See "11. Ordering Information" on page 41.
Line 3	RTTTTT	R = Product revision. TTTTT = Manufacturing trace code.
Line 4	Circle with 0.5 mm diameter; left-justified	Pin 1 indicator.
	YYWW	YY = Year. WW = Work week. Characters correspond to the year and work week of package assembly.

15. Device Errata

Please visit www.skyworksinc.com to access the device errata document.

Document Change List

Revision 0.4 to Revision 0.9

- Updated Table 2, “DC Characteristics,” on page 4.
  - Added core power supply specification in buffer mode.
- Updated Table 3, “Performance Characteristics,” on page 5.
  - Added T_{RESET} specification.
- Updated Table 4, “Input and Output Clock Characteristics,” on page 6.
  - Corrected V_I on pin 1 to 1.3 V (max).
  - Updated CML output voltage specification to 0.86 Vpp.
- Updated Table 6, “Crystal Specifications for 25 MHz,” on page 9.
  - Corrected CL to 18 pF (typical).
- Updated Table 7, “Crystal Specifications for 27 MHz,” on page 9.
  - Corrected CL to 18 pF (typical).
- Updated "3.4. Input Configuration" on page 19.
  - Revised text in Section 3.4.2.
- Updated "3.6.1. P5 and P6 Input Control" on page 24.
  - Added Figure 13 to replace Table 15.
- Updated Figure 21 on page 31.
- Updated Table 14 on page 23.
  - Corrected Assignable Pin Name column entries.
- Updated "3.10. Output Stage" on page 26.
  - Revised throughout and included termination circuit diagrams and text.
- Removed references to P4 as a programmable pin option throughout document. Pin 4 is now a ground pin.

Revision 0.9 to Revision 1.0

- Updated Table 9 on page 12.
  - DSL random jitter from 2.1 ps RMS (typ) to 1.95 ps RMS (typ) and from "—" (max) to 2.2 ps RMS (max).
- Corrected text in “9.2. Synchronous Frequency Translation” to match the capabilities of the ClockBuilder web utility.

Revision 1.0 to Revision 1.1

- Updated Table 8 on page 10 and Table 9 on page 12.
  - Updated typical specifications for total jitter for PCI Express 1.1 Common clocked topology.
  - Updated typical specifications for RMS jitter for PCI Express 2.1 Common clocked topology.
- Updated Table 10 on page 14.
  - Updated typical additive jitter (12 kHz–20MHz) from 0.150 to 0.165 ps RMS.
- Added " Document Change List" on page 46.

Revision 1.1 to Revision 1.2

- Removed down spread spectrum errata that has been corrected in revision B.
- Updated ordering information to refer to revision B silicon.
- Updated top marking explanation in Section 14.2.

Revision 1.2 to Revision 1.3

- Added link to errata document.

Revision 1.3 to Revision 1.4

- Updated Features on page 1.
- Updated Description on page 1.
- Updated specs in Table 8.
- Updated specs in Table 9.

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