



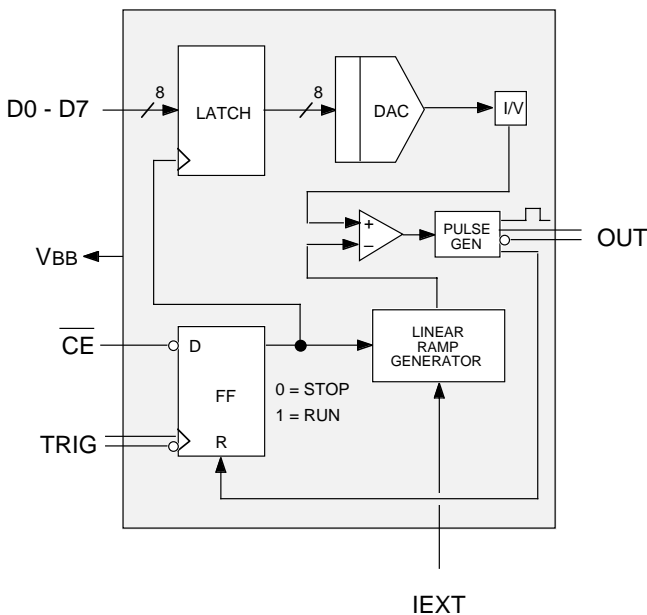
**THE DATASHEET OF
SY604JZ-TR**



FEATURES

- True 125MHz retrigger rate
- Pin-compatible with Bt604
- 15ps delay resolution
- Less than ± 1 LSB timing accuracy
- Differential TRIGGER inputs
- Delay spans from 4 to 40ns
- Compatible with 10KH ECL logic
- Lower power dissipation 350mW typical
- Available in 28-pin plastic (PLCC) or metal (MLCC) J-lead package

BLOCK DIAGRAM



DESCRIPTION

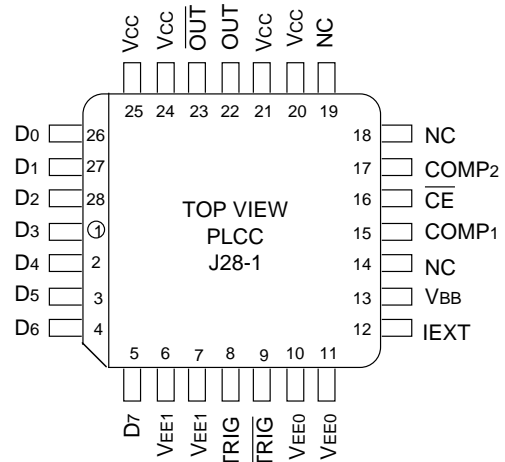
Micrel-Synergy's SY604 is an ECL-compatible timing vernier (delay generator) whose time delay is programmed via an 8-bit code which is loaded concurrently with the circuit trigger. The SY604 is fabricated in Micrel-Synergy's proprietary ASSET™ bipolar process.

This device can be retriggered at speeds up to 125MHz, with a delay span as short as 4ns. At minimum span, the resolution is $4\text{ns}/255 = 15.7\text{ps}$ per step. The delay span is externally adjustable up to 40ns. The SY604 employs differential TRIGGER inputs, and produces a differential OUTPUT pulse; all other control signals are single-ended ECL. Edge delay is specified by an 8-bit input which is loaded into the device with the TRIGGER. The output pulse width will typically be 3.5ns.

The SY604 is commonly used in Automatic Test Equipment to provide precise timing edge placement; it is also found in many instrumentation and communications applications.

Micrel-Synergy's circuit design techniques coupled with ASSET™ technology result in not only ultra-fast performance, but allow device operation at lower power dissipation than competing technologies. Outstanding reliability is achieved in volume production.

PIN CONFIGURATION



PIN DESCRIPTION

D0 – D7

Data input pins (ECL compatible). On the rising edge of TRIG, a ramp is initiated whereupon D0-D7 are latched into the device. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.

\overline{CE}

Chip enable input (ECL compatible). \overline{CE} must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If \overline{CE} is floating, the trigger will always be enabled.

TRIG, \overline{TRIG}

Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if \overline{CE} is a logical zero. If \overline{CE} is a logical one, no operation occurs. It is recommended that triggering be performed with differential inputs.

OUT, \overline{OUT}

Differential outputs (ECL compatible).

IEXT

Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically $-1.25V$.

COMP1, COMP2

Compensation pins. A $0.1\mu F$ ceramic capacitor must be connected between COMP1 and V_{EE0} , and COMP2 and V_{EE0} (see Figure 3).

V_{EE}

Device power. All V_{EE} pins must be connected.

V_{CC}

Device ground. All V_{CC} pins must be connected together.

V_{BB}

A $-1.36V$ (typical) output.

FUNCTIONAL DESCRIPTION

The output pulse generation cycle begins with the arrival of TRIG shown in **Figure 1**. When TRIG transitions to a high and \overline{CE} is low, the values on D0 - D7 are latched, thereby setting the DAC values. Simultaneously with the latching of D0 - D7, the linear ramp generator is enabled.

When the ramp level reaches that of the DAC, the comparator initiates the pulse generator to produce an output pulse of fixed width. The generation of an output pulse resets the ramp and the cycle is ready to begin again.

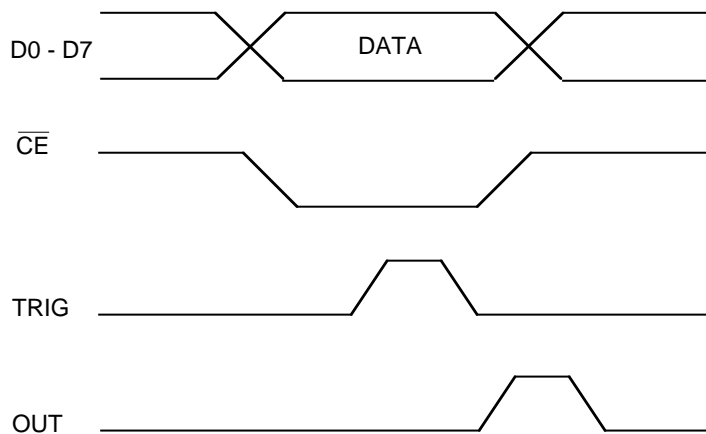


Figure 1.

ABSOLUTE MAXIMUM RATING⁽¹⁾

Symbol	Parameter	Value	Unit
VEE	Power Supply (V _{CC} = 0V)	-8 to 0	V
V _I	Input Voltage (V _{CC} = 0V)	0 to VEE	V
I _{OUT}	Output Current — Continuous — Surge	50 100	mA
TA	Operating Temperature Range	0 to +85	°C
VEE	Operating Range ⁽²⁾	-5.7 to -4.2	V

NOTES:

- Beyond which device life may be impaired.
- Parametric values specified at 10E Series: - 4.75V to - 5.5V.

DC CHARACTERISTICS⁽¹⁾

Symbol	Parameter	TA = +0°C			TA = +25°C			TA = +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{IH}	Input HIGH Voltage (10K)	-1170	—	-840	-1130	—	-810	-1070	—	-735	mV
V _{IL}	Input LOW Voltage (10K)	-1950	—	-1480	-1950	—	-1480	-1950	—	-1450	mV
V _{OH}	Output HIGH Voltage (10K)	-1020	-975	-840	-980	-920	-810	-920	-850	-735	mV
V _{OL}	Output LOW Voltage (10K)	-1950	-1755	-1630	-1950	-1750	-1630	-1950	-1720	-1600	mV
I _{IH}	Input High Current (V _{in} = V _{IH} max)	—	100	150	—	100	150	—	100	150	μA
I _{IH}	TRIG, $\overline{\text{TRIG}}$	—	100	150	—	100	150	—	100	150	μA
I _{IL}	Input Low Current (V _{in} = V _{IL} min)	—	100	150	—	100	150	—	100	150	μA
I _{IL}	TRIG, $\overline{\text{TRIG}}$	—	100	150	—	100	150	—	100	150	μA
DL	Output Delay Spans	—	±0.84	±0.9	—	±0.84	±0.9	—	±0.84	±0.9	LSB
IL	Differential Linearity Error**	—	±1.16	±1.25	—	±0.89	±1.0	—	±0.89	±1.0	LSB
IL	Integral Linearity Error**	—	±1.16	±1.25	—	±0.89	±1.0	—	±0.89	±1.0	LSB
V _{BB}	V _{BB} Output Voltage	-1.44	—	-1.25	-1.44	-1.35	-1.25	-1.44	—	-1.25	V
I _{EXT}	I _{EXT} for Tspans										
	Tspan = 4ns	1.80	2.38	2.80	1.80	2.38	2.80	1.80	2.38	2.80	mA
	Tspan = 5ns	1.45	1.85	2.40	1.45	1.85	2.40	1.45	1.85	2.40	mA
	Tspan = 10ns	0.70	0.93	1.20	0.70	0.93	1.20	0.70	0.93	1.20	mA
	Tspan = 15ns	0.45	0.62	0.80	0.45	0.62	0.80	0.45	0.62	0.80	mA
	Tspan = 20ns	0.34	0.46	0.60	0.34	0.46	0.60	0.34	0.46	0.60	mA
	Tspan = 30ns	0.20	0.30	0.40	0.20	0.30	0.40	0.20	0.30	0.40	mA
	Tspan with I _{EXT} = 1.8 mA (Tspan = T _{max} - T _{min})	4.1	—	6.5	4.1	—	6.5	4.1	—	6.5	ns
T _{min}	Minimum Delay Time*										
	Data = 00, Tspan = 5ns	—	2.8	3.8	—	2.8	3.8	—	2.8	3.8	ns
	Tspan = 10ns	—	3.4	4.9	—	3.4	4.9	—	3.4	4.9	ns
	Tspan = 15ns	—	4.0	6.0	—	4.0	6.0	—	4.0	6.0	ns
	Tspan = 20ns	—	4.6	7.1	—	4.6	7.1	—	4.6	7.1	ns
	Tspan = 25ns	—	5.2	8.2	—	5.2	8.2	—	5.2	8.2	ns
	Tspan = 30ns	—	5.8	9.3	—	5.8	9.3	—	5.8	9.3	ns
I _{EE}	VEE Supply Current	—	—	100	—	70	100	—	—	100	mA

NOTE:

- 10K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts.

AC CHARACTERISTICS

ECL input values are -0.9 to -1.7V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs.

OUT and $\overline{\text{OUT}}$ loading with 50Ω to -2.0V. Typical values are based on nominal temperature, i.e., and nominal voltage, i.e., -5.2V.

Symbol	Parameter	TA = +0°C			TA = +25°C			TA = +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
fMAX	Trigger Rate ⁽¹⁾	—	—	125	—	—	125	—	—	125	MHz
tWI	Trigger Width High	2.0	1.0	—	2.0	1.0	—	2.0	1.0	—	ns
tWO	Output Pulse Width High Time	2.5	3.5	4.5	2.5	3.5	4.5	2.5	3.5	4.5	ns
ts	Output Pulse Rise/Fall Time (20/80%)	—	550	750	—	550	750	—	550	750	ps
	Output Pulse Spacing Span = 4ns @ 1 LSB	8.0	—	—	8.0	—	—	8.0	—	—	ns
	Minimum Delay Time vs. Tspan ΔT_{00} / ns (Tspan = 5 to 10ns)	—	125	220	—	125	220	—	125	220	ps/ns
1 LSB	Output Delay	4.0	—	40	4.0	—	40	4.0	—	40	ns
1 LSB	Tspan (Tspan = Tmax - Tmin)	15.7	—	157	15.7	—	157	15.7	—	157	ps
	Resolution (Tspan / 225)	—	—	—	—	—	—	—	—	—	ps
	Tempo (5ns Span)	—	2	—	—	2	—	—	2	—	ps/°C
	ΔT_{span} / °C	—	2	—	—	2	—	—	2	—	ps/°C
	ΔT_{min} / °C	—	60	—	—	60	—	—	60	—	ps/V
	Power Supply Rejection (Data = 0-FF HEX, Tspan = 5ns)	—	60	—	—	60	—	—	60	—	ps/V
ts	$\overline{\text{CE}}$ Setup Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
tH	$\overline{\text{CE}}$ Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns
tWH	WRITE Pulse Width High Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
tDS	D0 - D7 Setup Time	1.0	—	—	1.0	—	—	1.0	—	—	ns
tDH	D0 - D7 Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns

NOTE:

1. See chart below:

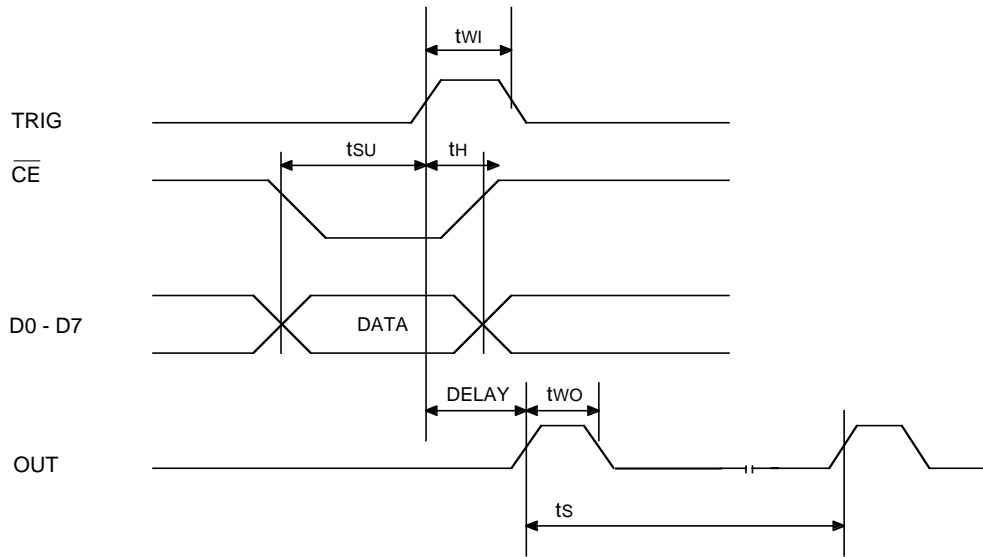
Maximum Tspan and Trigger Rates

Maximum Tspan (ns) Maintaining Linearity	Minimum Trigger Periods (ns)
of ± 1 LSB	
4.0	8.0
5.1	10.0
5.8	11.1
6.75	12.5
8.1	14.3
9.9	16.6
12.0	20.0
15.5	25.0
22.0	33.3

The information in this table is guaranteed but not 100% production tested.

See Figure 2 for a graphical representation.

TIMING DIAGRAMS



**± 1 LSB
Span vs. Trigger Rates**

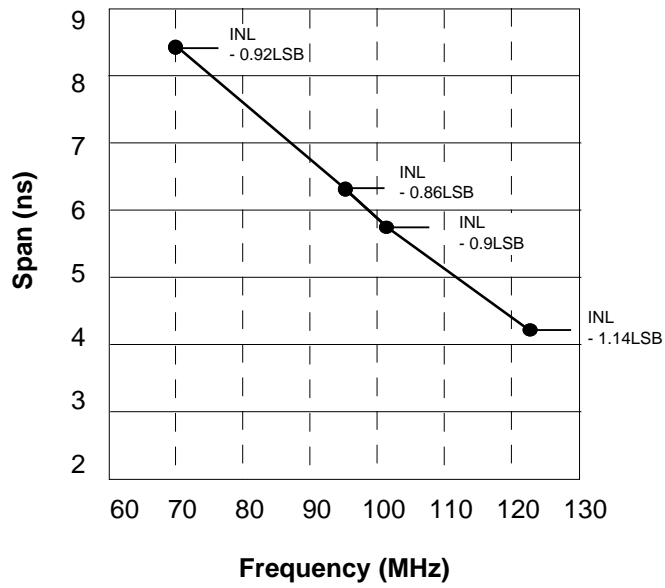
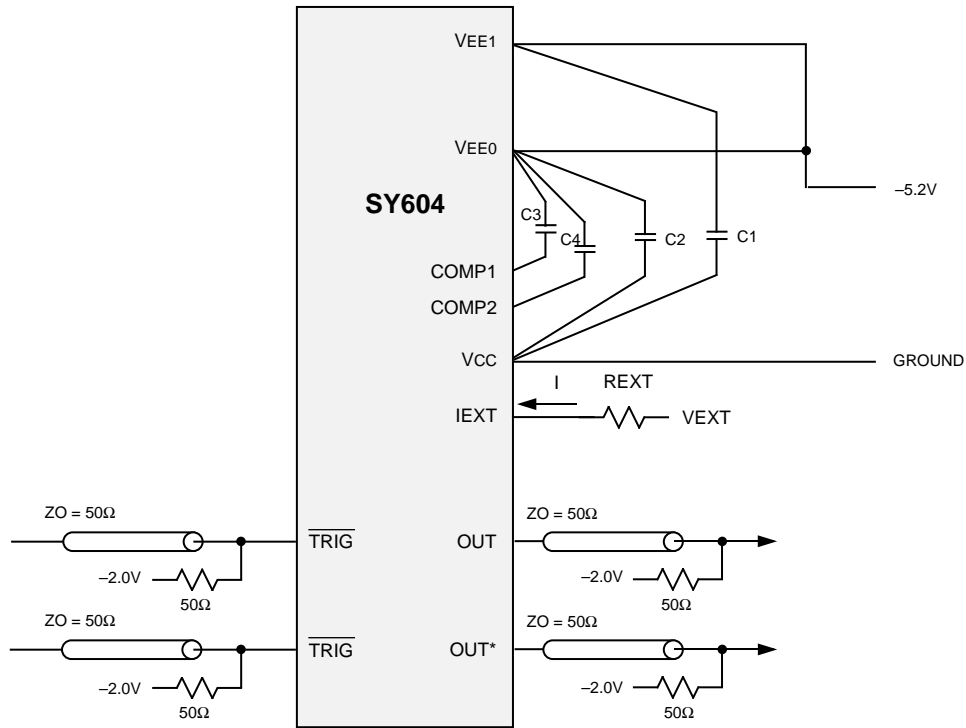


Figure 2.

APPLICATION DIAGRAM



REXT Calculation:

$$REXT = (VEXT + 1.25V)/IEXT$$

For Example:

If Tspan is around 15ns, then IEXT is around 0.6mA, (see DC Characteristic Table) and assume IEXT pin is tied to Vcc with the resistor.

$$REXT = 0 + 1.25V/0.6mA$$

$$= 2.08K\ ohm$$

Location	Description	Vendor Part Number
C1–C4	0.1µF ceramic capacitor	Erie RPE112Z5U104M50V
REXT	1% metal film resistor (selected for proper Tspan)	CB301210 Dale CMF-55C

NOTE:

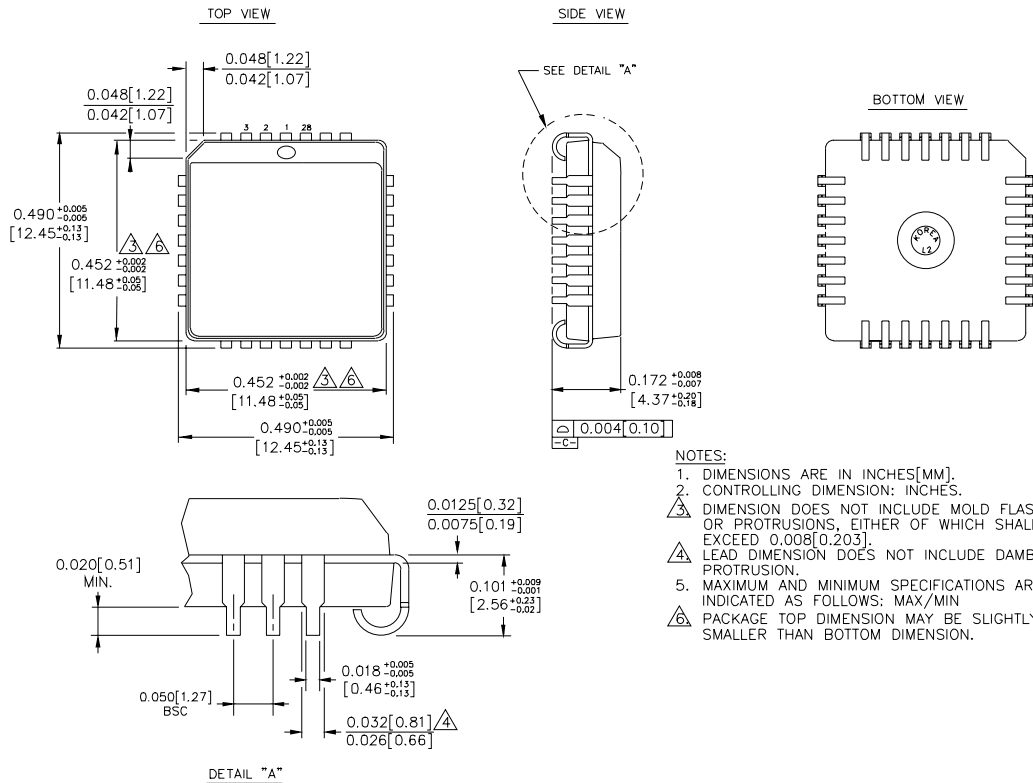
The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SY604. All devices should be as close as possible to the SY604.

Figure 3. Typical Connection Diagram and Parts List.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY604JC	J28-1	Commercial
SY604JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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