



**THE DATASHEET OF  
S6E1C12B0AGN20000**





**THIS SPEC IS OBSOLETE**

Spec No: 002-00234

Spec Title: S6E1C1 SERIES 32-BIT ARM(R) CORTEX(R)-  
M0+ FM0+ MICROCONTROLLER

Replaced by: 002-00233

The S6E1C1 Series is a series of highly integrated 32-bit microcontrollers designed for embedded controllers aiming at low power consumption and low cost. This series has the ARM Cortex-M0+ Processor with on-chip Flash memory and SRAM, and consists of peripheral functions such as various timers, ADC and communication interfaces (UART, CSIO (SPI), I<sup>2</sup>C, I<sup>2</sup>S, and Smart Card). The products which are described in this data sheet are placed into TYPE3-M0+ product categories in "FM0+ Family Peripheral Manual".

## Features

### 32-bit ARM Cortex-M0+ Core

- Processor version: r0p1
- Maximum operating frequency: 40.8 MHz
- Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 24 peripheral interrupt with 4 selectable interrupt priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

### Bit Band Operation

Compatible with Cortex-M3 bit band operation.

### On-Chip Memory

- Flash memory
  - Up to 128 Kbytes
  - Read cycle: 0 wait-cycle
  - Security function for code protection
- SRAM  
The on-chip SRAM of this series has one independent SRAM .
  - Up to 16 Kbytes
  - 4Kbytes: can retain value in Deep standby Mode

### Multi-Function Serial Interface (Max 6channels)

- 3 channels with 64Byte FIFO (Ch.4, 6 and 7), 3 channels without FIFO (Ch.0, 1 and 3)
- The operation mode of each channel can be selected from one of the following.
  - UART
  - CSIO (CSIO is known to many customers as SPI)
  - I<sup>2</sup>C
- UART
  - Full duplex double buffer
  - Parity can be enabled or disabled.
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control\* : Automatically control the transmission by CTS/RTS (only ch.4)
  - \* : S6E1C12B0A/S6E1C11B0A and S6E1C12C0A/S6E1C11C0A do not support Hardware Flow control.
  - Various error detection functions (parity errors, framing errors, and overrun errors)

- CSIO (also known as SPI)
  - Full duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detection function
  - Serial chip select function (ch1 and ch6 only)
  - Data length: 5 to 16 bits
- I<sup>2</sup>C
  - Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400 kbps) supported.
- I<sup>2</sup>S (MFS-I2S)
  - Using CSIO (Max 2 ch: ch.4, ch.6) and I<sup>2</sup>S clock generator
  - Supports two transfer protocol
    - I<sup>2</sup>S
    - MSB-justified
  - Master mode only

### I2C Slave

- I2C Slave supports the slave function of I2C and wake-up function from Standby mode.

### Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor that has already been constructed on the memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

### A/D Converter (Max: 8 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 μs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

### Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

## General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1 cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 54 fast general-purpose I/O ports @64-pin package
- Certain ports are 5 V tolerant.  
See 4.List of Pin Functions and 5.I/O Circuit Type for the corresponding pins.

## Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

## Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

## Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

## External Interrupt Controller Unit

- Up to 12 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

## Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

## CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

## HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

## Smart Card Interface (Max 1 Channel)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

## Clock and Reset

- Clocks
 

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 8 MHz to 48 MHz

- Sub clock: 32.768 kHz
- Built-in high-speed CR clock: 8 MHz
- Built-in low-speed CR clock: 100 kHz
- Main PLL clock: 8MHz to 16MHz (Input), 75MHz to 150MHz (Output)

### ■ Resets

- Reset request from the INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detection reset
- Clock supervisor reset

### Clock Supervisor (CSV)

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

### Low-Voltage Detector (LVD)

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVD1: monitor VCC and error reporting via an interrupt
- LVD2: auto-reset operation

### Low Power Consumption Mode

This series has six low power consumption modes.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable between keeping the value of RAM and not)
- Deep standby Stop (selectable between keeping the value of RAM and not)

### Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

### Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

### Unique ID

A 41-bit unique value of the device has been set.

### Power Supply

- Wide voltage range: VCC = 1.65V to 3.6 V

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# 1. Product Lineup

## Memory Size

Product name	S6E1C11B0A/ S6E1C11C0A/ S6E1C11D0A	S6E1C12B0A/ S6E1C12C0A/ S6E1C12D0A
On-chip Flash memory	64 Kbytes	128 Kbytes
On-chip SRAM	12 Kbytes	16 Kbytes

## Function

Product name	S6E1C12B0A/ S6E1C11B0A	S6E1C12C0A/ S6E1C12C0A	S6E1C11D0A/ S6E1C12D0A
Pin count	32	48	64
CPU	Cortex-M0+		
Frequency	40.8 MHz		
Power supply voltage range	1.65 V to 3.6 V		
DSTC	64 ch.		
Multi-function Serial Interface (UART/CSIO/I <sup>2</sup> C/I2S)	4 ch. (Max) Ch.0/1/3 without FIFO Ch. 6 with FIFO	6 ch. (Max) Ch.0/1/3 without FIFO Ch.4/6/7 with FIFO	6 ch. (Max) Ch.0/1/3 without FIFO Ch.4/6/7 with FIFO
	I2S : No	I2S : 1 ch (Max) Ch. 6 with FIFO	I2S : 2 ch (Max) Ch. 4/6 with FIFO
Base Timer (PWC/Reload timer/PWM/PPG)	8 ch. (Max)		
Dual Timer	1 unit		
HDMI-CEC/ Remote Control Receiver	1 ch.(Max) Ch.1	2 ch (Max) Ch.0/1	
I2C Slave	1 ch (Max)		
Smart Card Interface	No	1 ch (Max)	
Real-time Clock	1 unit		
Watch Counter	1 unit		
CRC Accelerator	Yes		
Watchdog timer	1 ch. (SW) + 1 ch. (HW)		
External Interrupt	7 pins (Max), NMI x 1	9 pins (Max), NMI x 1	12 pins (Max), NMI x 1
I/O port	24 pins (Max)	38 pins (Max)	54 pins (Max)
12-bit A/D converter	6 ch. (1 unit)	8 ch. (1 unit)	8 ch. (1 unit)
CSV (Clock Supervisor)	Yes		
LVD (Low-voltage Detection)	2 ch.		
Built-in CR	High-speed	8 MHz (Typ)	
	Low-speed	100 kHz (Typ)	
Debug Function	SW-DP		
Unique ID	Yes		

### Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.  
See "11. Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

## 2. Packages

Package	Product name	S6E1C12B0A/ S6E1C11B0A	S6E1C12C0A/ S6E1C11C0A	S6E1C12D0A/ S6E1C11D0A
LQFP: LQB032 (0.80 mm pitch)		○	-	-
QFN: WNU032 (0.50 mm pitch)		○		
LQFP: LQA048-02 (0.50 mm pitch)		-	○	-
QFN: WNY048 (0.50 mm pitch)		-	○	-
LQFP: LQD064-02 (0.50 mm pitch)		-	-	○
QFN: WNS064 (0.50 mm pitch)		-	-	○

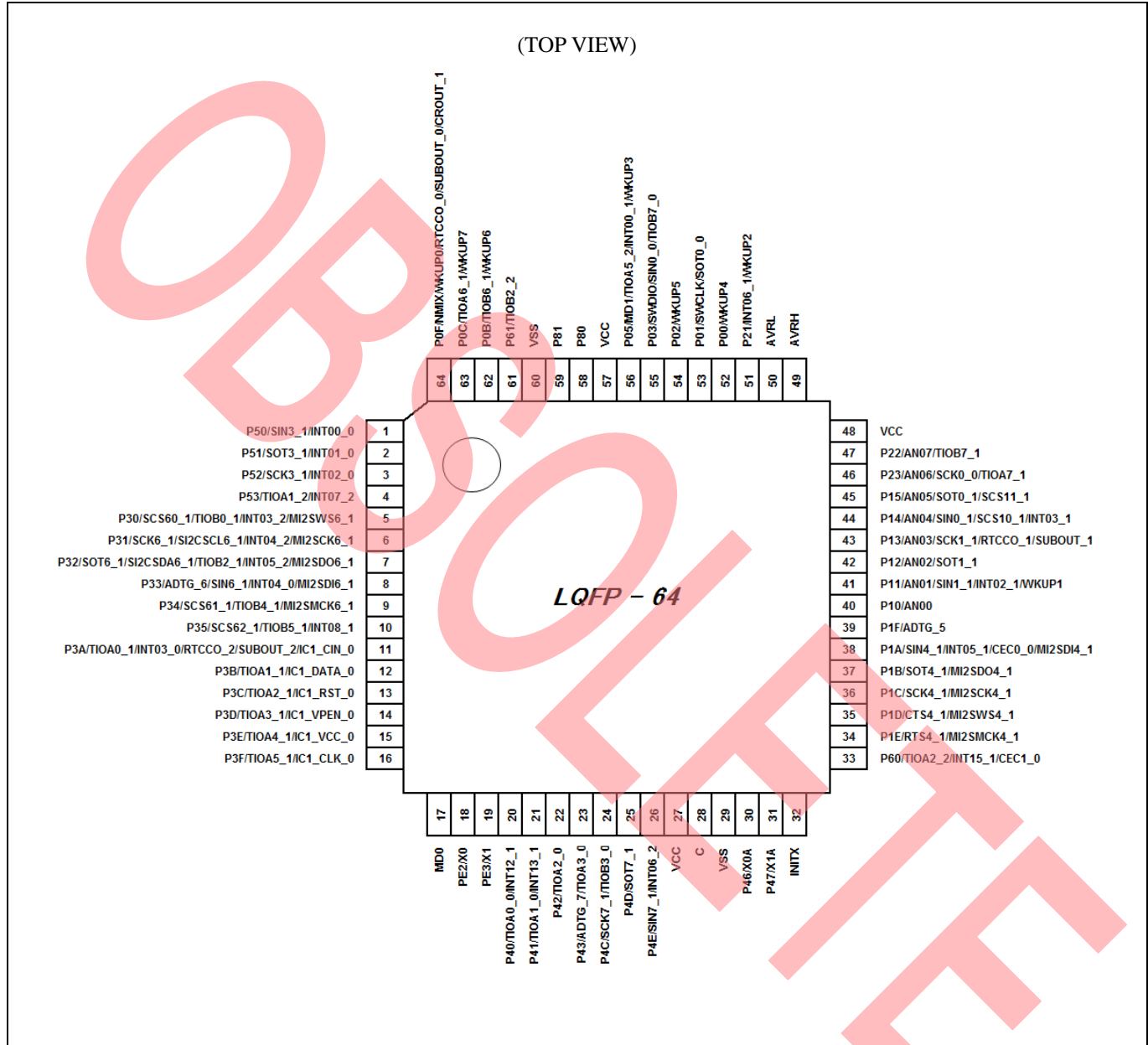
○: Available

**Note:**

- See "13. Package Dimensions" for detailed information on each package.

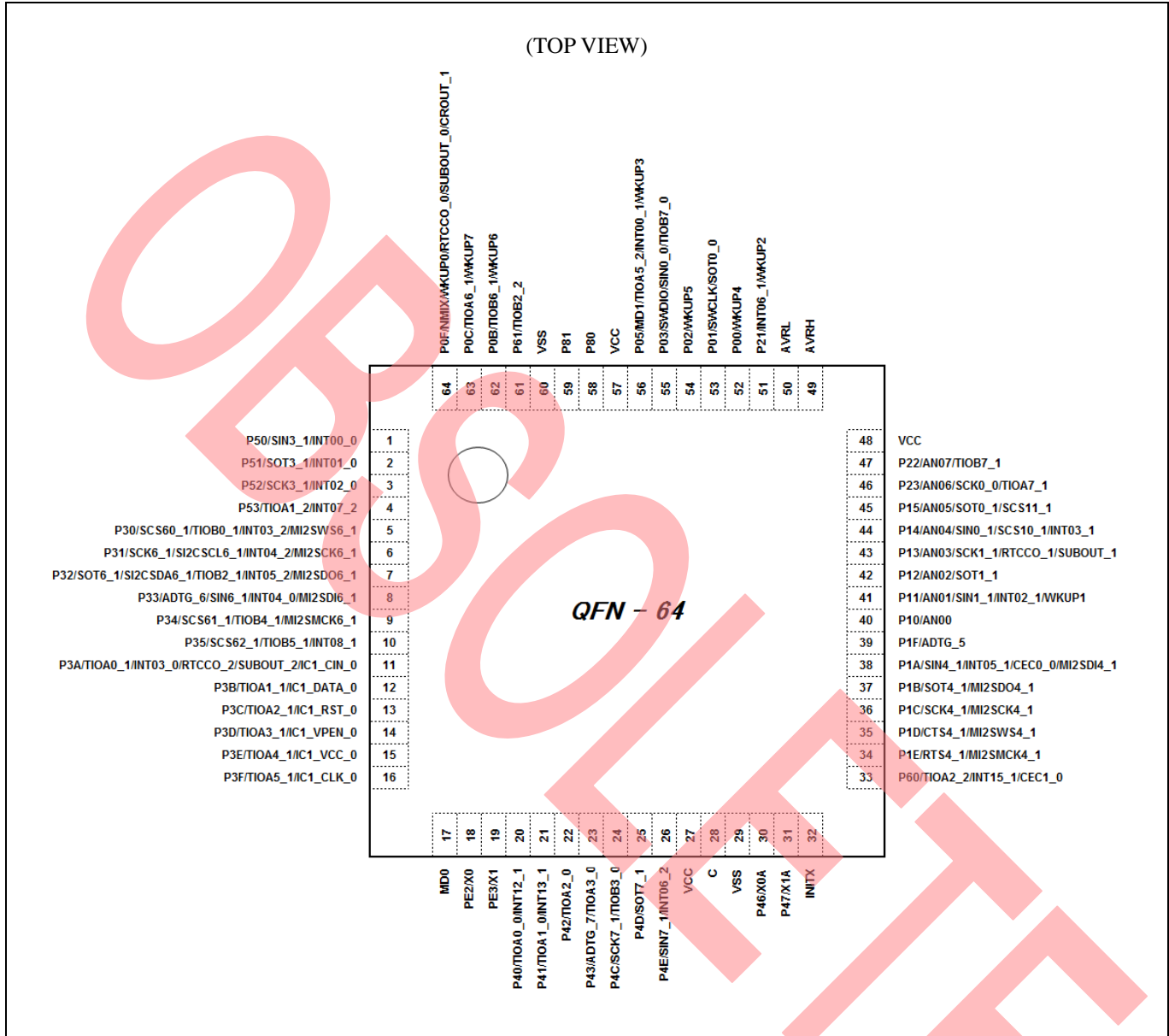
### 3. Pin Assignment

LQD064-02



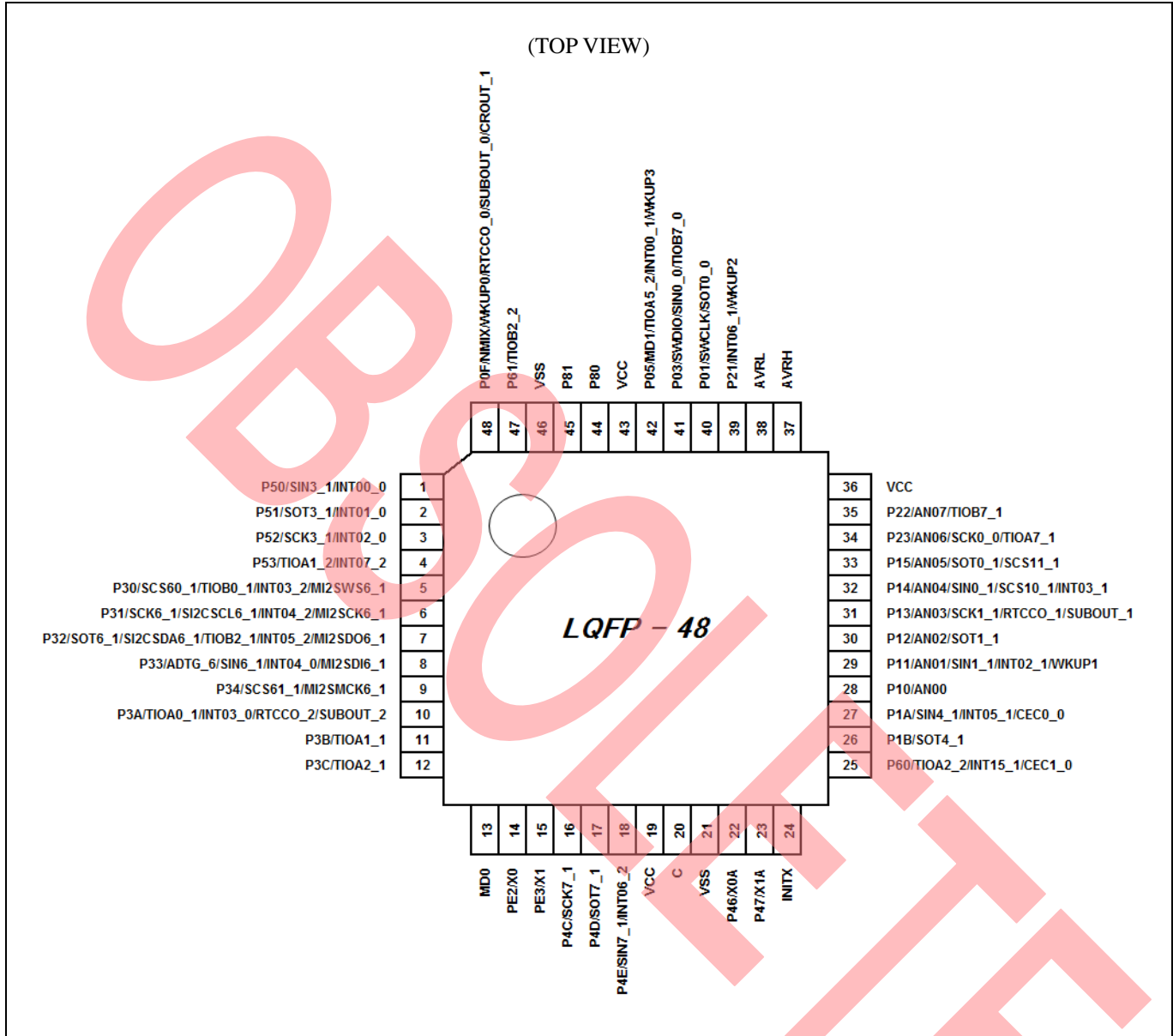
**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.



**Note:**

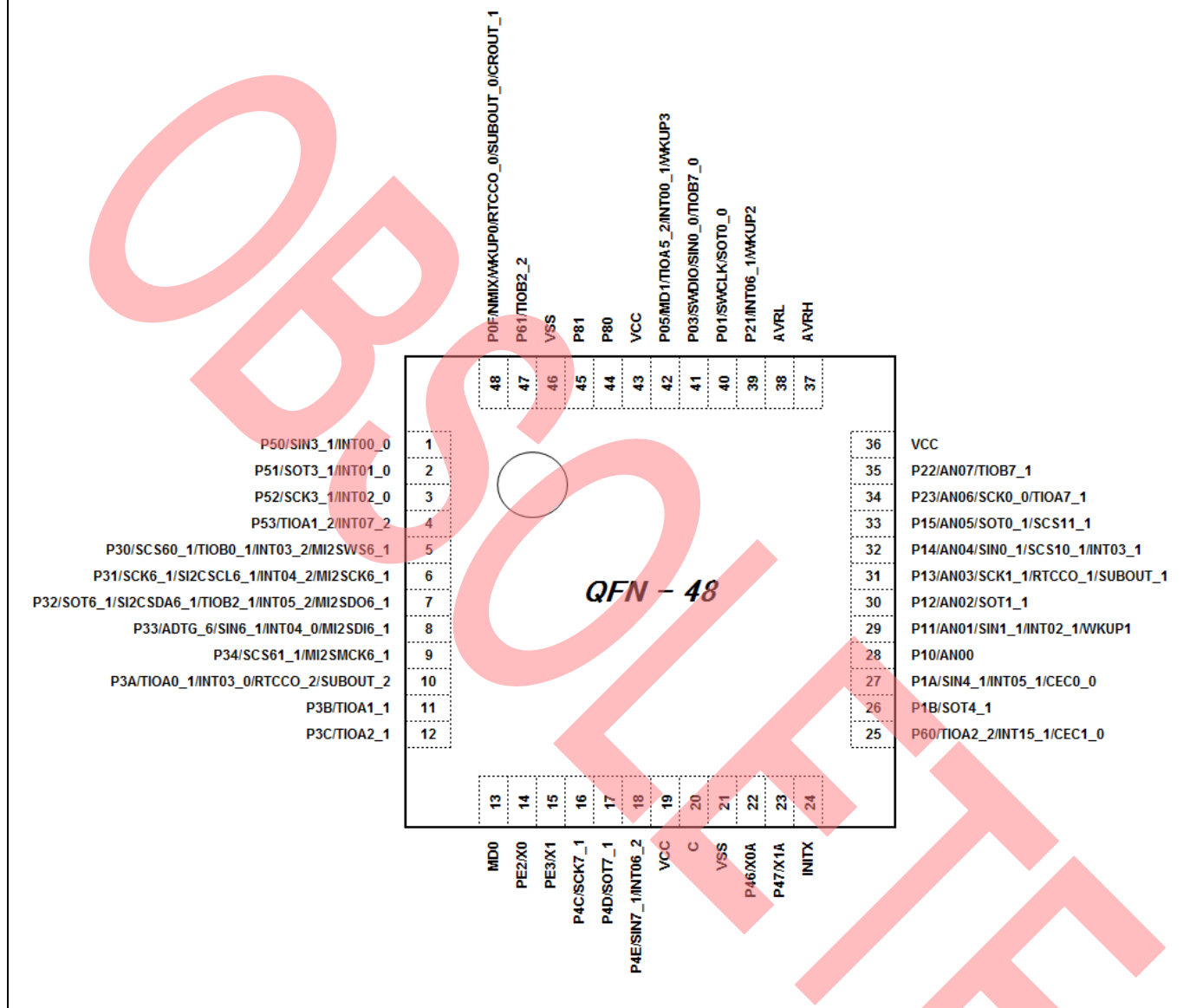
- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the *Extended Port Function Register (EPFR)* to select the pin to be used.



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the *Extended Port Function Register (EPFR)* to select the pin to be used.

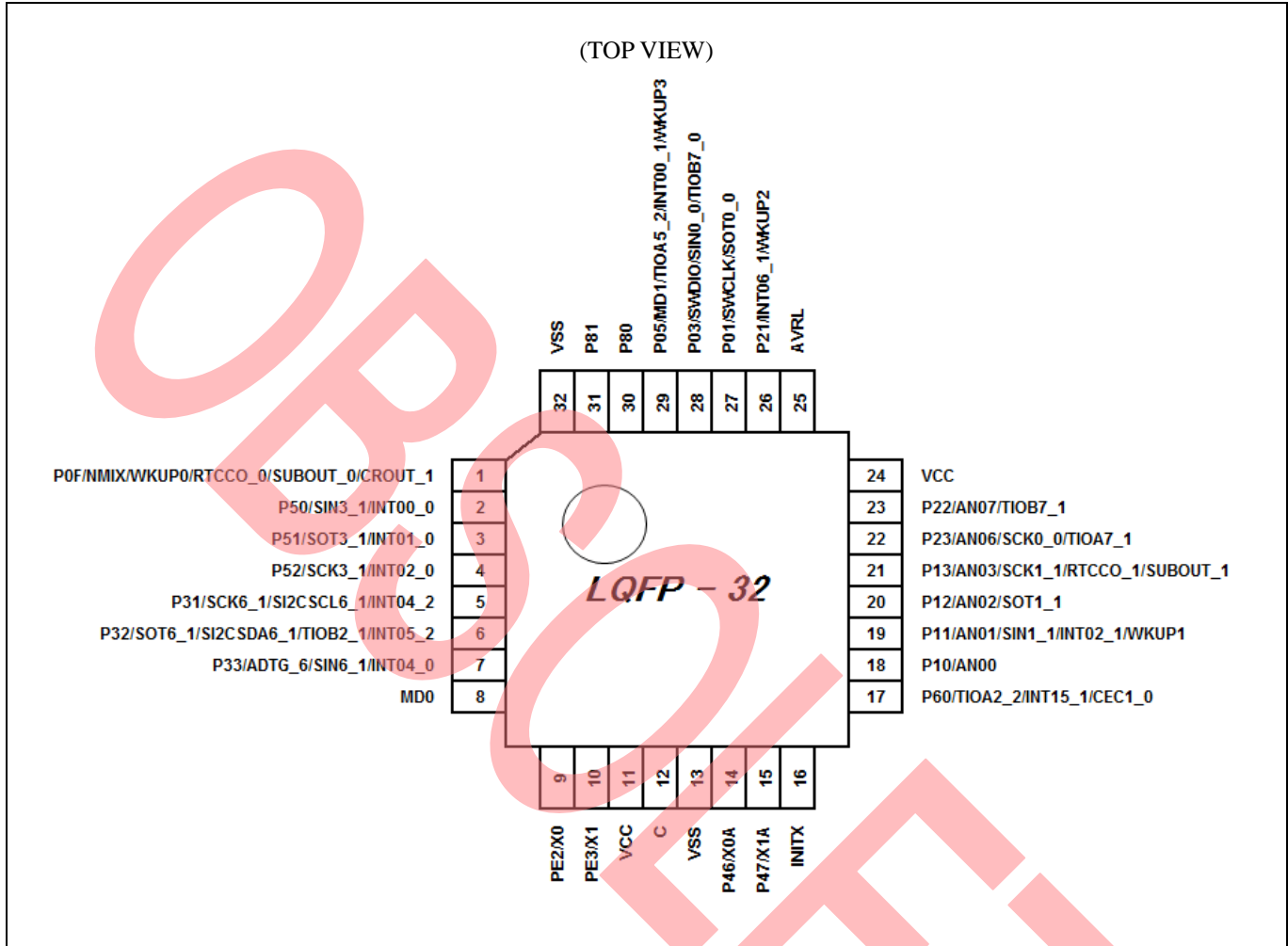
(TOP VIEW)



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

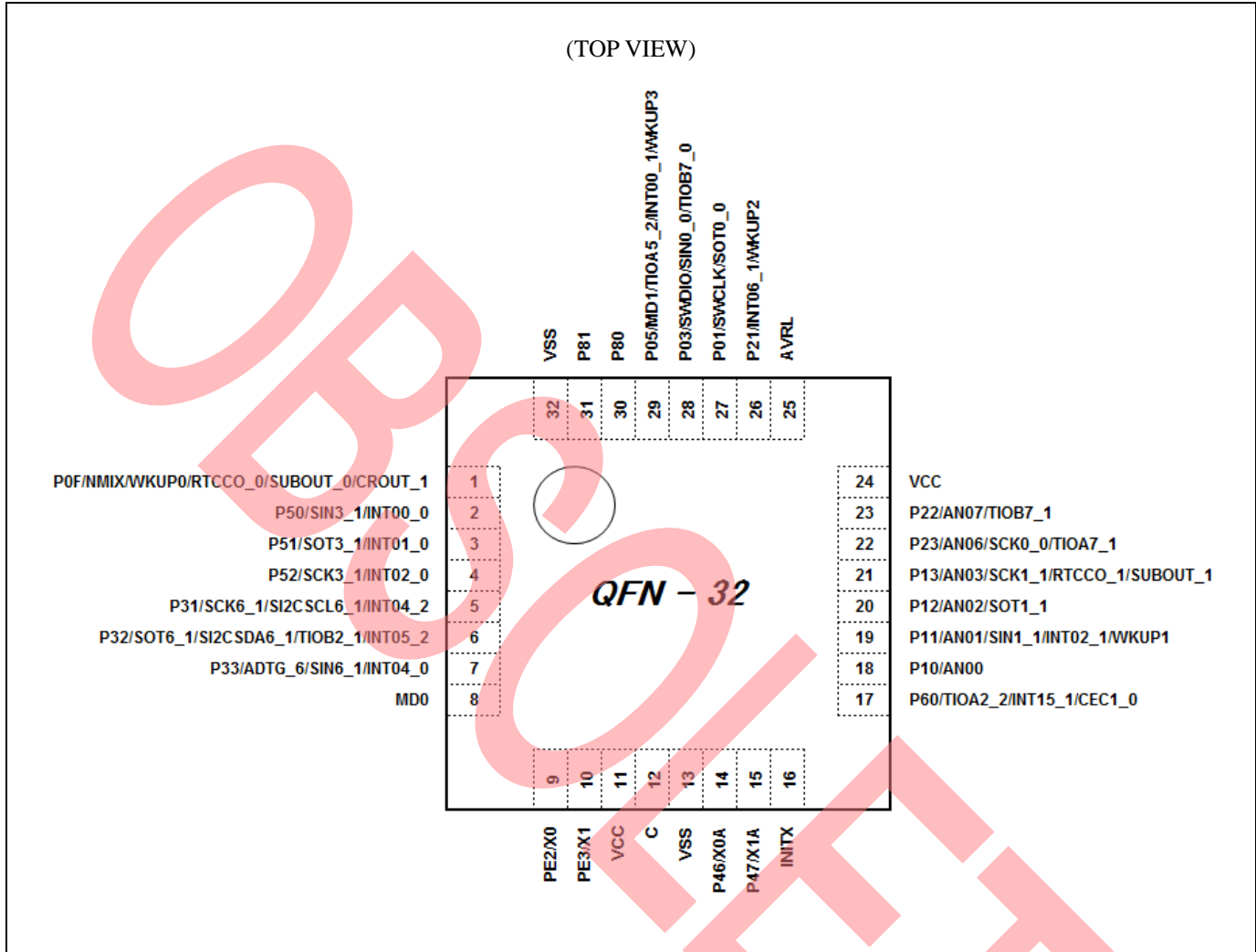
**LQB032**



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

WNU032



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the *Extended Port Function Register (EPFR)* to select the pin to be used.

## 4. List of Pin Functions

### List of Pin Numbers

The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	2	P50	D	K
			SIN3_1		
			INT00_0		
2	2	3	P51	D	K
			SOT3_1		
			INT01_0		
3	3	4	P52	D	K
			SCK3_1		
			INT02_0		
4	4	-	P53	D	K
			TIOA1_2		
			INT07_2		
5	5	-	P30	D	K
			SCS60_1		
			TIOB0_1		
			INT03_2		
			MI2SWS6_1		
6	6	-	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
			MI2SCK6_1		
-	-	5	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
7	7	-	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		
			MI2SDO6_1		
-	-	6	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
8	8	-	P33	H	K
			ADTG_6		
			SIN6_1		
			INT04_0		
			MI2SDI6_1		
-	-	7	P33	H	K
			ADTG_6		
			SIN6_1		
			INT04_0		
9	-	-	P34	D	K
			SCS61_1		
			TIOB4_1		
			MI2SMCK6_1		
-	9	-	P34	D	K
			SCS61_1		
			MI2SMCK6_1		
10	-	-	P35	D	K
			SCS62_1		
			TIOB5_1		
			INT08_1		
11	-	-	P3A	D	K
			TIOA0_1		
			INT03_0		
			RTCCO_2		
			SUBOUT_2		
			IC1_CIN_0		
-	10	-	P3A	D	K
			TIOA0_1		
			INT03_0		
			RTCCO_2		
			SUBOUT_2		
12	-	-	P3B	D	K
			TIOA1_1		
			IC1_DATA_0		
-	11	-	P3B	D	K
			TIOA1_1		
13	-	-	P3C	D	K
			TIOA2_1		
			IC1_RST_0		
-	12	-	P3C	D	K
			TIOA2_1		
14	-	-	P3D	D	K
			TIOA3_1		
			IC1_VPEN_0		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
15	-	-	P3E	D	K
			TIOA4_1		
			IC1_VCC_0		
16	-	-	P3F	D	K
			TIOA5_1		
			IC1_CLK_0		
17	13	8	MD0	I	F
18	14	9	PE2	A	A
			X0		
19	15	10	PE3	A	B
			X1		
20	-	-	P40	D	K
			TIOA0_0		
			INT12_1		
21	-	-	P41	D	K
			TIOA1_0		
			INT13_1		
22	-	-	P42	D	K
			TIOA2_0		
23	-	-	P43	D	K
			ADTG_7		
			TIOA3_0		
24	-	-	P4C	D	K
			SCK7_1		
			TIOB3_0		
-	16	-	P4C	D	K
-	-	-	SCK7_1	D	K
25	17	-	P4D	D	K
			SOT7_1		
26	18	-	P4E	D	K
			SIN7_1		
			INT06_2		
27	19	11	VCC	-	-
28	20	12	C	-	-
29	21	13	VSS	-	-
30	22	14	P46	C	C
			X0A		
31	23	15	P47	C	D
			X1A		
32	24	16	INITX	B	E
33	25	17	P60	H	K
			TIOA2_2		
			INT15_1		
			CEC1_0		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
34	-	-	P1E	D	K
			RTS4_1		
			MI2SMCK4_1		
35	-	-	P1D	D	K
			CTS4_1		
			MI2SWS4_1		
36	-	-	P1C	D	K
			SCK4_1		
			MI2SCK4_1		
37	-	-	P1B	D	K
			SOT4_1		
			MI2SDO4_1		
-	26	-	P1B	D	K
			SOT4_1		
38	-	-	P1A	H	K
			SIN4_1		
			INT05_1		
			CEC0_0		
			MI2SDI4_1		
-	27	-	P1A	H	K
			SIN4_1		
			INT05_1		
			CEC0_0		
39	-	-	P1F	D	K
			ADTG_5		
40	28	18	P10	F	J
			AN00		
41	29	19	P11	G	J
			AN01		
			SIN1_1		
			INT02_1		
			WKUP1		
42	30	20	P12	F	J
			AN02		
			SOT1_1		
43	31	21	P13	F	J
			AN03		
			SCK1_1		
			RTCCO_1		
			SUBOUT_1		
44	32	-	P14	F	J
			AN04		
			SIN0_1		
			SCS10_1		
			INT03_1		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	33	-	P15	F	J
			AN05		
			SOT0_1		
			SCS11_1		
46	34	22	P23	F	J
			AN06		
			SCK0_0		
47	35	23	TIOA7_1	F	J
			P22		
			AN07		
48	36	24	TIOB7_1	-	-
			VCC		
49	37	-	AVRH *	-	-
50	38	25	AVRL	-	-
51	39	26	P21	E	K
			INT06_1		
			WKUP2		
52	-	-	P00	E	K
			WKUP4		
53	40	27	P01	D	K
			SWCLK		
			SOT0_0		
54	-	-	P02	E	K
			WKUP5		
55	41	28	P03	D	K
			SWDIO		
			SIN0_0		
			TIOB7_0		
56	42	29	P05	E	K
			MD1		
			TIOA5_2		
			INT00_1		
			WKUP3		
57	43	-	VCC	-	-
58	44	30	P80	J	G
59	45	31	P81	J	G
60	46	32	VSS	-	-
61	47	-	P61	H	K
			TIOB2_2		
62	-	-	P0B	E	K
			TIOB6_1		
			WKUP6		
63	-	-	P0C	E	K
			TIOA6_1		
			WKUP7		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
64	48	1	P0F	E	I
			NMIX		
			WKUP0		
			RTCCO_0		
			SUBOUT_0		
			CROUT_1		

\*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

## List of Pin Functions

The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
ADC	ADTG_5	A/D converter external trigger input pin	39	-	-
	ADTG_6		8	8	7
	ADTG_7		23	-	-
ADC	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	40	28	18
	AN01		41	29	19
	AN02		42	30	20
	AN03		43	31	21
	AN04		44	32	-
	AN05		45	33	-
	AN06		46	34	22
	AN07		47	35	23
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	20	-	-
	TIOA0_1		11	10	-
	TIOB0_1	Base timer ch.0 TIOB pin	5	5	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	21	-	-
	TIOA1_1		12	11	-
	TIOA1_2		4	4	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	22	-	-
	TIOA2_1		13	12	-
	TIOA2_2		33	25	17
	TIOB2_1	Base timer ch.2 TIOB pin	7	7	6
	TIOB2_2	61	47	-	
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	23	-	-
	TIOA3_1		14	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	24	-	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	15	-	-
	TIOB4_1	Base timer ch.4 TIOB pin	9	-	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	16	-	-
	TIOA5_2		56	42	29
	TIOB5_1	Base timer ch.5 TIOB pin	10	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	63	-	-
	TIOB6_1	Base timer ch.6 TIOB pin	62	-	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	34	22
	TIOB7_0	Base timer ch.7 TIOB pin	55	41	28
	TIOB7_1		47	35	23
Debugger	SWCLK	Serial wire debug interface clock input pin	53	40	27
	SWDIO	Serial wire debug interface data input / output pin	55	41	28

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
External Interrupt	INT00_0	External interrupt request 00 input pin	1	1	2
	INT00_1		56	42	29
	INT01_0	External interrupt request 01 input pin	2	2	3
	INT02_0	External interrupt request 02 input pin	3	3	4
	INT02_1		41	29	19
	INT03_0	External interrupt request 03 input pin	11	10	-
	INT03_1		44	32	-
	INT03_2		5	5	-
	INT04_0	External interrupt request 04 input pin	8	8	7
	INT04_2		6	6	5
	INT05_1	External interrupt request 05 input pin	38	27	-
	INT05_2		7	7	6
	INT06_1	External interrupt request 06 input pin	51	39	26
	INT06_2		26	18	-
	INT07_2	External interrupt request 07 input pin	4	4	-
	INT08_1	External interrupt request 08 input pin	10	-	-
	INT12_1	External interrupt request 12 input pin	20	-	-
	INT13_1	External interrupt request 13 input pin	21	-	-
	INT15_1	External interrupt request 15 input pin	33	25	17
NMIX	Non-Maskable Interrupt input pin	64	48	1	
GPIO	P00	General-purpose I/O port 0	52	-	-
	P01		53	40	27
	P02		54	-	-
	P03		55	41	28
	P05		56	42	29
	P0B		62	-	-
	P0C		63	-	-
	P0F		64	48	1
GPIO	P10	General-purpose I/O port 1	40	28	18
	P11		41	29	19
	P12		42	30	20
	P13		43	31	21
	P14		44	32	-
	P15		45	33	-
	P1A		38	27	-
	P1B		37	26	-
	P1C		36	-	-
	P1D		35	-	-
	P1E		34	-	-
	P1F		39	-	-
GPIO	P21	General-purpose I/O port 2	51	39	26
	P22		47	35	23
	P23		46	34	22

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P30	General-purpose I/O port 3	5	5	-
	P31		6	6	5
	P32		7	7	6
	P33		8	8	7
	P34		9	9	-
	P35		10	-	-
	P3A		11	10	-
	P3B		12	11	-
	P3C		13	12	-
	P3D		14	-	-
	P3E		15	-	-
	P3F		16	-	-
GPIO	P40	General-purpose I/O port 4	20	-	-
	P41		21	-	-
	P42		22	-	-
	P43		23	-	-
	P46		30	22	14
	P47		31	23	15
	P4C		24	16	-
	P4D		25	17	-
GPIO	P50	General-purpose I/O port 5	1	1	2
	P51		2	2	3
	P52		3	3	4
	P53		4	4	-
GPIO	P60	General-purpose I/O port 6	33	25	17
	P61		61	47	-
GPIO	P80	General-purpose I/O port 8	58	44	30
	P81		59	45	31
GPIO	PE2	General-purpose I/O port E	18	14	9
	PE3		19	15	10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	55	41	28
	SIN0_1		44	32	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I2C pin (operation mode 4).	53	40	27
	SOT0_1 (SDA0_1)		45	33	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I2C pin (operation mode 4).	46	34	22

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	41	29	19
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I2C pin (operation mode 4).	42	30	20
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I2C pin (operation mode 4).	43	31	21
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 input/output pin.	44	32	-
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	45	33	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	1	1	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I2C pin (operation mode 4).	2	2	3
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I2C pin (operation mode 4).	3	3	4

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I2C pin (operation mode 4).	37	26	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I2C pin (operation mode 4).	36	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-
Multi-function Serial 6	SIN6_1	Multi-function serial interface ch.6 input pin	8	8	7
	SOT6_1 (SDA6_1)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I2C pin (operation mode 4).	7	7	6
	SCK6_1 (SCL6_1)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I2C pin (operation mode 4).	6	6	5
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	5	5	-
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 output pin.	9	9	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 output pin.	10	-	-
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	26	18	-
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I2C pin (operation mode 4).	25	17	-
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I2C pin (operation mode 4).	24	16	-

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
I2S(MFS)	MI2SDI4_1	I2S Serial Data Input pin (operation mode 2).	38	-	-
	MI2SDO4_1	I2S Serial Data Output pin (operation mode 2).	37	-	-
	MI2SCK4_1	I2S Serial Clock Output pin (operation mode 2).	36	-	-
	MI2SWS4_1	I2S Word Select Output pin (operation mode 2).	35	-	-
	MI2SMCK4_1	I2S Master Clock Input/output pin (operation mode 2).	34	-	-
	MI2SDI6_1	I2S Serial Data Input pin (operation mode 2).	8	8	-
	MI2SDO6_1	I2S Serial Data Output pin (operation mode 2).	7	7	-
	MI2SCK6_1	I2S Serial Clock Output pin (operation mode 2).	6	6	-
	MI2SWS6_1	I2S Word Select Output pin (operation mode 2).	5	5	-
	MI2SMCK6_1	I2S Master Clock Input/output pin (operation mode 2).	9	9	-
Smart Card Interface	IC1_CIN_0	Smart Card insert detection output pin	11	-	-
	IC1_CLK_0	Smart Card serial interface clock output pin	16	-	-
	IC1_DATA_0	Smart Card serial interface data input pin	12	-	-
	IC1_RST_0	Smart Card reset output pin	13	-	-
	IC1_VCC_0	Smart Card power enable output pin	15	-	-
	IC1_VPEN_0	Smart Card programming output pin	14	-	-
Real-time Clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	64	48	1
	RTCCO_1		43	31	21
	RTCCO_2		11	10	-
	SUBOUT_0	Sub clock output pin	64	48	1
	SUBOUT_1		43	31	21
	SUBOUT_2		11	10	-
HDMI-CEC/Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	38	27	-
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	33	25	17

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Low Power Consumption Mode	WKUP0	Deep Standby mode return signal input pin 0	64	48	1
	WKUP1	Deep Standby mode return signal input pin 1	41	29	19
	WKUP2	Deep Standby mode return signal input pin 2	51	39	26
	WKUP3	Deep Standby mode return signal input pin 3	56	42	29
	WKUP4	Deep Standby mode return signal input pin 4	52	-	-
	WKUP5	Deep Standby mode return signal input pin 5	54	-	-
	WKUP6	Deep Standby mode return signal input pin 6	62	-	-
	WKUP7	Deep Standby mode return signal input pin 7	63	-	-
I2C Slave	SI2CSCL6_1	I2C Clock Pin	6	6	5
	SI2CSDA6_1	I2C Data Pin	7	7	6
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	32	24	16
MODE	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	17	13	8
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	42	29
CLOCK	X0	Main clock (oscillation) input pin	18	14	9
	X0A	Sub clock (oscillation) input pin	30	22	14
	X1	Main clock (oscillation) I/O pin	19	15	10
	X1A	Sub clock (oscillation) I/O pin	31	23	15
	CROUT_1	Built-in high-speed CR oscillation clock output port	64	48	1
POWER	VCC	Power supply pin	27	19	11
	VCC		48	36	24
	VCC		57	43	-
GND	VSS	GND pin	29	21	13
	VSS		60	46	32
Analog Reference	AVRH *	A/D converter analog reference voltage input pin	49	37	-
	AVRL	A/D converter analog reference voltage input pin	50	38	25
C pin	C	Power supply stabilization capacitance pin	28	20	12

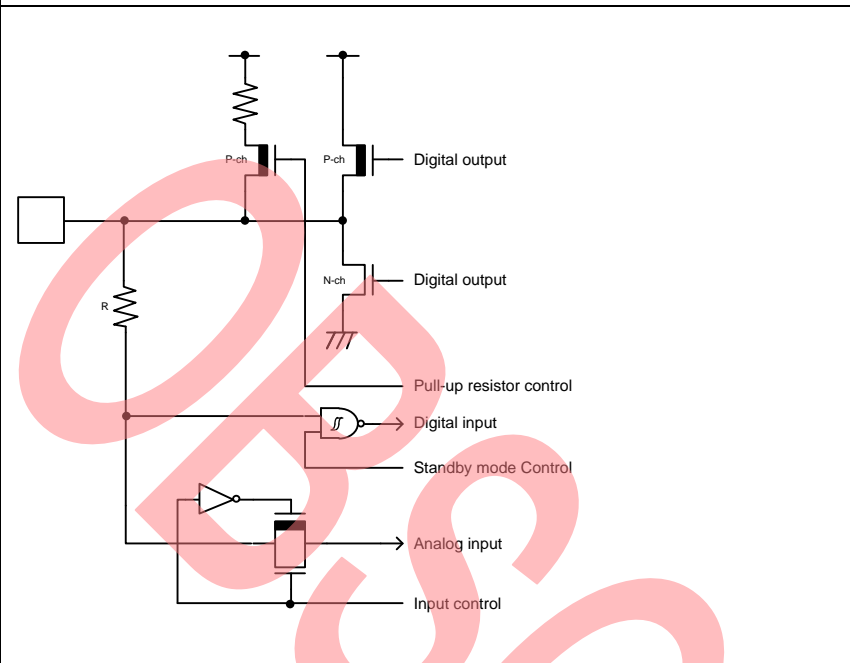
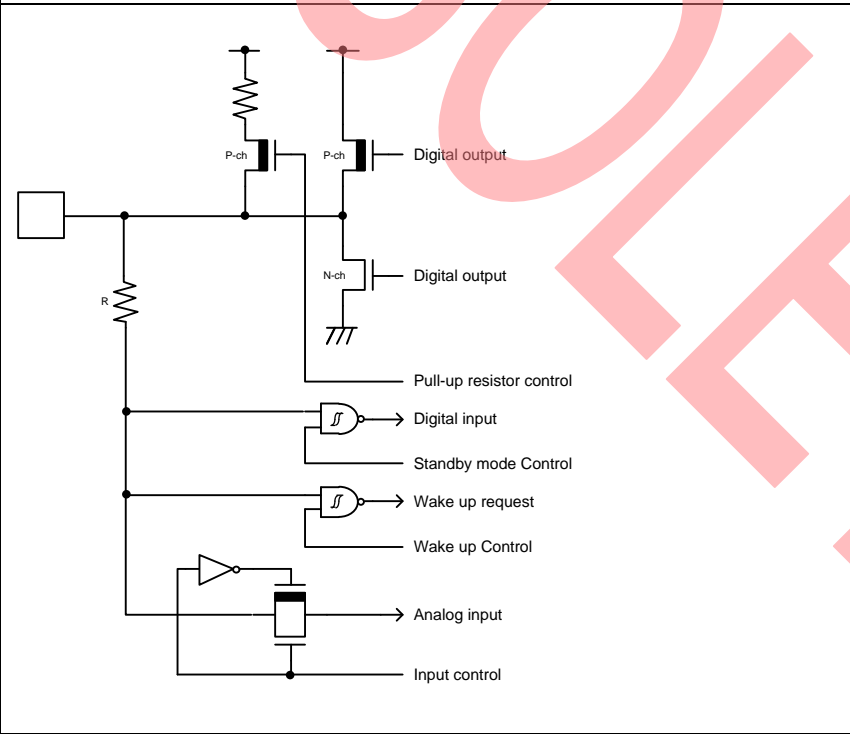
\*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

## 5. I/O Circuit Type

Type	Circuit	Remarks
A	<p>The diagram for Type A shows two I/O pins, X1 and X0. Pin X1 is connected to a pull-up resistor R and a P-channel MOSFET. Pin X0 is connected to a pull-up resistor R, a P-channel MOSFET, and an N-channel MOSFET. The diagram includes labels for Digital output, Digital input, Standby mode Control, Clock input, and Pull-up resistor control.</p>	<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately <math>1M\Omega</math></li> <li>• With standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately <math>33k\Omega</math></li> <li>• <math>I_{OH} = -4mA, I_{OL} = 4mA</math></li> </ul>
B	<p>The diagram for Type B shows a pull-up resistor connected to a digital input pin through a resistor and a hysteresis input.</p>	<p>CMOS level hysteresis input Pull-up resistor : Approximately <math>33k\Omega</math></p>

Type	Circuit	Remarks
C	<p>The diagram illustrates the internal circuitry for Type C. It features two oscillators, X1A and X0A, each connected to a pull-up resistor R. The X1A oscillator output is connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch), which serve as digital outputs. The X0A oscillator output is also connected to P-ch and N-ch MOSFETs for digital outputs. The circuit includes pull-up resistor control signals, digital inputs (with Schmitt triggers), and standby mode control signals. Logic gates (AND and OR) are used to manage the control signals. The diagram also shows a clock input and a pull-up resistor control signal for the X0A section.</p>	<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately 5MΩ</li> <li>• With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33kΩ</li> </ul> <p><math>I_{OH} = -4\text{mA}</math>, <math>I_{OL} = 4\text{mA}</math></p>

Type	Circuit	Remarks
D	<p>The diagram for Type D shows a CMOS output stage. A pull-up resistor R is connected to the output node. The output node is driven by a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch transistor's gate is connected to a pull-up resistor control signal. The N-ch transistor's gate is connected to a digital input signal. A standby mode control signal is connected to the gates of both transistors. The output node is also connected to a digital output terminal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33kΩ</li> <li>• IOH= -4mA, IOL= 4mA</li> <li>• When this pin is used as an I2C pin, the digital output P-ch transistor is always off</li> </ul>
E	<p>The diagram for Type E shows a CMOS output stage similar to Type D. It includes a pull-up resistor R, P-ch and N-ch transistors, and a digital input signal. In addition to the standby mode control signal, it includes a wake up request signal and a wake up control signal, both connected to the gates of the P-ch and N-ch transistors. The output node is connected to a digital output terminal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33kΩ</li> <li>• IOH= -4mA, IOL= 4mA</li> <li>• When this pin is used as an I2C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
F	 <p>The diagram for Type F shows a pin connected to a pull-up resistor R. The pin is connected to the gates of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to VDD and its drain to the pin. The N-ch MOSFET's source is connected to GND and its drain to the pin. A pull-up resistor R is connected between VDD and the pin. The pin is also connected to a digital input through an AND gate, a standby mode control through an AND gate, and an analog input through a buffer and a switch controlled by an input control signal. The digital output is taken from the pin, and the P-ch transistor is always off when used as an I2C pin.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33k<math>\Omega</math></li> <li>• IOH= -4mA, IOL= 4mA</li> <li>• When this pin is used as an I2C pin, the digital output P-ch transistor is always off</li> </ul>
G	 <p>The diagram for Type G shows a pin connected to a pull-up resistor R. The pin is connected to the gates of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to VDD and its drain to the pin. The N-ch MOSFET's source is connected to GND and its drain to the pin. A pull-up resistor R is connected between VDD and the pin. The pin is also connected to a digital input through an AND gate, a standby mode control through an AND gate, a wake up request through an AND gate, and a wake up control through an AND gate. The digital output is taken from the pin, and the P-ch transistor is always off when used as an I2C pin.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33k<math>\Omega</math></li> <li>• IOH= -4mA, IOL= 4mA</li> <li>• When this pin is used as an I2C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
H		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33kΩ</li> <li>• IOH= -4mA, IOL= 4mA</li> <li>• Available to control PZR registers</li> <li>• When this pin is used as an I2C pin, the digital output P-ch transistor is always off</li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby mode control</li> </ul>

## 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

##### (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

##### (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

##### (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

## Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

## Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

## Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

## Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

## Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

## Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

## Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.  
Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

## Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

## Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%.  
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

## 7. Handling Devices

### Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pin and GND pin, between AVRH pin and AVRL pin near this device.

### Stabilizing Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  when there is a momentary fluctuation on switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

#### ■ Surface mount type

Size: More than 3.2 mm  $\times$  1.5 mm

Load capacitance: Approximately 6 pF to 7 pF

#### ■ Lead type

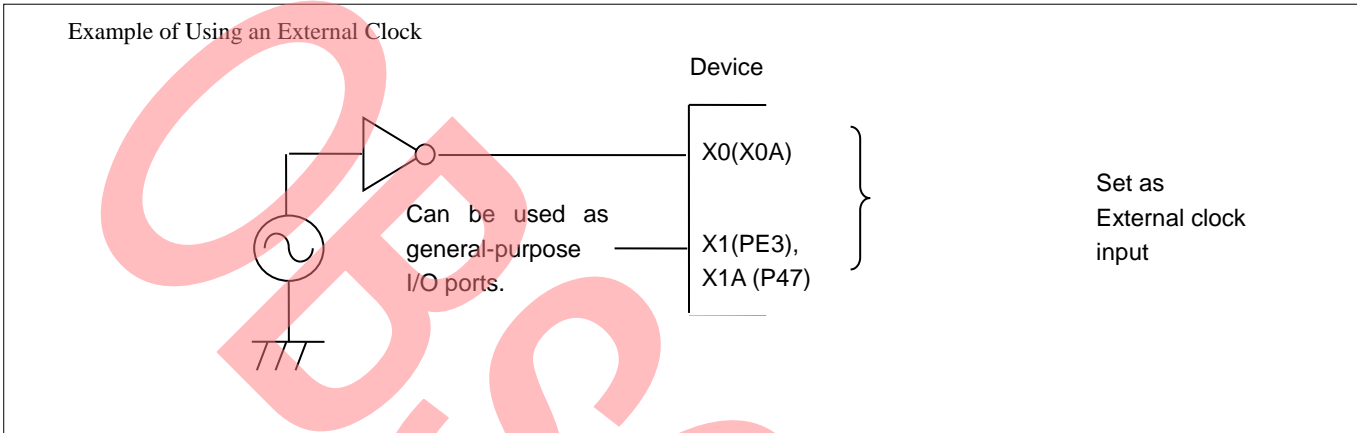
Load capacitance: Approximately 6 pF to 7 pF

## Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.

Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

However in the Deep Standby mode, an external clock as an input of the sub clock cannot be used.



## Handling when Using Multi-Function Serial Pin as I<sup>2</sup>C Pin

If it is using the multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disabled. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to the external I<sup>2</sup>C bus system with power OFF.

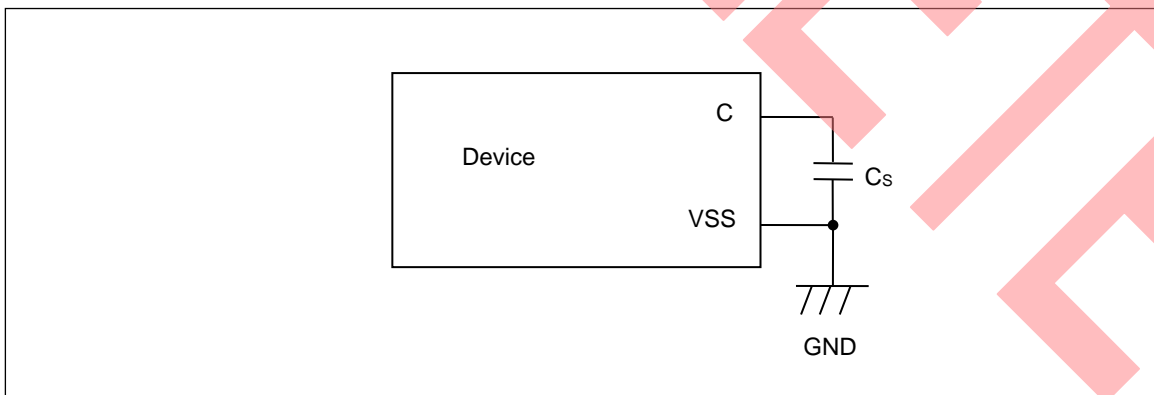
## C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C<sub>s</sub>) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.

However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7 μF would be recommended for this series.

Incidentally, the C pin becomes floating in Deep standby mode.



## Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

## Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VCC →AVRH

Turning off : AVRH →VCC

## Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.

If an error is detected, retransmit the data.

## Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

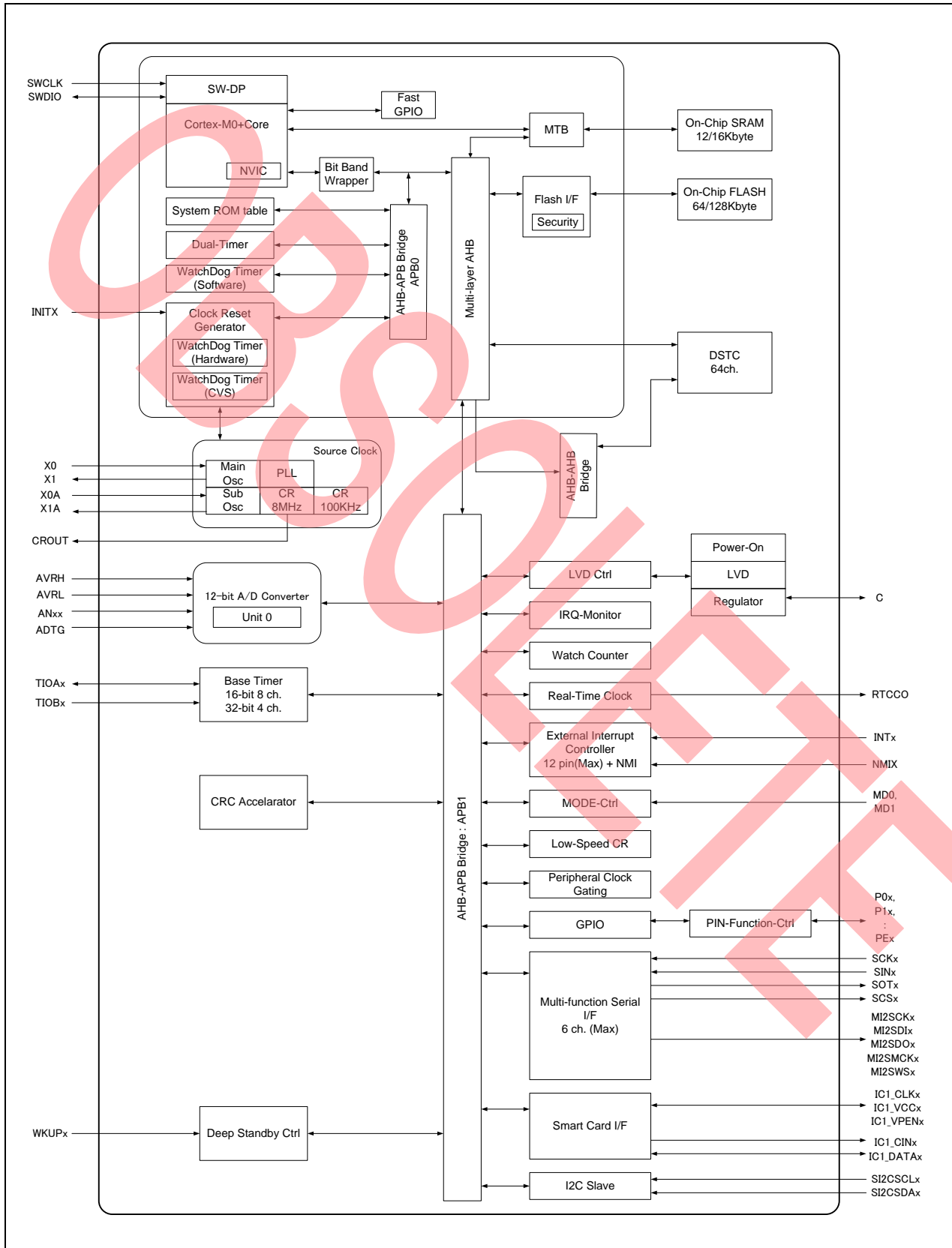
## Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

## Handling when Using Debug Pins

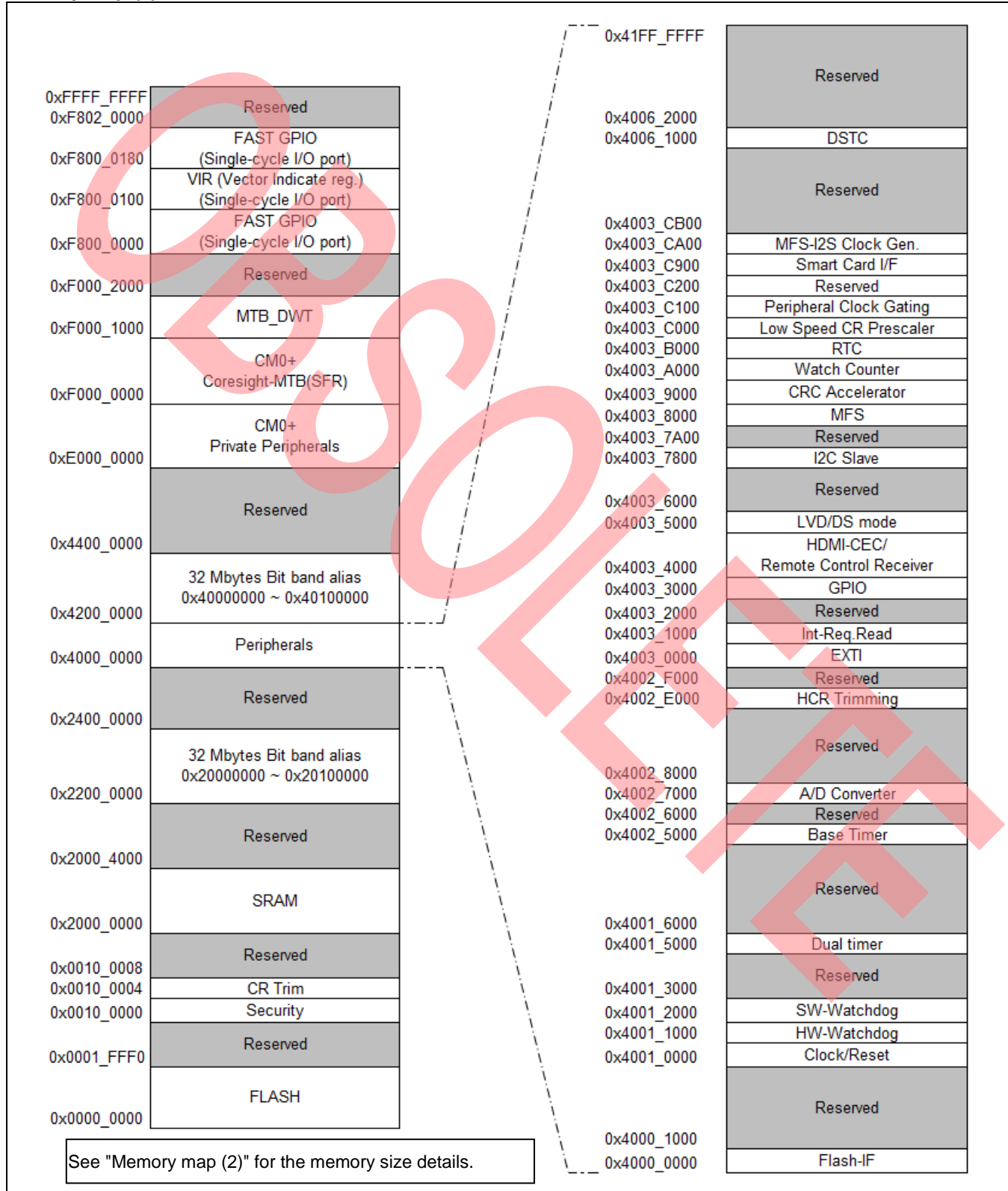
When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

## 8. Block Diagram

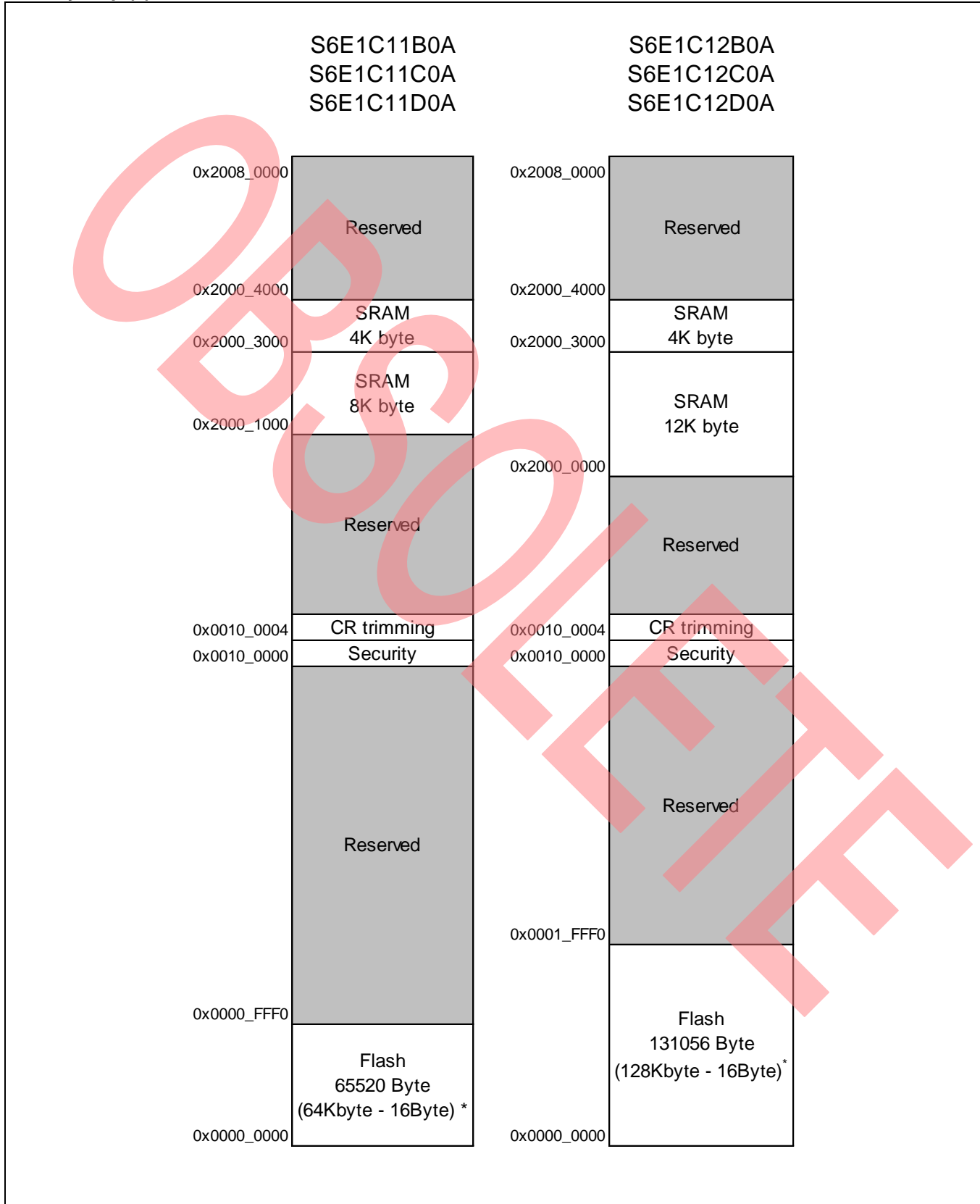


## 9. Memory Map

### Memory Map (1)



**Memory Map (2)**



\*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

## Peripheral Address Map

Start address	End address	Bus	Peripheral	
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register	
0x4000_1000	0x4000_FFFF		Reserved	
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control	
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer	
0x4001_2000	0x4001_2FFF		Software Watchdog Timer	
0x4001_3000	0x4001_4FFF		Reserved	
0x4001_5000	0x4001_5FFF		Dual-Timer	
0x4001_6000	0x4001_FFFF		Reserved	
0x4002_0000	0x4002_0FFF		Reserved	
0x4002_1000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	Reserved		
0x4002_5000	0x4002_5FFF	Base Timer		
0x4002_6000	0x4002_6FFF	Reserved		
0x4002_7000	0x4002_7FFF	A/D Converter		
0x4002_8000	0x4002_DFFF	Reserved		
0x4002_E000	0x4002_EFFF	Built-in CR trimming		
0x4002_F000	0x4002_FFFF	Reserved		
0x4003_0000	0x4003_0FFF	APB1	External Interrupt Controller	
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function	
0x4003_2000	0x4003_2FFF		Reserved	
0x4003_3000	0x4003_3FFF		GPIO	
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote Control Receiver	
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration	
0x4003_6000	0x4003_6FFF		Reserved	
0x4003_7000	0x4003_77FF		Reserved	
0x4003_7800	0x4003_79FF		I2C Slave	
0x4003_7A00	0x4003_7FFF		Reserved	
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface	
0x4003_9000	0x4003_9FFF		CRC	
0x4003_A000	0x4003_AFFF		Watch Counter	
0x4003_B000	0x4003_BFFF		Real-time clock	
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler	
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating	
0x4003_C800	0x4003_C8FF		Reserved	
0x4003_C900	0x4003_C9FF		Smart Card Interface	
0x4003_CA00	0x4003_CAFF		MFS-I2S Clock Generator	
0x4003_CB00	0x4003_FFFF		Reserved	
0x4004_0000	0x4004_FFFF		AHB	Reserved
0x4005_0000	0x4006_0FFF			Reserved
0x4006_1000	0x4006_1FFF			DSTC
0x4006_2000	0x41FF_FFFF			Reserved

## 10. Pin Status in Each CPU State

The following table shows pin status in each CPU state.

Type	Selected Pin function		CPU state							
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
A	Main oscillation circuit selected *1	Main oscillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O selected *2	Main clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
B	Main oscillation circuit selected *1	Main oscillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O selected *2	GPIO selected	-	-	PC	HC	IS	GS	IS	GS
C	Sub oscillation circuit selected *1	Sub oscillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O selected *2	Sub clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
D	Sub oscillation circuit selected *1	Sub oscillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O selected *2	GPIO selected	-	-	PC	HC	IS	HS	IS	HS
E	Digital I/O selected	INITX input	This pin is digital input pin, pull up register is on, and digital input is not shut off in all CPU state..							
F	Digital I/O selected	MD0 input	This pin is digital input pin, pull up register is none, digital input is not shut off in all CPU state..							
G	Digital I/O selected *6	GPIO selected	IS	IE	CP	HC	IS	HS	IS	HS
H	Digital I/O selected	SW selected	IS	IP *5	PC	IP	IP	IP	IP	IP
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
I	Digital I/O selected	NMI selected	-	-	IP	IP	IP	-	-	-
		WKUP0 enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		GPIO selected	IS	IE	PC	HC	IS	-	-	-
J	Analog input selected *3	Analog input selected	Analog input is enable in all CPU state							
	Digital I/O selected *4	WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		External interrupt enable and input selected	-	-	IP	IP	IP	GS	IS	GS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS
K	Digital I/O selected	CEC pin selected	-	-	CP	CP	CP	CP	CP	CP
		WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		I2CSLAVE enable selected	-	-	PC	HC	IP	GS	IS	GS
		External interrupt enable and input selected	-	-	PC	HC	IP	GS	IS	GS
		GPIO selected	IS	IE	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS

Each term in above table have the following meanings.

## Type

This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

## Selected Pin function

This indicates a pin function that is selected by user program.

## CPU state

This indicates a state of the CPU that is shown below.

- (1) Reset state.  
CPU is initialized by Power-on reset or a reset due to low Power voltage supply.
- (2) Reset state.  
CPU is initialized by INITX input signal or system initialization after power on reset.
- (3) Run mode or SLEEP mode state.  
Timer mode, RTC mode or STOP mode state.
- (4) The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "0".  
Timer mode, RTC mode or STOP mode state.
- (5) The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "1".  
Deep standby STOP mode or Deep standby RTC mode state,
- (6) The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "0"  
Deep standby STOP mode or Deep standby RTC mode state,
- (7) The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "1"  
Run mode state after returning from Deep Standby mode.
- (8) (I/O state hold function(CONTX) is fixed at 1)

## Each pin status

The meaning of the symbols in the pin status table is as follows.

- IS Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
- IE Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
- IP Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
- IE/IS Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
- OE The OSC is in operation state. However, it may be stopped in some operation mode of the CPU.  
For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
- OS The OSC is in stop state. (Hi-Z)
- PC Digital output and pull up register is controlled by the register in the GPIO or peripheral function.  
Digital input is not shut off
- CP Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off.  
Digital input is not shut off.
- HC Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
- HS Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
- GS Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

**Additional note**

Additional note is described below.

- \*1 In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.
- \*2 In this type, when Digital I/O function is selected, internal oscillation function is disabled.
- \*3 In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.
- \*4 In this type, when Digital I/O function is selected, analog input function is not available.
- \*5 In this case, PCR register is initialized to "1". Pull up register is on.
- \*6 This pin does not have pull up register.

## 11. Electrical Characteristics

### 11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 4.6	V	
Analog reference voltage*1, *3	AVRH	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 4.6	V	
Input voltage*1	V <sub>I</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 4.6 V)	V	
		V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	5 V tolerant
Analog pin input voltage*1	V <sub>IA</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 4.6 V)	V	
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 4.6 V)	V	
L level maximum output current*4	I <sub>OL</sub>	-	10	mA	4 mA type
L level average output current*5	I <sub>OLAV</sub>	-	4	mA	4 mA type
L level total maximum output current	∑I <sub>OL</sub>	-	100	mA	
L level total average output current*6	∑I <sub>OLAV</sub>	-	50	mA	
H level maximum output current*4	I <sub>OH</sub>	-	- 10	mA	4 mA type
H level average output current*5	I <sub>OHAV</sub>	-	- 4	mA	4 mA type
H level total maximum output current	∑I <sub>OH</sub>	-	- 100	mA	
H level total average output current*6	∑I <sub>OHAV</sub>	-	- 50	mA	
Power consumption	P <sub>D</sub>	-	200	mW	
Storage temperature	T <sub>STG</sub>	- 55	+ 150	°C	

\*1: These parameters are based on the condition that V<sub>SS</sub> = 0 V.

\*2: V<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5 V.

\*3: Ensure that the voltage does not exceed V<sub>CC</sub> + 0.5 V at power-on.

\*4: The maximum output current is the peak value for a single pin.

\*5: The average output is the average current for a single pin over a period of 100 ms.

\*6: The total average output current is the average current for all pins over a period of 100 ms.

#### <WARNING>

- Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 11.2 Recommended Operating Conditions

(V<sub>SS</sub>= 0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V <sub>CC</sub>	-	1.65 *2	3.6	V	
Analog reference voltage	AVRH	-	2.7	V <sub>CC</sub>	V	V <sub>CC</sub> ≥ 2.7 V
			V <sub>CC</sub>	V <sub>CC</sub>	V	V <sub>CC</sub> < 2.7 V
	AVRL	-	V <sub>SS</sub>	V <sub>SS</sub>	V	
Smoothing capacitor	C <sub>S</sub>	-	1	10	μF	For regulator*1
Operating temperature	T <sub>a</sub>	-	- 40	+ 105	°C	

\*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

\*2: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

### <WARNING>

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 11.3 DC Characteristics

### 11.3.1 Current Rating

Symbol (Pin Name)	Conditions	HCLK Frequency <sup>4</sup>	Value		Unit	Remarks	
			Typ <sup>1</sup>	Max <sup>2</sup>			
I <sub>CC</sub> (VCC)	Run mode, code executed from Flash	8 MHz external clock input, PLL ON <sup>8</sup> NOP code executed	8 MHZ	1.4	2.7	mA	*3
		Built-in high speed CR stopped All peripheral clock stopped by CKENx	20 MHZ	2.6	4.1		
		40 MHZ	3.9	5.6			
	Run mode, code executed from Flash	8 MHz external clock input, PLL ON <sup>8</sup> Benchmark code executed	8 MHZ	1.3	2.6	mA	*3
		Built-in high speed CR stopped PCLK1 stopped	20 MHZ	2.3	3.8		
		40 MHZ	3.4	5.1			
	Run mode, code executed from RAM	8 MHz crystal oscillation, PLL ON <sup>8</sup> NOP code executed	8 MHZ	1.6	3.0	mA	*3, *9
		Built-in high speed CR stopped All peripheral clock stopped by CKENx	20 MHZ	2.8	4.4		
		40 MHZ	4.1	5.9			
	Run mode, code executed from RAM	8 MHz external clock input, PLL ON <sup>8</sup> NOP code executed	8 MHZ	1.0	2.1	mA	*3
		Built-in high speed CR stopped All peripheral clock stopped by CKENx	20 MHZ	1.7	2.9		
		40 MHZ	2.7	4.0			
Run mode, code executed from Flash	8 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHZ	1.6	3.1	mA	*3,*6,*7	
Run mode, code executed from Flash	Built-in high speed CR <sup>5</sup> NOP code executed	8 MHZ	1.1	2.4	mA	*3	
	All peripheral clock stopped by CKENx	32 kHz	240	1264			
	32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	100 kHz	246	1271			
I <sub>CCS</sub> (VCC)	Sleep operation	8 MHz external clock input, PLL ON <sup>8</sup> All peripheral clock stopped by CKENx	8 MHZ	0.8	1.9	mA	*3
		Built-in high speed CR <sup>5</sup> All peripheral clock stopped by CKENx	8 MHZ	0.6	1.7		
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	237	1261		
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	238	1262	μA	*3

\*1 : T<sub>A</sub>=+25°C, V<sub>CC</sub>=3.3 V

\*2 : T<sub>A</sub>=+105°C, V<sub>CC</sub>=3.6 V

\*3 : All ports are fixed

\*4 : PCLK0 is set to divided rate 8

\*5 : The frequency is set to 8 MHz by trimming

\*6 : Flash sync down is set to FRWTR.RWT=111 and FSYNDN.SD=1111

\*7 : V<sub>CC</sub>=1.65 V

\*8 : When HCLK=8 MHz, PLL OFF

\*9 : When IMAINSEL bit(MOSC\_CTL:IMAINSEL) is "10" (default).

Parameter	Symbol (Pin Name)	Conditions	Value		Unit	Remarks	
			Typ	Max			
Power supply current	I <sub>CCH</sub> (VCC)	Stop mode	Ta=25°C Vcc=3.3 V	12.4	52.4	μA	*1, *2
			Ta=25°C Vcc=1.65 V	12.0	52.0	μA	*1, *2
			Ta=105°C Vcc=3.6 V	-	597	μA	*1, *2
	I <sub>CC<sub>T</sub></sub> (VCC)	Sub timer mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	15.6	55.6	μA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	15.0	55.0	μA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	601	μA	*1, *2
	I <sub>CCR</sub> (VCC)	RTC mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	13.2	53.2	μA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	12.7	52.7	μA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	598	μA	*1, *2

\*1: All ports are fixed. LVD off. Flash off.

\*2: When CALDONE bit(CAL\_CTL:CALDONE) is "1". In case of "0", Bipolar Vref current is added.

Parameter	Symbol (Pin Name)	Conditions	Value		Unit	Remarks		
			Typ	Max				
Power supply current	I <sub>CCHD</sub> (VCC)	Deep standby Stop mode	RAM off	Ta=25°C Vcc=3.3 V	0.58	1.85	μA	*1, *2
				Ta=25°C Vcc=1.65 V	0.56	1.83	μA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	μA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	0.78	6.6	μA	*1, *2
				Ta=25°C Vcc=1.65 V	0.76	6.6	μA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	μA	*1, *2
	I <sub>CCRD</sub> (VCC)	Deep standby RTC mode	RAM off	Ta=25°C Vcc=3.3 V	1.16	2.4	μA	*1, *2
				Ta=25°C Vcc=1.65 V	1.15	2.4	μA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	μA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	1.37	7.2	μA	*1, *2
				Ta=25°C Vcc=1.65 V	1.35	7.2	μA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	μA	*1, *2

\*1: All ports are fixed. LVD off.

\*2: When CALDONE bit(CAL\_CTL:CALDONE) is "1". In case of "0", Bipolar Vref current is added.

### LVD Current

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I <sub>CC</sub> LVD	VCC	At operation	0.15	0.3	μA	For occurrence of reset
				0.10	0.3	μA	For occurrence of interrupt

### Bipolar V<sub>ref</sub> Current

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Bipolar V <sub>ref</sub> Current	I <sub>CC</sub> BGR	VCC	At operation	100	200	μA	

### Flash Memory Current

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I <sub>CC</sub> FLASH	VCC	At Write/Erase	4.4	5.6	mA	

### A/D converter Current

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>CC</sub> AD	VCC	At operation	0.5	0.75	mA	
Reference power supply current (AVRH)	I <sub>CC</sub> AVRH	AVRH	At operation	0.69	1.3	mA	AVRH=3.6 V
			At stop	0.1	1.3	μA	

## Peripheral Current Dissipation

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Clock System	Peripheral	Conditions	Frequency (MHz)			Unit	Remarks
			8	20	40		
HCLK	GPIO	At all ports operation	0.05	0.12	0.23	mA	
	DSTC	At 2ch operation	0.02	0.06	0.10		
PCLK1	Base timer	At 4ch operation	0.02	0.05	0.10	mA	
	ADC	At 1 unit operation	0.04	0.10	0.21		
	Multi-function serial	At 1ch operation	0.01	0.03	0.06		
	MFS-I2S	At 1ch operation	0.02	0.05	0.08		
	Smart Card I/F	At 1ch operation	0.04	0.08	0.18		

### 11.3.2 Pin Characteristics

( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	$V_{IHS}$	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7\text{ V}$	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
			$V_{CC} < 2.7\text{ V}$	$V_{CC} \times 0.7$				
		5 V tolerant input pin	$V_{CC} \geq 2.7\text{ V}$	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
			$V_{CC} < 2.7\text{ V}$	$V_{CC} \times 0.7$				
L level input voltage (hysteresis input)	$V_{ILS}$	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7\text{ V}$	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7\text{ V}$			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7\text{ V}$	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7\text{ V}$		-	$V_{CC} \times 0.3$		
H level output voltage	$V_{OH}$	4 mA type	$V_{CC} \geq 2.7\text{ V}$ , $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 2.7\text{ V}$ , $I_{OH} = -2\text{ mA}$	$V_{CC} - 0.45$				
L level output voltage	$V_{OL}$	4 mA type	$V_{CC} \geq 2.7\text{ V}$ , $I_{OL} = 4\text{ mA}$	$V_{SS}$	-	0.4	V	
			$V_{CC} < 2.7\text{ V}$ , $I_{OL} = 2\text{ mA}$					
Input leak current	$I_{IL}$	-	-	-5	-	+5	$\mu\text{A}$	
Pull-up resistance value	$R_{PU}$	Pull-up pin	$V_{CC} \geq 2.7\text{ V}$	21	33	48	k $\Omega$	
			$V_{CC} < 2.7\text{ V}$	-	-	88		
Input capacitance	$C_{IN}$	Other than VCC, VSS, AVRH	-	-	5	15	pF	

## 11.4 AC Characteristics

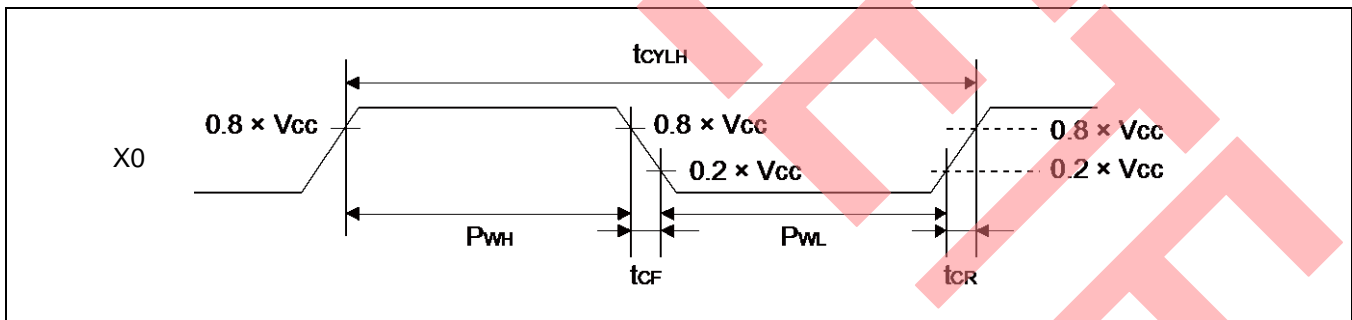
### 11.4.1 Main Clock Input Characteristics

( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$F_{CH}$	X0, X1	$V_{CC} \geq 2.7\text{V}$	8	48	MHz	When the crystal oscillator is connected
			$V_{CC} < 2.7\text{V}$	8	20		
Input clock cycle	$t_{CYLH}$	X0, X1	-	20.83	125	ns	When the external clock is used
Input clock pulse width	-	-	$P_{WH}/t_{CYLH}$ , $P_{WL}/t_{CYLH}$	45	55	%	When the external clock is used
Input clock rising time and falling time	$t_{CF}$ , $t_{CR}$	-	-	-	5	ns	When the external clock is used
Internal operating clock <sup>*1</sup> frequency	$F_{CM}$	-	-	-	40.8	MHz	Master clock
	$F_{CC}$	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	$F_{CP0}$	-	-	-	40.8	MHz	APB0 bus clock <sup>*2</sup>
	$F_{CP1}$	-	-	-	40.8	MHz	APB1 bus clock <sup>*2</sup>
Internal operating clock <sup>*1</sup> cycle time	$t_{CYCCM}$	-	-	24.5	-	ns	Master clock
	$t_{CYCC}$	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	$t_{CYCP0}$	-	-	24.5	-	ns	APB0 bus clock <sup>*2</sup>
	$t_{CYCP1}$	-	-	24.5	-	ns	APB1 bus clock <sup>*2</sup>

\*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

\*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".

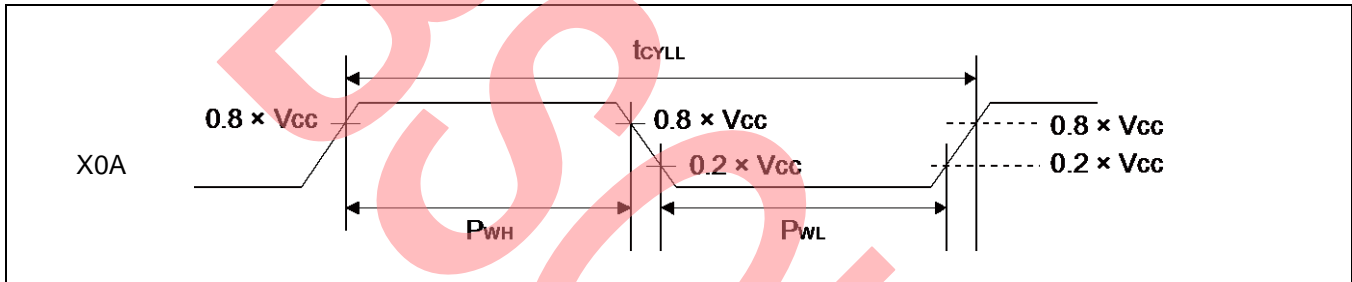


### 11.4.2 Sub Clock Input Characteristics

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$f_{CL}$	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	$t_{CYLL}$		-	10	-	31.25	$\mu$ s	When the external clock is used
Input clock pulse width	-		$P_{WH}/t_{CYLL}$ , $P_{WL}/t_{CYLL}$	45	-	55	%	When the external clock is used

\*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



### 11.4.3 Built-in CR Oscillation Characteristics

#### Built-in High-Speed CR

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub> = 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F <sub>CRH</sub>	Ta = - 10°C to + 105°C,	7.92	8	8.08	MHz	After trimming *1
		Ta = - 40°C to + 105°C,	7.84	8	8.16	MHz	
Frequency stabilization time	t <sub>CRWT</sub>	-	-	-	300	μs	*2

\*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

\*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

#### Built-in Low-Speed CR

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f <sub>CRL</sub>	-	50	100	150	kHz	

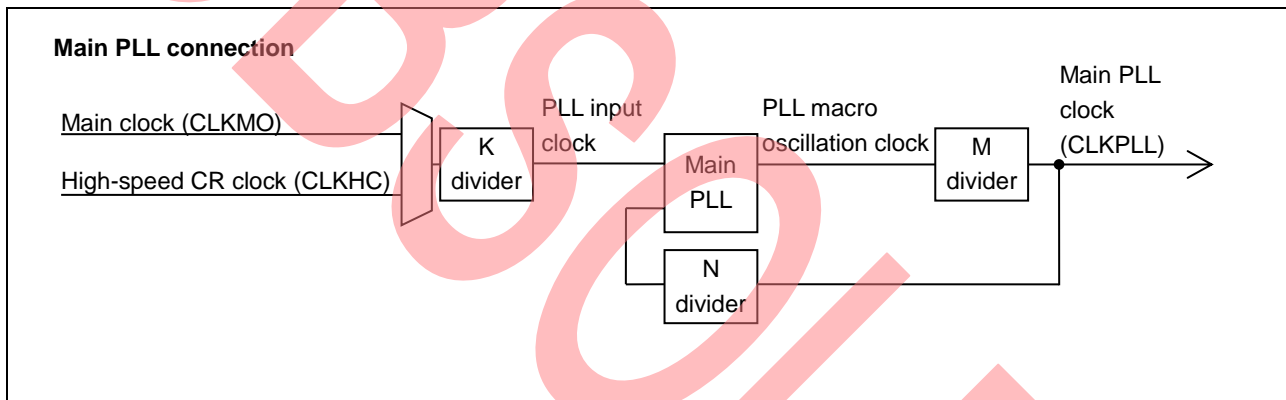
**11.4.4 Operating Conditions of Main PLL**  
**(In the Case of Using the Main Clock as the Input Clock of the PLL)**

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	$t_{LOCK}$	50	-	-	$\mu$ s	
PLL input clock frequency	$F_{PLLI}$	8	-	16	MHz	
PLL multiple rate	-	5	-	18	multiple	
PLL macro oscillation clock frequency	$F_{PLLO}$	75	-	150	MHz	
Main PLL clock frequency*2	$F_{CLKPLL}$	-	-	40	MHz	

\*1: The wait time is the time it takes for PLL oscillation to stabilize.

\*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".



**11.4.5 Operating Conditions of Main PLL**  
**(In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)**

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	$t_{LOCK}$	50	-	-	$\mu$ s	
PLL input clock frequency	$F_{PLLI}$	7.84	8	8.16	MHz	
PLL multiple rate	-	9	-	18	multiple	
PLL macro oscillation clock frequency	$F_{PLLO}$	75	-	150	MHz	
Main PLL clock frequency*2	$F_{CLKPLL}$	-	-	40.8	MHz	

\*1: The wait time is the time it takes for PLL oscillation to stabilize.

\*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

**Note:**

- For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency and temperature have been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

### 11.4.6 Reset Input Characteristics

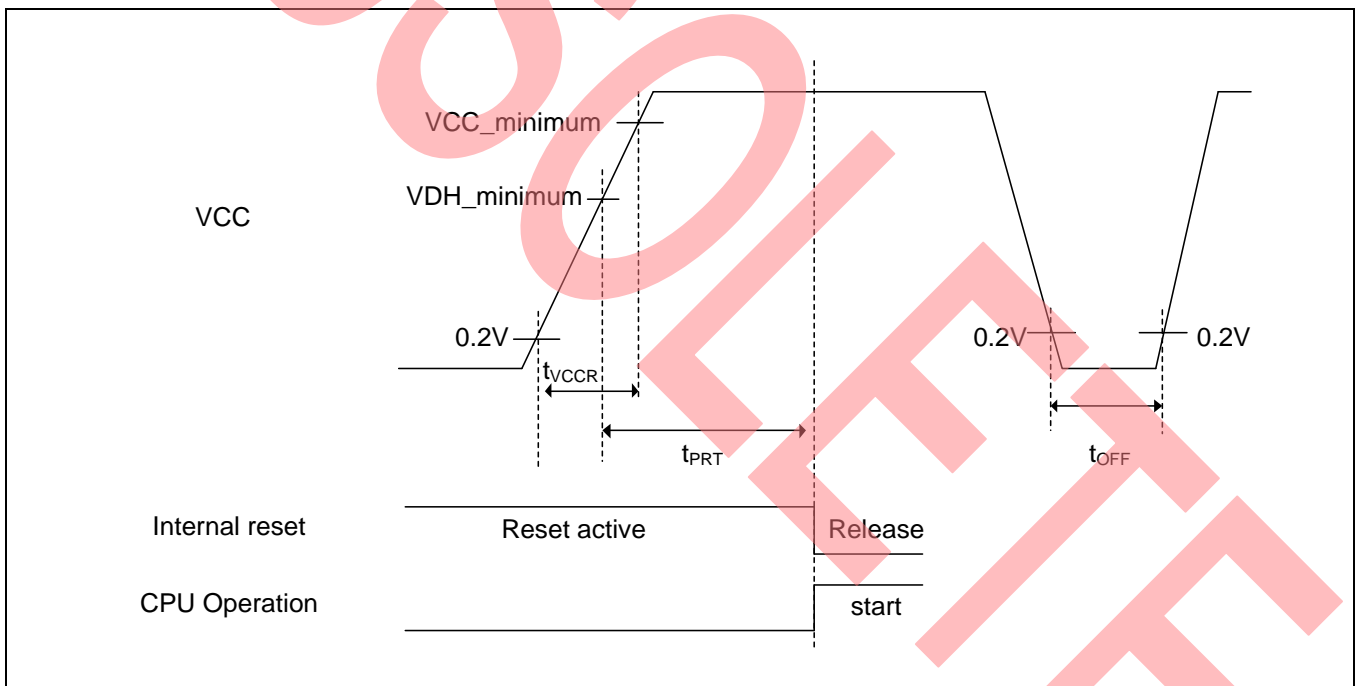
( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{INITX}$	INITX	-	500	-	ns	

### 11.4.7 Power-on Reset Timing

( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_{VCCR}$	VCC	0	-	ms	
Power supply shut down time	$t_{OFF}$		1	-	ms	$V_{CC} < 0.2\text{ V}$
Time until releasing Power-on reset	$t_{PRT}$		0.43	3.4	ms	



#### Glossary

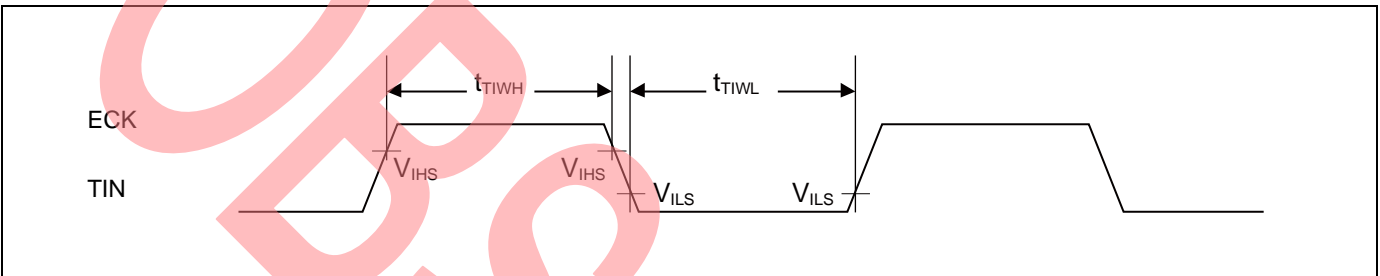
- $V_{CC\_minimum}$  : Minimum  $V_{CC}$  of recommended operating conditions.
  - $VDH\_minimum$  : Minimum detection voltage of Low-Voltage detection reset.
- See "11.6 Low-Voltage Detection Characteristics".

### 11.4.8 Base Timer Input Timing

#### Timer Input Timing

( $V_{CC}= 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}= 0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

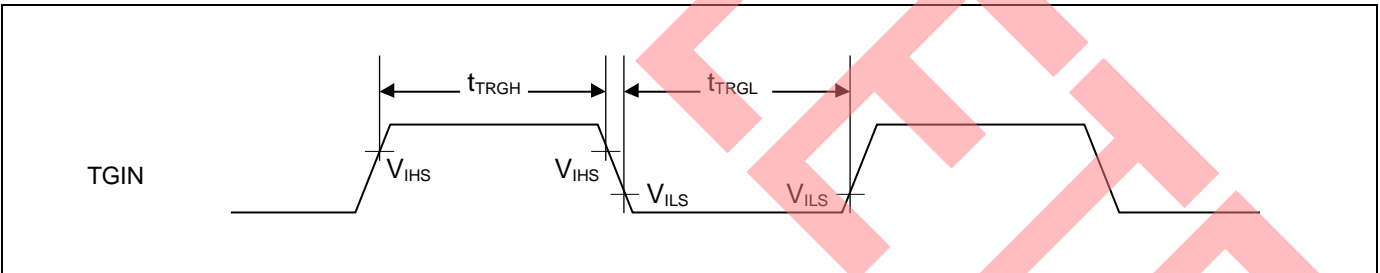
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2 t_{CYCP}$	-	ns	



#### Trigger Input Timing

( $V_{CC}= 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}= 0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2 t_{CYCP}$	-	ns	



#### Note:

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

### 11.4.9 CSIO/SPI/UART Timing

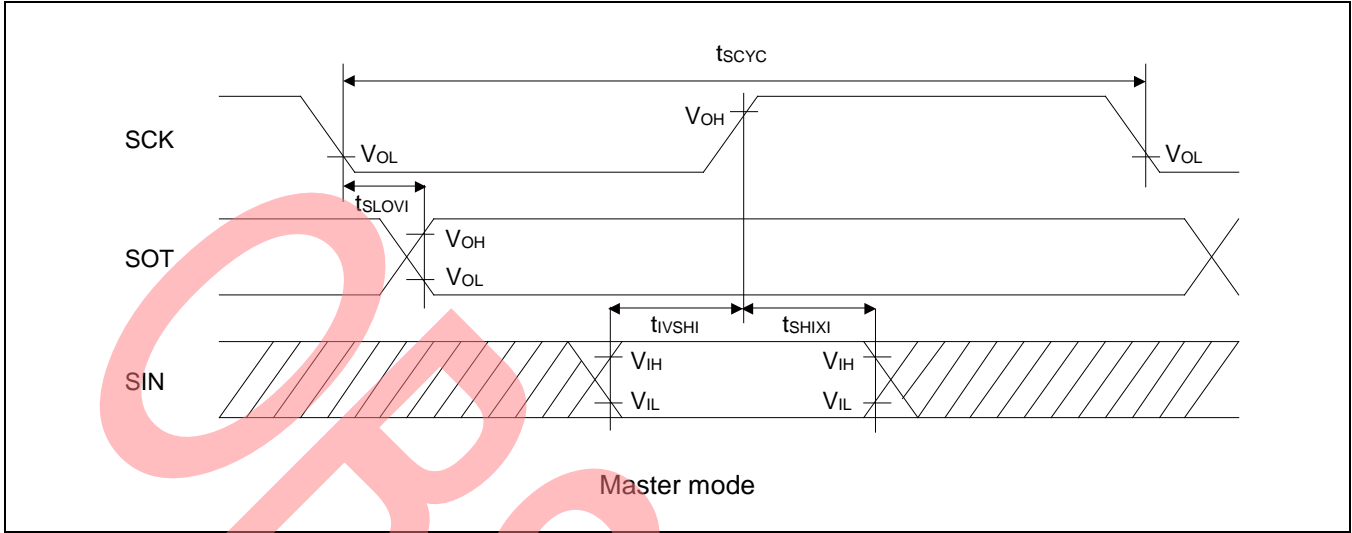
#### CSIO (SPI=0, SCINV=0)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

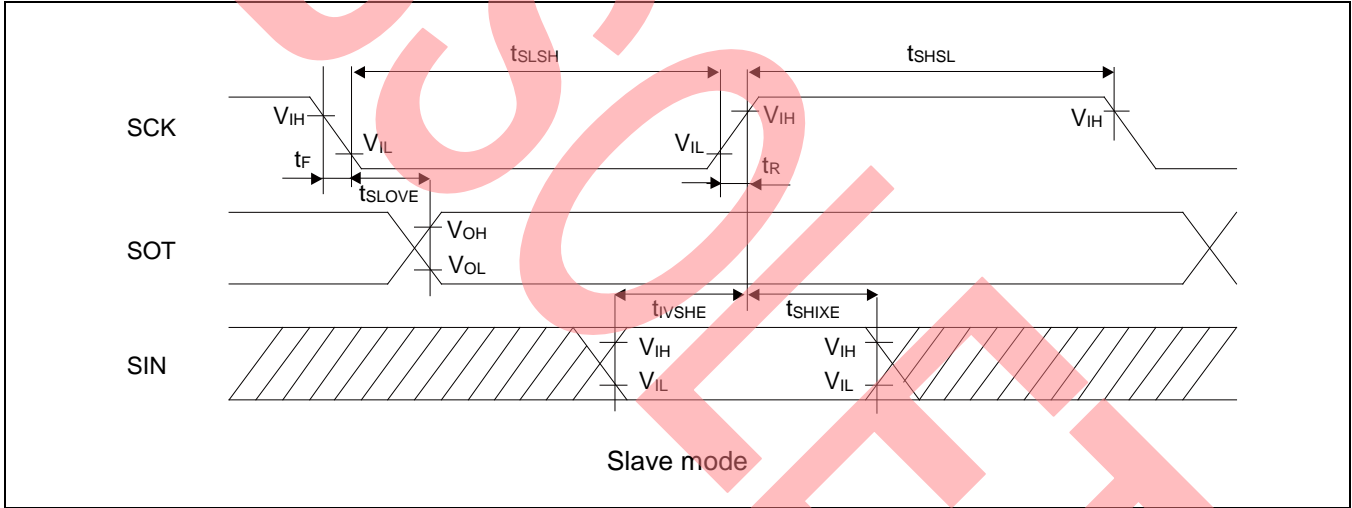
Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Master mode	4 t <sub>CYCP</sub>	-	4 t <sub>CYCP</sub>	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t <sub>IVSHI</sub>	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t <sub>LSH</sub>	SCKx	Slave mode	2 t <sub>CYCP</sub> - 10	-	2 t <sub>CYCP</sub> - 10	-	ns
Serial clock "H" pulse width	t <sub>HSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVE</sub>	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t <sub>IVSHE</sub>	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK falling time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rising time	t <sub>R</sub>	SCKx		-	5	-	5	ns

#### Notes:

- The above AC characteristics are for clock synchronous mode.
- t<sub>CYCP</sub> represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance C<sub>L</sub>=30 pF



Master mode



Slave mode

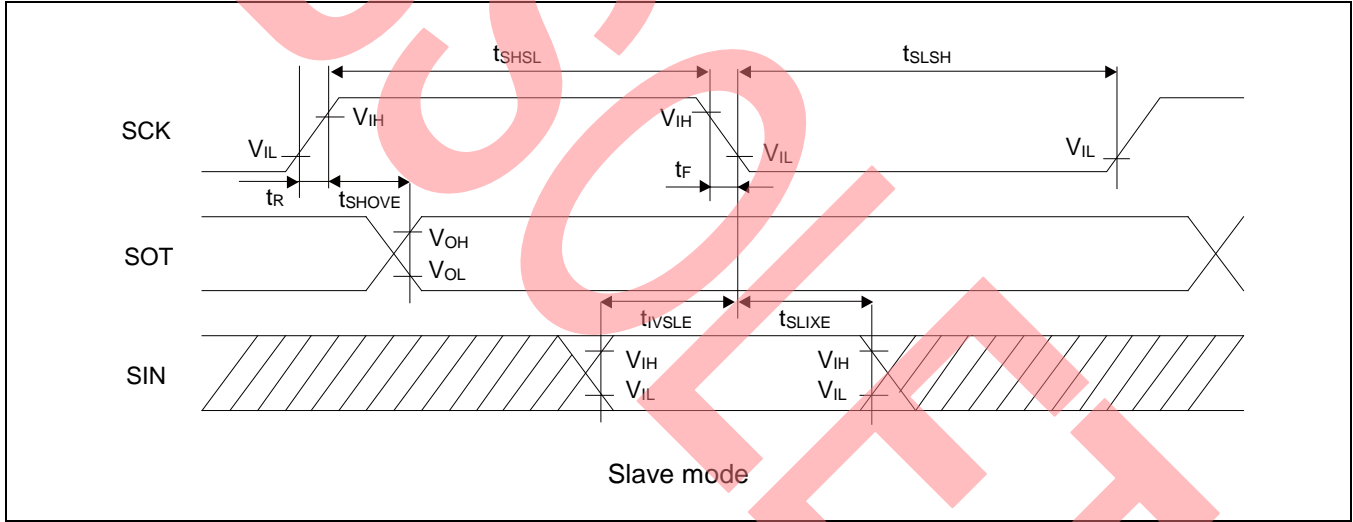
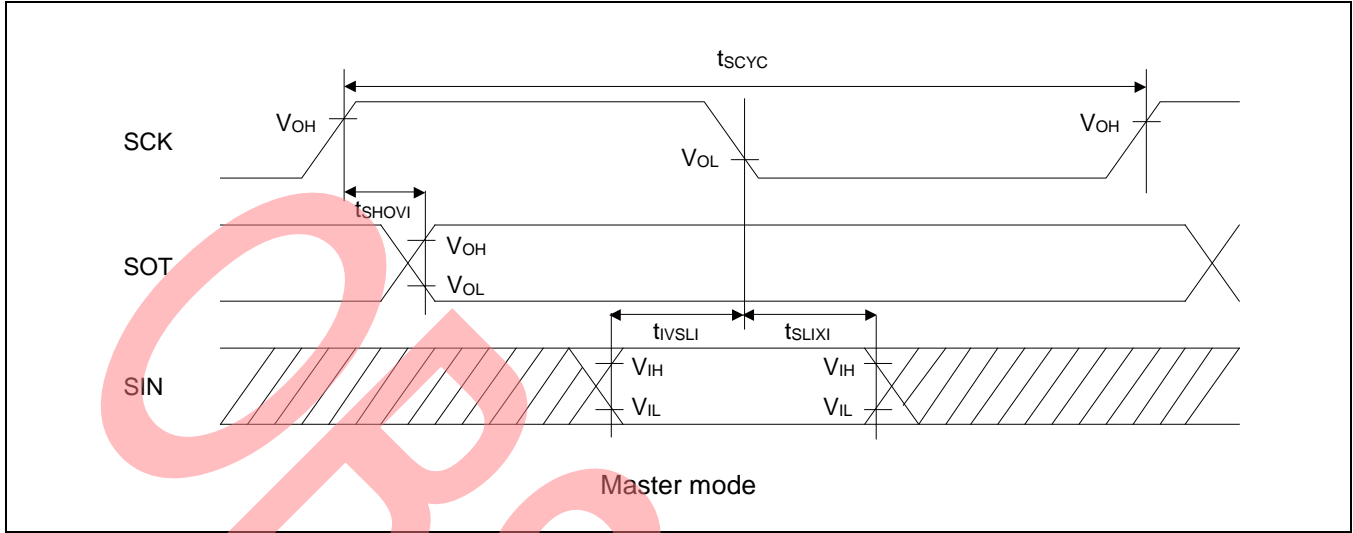
## CSIO (SPI=0, SCINV=1)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 2.7V		V <sub>CC</sub> ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Master mode	4 t <sub>CYCP</sub>	-	4 t <sub>CYCP</sub>	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	36	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCKx	Slave mode	2 t <sub>CYCP</sub> - 10	-	2 t <sub>CYCP</sub> - 10	-	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK falling time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rising time	t <sub>R</sub>	SCKx		-	5	-	5	ns

### Notes:

- The above AC characteristics are for clock synchronous mode.
- t<sub>CYCP</sub> represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance C<sub>L</sub>=30 pF



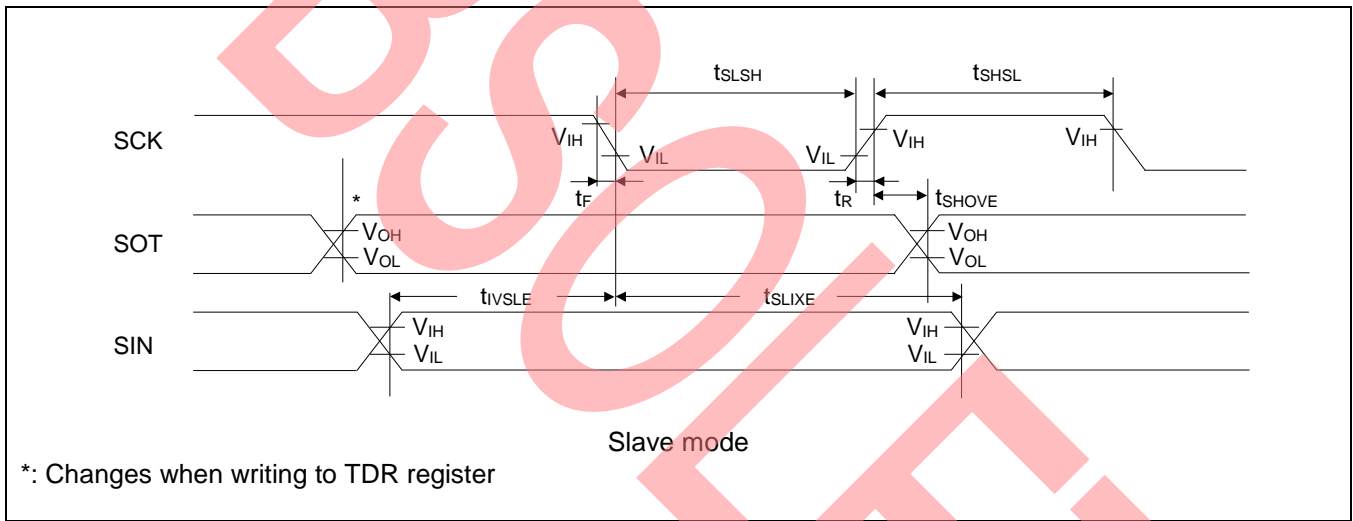
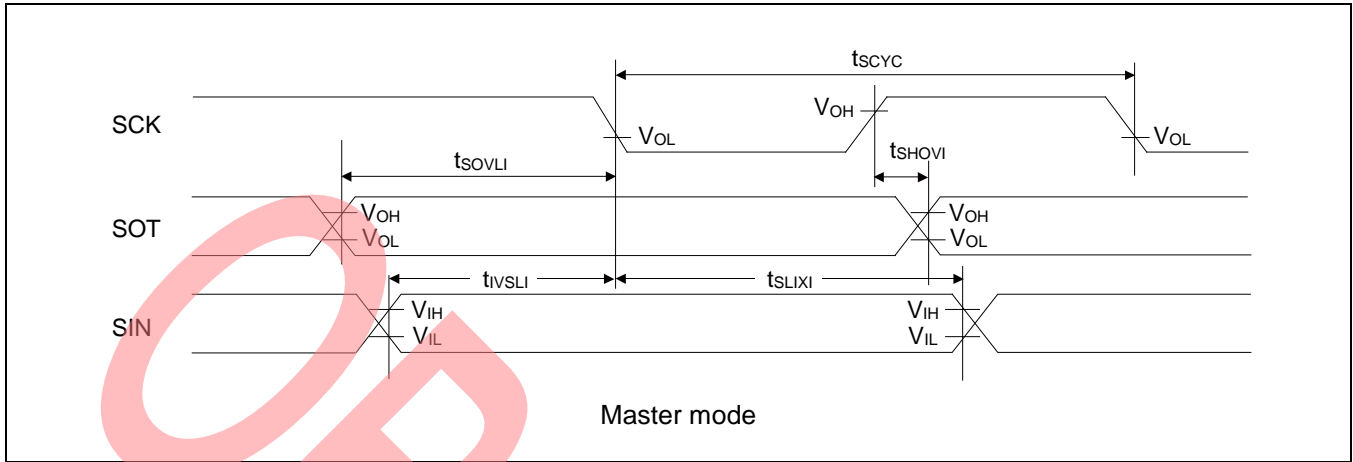
## SPI (SPI=1, SCINV=0)

( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4 t_{CYCP}$	-	$4 t_{CYCP}$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		50	-	36	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKx, SINx		0	-	0	-	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKx, SOTx		$2 t_{CYCP} - 30$	-	$2 t_{CYCP} - 30$	-	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKx	Slave mode	$2 t_{CYCP} - 10$	-	$2 t_{CYCP} - 10$	-	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCKx, SOTx		-	50	-	33	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		10	-	10	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

### Notes:

- The above AC characteristics are for clock synchronous mode.
- $t_{CYCP}$  represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance  $C_L = 30\text{ pF}$



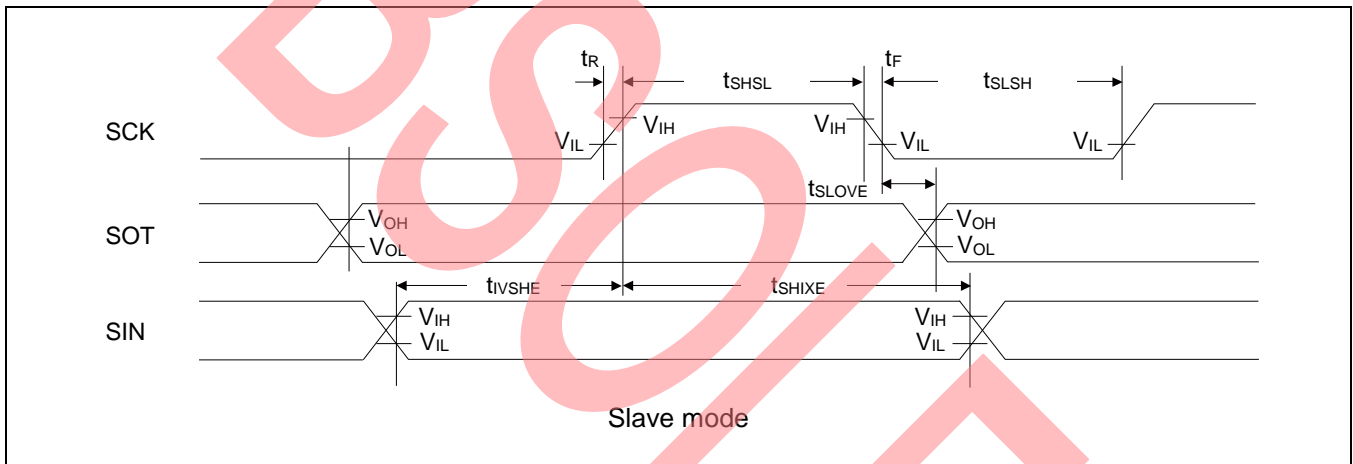
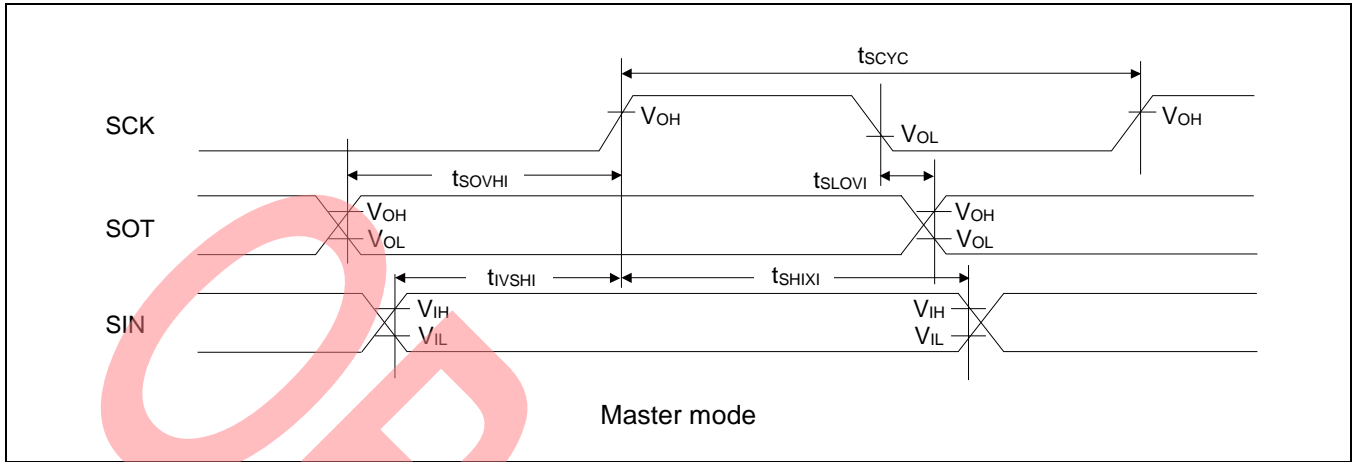
## SPI (SPI=1, SCINV=1)

( $V_{CC}$  = 1.65 V to 3.6 V,  $V_{SS}$  = 0 V,  $T_A$  = -40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7$ V		$V_{CC} \geq 2.7$ V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4 t_{CYCP}$	-	$4 t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	$t_{SOVHI}$	SCKx, SOTx		$2 t_{CYCP} - 30$	-	$2 t_{CYCP} - 30$	-	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKx	Slave mode	$2 t_{CYCP} - 10$	-	$2 t_{CYCP} - 10$	-	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

### Notes:

- The above AC characteristics are for clock synchronous mode.
- $t_{CYCP}$  represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance  $C_L=30$  pF



### When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t <sub>CSSI</sub>	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t <sub>CSE</sub>	Slave mode	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK↑→SCS↑ hold time	t <sub>CSE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSE</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS↓→SOT delay time	t <sub>DSE</sub>		-	55	-	40	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

\*1: CSSU bit value x serial chip select timing operating clock cycle.

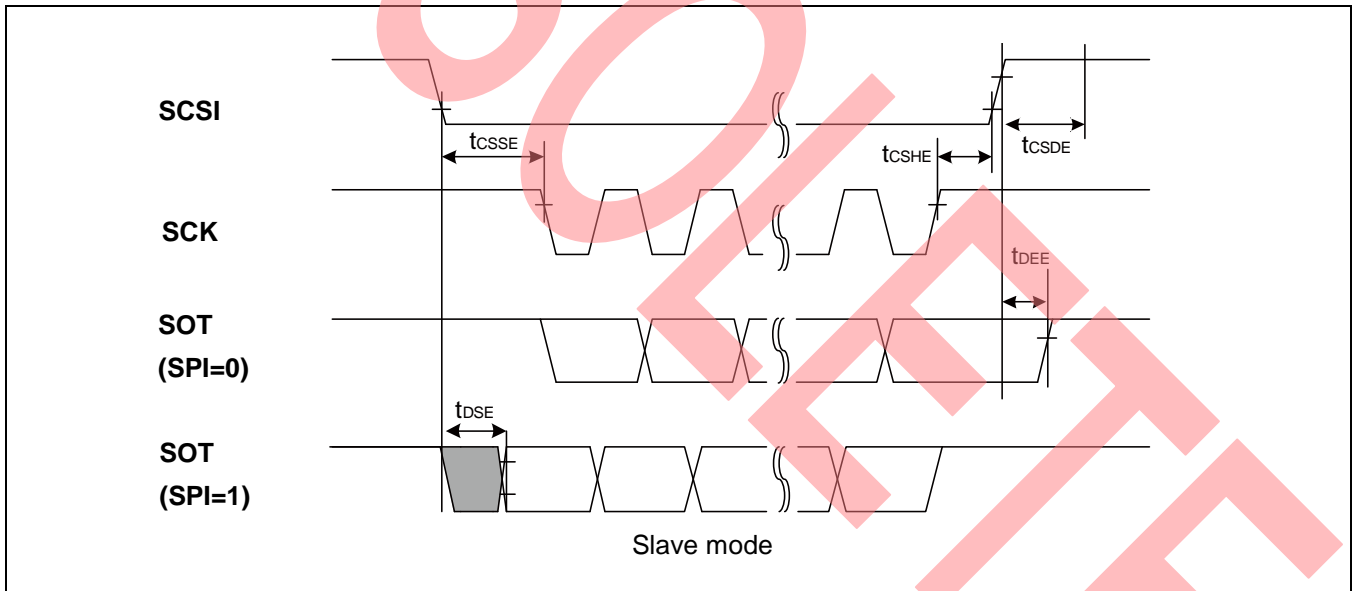
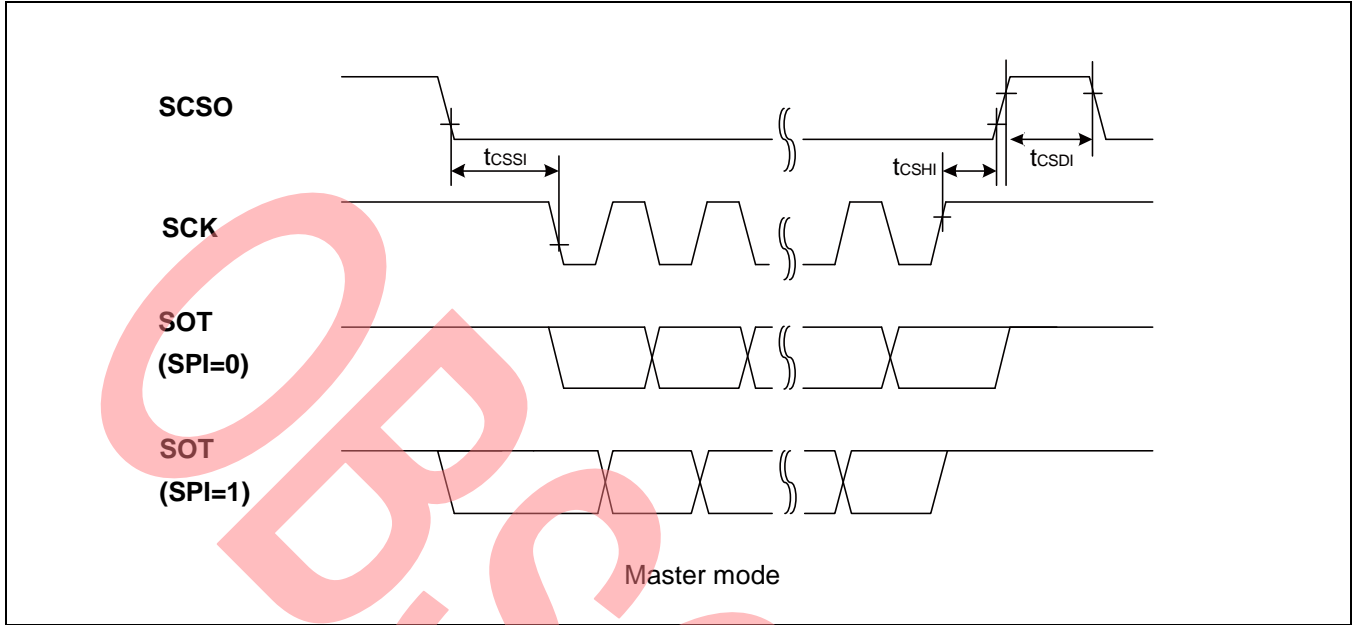
\*2: CSHD bit value x serial chip select timing operating clock cycle.

\*3: CSDS bit value x serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, 5t<sub>CYCP</sub> or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

#### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub>=30 pF.



## When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS <sub>↓</sub> →SCK <sub>↑</sub> setup time	t <sub>CSSI</sub>	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK <sub>↓</sub> →SCS <sub>↑</sub> hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS <sub>↓</sub> →SCK <sub>↑</sub> setup time	t <sub>CSE</sub>	Slave mode	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK <sub>↓</sub> →SCS <sub>↑</sub> hold time	t <sub>CSEH</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSEDE</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS <sub>↓</sub> →SOT delay time	t <sub>DSE</sub>		-	55	-	40	ns
SCS <sub>↑</sub> →SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

\*1: CSSU bit value × serial chip select timing operating clock cycle.

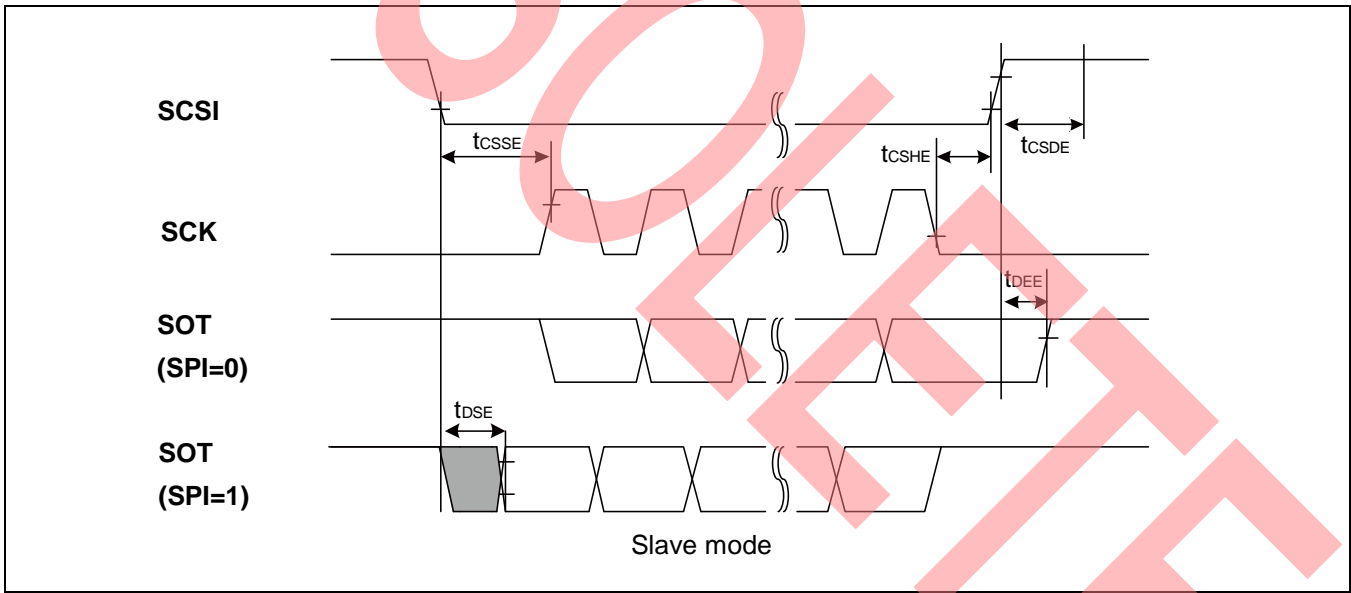
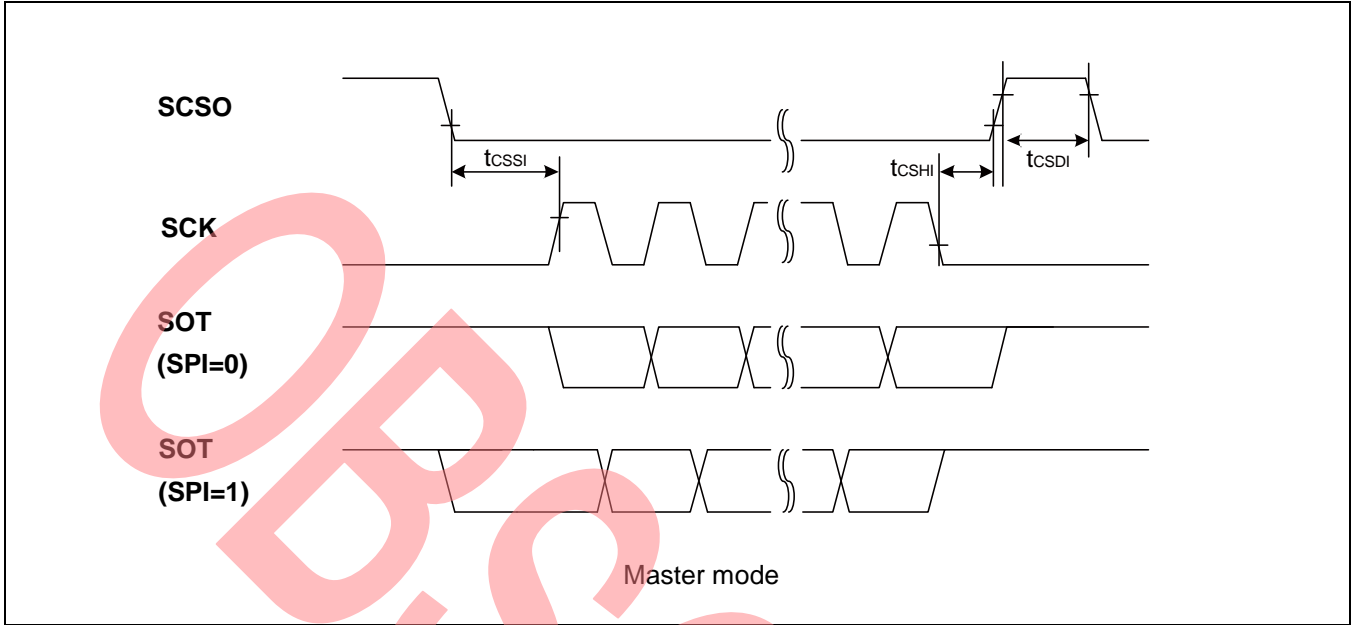
\*2: CSHD bit value × serial chip select timing operating clock cycle.

\*3: CSDS bit value × serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, 5t<sub>CYCP</sub> or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub>=30 pF.



## When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t <sub>CSSI</sub>	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t <sub>CSSe</sub>	Slave mode	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK↑→SCS↓ hold time	t <sub>CShE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDe</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS↑→SOT delay time	t <sub>DSE</sub>		-	55	-	40	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

\*1: CSSU bit value × serial chip select timing operating clock cycle.

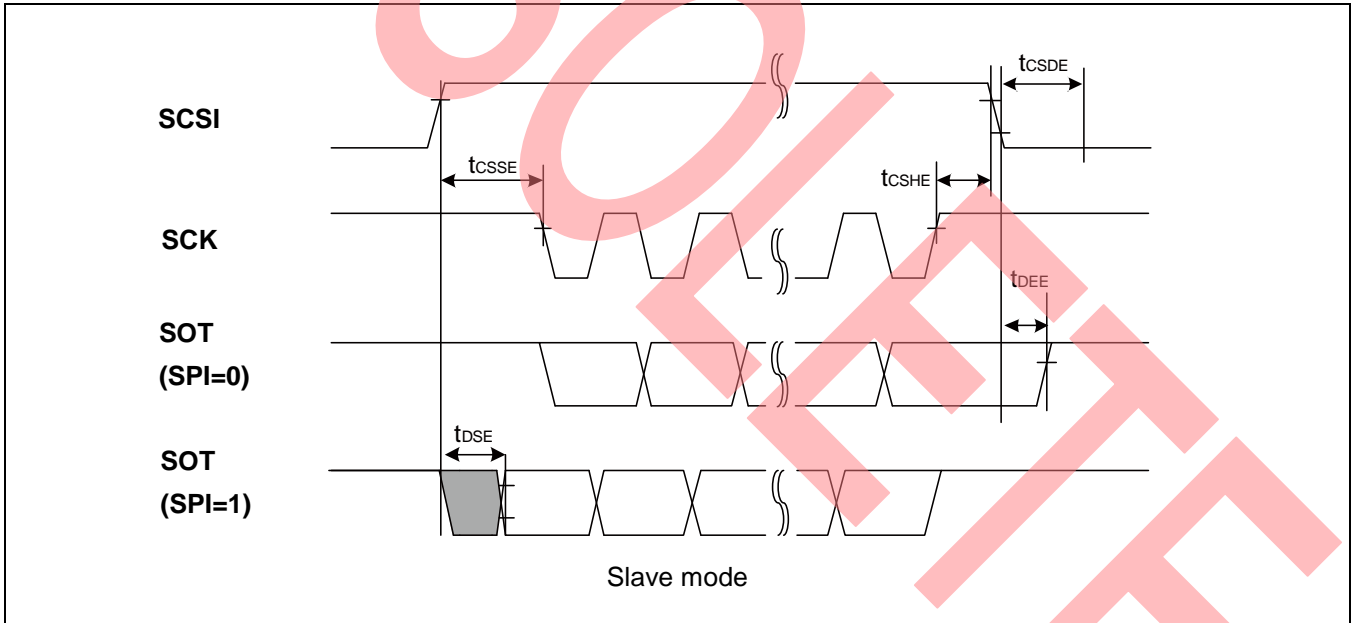
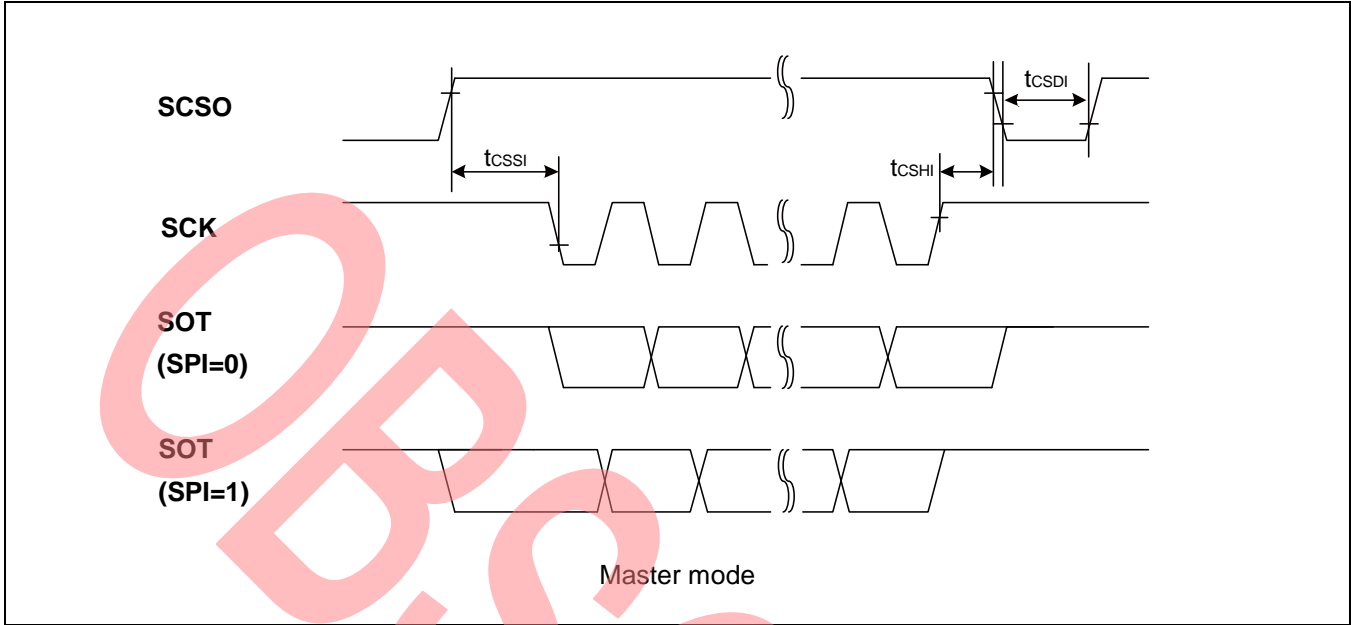
\*2: CSHD bit value × serial chip select timing operating clock cycle.

\*3: CSDS bit value × serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, 5t<sub>CYCP</sub> or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

### Notes:

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub>=30 pF.



## When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t <sub>CSSI</sub>	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t <sub>CSDI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t <sub>CSE</sub>	Slave mode	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK↓→SCS↓ hold time	t <sub>CSE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSE</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS↑→SOT delay time	t <sub>DEE</sub>		-	55	-	40	ns
SCS↓→SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

\*1: CSSU bit value × serial chip select timing operating clock cycle.

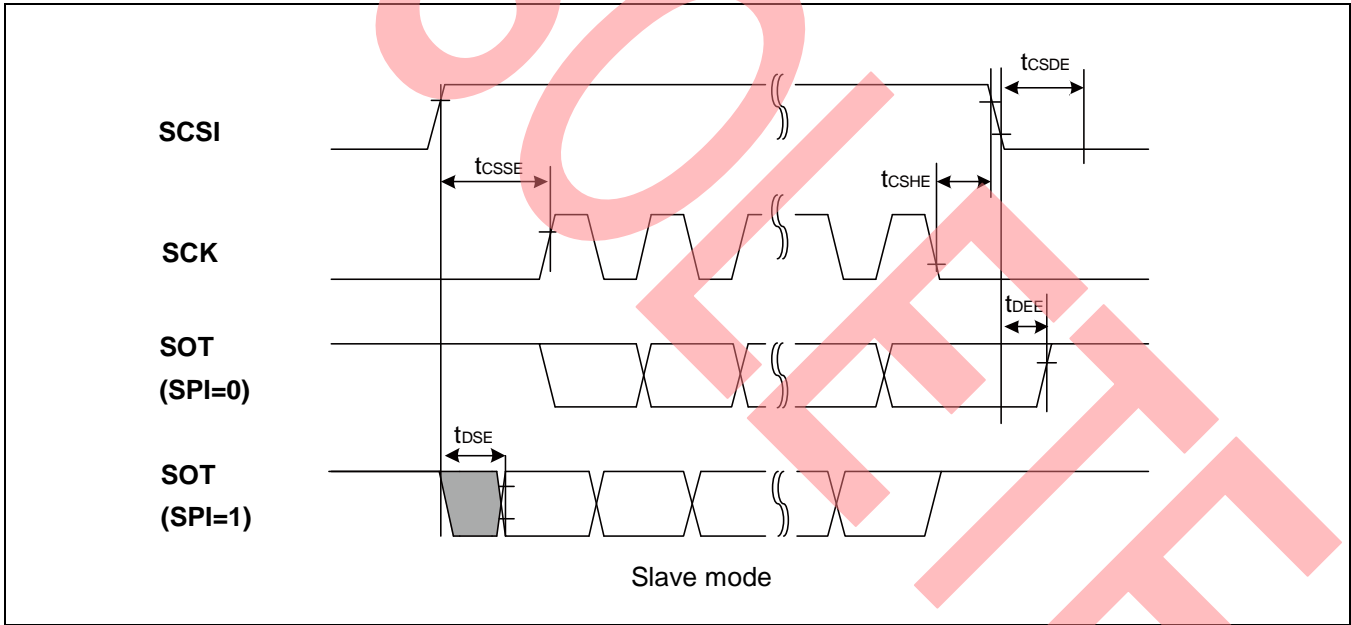
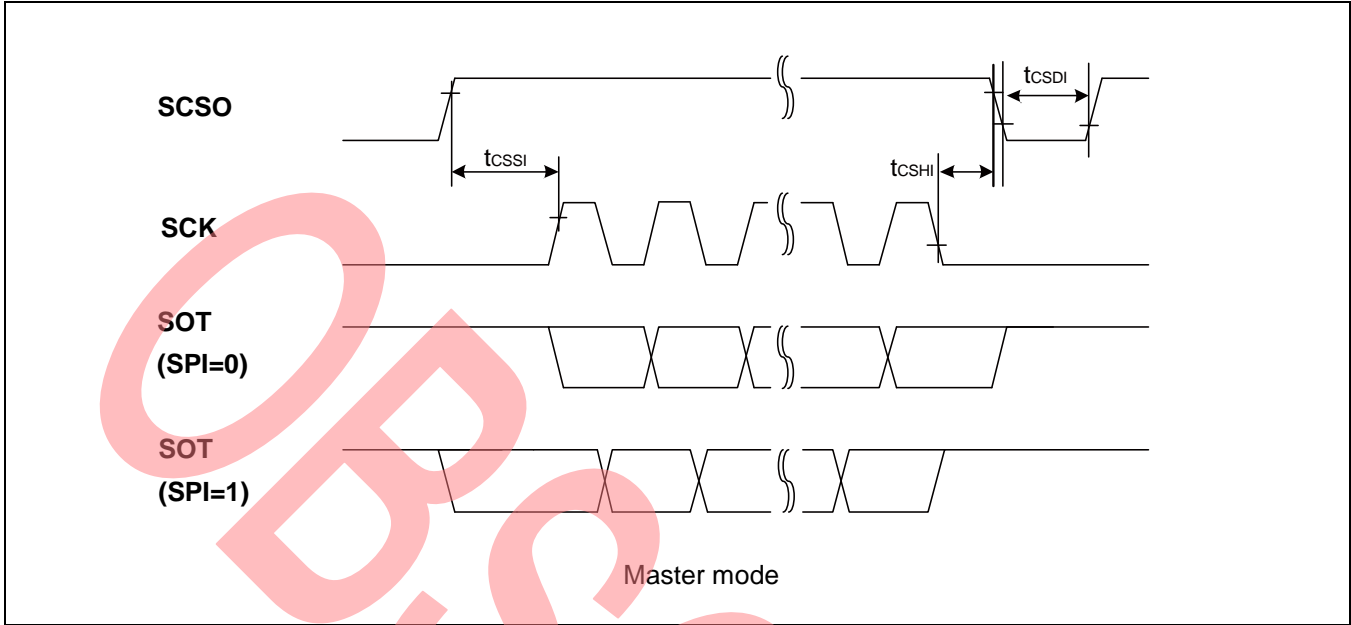
\*2: CSHD bit value × serial chip select timing operating clock cycle.

\*3: CSDS bit value × serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, 5t<sub>CYCP</sub> or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

### Notes:

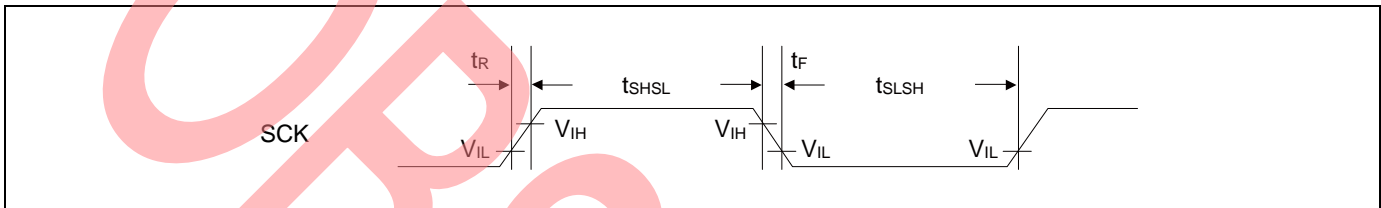
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub>=30 pF.



**UART external clock input (EXT=1)**

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L=30$ pF	$t_{CYCP} +10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} +10$	-	ns	
SCK falling time	$t_F$		-	5	ns	
SCK rising time	$t_R$		-	5	ns	



### 11.4.10 External Input Timing

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{INH}$ , $t_{INL}$	ADTGx	-	$2 t_{CYCP}^{*1}$	-	ns	A/D converter trigger input
		INT00 to INT08, INT12, INT13, INT15, NMIX	*2	$2 t_{CYCP} + 100^{*1}$	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

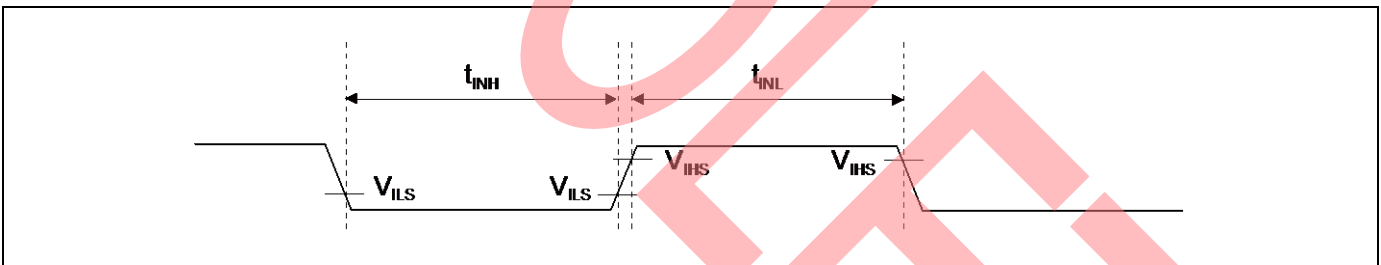
\*1:  $t_{CYCP}$  represents the APB bus clock cycle time.

For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

\*2: In Run mode and Sleep mode

\*3: In Timer mode, RTC mode and Stop mode

\*4: In Deep Standby RTC mode and Deep Standby Stop mode

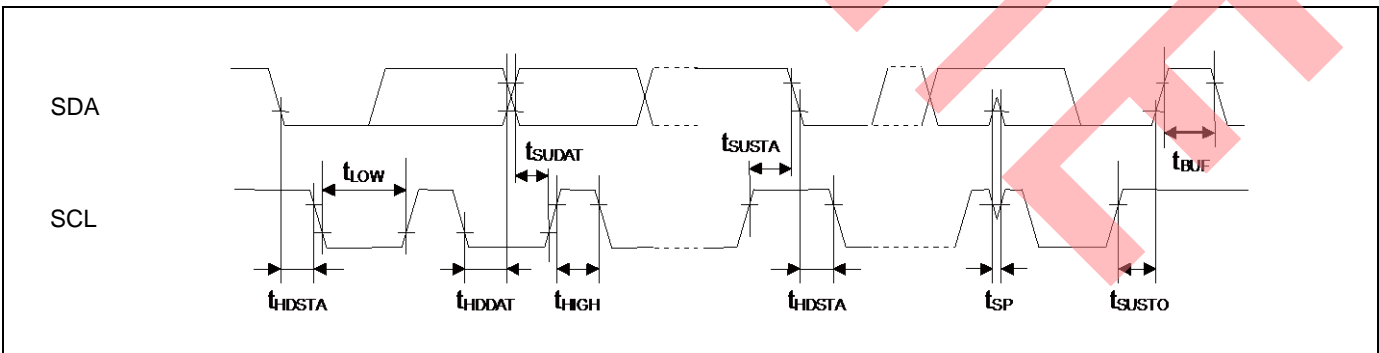


### 11.4.11 I<sup>2</sup>C Timing / I2C Slave Timing

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL(SI2CSCL) clock frequency	F <sub>SCL</sub>		0	100	0	400	kHz	
(Repeated) Start condition hold time SDA(SI2CSDA) ↓ → SCL(SI2CSCL) ↓	t <sub>HDSTA</sub>		4.0	-	0.6	-	μs	
SCL(SI2CSCL) clock L width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCL(SI2CSCL) clock H width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) Start setup time SCL(SI2CSCL) ↑ → SDA (SI2CSDA) ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL(SI2CSCL) ↓ → SDA(SI2CSDA) ↓ ↑	t <sub>HDDAT</sub>	C <sub>L</sub> =30 pF, R=(V <sub>P</sub> /I <sub>OL</sub> )* <sup>1</sup>	0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs	
Data setup time SDA(SI2CSDA) ↓ ↑ → SCL(SI2CSCL) ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
Stop condition setup time SCL(SI2CSCL) ↑ → SDA (SI2CSDA) ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between Stop condition and Start condition	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	ns	except I2C Slave

- \*1: R represents the pull-up resistance of the SCL and SDA lines, and C<sub>L</sub> the load capacitance of the SCL and SDA lines. V<sub>P</sub> represents the power supply voltage of the pull-up resistance, and I<sub>OL</sub> the V<sub>OL</sub> guaranteed current.
- \*2: The maximum t<sub>HDDAT</sub> must satisfy at least the condition that the period during which the device is holding the SCL signal at L (t<sub>LOW</sub>) does not extend.
- \*3: A Fast-mode I<sup>2</sup>C bus device can be used in a Standard-mode I<sup>2</sup>C bus system, provided that the condition of t<sub>SUDAT</sub> ≥ 250 ns is fulfilled.
- \*4: t<sub>CYCP</sub> represents the APB bus clock cycle time.  
For the number of the APB bus to which the I<sup>2</sup>C is connected, see "8. Block Diagram".  
To use Standard-mode, set the APB bus clock at 2 MHz or more.  
To use Fast-mode, set the APB bus clock at 8 MHz or more.



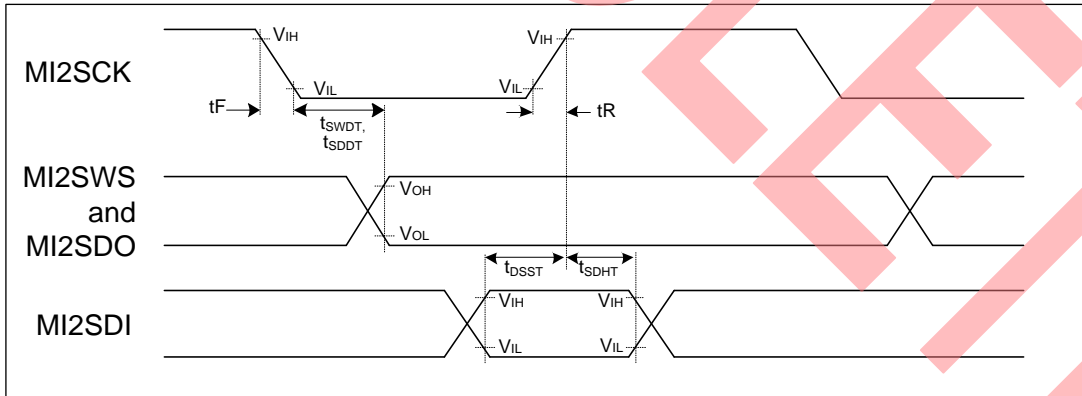
### 11.4.12 I<sup>2</sup>S Timing (MFS-I<sup>2</sup>S Timing)

#### Master Mode Timing

(V<sub>CC</sub>= 1.65 V to 3.6 V, V<sub>SS</sub>= 0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency (*1)	F <sub>MI2SCK</sub>	MI2SCKx	C <sub>L</sub> =30 pF	-	6.144	-	6.144	MHz
I <sup>2</sup> S clock cycle time (*1)	t <sub>CYC</sub>	MI2SCKx		4 t <sub>CYCP</sub>	-	4 t <sub>CYCP</sub>	-	ns
I <sup>2</sup> S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t <sub>SWDT</sub>	MI2SWS <sub>x</sub>		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t <sub>SDDT</sub>	MI2SDO <sub>x</sub>		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t <sub>DSST</sub>	MI2SCKx MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t <sub>SDHT</sub>	MI2SCKx MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t <sub>F</sub>	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t <sub>R</sub>	MI2SCKx	-	5	-	5	ns	

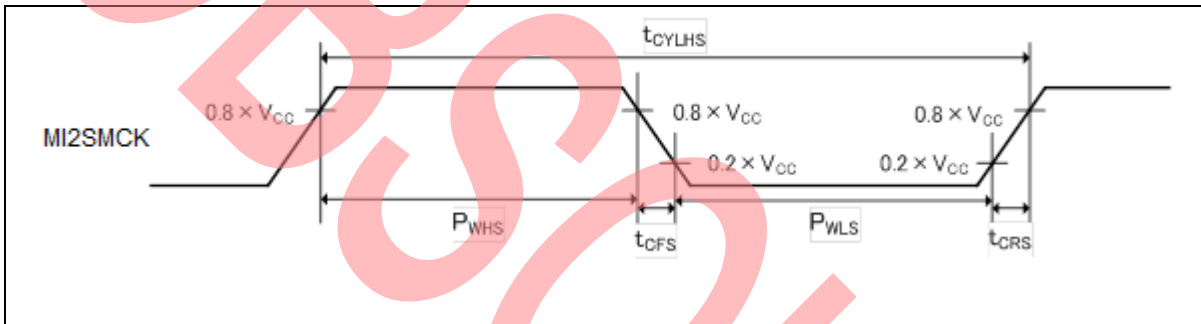
\*1: I<sup>2</sup>S clock should meet the multiple of PCLK(t<sub>CYC</sub>) and the frequency less than F<sub>MI2SCK</sub> meantime. The detail information please refer to Chapter I<sup>2</sup>S of Communication Macro Part of Peripheral Manual.



### MI2SMCK Input Characteristics

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CHS}$	MI2SMCK	-	-	12.288	MHz	
Input clock cycle	$t_{CYLHS}$	-	-	81.3	-	ns	
Input clock pulse width	-	-	$P_{WHS}/t_{CYLHS}$ $P_{WLS}/t_{CYLHS}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CFS}$ $t_{CRS}$	-	-	-	5	ns	When using external clock



### MI2SMCK Output Characteristics

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	$f_{CHS}$	MI2SMCK	-	-	25	MHz	$V_{CC} \geq 2.7$ V
				-	20	MHz	$V_{CC} < 2.7$ V

### 11.4.13 Smart Card Interface Characteristics

( $V_{CC}$ = 1.65 V to 3.6 V,  $V_{SS}$ = 0 V,  $T_A$ =- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	$t_R$	ICx_VCC, ICx_RST,	C <sub>L</sub> =30 pF	4	20	ns	
Output falling time	$t_F$	ICx_CLK, ICx_DATA		4	20	ns	
Output clock frequency	$f_{CLK}$	ICx_CLK		-	20	MHz	
Duty cycle	$\Delta$			45%	55%		

- External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx\_CIN pin when it's used as smart card reader function.

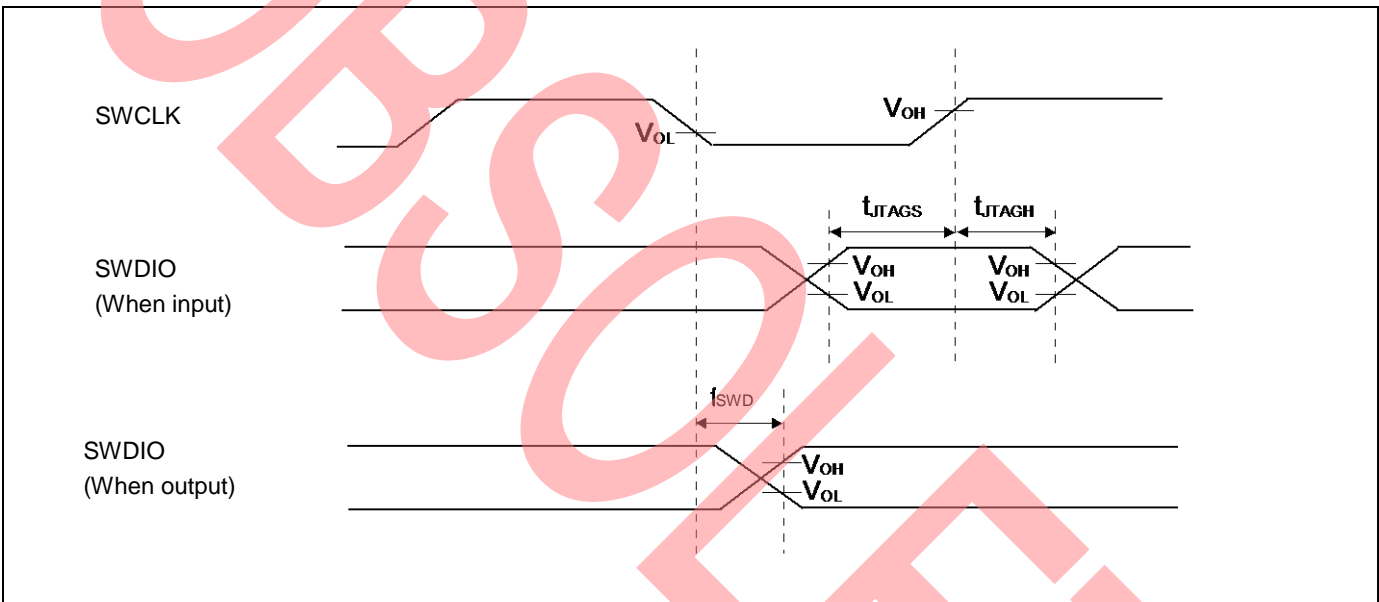
### 11.4.14 SW-DP Timing

( $V_{CC}$  = 1.65 V to 3.6 V,  $V_{SS}$  = 0 V,  $T_A$  = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	$t_{sws}$	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	$t_{swh}$	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	$t_{swd}$	SWCLK, SWDIO	-	-	45	ns	

**Note:**

- External load capacitance  $C_L$  = 30 pF



## 11.5 12-bit A/D Converter

### Electrical Characteristics of A/D Converter (Preliminary Values)

( $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	$V_{ZT}$	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	$V_{FST}$	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time*1	-	-	1.0	-	-	$\mu\text{s}$	$V_{CC} \geq 2.7\text{ V}$
			4.0	-	-		$1.8 \leq V_{CC} < 2.7\text{ V}$
			10	-	-		$1.65 \leq V_{CC} < 1.8\text{ V}$
Sampling time *2	$T_s$	-	0.3	-	10	$\mu\text{s}$	$V_{CC} \geq 2.7\text{ V}$
			1.2	-			$1.8 \leq V_{CC} < 2.7\text{ V}$
			3.0	-			$1.65 \leq V_{CC} < 1.8\text{ V}$
Compare clock cycle *3	$T_{cck}$	-	50	-	1000	ns	$V_{CC} \geq 2.7\text{ V}$
			200	-			$1.8 \leq V_{CC} < 2.7\text{ V}$
			500	-			$1.65 \leq V_{CC} < 1.8\text{ V}$
State transition time to operation permission	$T_{stt}$	-	-	-	1.0	$\mu\text{s}$	
Analog input capacity	$C_{AIN}$	-	-	-	7.5	pF	
Analog input resistance	$R_{AIN}$	-	-	-	2.2	k $\Omega$	$V_{CC} \geq 2.7\text{ V}$
					5.5		$1.8 \leq V_{CC} < 2.7\text{ V}$
					10.5		$1.65 \leq V_{CC} < 1.8\text{ V}$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	$\mu\text{A}$	
Analog input voltage	-	ANxx	$V_{SS}$	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	$V_{CC}$	V	$V_{CC} \geq 2.7\text{ V}$
			$V_{CC}$				$V_{CC} < 2.7\text{ V}$
		AVRL	$V_{SS}$	-	$V_{SS}$	V	

\*1: The conversion time is the value of sampling time ( $t_s$ ) + compare time ( $t_c$ ).

The minimum conversion time is computed according to the following conditions:

$V_{CC} \geq 2.7\text{ V}$	sampling time=0.3 $\mu\text{s}$ , compare time=0.7 $\mu\text{s}$
$1.8 \leq V_{CC} < 2.7\text{ V}$	sampling time=1.2 $\mu\text{s}$ , compare time=2.8 $\mu\text{s}$
$1.65 \leq V_{CC} < 1.8\text{ V}$	sampling time=3.0 $\mu\text{s}$ , compare time=7.0 $\mu\text{s}$

Ensure that the conversion time satisfies the specifications of the sampling time ( $t_s$ ) and compare clock cycle ( $t_{cck}$ ).

For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

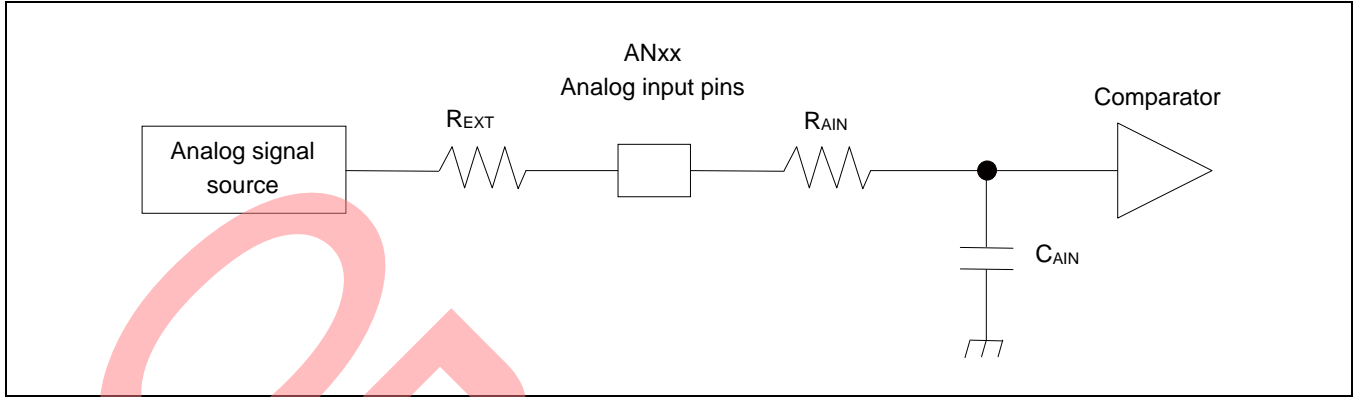
For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".

The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

\*2: The required sampling time varies according to the external impedance.

Set a sampling time that satisfies (Equation 1).

\*3: The compare time ( $t_c$ ) is the result of (Equation 2).



(Equation 1)  $t_s \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

$t_s$ : Sampling time

$R_{AIN}$ : Input resistance of A/D Converter = 2.2 k $\Omega$  with  $2.7 \leq V_{CC} \leq 3.6$

Input resistance of A/D Converter = 5.5 k $\Omega$  with  $1.8 \leq V_{CC} \leq 2.7$

Input resistance of A/D Converter = 10.5 k $\Omega$  with  $1.65 \leq V_{CC} \leq 1.8$

$C_{AIN}$ : Input capacitance of A/D Converter = 7.5 pF with  $1.65 \leq V_{CC} \leq 3.6$

$R_{EXT}$ : Output impedance of external circuit

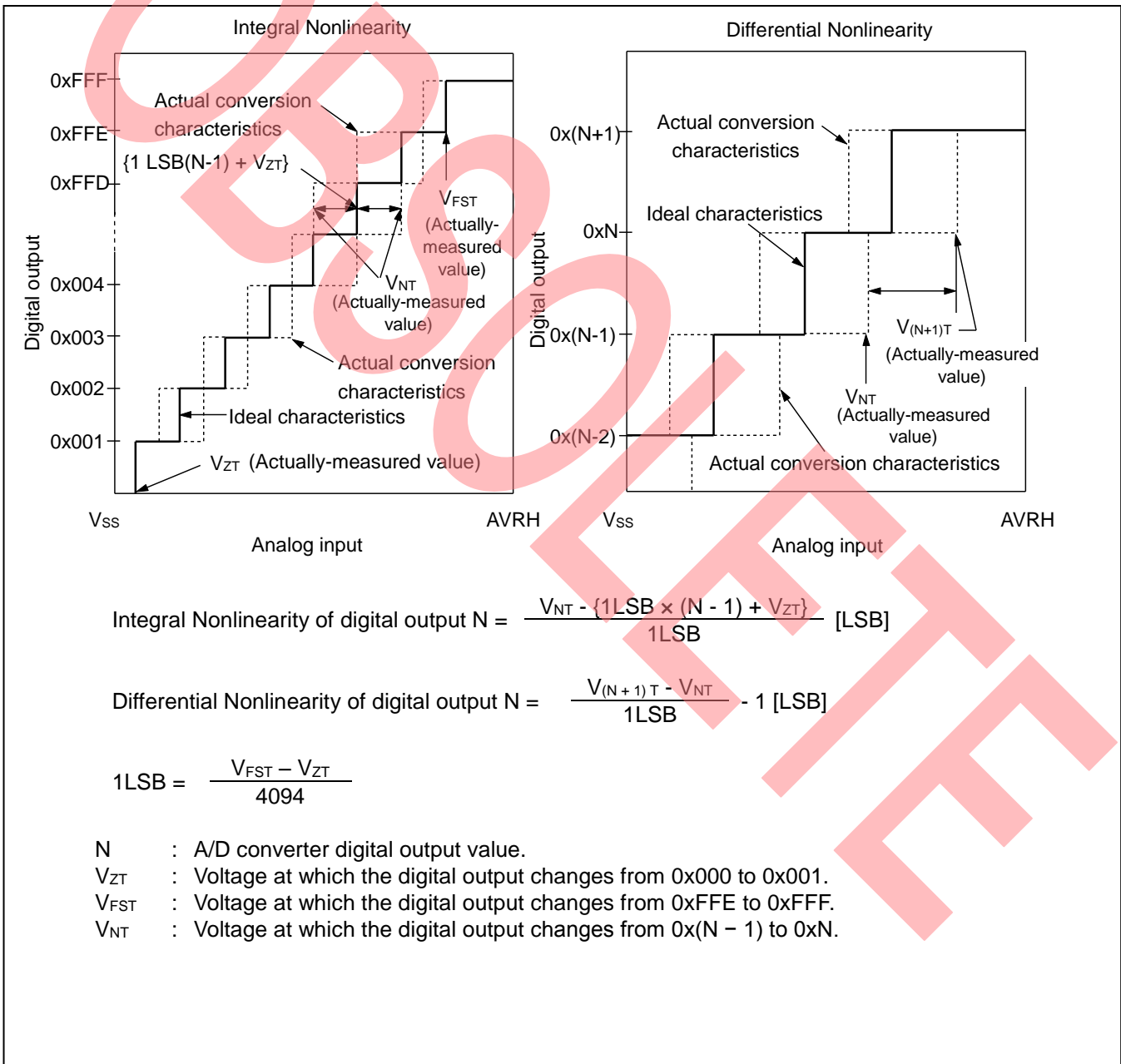
(Equation 2)  $t_c = t_{CCK} \times 14$

$t_c$ : Compare time

$t_{CCK}$ : Compare clock cycle

## Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



## 11.6 Low-Voltage Detection Characteristics

### 11.6.1 Low-Voltage Detection Reset

(T<sub>A</sub>=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V <sub>DL</sub>	Fixed*1	1.38	1.50	1.60	V	When voltage drops
Released voltage	V <sub>DH</sub>		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	T <sub>LVDW</sub>	-	-	-	8160x t <sub>CYCP</sub> *2	μs	
LVD detection delay time	T <sub>LVDL</sub>	-	-	-	200	μs	

\*1: The value of low voltage detection reset is always fixed.

\*2: t<sub>CYCP</sub> indicates the APB1 bus clock cycle time.

### 11.6.2 Low-Voltage Detection Interrupt

(T<sub>A</sub>=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T <sub>LVDW</sub>	-	-	-	8160 × t <sub>CYCP</sub> *	μs	
LVD detection delay time	T <sub>LVDL</sub>	-	-	-	200	μs	

\*: t<sub>CYCP</sub> represents the APB1 bus clock cycle time.

## 11.7 Flash Memory Write/Erase Characteristics

(V<sub>CC</sub>=1.65 V to 3.6 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	μs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	4.5	11.7	s	The chip erase time includes the time of writing prior to internal erase.

\*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

### Write/Erase Cycle and Data Hold Time

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

\*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

## 11.8 Return Time from Low-Power Consumption Mode

### 11.8.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

#### Return Count Time

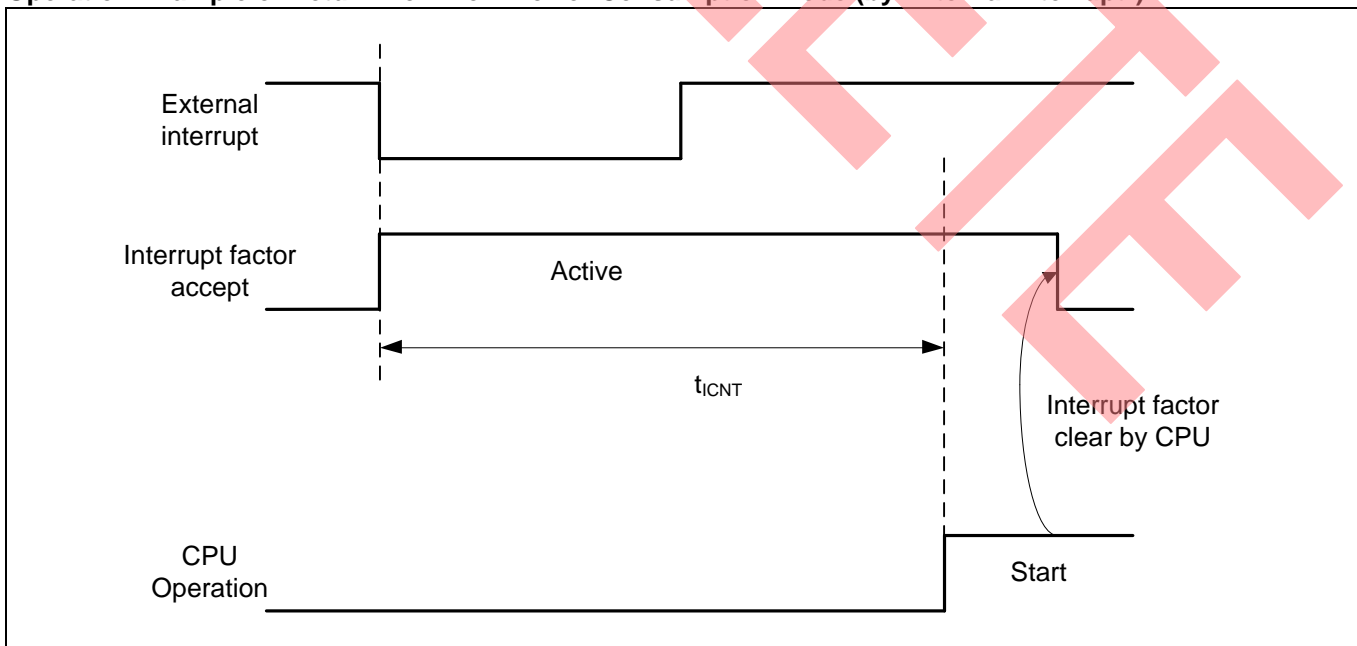
( $V_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter		Symbol	Value		Unit	Remarks
Current Mode	Mode to return		Typ	Max*1		
Sleep mode	each Run Modes	ticNT	4*HCLK		$\mu\text{s}$	When High-speed CR is enabled
Timer mode	High-speed CR Run mode Main Run mode PLL Run mode		12*HCLK	13*HCLK	$\mu\text{s}$	When High-speed CR is enabled
	Low-speed CR Run mode Sub Run mode		34+12*HCLK	72+13*HCLK	$\mu\text{s}$	
Stop Mode	High-speed CR Run mode Low-speed CR Run mode		34+12*HCLK	72+13*HCLK	$\mu\text{s}$	
	Main Run mode Sub Run mode PLL Run mode		34+12*HCLK +tOSCWT	72+13*HCLK +tOSCWT	$\mu\text{s}$	*2
RTC mode	High-speed CR Run mode Low-speed CR Run mode Sub Run mode		34+12*HCLK	72+13*HCLK	$\mu\text{s}$	
	Main Run mode PLL Run mode		34+12*HCLK +tOSCWT	72+13*HCLK +tOSCWT	$\mu\text{s}$	*2
Deep Standby RTC mode Deep Standby Stop mode	High-speed CR Run mode		43	281	$\mu\text{s}$	

\*1: The maximum value depends on the condition of environment.

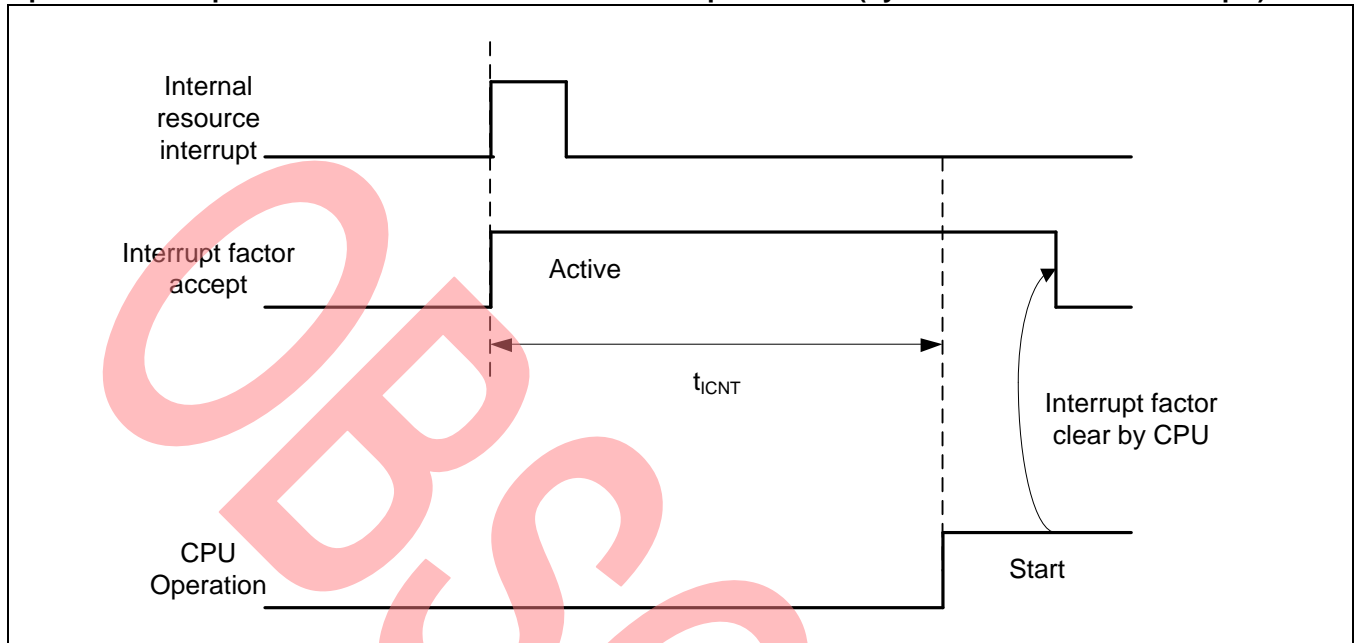
\*2: tOSCWT : Oscillator stabilization time.

#### Operation Example of Return from Low-Power Consumption Mode (by External Interrupt\*)



\*: External interrupt is set to detecting fall edge.

### Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt\*)



\*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

#### Notes:

- The return factor is different in each Low-Power consumption modes. See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".

### 11.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

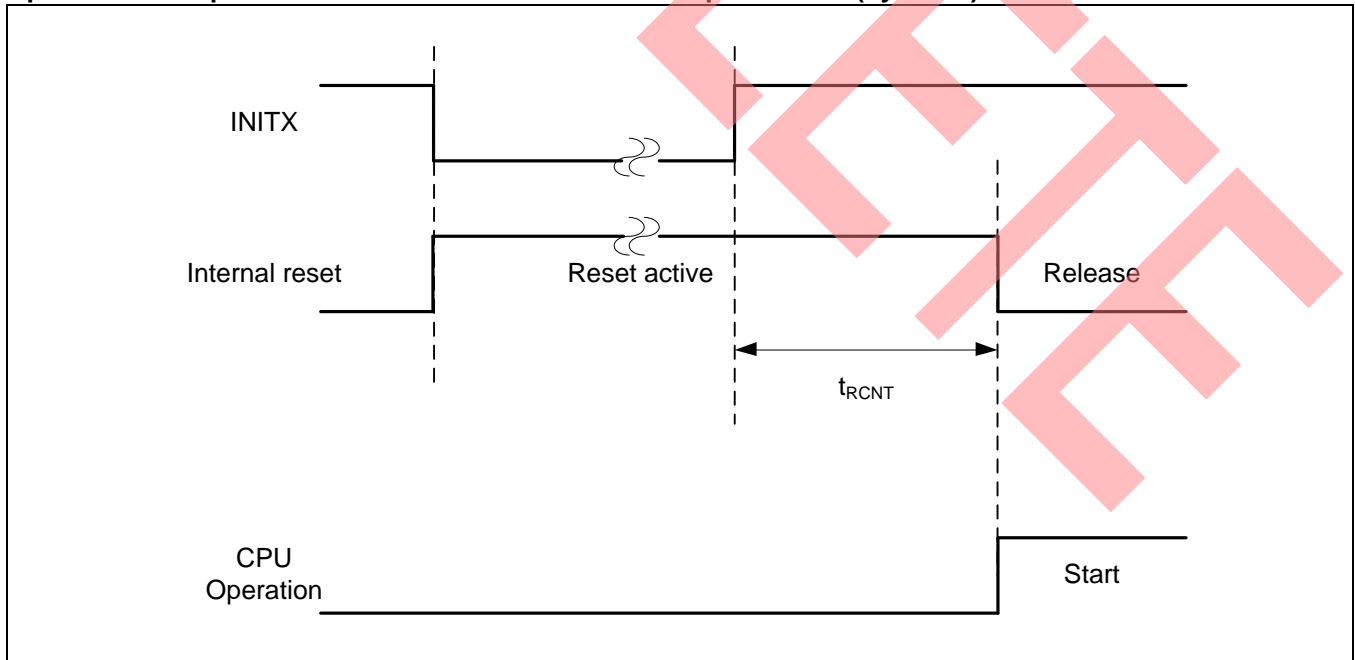
#### Return Count Time

( $V_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

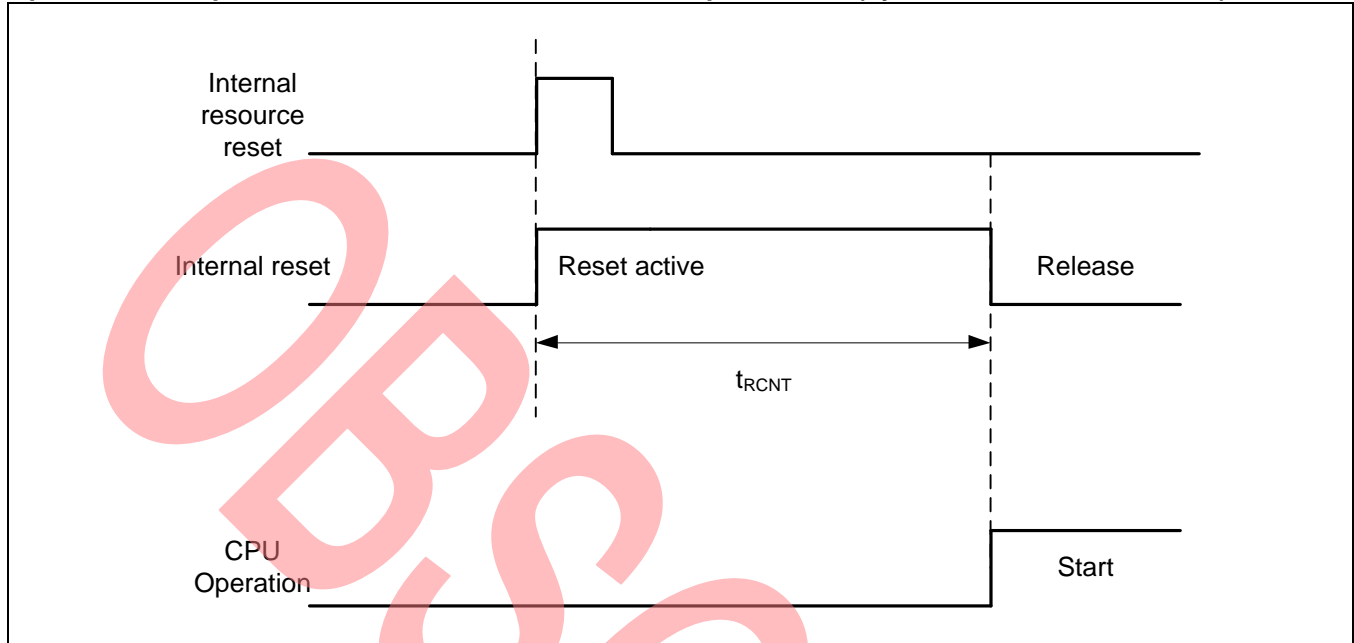
Parameter		Symbol	Value		Unit	Remarks
Current Mode	Mode to return		Typ	Max*		
High-speed CR Sleep mode Main Sleep mode PLL Sleep mode	High-speed CR Run mode	$t_{RCNT}$	20	22	$\mu\text{s}$	When High-speed CR is enabled
Low-speed CR Sleep mode			50	106	$\mu\text{s}$	When High-speed CR is enabled
Sub Sleep mode			112	137	$\mu\text{s}$	When High-speed CR is enabled
High-speed CR Timer mode Main Timer mode PLL Timer mode			20	22	$\mu\text{s}$	When High-speed CR is enabled
Low-speed CR Timer mode			87	159	$\mu\text{s}$	
Sub Timer mode			148	209	$\mu\text{s}$	
Stop mode RTC mode			45	68	$\mu\text{s}$	
Deep Standby RTC mode Deep Standby Stop mode			43	281	$\mu\text{s}$	

\*: The maximum value depends on the accuracy of built-in CR.

#### Operation Example of Return from Low-Power Consumption Mode (by INITX)



### Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset\*)



\*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

#### Notes:

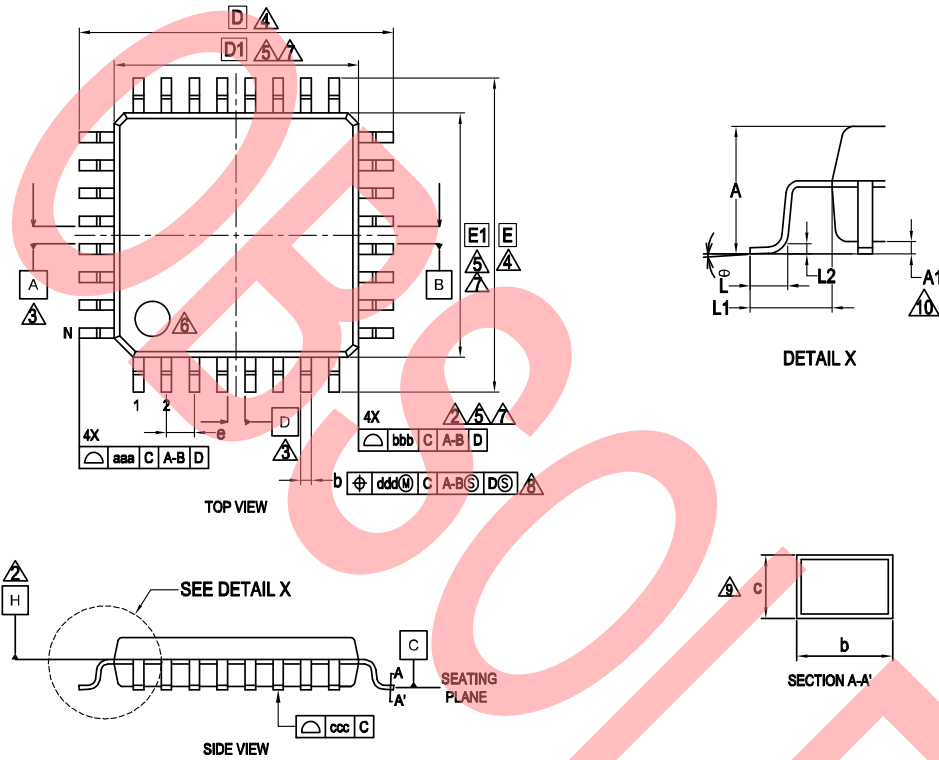
- The return factor is different in each Low-Power consumption modes. See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".
- The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low-voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

## 12. Ordering Information

Part number	On-chip Flash memory	On-Chip SRAM	Package	Packing
	[Kbyte]	[Kbyte]		
S6E1C12D0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 64 pins (LQD064-02)	Tray
S6E1C11D0AGV20000	64	12		
S6E1C12C0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 48 pins (LQA048-02)	Tray
S6E1C11C0AGV20000	64	12		
S6E1C12B0AGP20000	128	16	Plastic • LQFP (0.80 mm pitch), 32 pins (LQB032)	Tray
S6E1C11B0AGP20000	64	12		
S6E1C12D0AGN20000	128	16	Plastic • QFN64 (0.50 mm pitch), 64 pins (WNS064)	Tray
S6E1C11D0AGN20000	64	12		
S6E1C12C0AGN20000	128	16	Plastic • QFN48 (0.50 mm pitch), 48 pins (WNY048)	Tray
S6E1C11C0AGN20000	64	12		
S6E1C12B0AGN20000	128	16	Plastic • QFN32 (0.50 mm pitch), 32 pins (WNU032)	Tray
S6E1C11B0AGN20000	64	12		

### 13. Package Dimensions

#### LQB032 032 LEAD PLASTIC LOW PROFILE QUAD FLAT PACKAGE



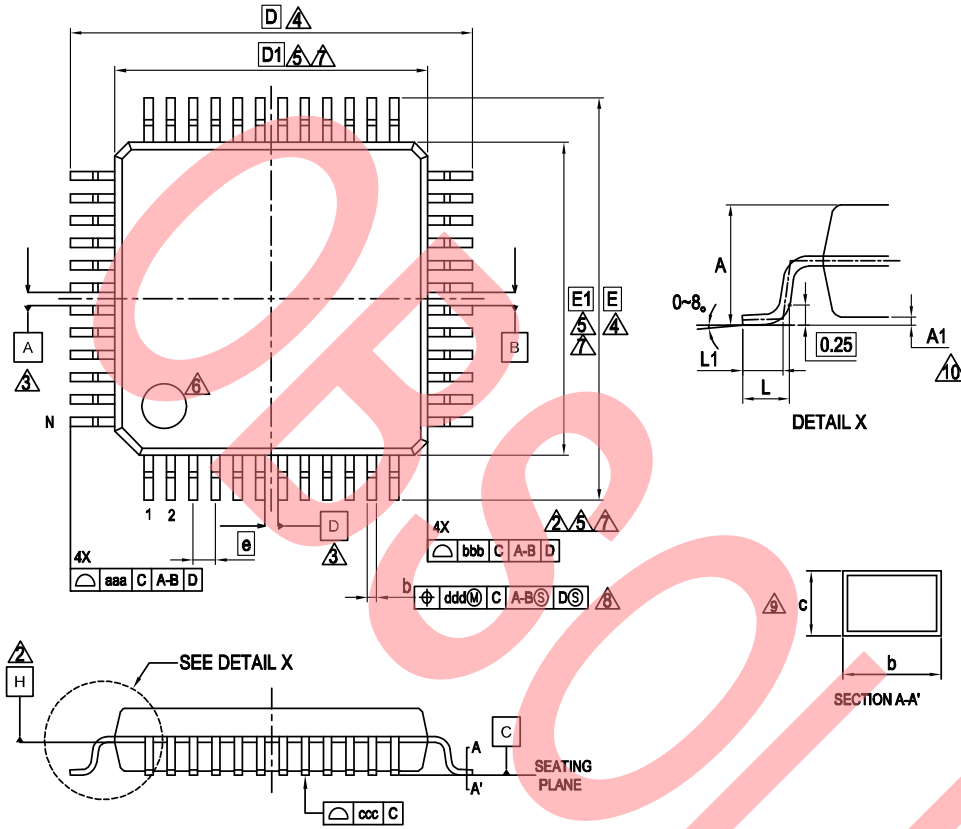
PACKAGE	LQB032			SYMBOL	TOLERANCES OF FORM AND POSITION
SYMBOL	MIN.	NOM.	MAX.		
A	—	—	1.60	N	32
A1	0.05	—	0.15	aaa	0.20
b	0.32	0.35	0.42	bbb	0.10
c	0.13	—	0.18	ccc	0.10
D	9.00 BSC			ddd	0.20
D1	7.00 BSC				
e	0.80 BSC				
E	9.00 BSC				
E1	7.00 BSC				
θ	0°	—	7°		
L	0.45	0.60	0.75		
L1	1.00 REF				
L2	0.25 BSC				

#### NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev.0B

LQA048-02 , 48 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQA048-02		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
e	0.50 BSC		
E	9.00 BSC.		
E1	7.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	48		

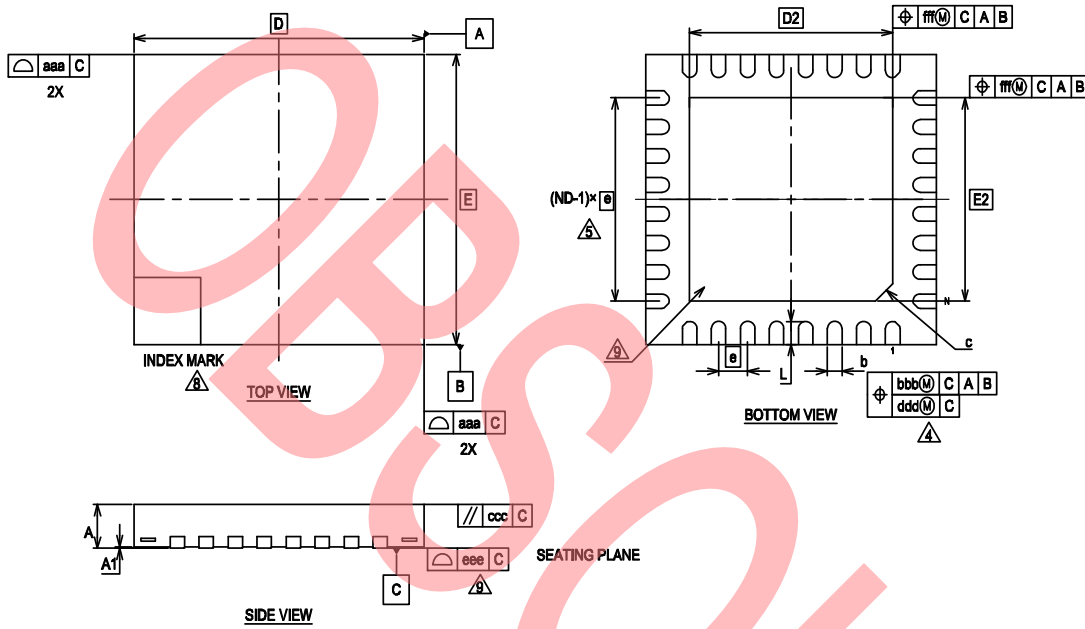
NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A



WNU032 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES

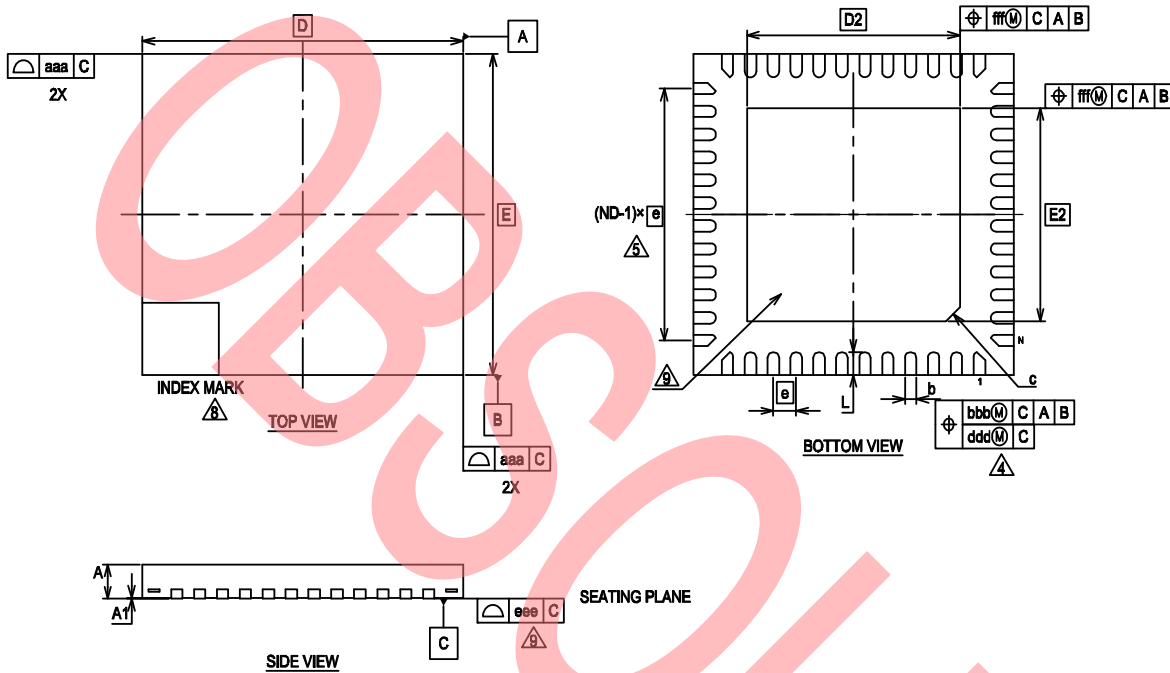


SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.80	PROFILE
A1	0.00	—	0.05	TERMINAL HEIGHT
D	5.00 BSC			BODY SIZE
E	5.00 BSC			BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D2	3.20 BSC			EXPOSED PAD SIZE
E2	3.20 BSC			EXPOSED PAD SIZE
e	0.50 BSC			TERMINAL PITCH
c	0.25 REF			EXPOSED PAD CHAMFER
L	0.35	0.40	0.45	TERMINAL LENGTH
N	32			TERMINAL COUNT
aaa	0.10			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
fff	0.10			

- DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- N IS THE TOTAL NUMBER OF TERMINALS.
- DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
- MAX. PACKAGE WARPAGE IS 0.05mm.
- MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
- PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
- BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Rev. 0A

## WNY048 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.80	PROFILE
A1	0.00	—	0.05	TERMINAL HEIGHT
D	7.00 BSC			BODY SIZE
E	7.00 BSC			BODY SIZE
b	0.18	0.25	0.30	TERMINAL WIDTH
D2	4.65 BSC			EXPOSED PAD SIZE
E2	4.65 BSC			EXPOSED PAD SIZE
e	0.50 BSC			TERMINAL PITCH
c	0.30 REF			EXPOSED PAD CHAMFER
L	0.45	0.50	0.55	TERMINAL LENGTH
N	48			TERMINAL COUNT
aaa	0.10			
bbb	0.10			
ddd	0.05			
eee	0.05			
fff	0.15			

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. N IS THE TOTAL NUMBER OF TERMINALS.

4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.

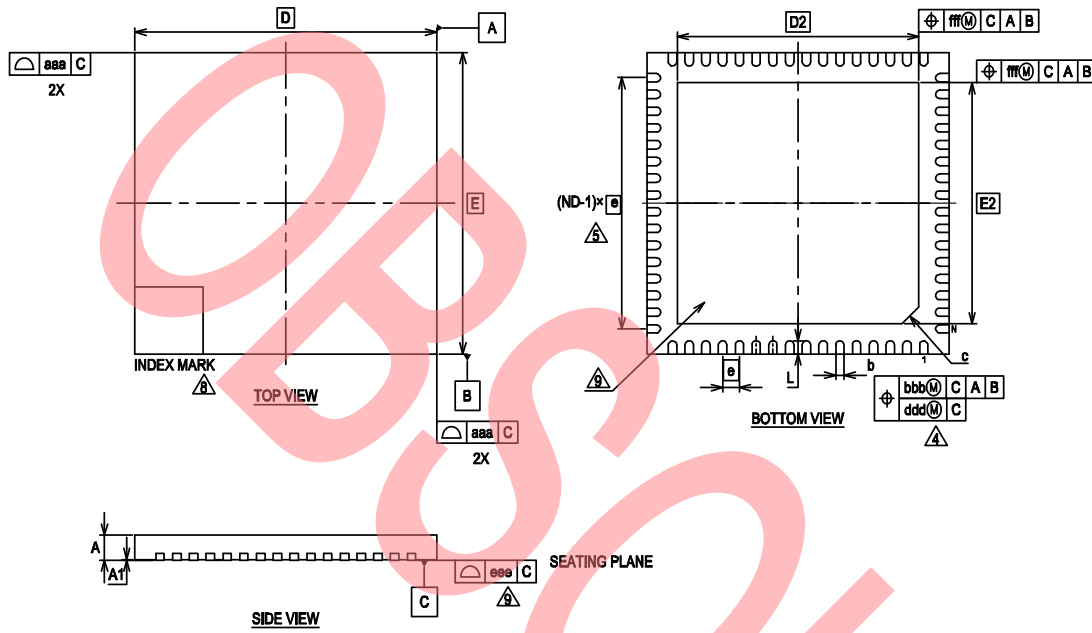
6. MAX. PACKAGE WARPAGE IS 0.05mm.

7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.

8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.

9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

**WNS064 VERY THIN PLASTIC QUAD FLAT NO LEAD PACKAGES**



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.80	PROFILE
A1	0.00	—	0.05	TERMINAL HEIGHT
D	9.00 BSC			BODY SIZE
E	9.00 BSC			BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D2	7.20 BSC			EXPOSED PAD SIZE
E2	7.20 BSC			EXPOSED PAD SIZE
e	0.50 BSC			TERMINAL PITCH
c	0.50 REF			EXPOSED PAD CHAMFER
L	0.35	0.40	0.45	TERMINAL LENGTH
N	64			TERMINAL COUNT
aaa	0.10			
bbb	0.10			
ddd	0.05			
eee	0.05			
fff	0.15			

- DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- N IS THE TOTAL NUMBER OF TERMINALS.
- DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.16 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
- MAX. PACKAGE WARPAGE IS 0.05mm.
- MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
- PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
- BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Rev. 0A

## Document History

Document Title: S6E1C1 Series 32-bit ARM® Cortex®-M0+ FM0+ Microcontroller  
 Document Number: 002-00234

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4896074	TEKA	08/31/2015	New Spec.
*A	4955136	TEKA	10/9/2015	AC/DC characteristics updated. Typo fixed in "List of Pin Functions".
*B	5158709	YUKT	03/04/2016	Added the frequency value of "Ta = - 10°C to + 105°C" on "11.4.3 Built-in CR Oscillation Characteristics". Added the remark of "VCC < 0.2V" on "11.4.7 Power-on Reset Timing". Added the measure condition(*9) of ICC on "11.3.1 Current Rating". Changed the package outlines to cypress format on "13. Package Dimensions". Changed the package codes to cypress codes on "3. Pin Assignment" and "12. Ordering Information".
*C	5760029	MBGR	06/01/2017	Consolidated the S6E1C datasheets in a single specification 002-00233, Rev. *D.

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