THE DATASHEET OF

S80C51RA24

ADVANCE INFORMATION

8XC51RA/RB/RC
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C51RA/83C51RA/80C51RA/87C51RB/83C51RB/87C51RC/83C51RC

*See Table 1 for Proliferation Options

- **High Performance CHMOS EPROM/ ROM/CPU**
- **24 MHz Operation**
- **512 Bytes of On-Chip Data RAM**
- **Dedicated Hardware Watchdog Timer (One-Time Enabled with Reset-Out)**
- **Three 16-Bit Timer/Counters**
- **Programmable Clock Out**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **8K/16K/32K On-Chip Program Memory**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **6 Interrupt Sources**
- **Programmable Serial Channel with:**
  - **Framing Error Detection**
  - **Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Four-Level Interrupt Priority**
- **Extended Temperature Range (−40°C to +85°C)**

MEMORY ORGANIZATION

ROMless Device	ROM Device	EPROM Version	ROM/EPROM Bytes	RAM Bytes
80C51RA	83C51RA	87C51RA	8K	512
80C51RA	83C51RB	87C51RB	16K	512
80C51RA	83C51RC	87C51RC	32K	512

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XC51RA/8XC51RB/8XC51RC is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS 51 family of controllers, the 8XC51RA/8XC51RB/8XC51RC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 family of products. The 8XC51RA/8XC51RB/8XC51RC is an enhanced version of the 8XC52/8XC54/8XC58. The added features make it an even more powerful microcontroller for applications that require 512 bytes of on-chip data RAM and dedicated hardware WatchDog Timer with reset-out features.

Throughout this document 8XC51RX will refer to the 8XC51RA, 8XC51RB and 8XC51RC unless information applies to a specific device.

For a detailed description of 8XC51RA/RB/RC, refer to the 8XC51RA/RB/RC Hardware Description, order number 272668.

December 1995 **Order Number: 272659-002**

Table 1. Proliferations Options

	Standard*1	-1	-20	-24
80C51RA	X	X	X	X
83C51RA	X	X	X	X
87C51RA	X	X	X	X
83C51RB	X	X	X	X
87C51RB	X	X	X	X
83C51RC	X	X	X	X
87C51RC	X	X	X	X

NOTES:
*1 3.5 MHz to 12 MHz; 5V ±20%
-1 3.5 MHz to 16 MHz; 5V ±20%
-20 3.5 MHz to 20 MHz; 5V ±20%
-24 3.5 MHz to 24 MHz; 5V ±10%

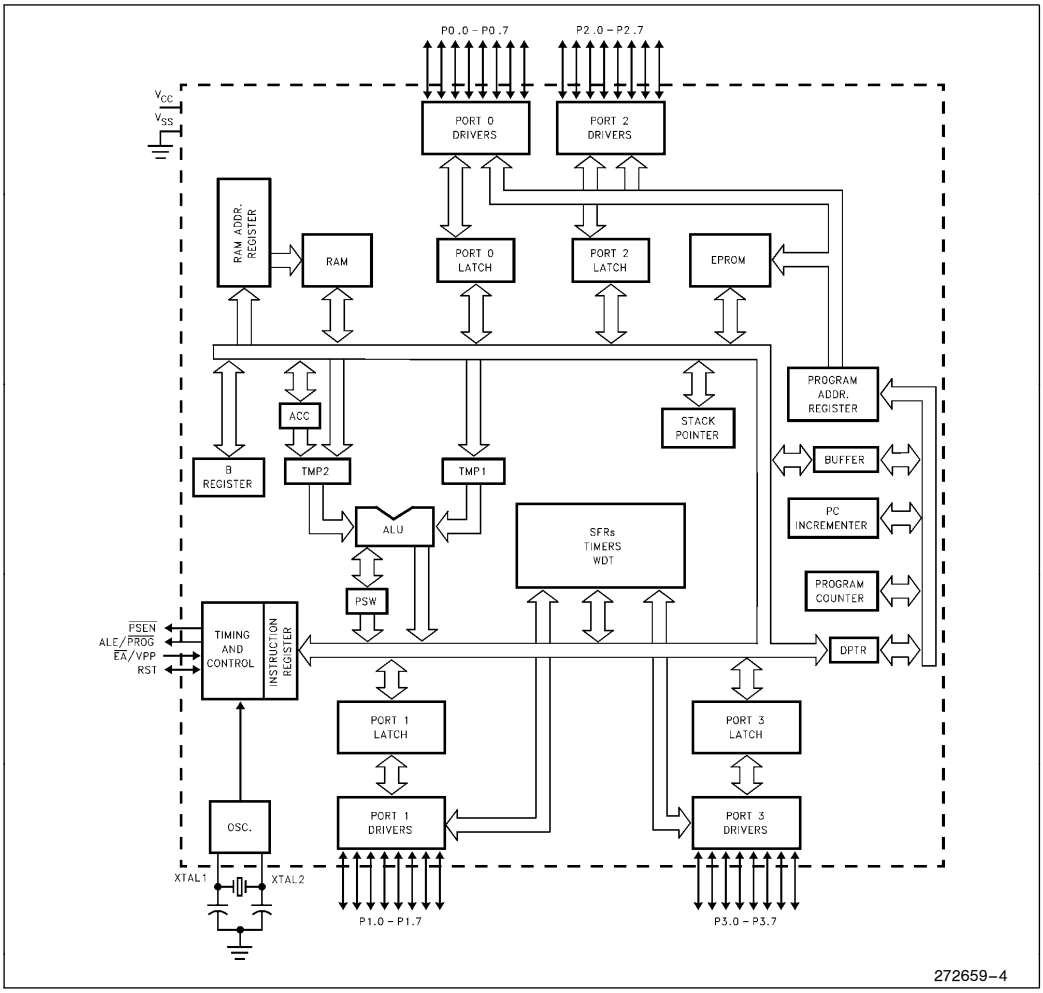


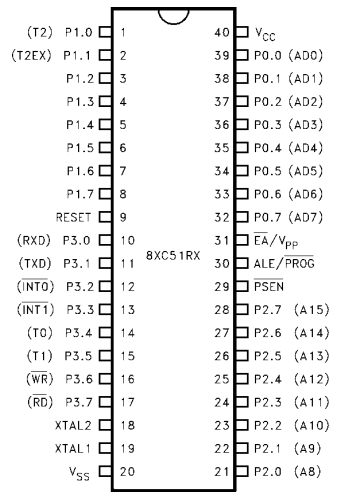
Figure 1. 8XC51RX Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.5, a CHMOS III-E process. Additional process and reliability information is available in the *Intel® Quality System Handbook*.

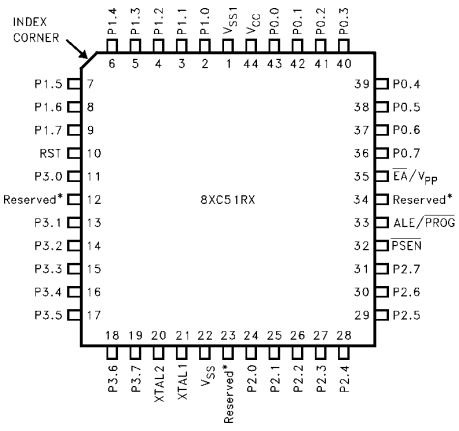
PACKAGES

Part	Prefix	Package Type
8XC51RX	P	40-Pin Plastic DIP (OTP)
8XC51RX	N	44-Pin PLCC (OTP)
8XC51RX	S	44-Pin QFP (OTP)



272659-1

DIP



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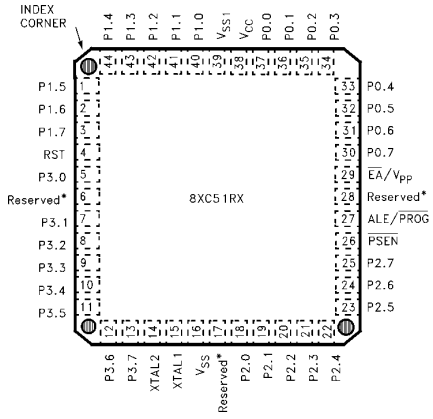
PLCC



272659-3

*Do not connect reserved pins.

QFP

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22). (Connection not necessary for proper operation.)

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51RX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset I/O. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}. After a WatchDog Timer overflow, this RST pin will drive an output high pulse at a minimum V_{OH2} for 96 x T_{OSC} duration while the internal reset signal is active.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to ex-

ternal memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51RX.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51RX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

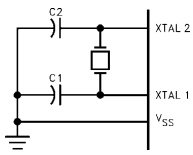
This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, ''Oscillators for Microcontrollers'', Order No. 230659.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

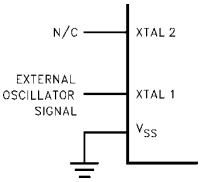


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51RX either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level, and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DEDICATED HARDWARE WATCHDOG TIMER (One-Time Enabled with Reset-Out)

The 8XC51RX contains a dedicated WatchDog Timer (WDT) to allow recovery from software or hardware upset. WDT is disabled upon power-up. To enable the WDT, user must write 1EH and E1H in sequence to WDTRST Special Function Register. Once the WDT is enabled, the 14-bit counter will increment every machine cycle. While the oscillator is running, the WDT will be incrementing and cannot be disabled. The counter is reset by writing 1EH and E1H in sequence to the WDTRST. If the counter is not reset before it reaches 3FFFH (16383D), the chip will be forced into reset sequence and the WDT will be disabled as upon power-up. During this reset, the chip will drive an output Reset-High pulse for the duration of 96 x T_{OSC} at the RST pin. The duration of the Reset-High pulse works out to 6.00 μs @ 16 MHz.

While in the Idle mode the WDT continues to count. If the user does not wish to exit the Idle mode with a reset, then the processor must periodically ''woken up'' to service the WDT. In Power Down mode, the WDT stops counting and holds its current value.

DESIGN CONSIDERATION

- The window on the D87C51RX must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may be functionally impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, (Order No. 270645) and Application Note AP-252 (Embedded Applications Handbook, Order No. 270648), ''Designing with the 80C51BH.''

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the 8XC51RX without the 8XC51RX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51RX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

8XC51RX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS 51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
N	PLCC	Commercial	No
S	QFP	Commercial	No
TP	Plastic	Extended	No
TN	PLCC	Extended	No
TS	QFP	Extended	No
LP	Plastic	Extended	Yes
LN	PLCC	Extended	Yes
LS	QFP	Extended	Yes

NOTE:
Contact distributor or local sales office to match EXPRESS prefix with proper device.

EXAMPLES:
P80C51RA indicates 80C51RA in a plastic package and specified for commercial temperature range, without burn-in. TS87C51RC indicates 87C51RC in a QFP package and specified for extended temperature range, without burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage			
	All Others	4.0	6.0	V
	8XC51RX-24	4.5	5.5	V
f_{OSC}	0scillator Frequency			
	8XC51RX	3.5	12	MHz
	8XC51RX-1	3.5	16	MHz
	8XC51RX-20	3.5	20	MHz
	8XC51RX-24	3.5	24	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

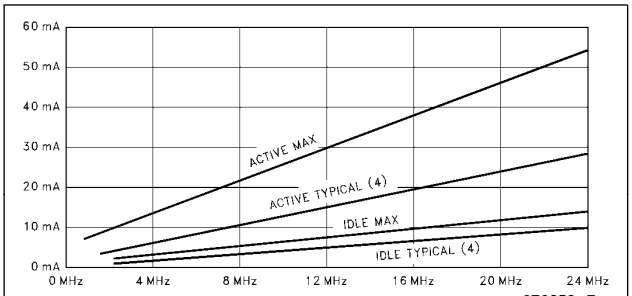
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC}-0.3$			V	$I_{OH} = -200\ \mu A$
		$V_{CC}-0.7$			V	$I_{OH} = -3.2$ mA
		$V_{CC}-1.5$			V	$I_{OH} = -7.0$ mA
V_{OH2}	Output High Voltage (RST)	0.5 V_{CC}			V	$I_{OH} = -800\ \mu A$
		0.75 V_{CC}			V	$I_{OH} = -300\ \mu A$
		0.9 V_{CC}			V	$I_{OH} = -80\ \mu A$
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	$V_{IN} = 0.45V$
I_{LI}	Input leakage Current (Port 0)			±10	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Commercial Express			 −675 −775	 μA μA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Active Mode at 12 MHz (Figure 5) at 16 MHz at 20 MHz at 24 MHz Idle Mode at 12 MHz (Figure 5) at 16 MHz at 20 MHz at 24 MHz Power Down Mode		 15 5 5	 30 38 47 56 7.5 9.5 11.5 13.5 75	 mA mA mA mA mA mA mA mA μA	(Note 3)

NOTES:

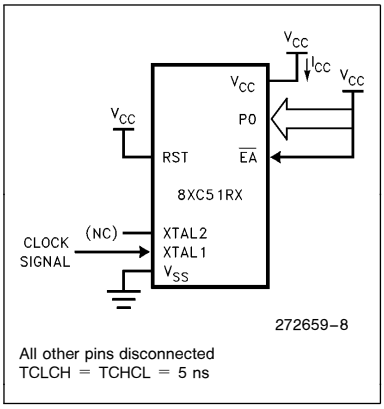
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



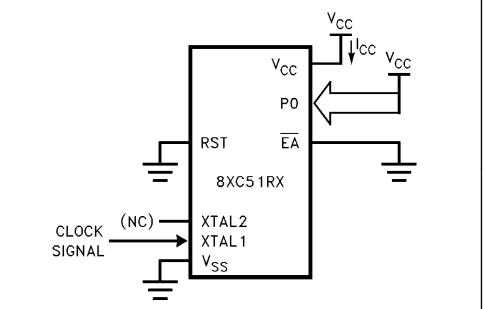
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = 2.2 × Freq + 3.1
Idle Mode
I_{CC} Max = 0.5 × Freq + 1.5
Where Freq is in MHz, I_{CC} Max is given in mA.

Figure 5. I_{CC} vs Frequency



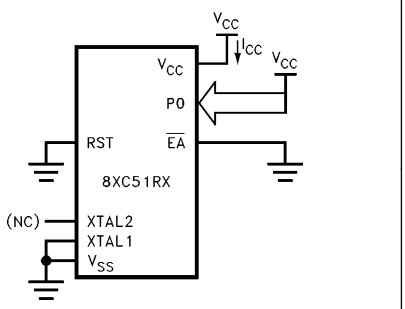
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

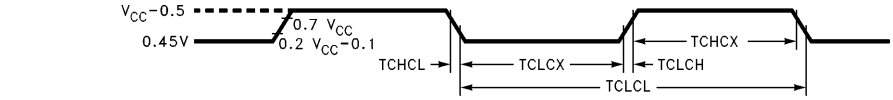


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XC51RX refers to 8XC51RX and 8XC51RX-1. 8XC51RX-24 refers to 8XC51RX-20 and 8XC51RX-24.

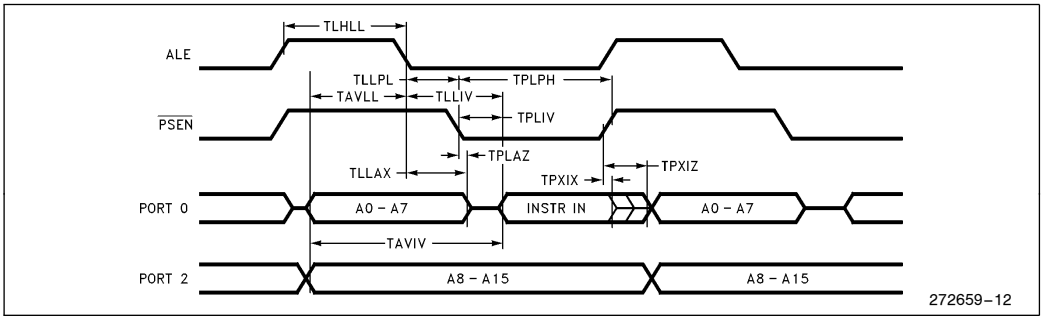
Symbol	Description	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XC51RX 8XC51RX-1 8XC51RX-20 8XC51RX-24							 3.5 3.5 3.5 3.5	 12 16 20 24	 MHz MHz MHz MHz
TLHLL	ALE Pulse Width	127		60		43		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		10		12		TCLCL − 40		ns
TLLAX	Address Hold After ALE Low	53		20		12		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instruction In 8XC51RX 8XC51RX-24		 234		 125		 91		 4 TCLCL − 100 4 TCLCL − 75	 ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		20		12		TCLCL − 30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		105		80		3 TCLCL − 45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In 8XC51RX 8XC51RX-24		 145		 60		 35		 3 TCLCL − 105 3 TCLCL − 90	 ns ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

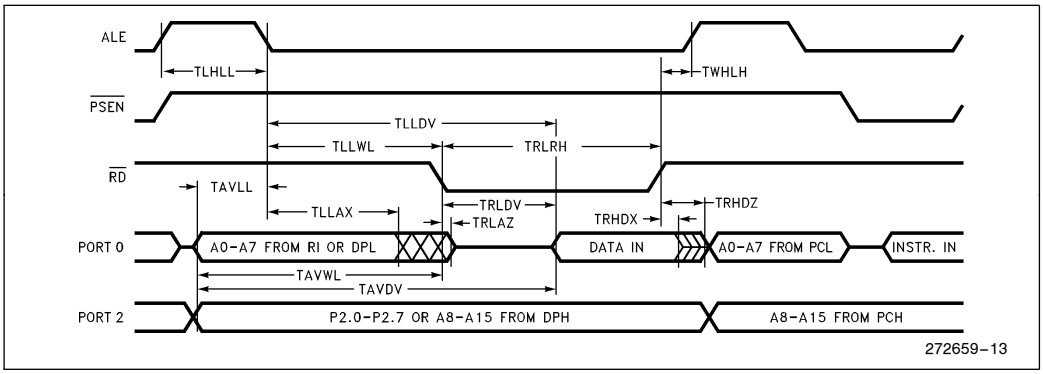
All parameter values apply to all devices unless otherwise indicated.

Symbol	Description	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instruction Float After $\overline{PSEN}$ 8XC51RX 8XC51RX-24		59		30		21		TCLCL−25 TCLCL−20	ns ns
TAVIV	Address to Valid Instruction In		312		145		103		5 TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		200		150		6 TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		200		150		6 TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In 8XC51RX 8XC51RX-24		252		155		113		5 TCLCL−165 5 TCLCL−95	ns ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		40		23		2 TCLCL−60	ns
TLLDV	ALE Low to Valid Data In 8XC51RX 8XC51RX-24		517		310		243		8 TCLCL−150 8 TCLCL−90	ns ns
TAVDV	Address to Valid Data In 8XC51RX 8XC51RX-24		585		360		285		9 TCLCL−165 9 TCLCL−90	ns ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	100	200	75	175	3 TCLCL−50	3 TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low 8XC51RX 8XC51RX-24	203		110		77		4 TCLCL−130 4 TCLCL−90		ns ns
TQVWX	Data Valid before $\overline{WR}$ 8XC51RX 8XC51RX-20 8XC51RX-24	33		15		12		TCLCL−50 TCLCL−35 TCLCL−30		ns ns ns
TWHQX	Data Hold after $\overline{WR}$ 8XC51RX 8XC51RX-20 8XC51RX-24	33		10		7		TCLCL−50 TCLCL−40 TCLCL−30		ns ns ns
TQVWH	Data Valid to $\overline{WR}$ High 8XC51RX 8XC51RX-24	433		280		222		7 TCLCL−150 7 TCLCL−70		ns ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 8XC51RX 8XC51RX-24	43	123	10	90	12	71	TCLCL−40 TCLCL−30	TCLCL+40 TCLCL+30	ns

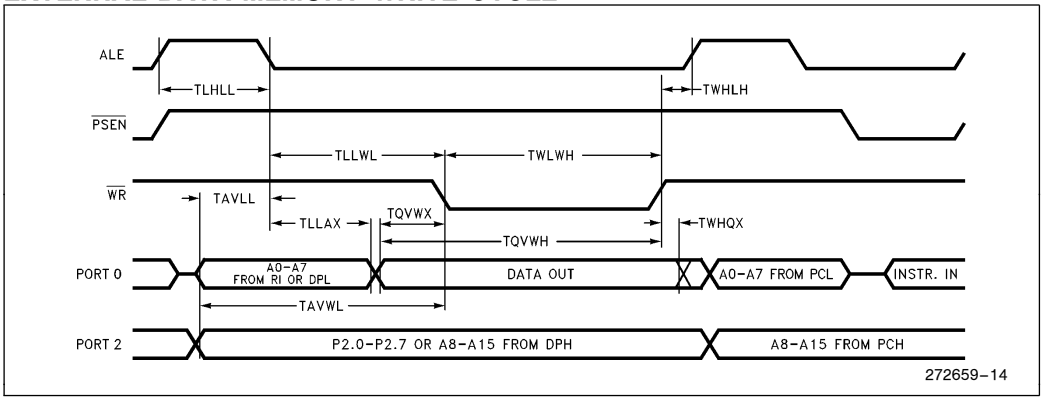
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

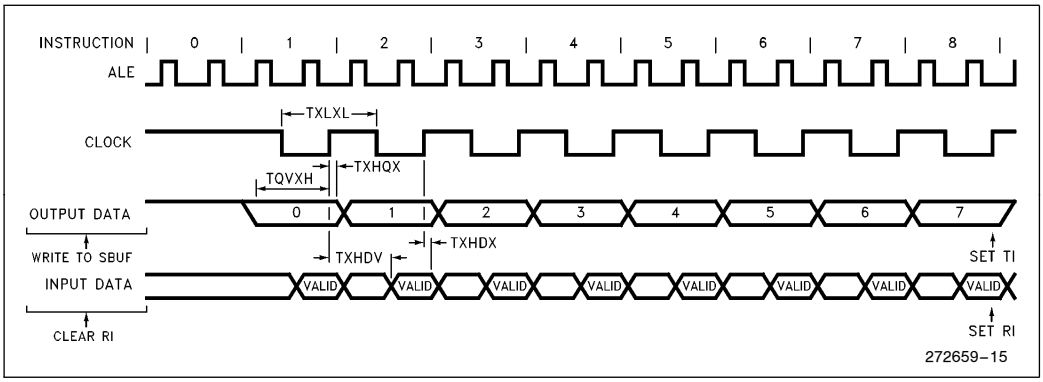


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.600		0.500		12 TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		367			284	10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge									
	8XC51RX	50						2 TCLCL − 117		ns
	8XC51RX-24			50		34		2 TCLCL − 50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		367		284		10 TCLCL − 133	ns

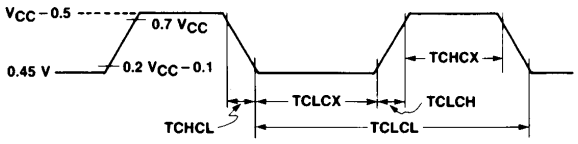
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

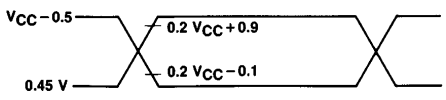
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC51RX 8XC51RX-1 8XC51RX-20 8XC51RX-24	 3.5 3.5 3.5 3.5	 12 16 20 24	MHz
TCHCX	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCX	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCH	Rise Time 8XC51RX 8XC51RX-24		 20 10	 ns ns
TCHCL	Fall Time20 8XC51RX 8XC51RX-24		 20 10	ns ns ns

EXTERNAL CLOCK DRIVE WAVEFORM



272659–16

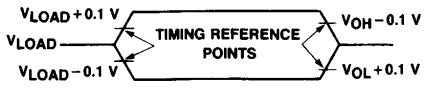
AC TESTING INPUT, OUTPUT WAVEFORMS



272659–17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272659–18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 4. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTES:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

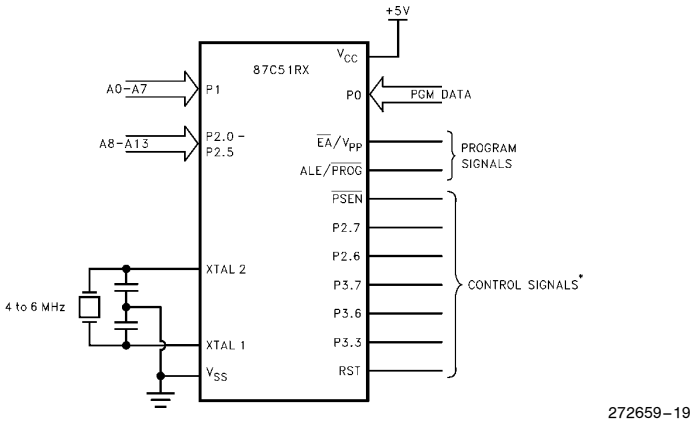
DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51RX the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51RX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

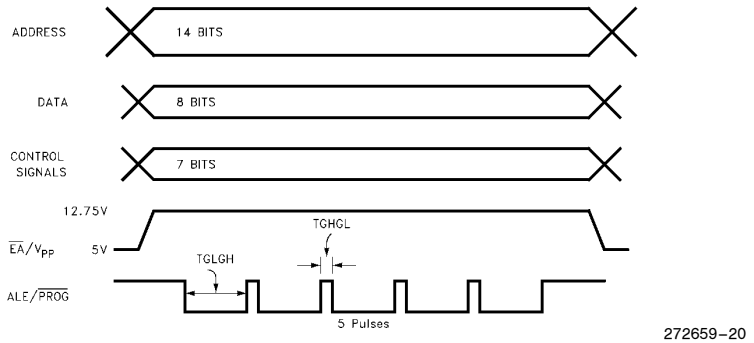


Figure 11. Programming Signal's Waveforms

ROM and EPROM Lock System

The program lock system, when programmed, protects the onboard program against software piracy.

The 83C51RX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 5. If program protection is desired. the user submits the encryption table with their code. and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51RX has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51RX has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

If any program lock bits were programmed, erasing the EPROM will not erase the program lock bits and programming of the EPROM is disabled.

Reading the Signature Bytes

The 8XC51RX has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	87C51RC	C2H
	87C51RB	C1H
	87C51RA	C0H
	83C51RC	42H/C2H
	83C51RB	41H/C1H
	83C51RA	40H/C0H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 5. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

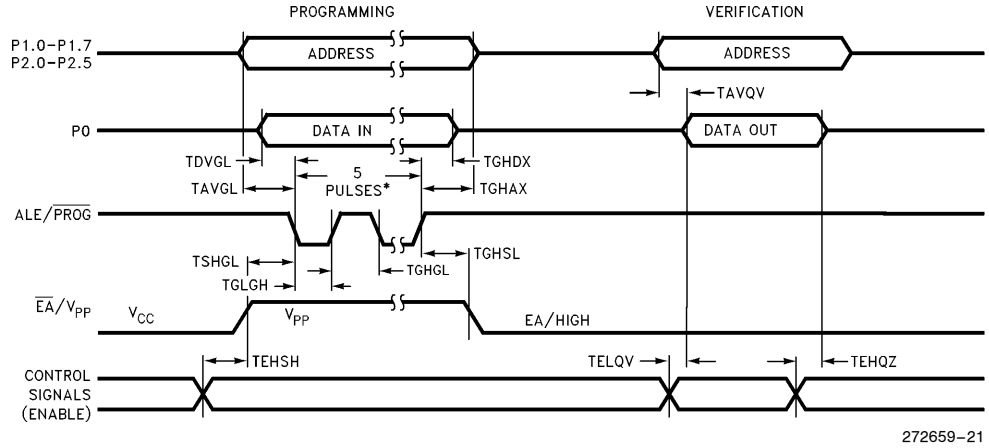
NOTE:
Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order Number 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	All
N	46°C/W	16°C/W	All
S	87°C/W	18°C/W	51RA
	96°C/W	24°C/W	51RB
	90°C/W	22°C/W	51RC

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272659-002) and the previous version (272659-001):

1. ADVANCE INFORMATION datasheet replaces PRODUCT PREVIEW datasheet.
2. I_{TL} (Commercial) changed from -650 μA to -675 μA.
3. I_{TL} (Express) changed from -750 μA to -775 μA.
4. 8XC51RX-24, V_{CC} changed from 5V $\pm$20% to 5V $\pm$10%.
5. Remove all CERDIP package types (prefix D, TD, LD).

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