



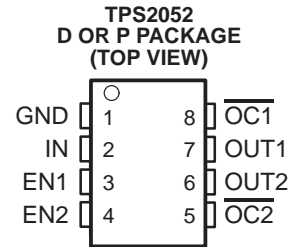
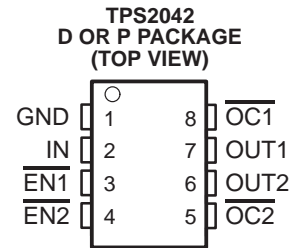
**THE DATASHEET OF
STR755FV1H6**



TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

- 135-m Ω -Maximum (5-V Input) High-Side MOSFET Switch
- 500 mA Continuous Current per Channel
- Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 μ A Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, -40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection
- UL Listed – File No. E169910



description

The TPS2042 and TPS2052 dual power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2042 and the TPS2052 incorporate in single packages two 135-m Ω N-channel MOSFET high-side power switches for power distribution systems that require multiple power switches. Each switch is controlled by a logic enable that is compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2042 and TPS2052 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{\text{OCx}}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS2042 and TPS2052 are designed to limit at 0.9-A load. These power distribution switches are available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP) and operate over an ambient temperature range of -40°C to 85°C .

AVAILABLE OPTIONS

| T _A | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A) | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A) | PACKAGED DEVICES | |
|---|-------------|--|--|--------------------------|-------------|
| | | | | SOIC (D) [†] | PDIP (P) |
| -40°C to 85°C | Active low | 0.5 | 0.9 | TPS2042D | TPS2042P |
| -40°C to 85°C | Active high | 0.5 | 0.9 | TPS2052D | TPS2052P |

[†] The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2042DR)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

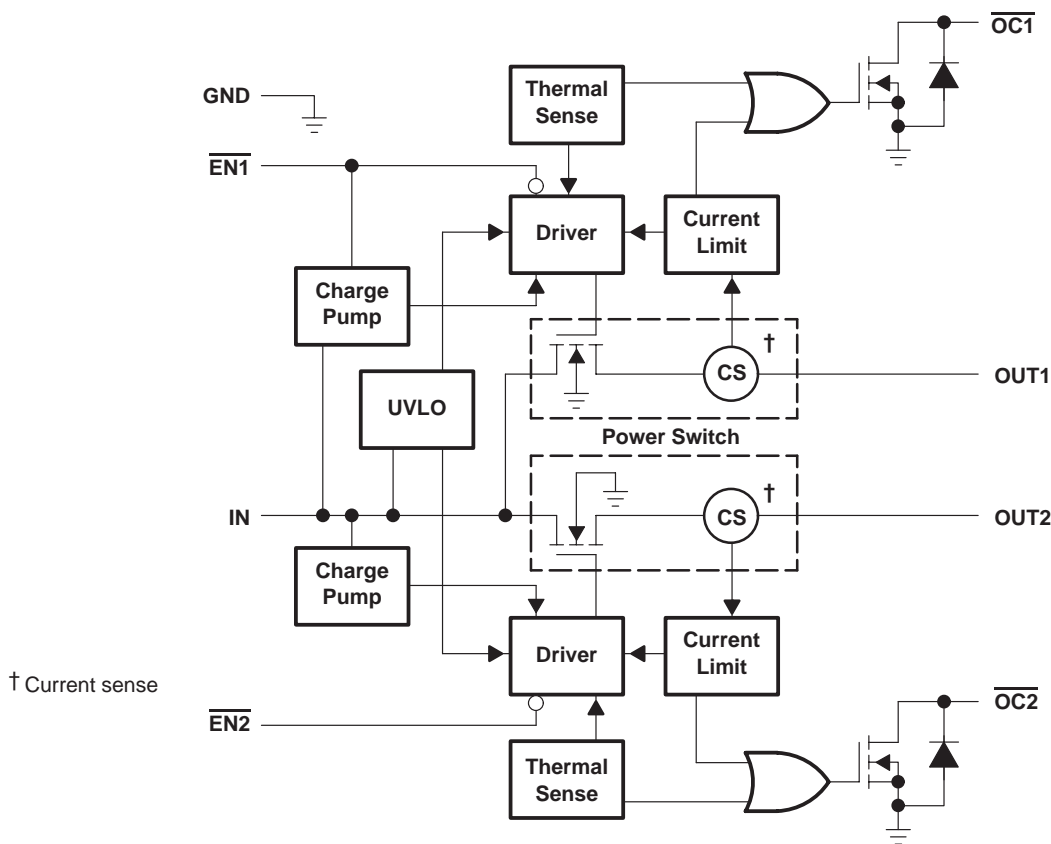
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TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

TPS2042 functional block diagram



Terminal Functions

| NAME | TERMINAL NO. | | I/O | DESCRIPTION |
|------|--------------|---------|-----|--|
| | D OR P | | | |
| | TPS2042 | TPS2052 | | |
| EN1 | 3 | – | I | Enable input. Logic low turns on power switch, IN-OUT1. |
| EN2 | 4 | – | I | Enable input. Logic low turns on power switch, IN-OUT2. |
| EN1 | – | 3 | I | Enable input. Logic high turns on power switch, IN-OUT1. |
| EN2 | – | 4 | I | Enable input. Logic high turns on power switch, IN-OUT2. |
| GND | 1 | 1 | I | Ground |
| IN | 2 | 2 | I | Input voltage |
| OC1 | 8 | 8 | O | Over current. Logic output active low, for power switch, IN-OUT1 |
| OC2 | 5 | 5 | O | Over current. Logic output active low, for power switch, IN-OUT2 |
| OUT1 | 7 | 7 | O | Power-switch output |
| OUT2 | 6 | 6 | O | Power-switch output |

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 m Ω ($V_{I(IN)} = 5$ V). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable (\overline{ENx} or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μ A when a logic high is present on \overline{ENx} (TPS2042) or a logic low is present on ENx (TPS2052). A logic zero input on \overline{ENx} or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent (\overline{OCx})

The \overline{OCx} open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2042 and TPS2052 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The (\overline{OCx}) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

TPS2042, TPS2052

DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-------------------------------|
| Input voltage range, $V_{I(IN)}$ (see Note1) | -0.3 V to 6 V |
| Output voltage range, $V_{O(OUTx)}$ (see Note1) | -0.3 V to $V_{I(IN)} + 0.3$ V |
| Input voltage range, $V_{I(ENx)}$ or $V_{I(ENx)}$ | -0.3 V to 6 V |
| Continuous output current, $I_{O(OUTx)}$ | internally limited |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating virtual junction temperature range, T_J | -40°C to 125°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C | 2 kV |
| Machine model | 0.2 kV |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| P | 1175 mW | 9.4 mW/°C | 752 mW | 611 mW |

recommended operating conditions

| | TPS2042 | | TPS2052 | | UNIT |
|---|---------|-----|---------|-----|------|
| | MIN | MAX | MIN | MAX | |
| Input voltage, $V_{I(IN)}$ | 2.7 | 5.5 | 2.7 | 5.5 | V |
| Input voltage, $V_{I(ENx)}$ or $V_{I(ENx)}$ | 0 | 5.5 | 0 | 5.5 | V |
| Continuous output current, $I_{O(OUTx)}$ | 0 | 500 | 0 | 500 | mA |
| Operating virtual junction temperature, T_J | -40 | 125 | -40 | 125 | °C |



TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $V_{I(ENx)} = 0\text{ V}$, $V_{I(ENx)} = \text{Hi}$ (unless otherwise noted)

power switch

| PARAMETER | | TEST CONDITIONS† | TPS2042 | | | TPS2052 | | | UNIT |
|--------------|--|--|---------|-----|-----|---------|-----|------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation | $V_{I(IN)} = 5\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 80 | 95 | | 80 | 95 | m Ω | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 90 | 120 | | 90 | 120 | | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 100 | 135 | | 100 | 135 | | |
| | Static drain-source on-state resistance, 3.3-V operation | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 85 | 105 | | 85 | 105 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 100 | 135 | | 100 | 135 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 0.5\text{ A}$ | 115 | 150 | | 115 | 150 | | |
| t_r | Rise time, output | $V_{I(IN)} = 5.5\text{ V}$, $T_J = 25^\circ\text{C}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | 2.5 | | | 2.5 | | ms | |
| | | $V_{I(IN)} = 2.7\text{ V}$, $T_J = 25^\circ\text{C}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | 3 | | | 3 | | | |
| t_f | Fall time, output | $V_{I(IN)} = 5.5\text{ V}$, $T_J = 25^\circ\text{C}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | 4.4 | | | 4.4 | | ms | |
| | | $V_{I(IN)} = 2.7\text{ V}$, $T_J = 25^\circ\text{C}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | 2.5 | | | 2.5 | | | |

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input \overline{ENx} or ENx

| PARAMETER | | TEST CONDITIONS | TPS2042 | | | TPS2052 | | | UNIT |
|-----------|--------------------------|---|---------|-----|-----|---------|-----|-----|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IH} | High-level input voltage | $2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$ | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | $4.5\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$ | | | 0.8 | | | 0.8 | V |
| | | $2.7\text{ V} \leq V_{I(IN)} \leq 4.5\text{ V}$ | | | 0.4 | | | 0.4 | |
| I_I | Input current | TPS2042 $V_{I(ENx)} = 0\text{ V}$ or $V_{I(ENx)} = V_{I(IN)}$ | -0.5 | | 0.5 | | | | μA |
| | | TPS2052 $V_{I(ENx)} = V_{I(IN)}$ or $V_{I(ENx)} = 0\text{ V}$ | | | | -0.5 | | 0.5 | |
| t_{on} | Turnon time | $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | | 20 | | | 20 | ms |
| t_{off} | Turnoff time | $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | | 40 | | | 40 | ms |

current limit

| PARAMETER | | TEST CONDITIONS† | TPS2042 | | | TPS2052 | | | UNIT |
|-----------|------------------------------|--|---------|-----|-----|---------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{OS} | Short-circuit output current | $V_{I(IN)} = 5\text{ V}$, OUT connected to GND, Device enable into short circuit | 0.7 | 0.9 | 1.1 | 0.7 | 0.9 | 1.1 | A |

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.



TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $V_{I(ENx)} = 0\text{ V}$, $V_{I(ENx)} = \text{Hi}$ (unless otherwise noted) (continued)

supply current

| PARAMETER | TEST CONDITIONS | | | TPS2042 | | | TPS2052 | | | UNIT |
|-----------------------------------|-------------------------------------|---|---|---------|-------|-----|---------|---------------|---------------|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Supply current, low-level output | No Load on OUT | $\overline{V_{I(ENx)}} = V_{I(IN)}$ | $T_J = 25^\circ\text{C}$ | TPS2042 | 0.015 | 1 | | | μA | |
| | | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | | 10 | | | | |
| | $V_{I(ENx)} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | TPS2052 | | 0.015 | 1 | | | | |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | | | 10 | | | | |
| Supply current, high-level output | No Load on OUT | $\overline{V_{I(ENx)}} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | TPS2042 | 80 | 100 | | μA | | |
| | | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | | 100 | | | | |
| | $\overline{V_{I(ENx)}} = V_{I(IN)}$ | $T_J = 25^\circ\text{C}$ | TPS2052 | | 80 | 100 | | | | |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | | | 100 | | | | |
| Leakage current | OUT connected to ground | $\overline{V_{I(ENx)}} = V_{I(IN)}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | TPS2042 | 100 | | | μA | | |
| | | $\overline{V_{I(ENx)}} = 0\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | TPS2052 | | 100 | | | | |
| Reverse leakage current | IN = high impedance | $\overline{V_{I(EN)}} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | TPS2042 | 0.3 | | | μA | | |
| | | $\overline{V_{I(EN)}} = \text{Hi}$ | | TPS2052 | | 0.3 | | | | |

undervoltage lockout

| PARAMETER | TEST CONDITIONS | TPS2042 | | | TPS2052 | | | UNIT |
|-------------------------|--------------------------|---------|-----|-----|---------|-----|-----|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Low-level input voltage | | 2 | | 2.5 | 2 | | 2.5 | V |
| Hysteresis | $T_J = 25^\circ\text{C}$ | | 100 | | | 100 | | mV |

overcurrent \overline{OCx}

| PARAMETER | TEST CONDITIONS | TPS2042 | | | TPS2052 | | | UNIT |
|--------------------------------|--|---------|-----|-----|---------|-----|-----|---------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Sink current [†] | $V_O = 5\text{ V}$ | | | 10 | | | 10 | mA |
| Output low voltage | $I_O = 5\text{ mA}$, $\overline{V_{OL(OCx)}}$ | | | 0.5 | | | 0.5 | V |
| Off-state current [†] | $V_O = 5\text{ V}$, $\overline{V_O} = 3.3\text{ V}$ | | | 1 | | | 1 | μA |

[†] Specified by design, not production tested.



PARAMETER MEASUREMENT INFORMATION

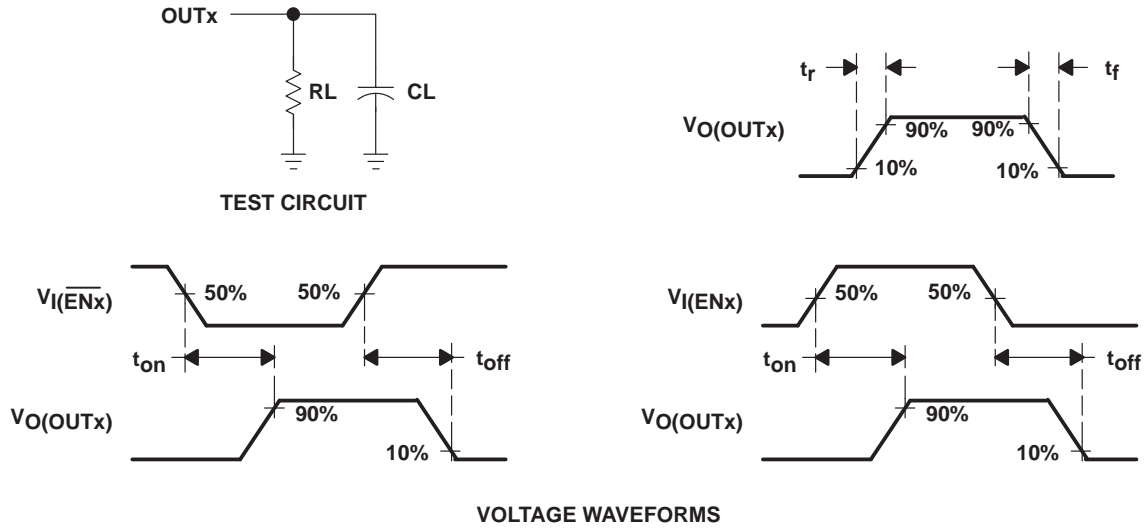


Figure 1. Test Circuit and Voltage Waveforms

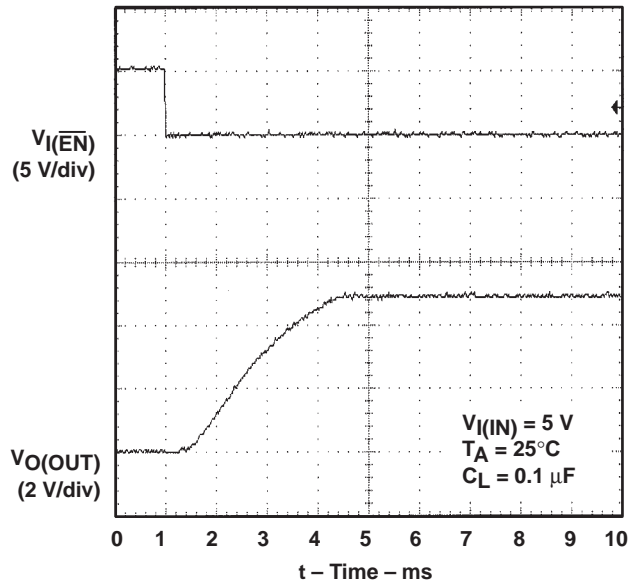


Figure 2. Turnon Delay and Rise Time with 0.1- μF Load

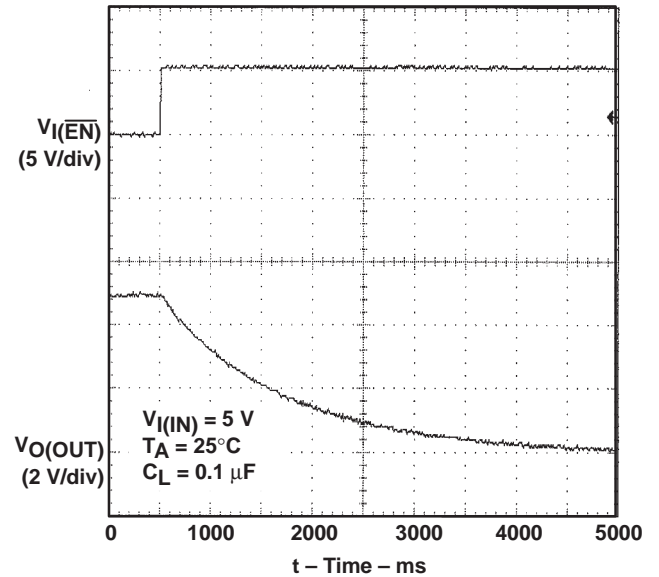


Figure 3. Turnoff Delay and Fall Time with 0.1- μF Load

PARAMETER MEASUREMENT INFORMATION

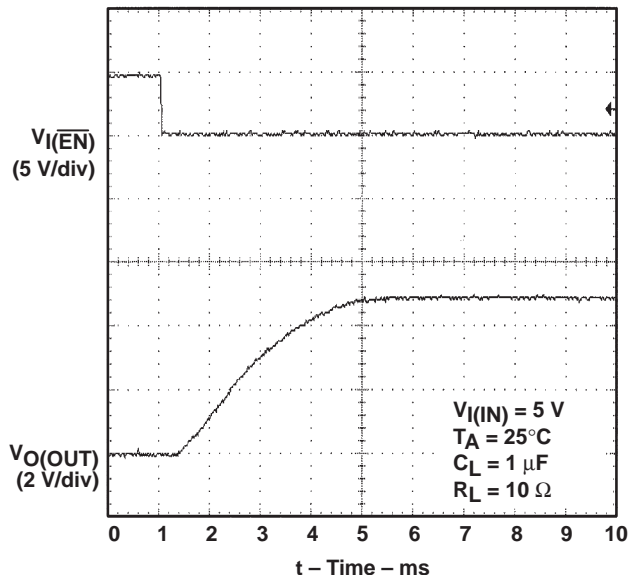


Figure 4. Turnon Delay and Rise Time with 1- μ F Load

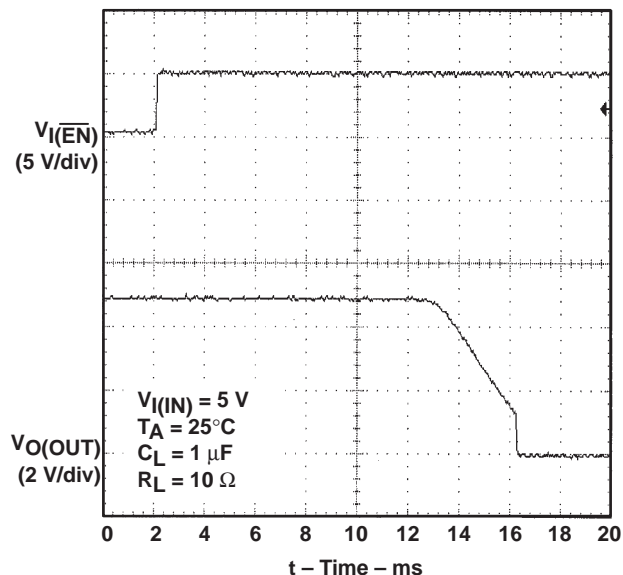


Figure 5. Turnoff Delay and Fall Time with 1- μ F Load

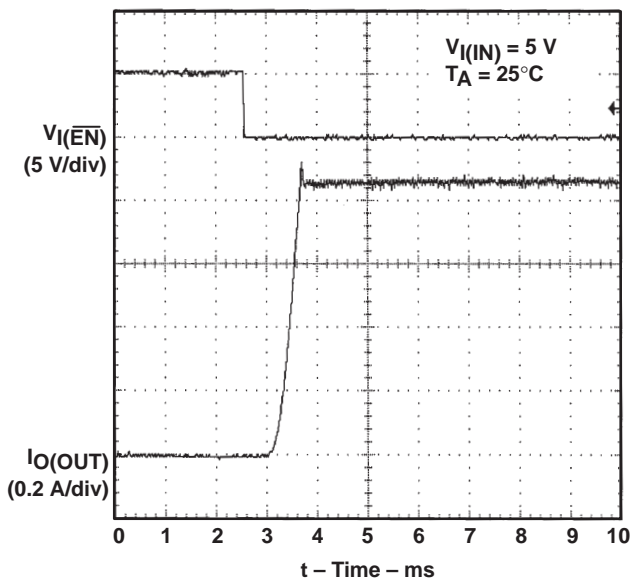


Figure 6. TPS2042, Short-Circuit Current, Device Enabled into Short

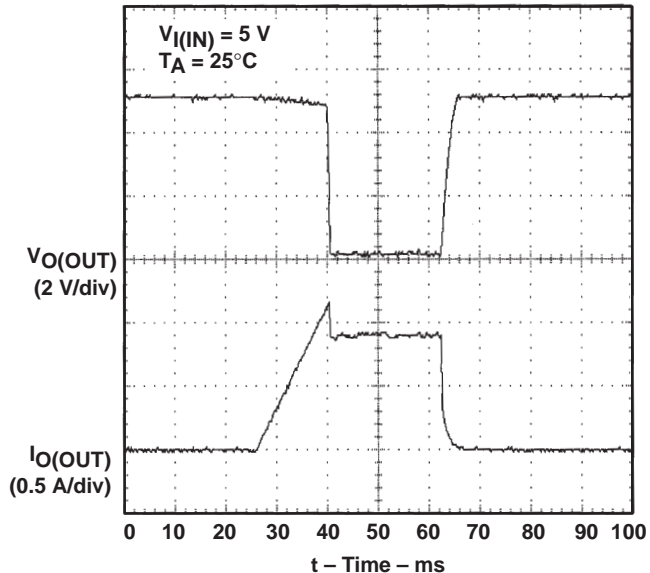


Figure 7. TPS2042, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

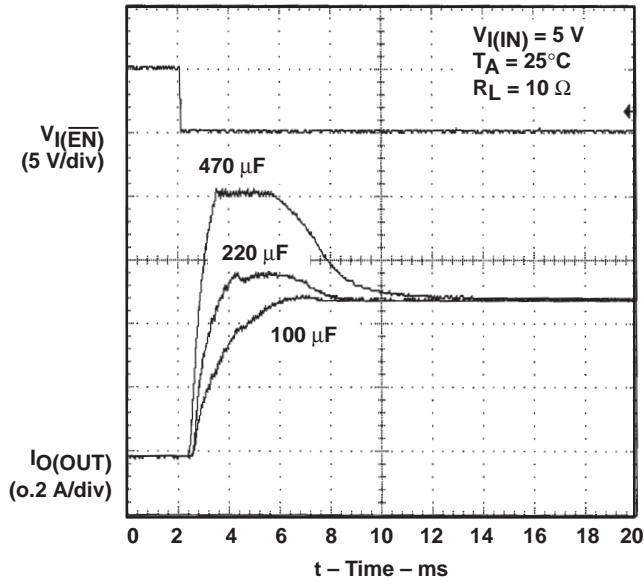


Figure 8. Inrush Current with 100- μ F, 220- μ F and 470- μ F Load Capacitance

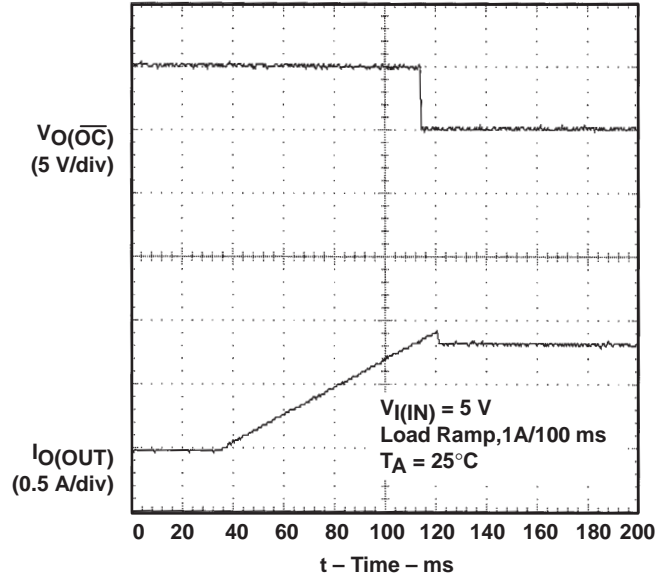


Figure 9. Ramped Load on Enabled Device

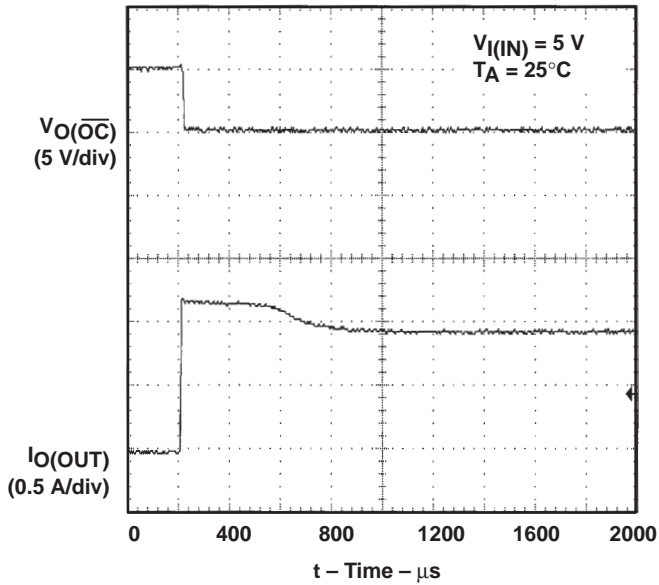


Figure 10. 4- Ω Load Connected to Enabled Device

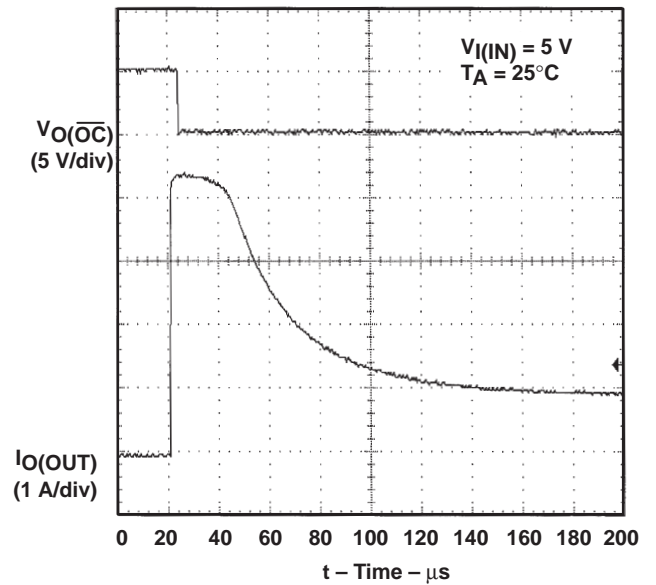


Figure 11. 1- Ω Load Connected to Enabled Device

TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

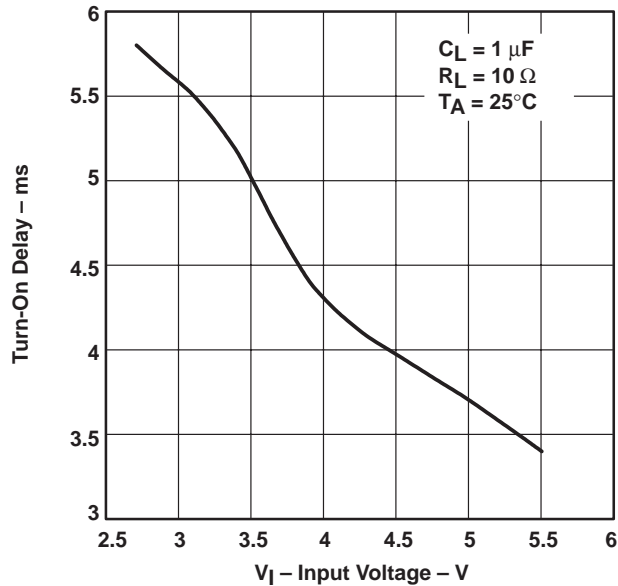


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

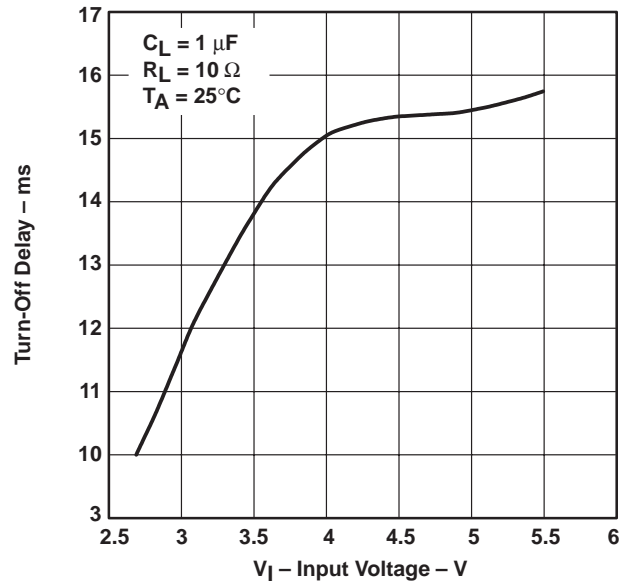


Figure 13

RISE TIME
vs
LOAD CURRENT

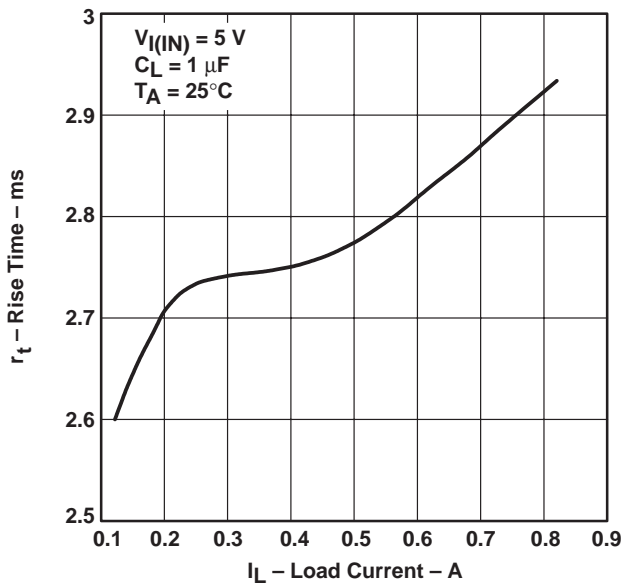


Figure 14

FALL TIME
vs
LOAD CURRENT

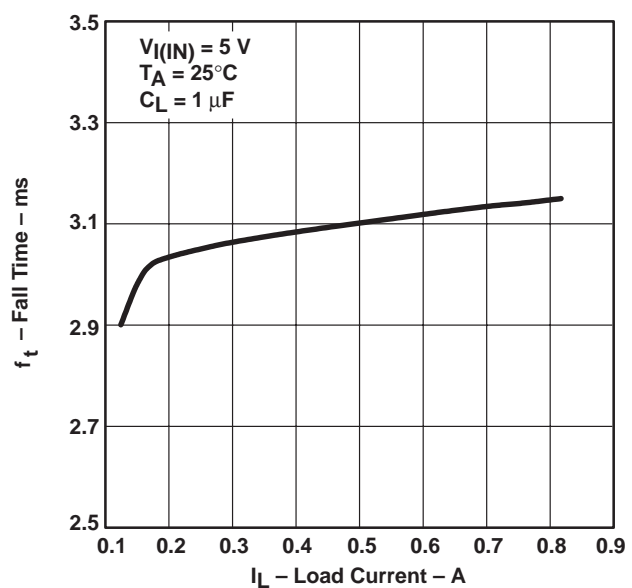
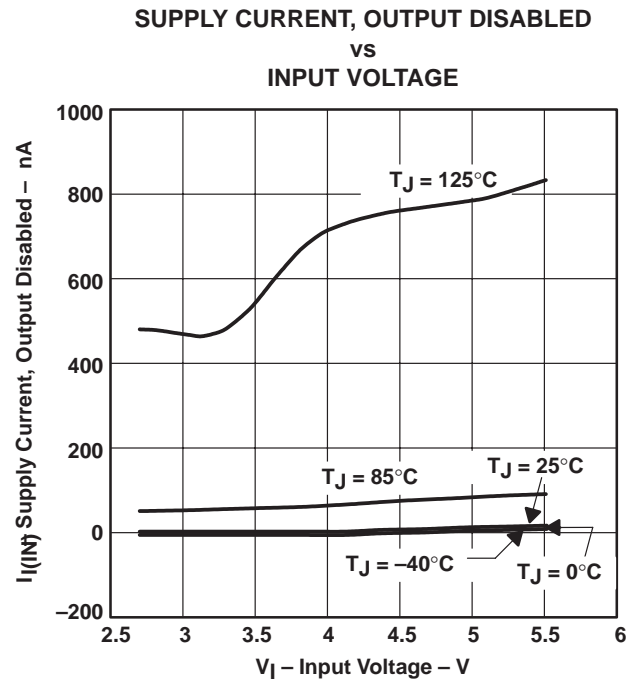
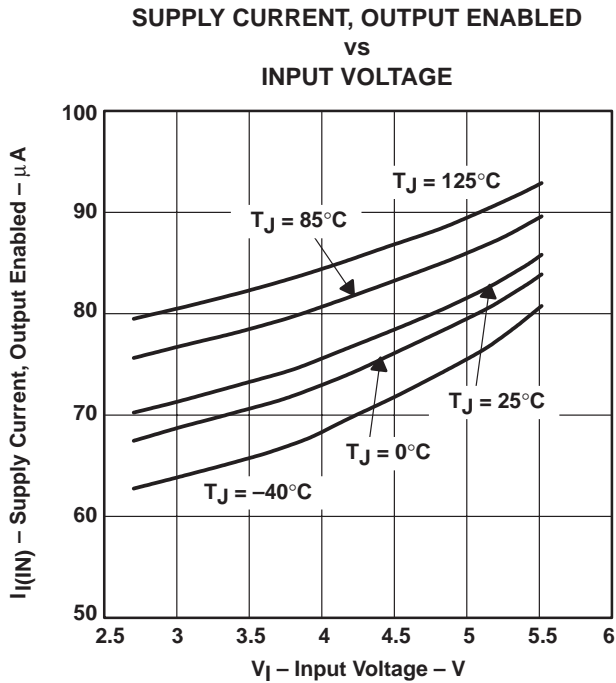
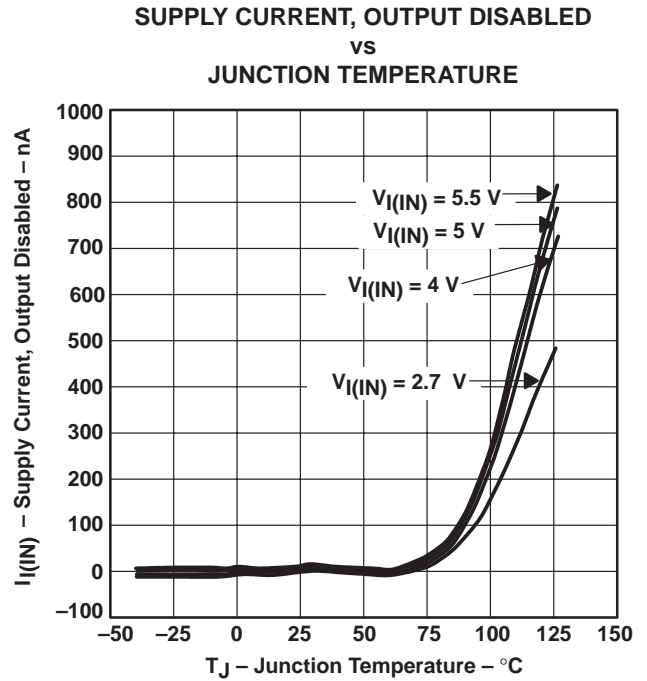
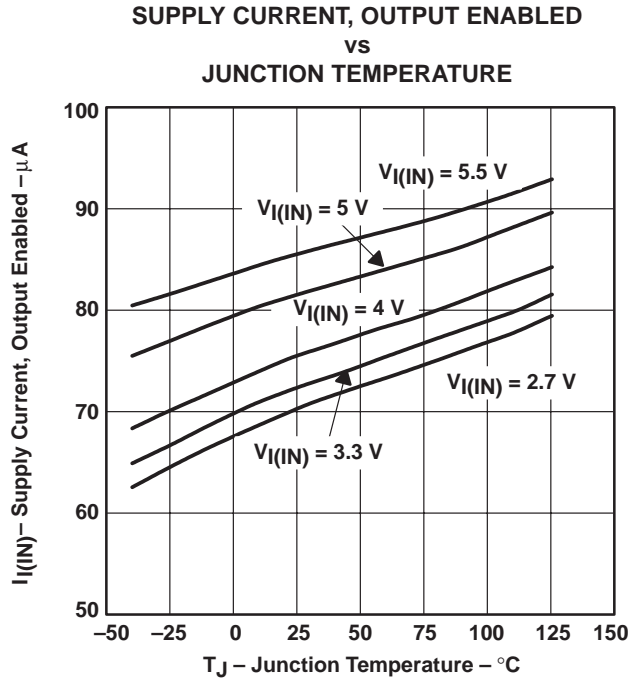


Figure 15

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
 vs
 JUNCTION TEMPERATURE

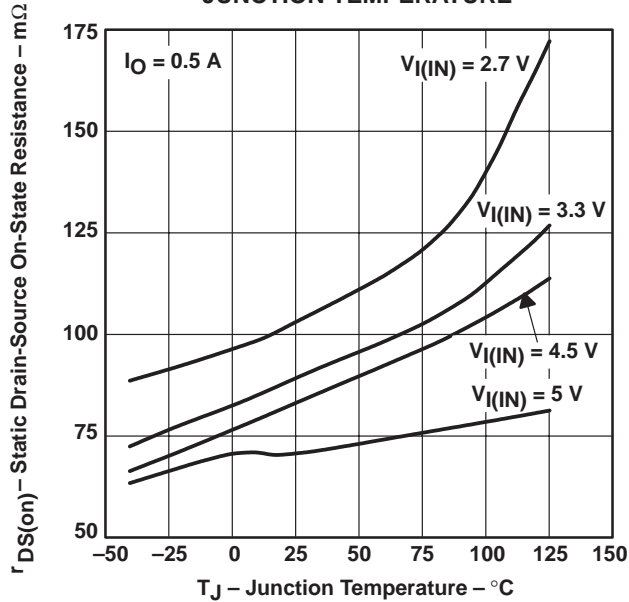


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
 vs
 INPUT VOLTAGE

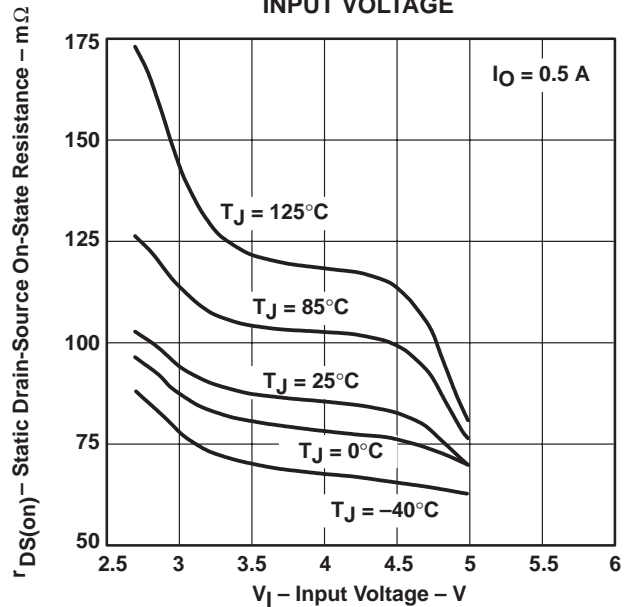


Figure 21

INPUT-TO-OUTPUT VOLTAGE
 vs
 LOAD CURRENT

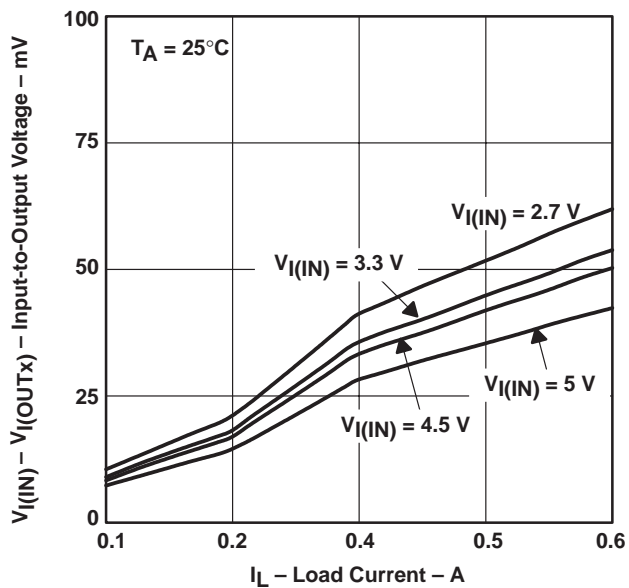


Figure 22

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 INPUT VOLTAGE

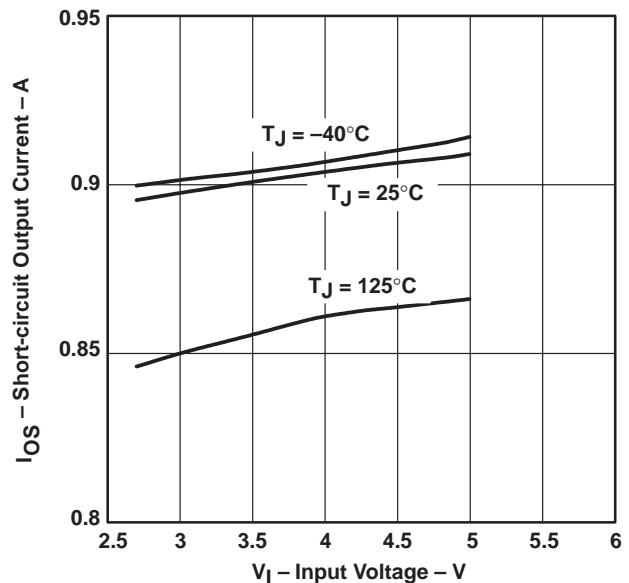
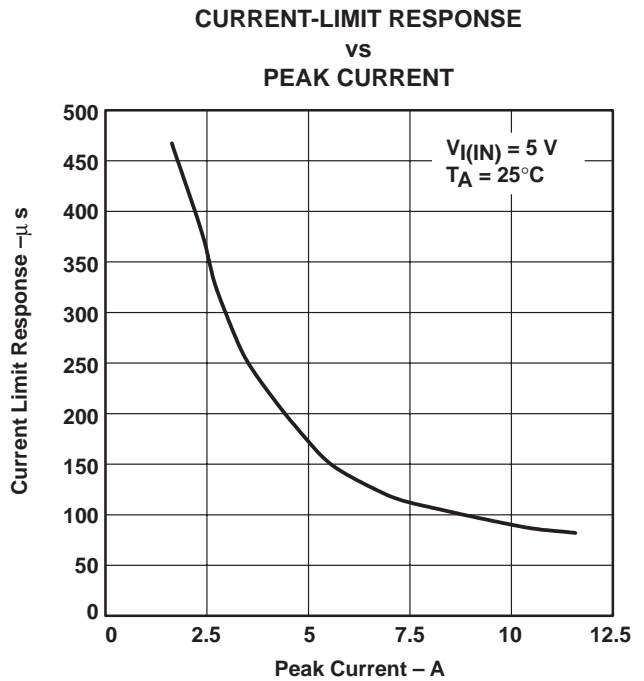
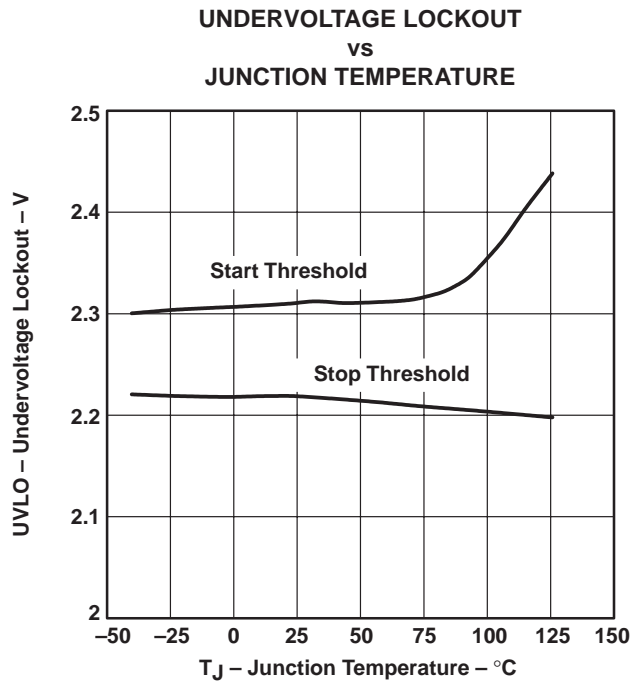
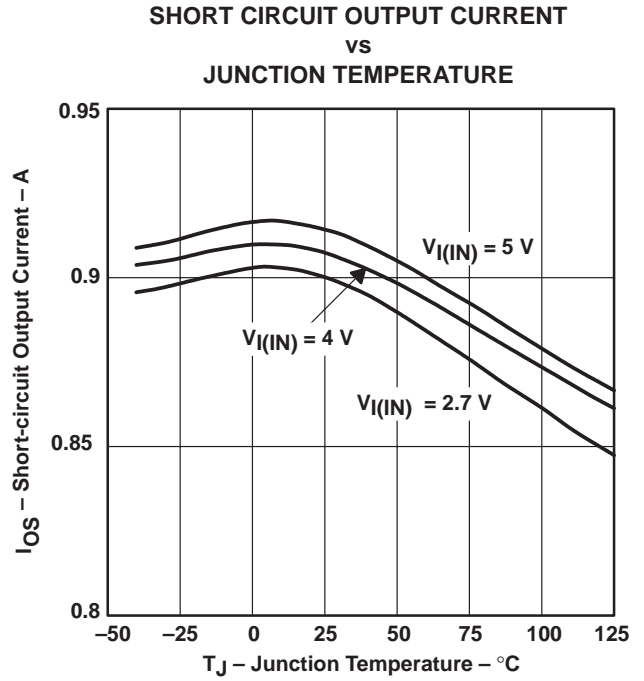
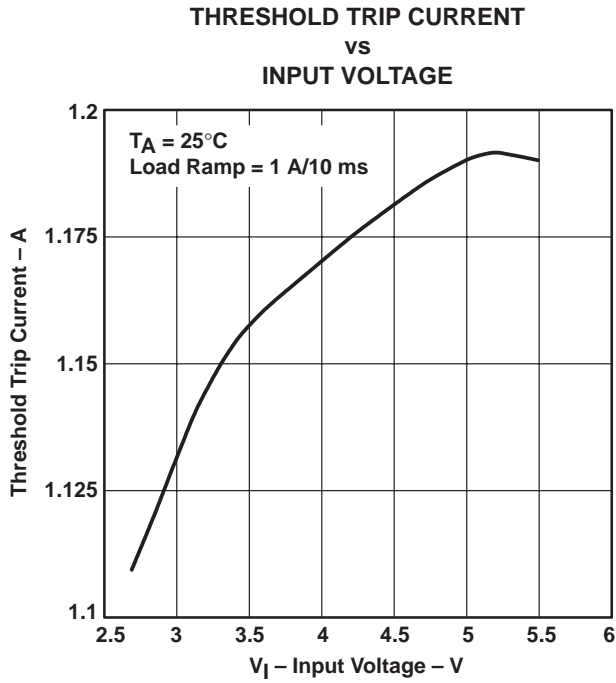


Figure 23

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS
OVERCURRENT RESPONSE TIME (\overline{OCx})
 vs
PEAK CURRENT

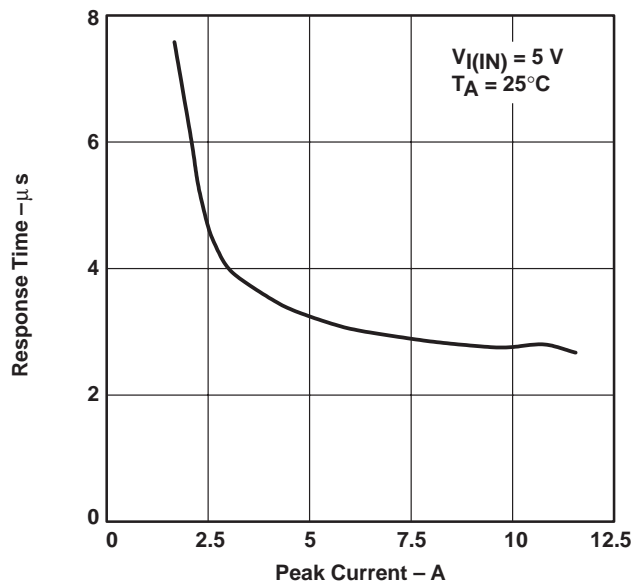


Figure 28

APPLICATION INFORMATION

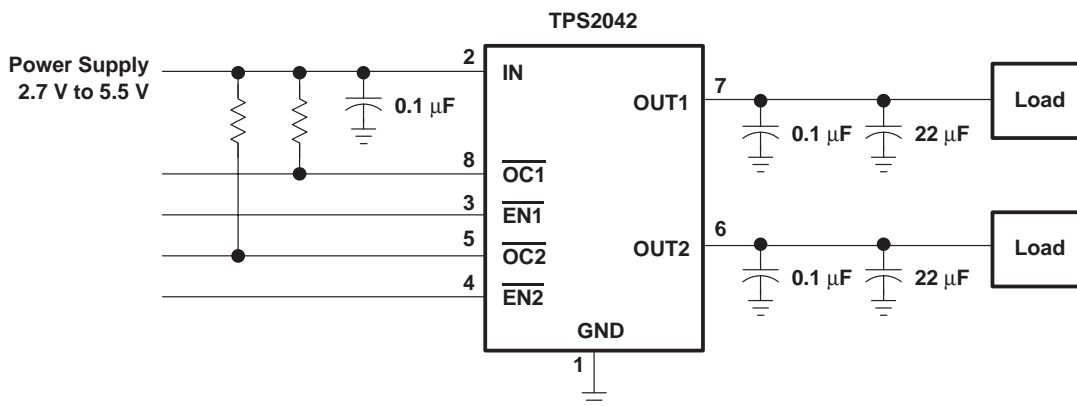


Figure 29. Typical Application

power-supply considerations

A 0.01- μ F to 0.1- μ F ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- μ F to 0.1- μ F ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2042 and TPS2052 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2042 and TPS2052 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

\overline{OC} response

The \overline{OC} open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 μ s (see Figure 30) can be connected to the \overline{OC} pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

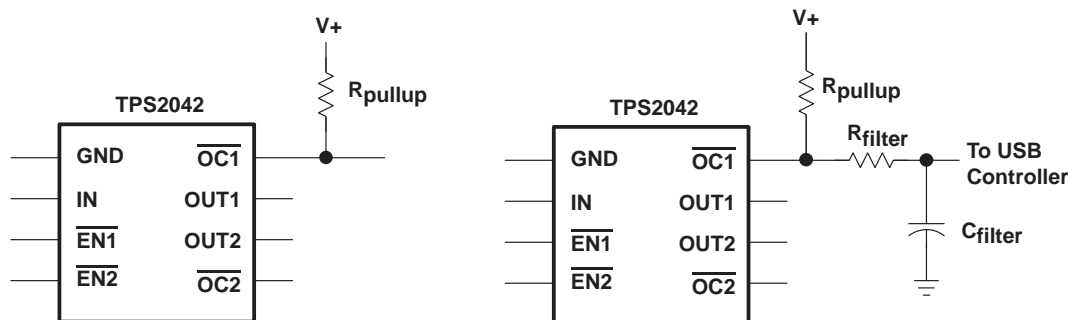


Figure 30. Typical Circuit for \overline{OC} Pin and RC Filter for Damping Inrush \overline{OC} Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2042 and TPS2052 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2042 and TPS2052 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The \overline{OC} open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

host/self-powered and bus-powered hubs (continued)

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 32).

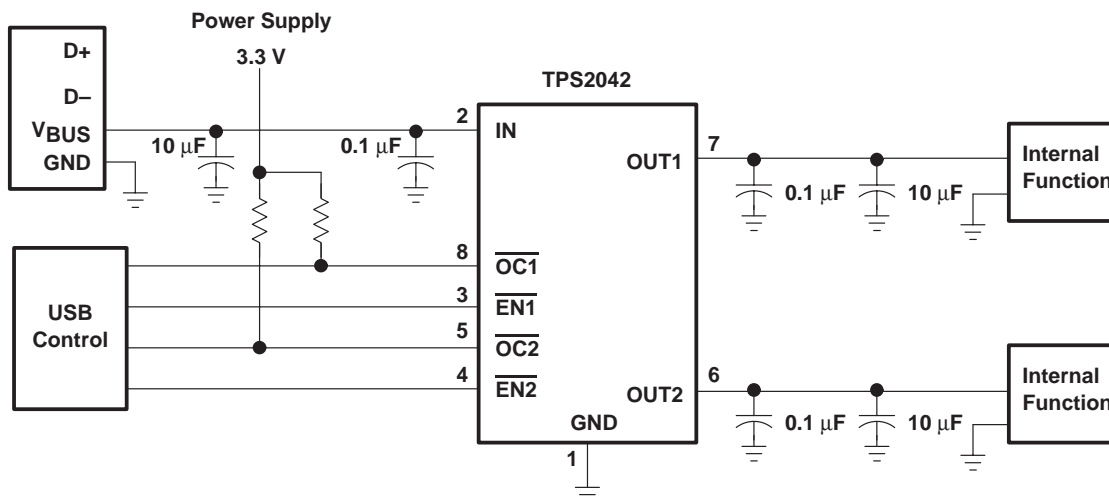


Figure 32. High-Power Bus-Powered Function

APPLICATION INFORMATION

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

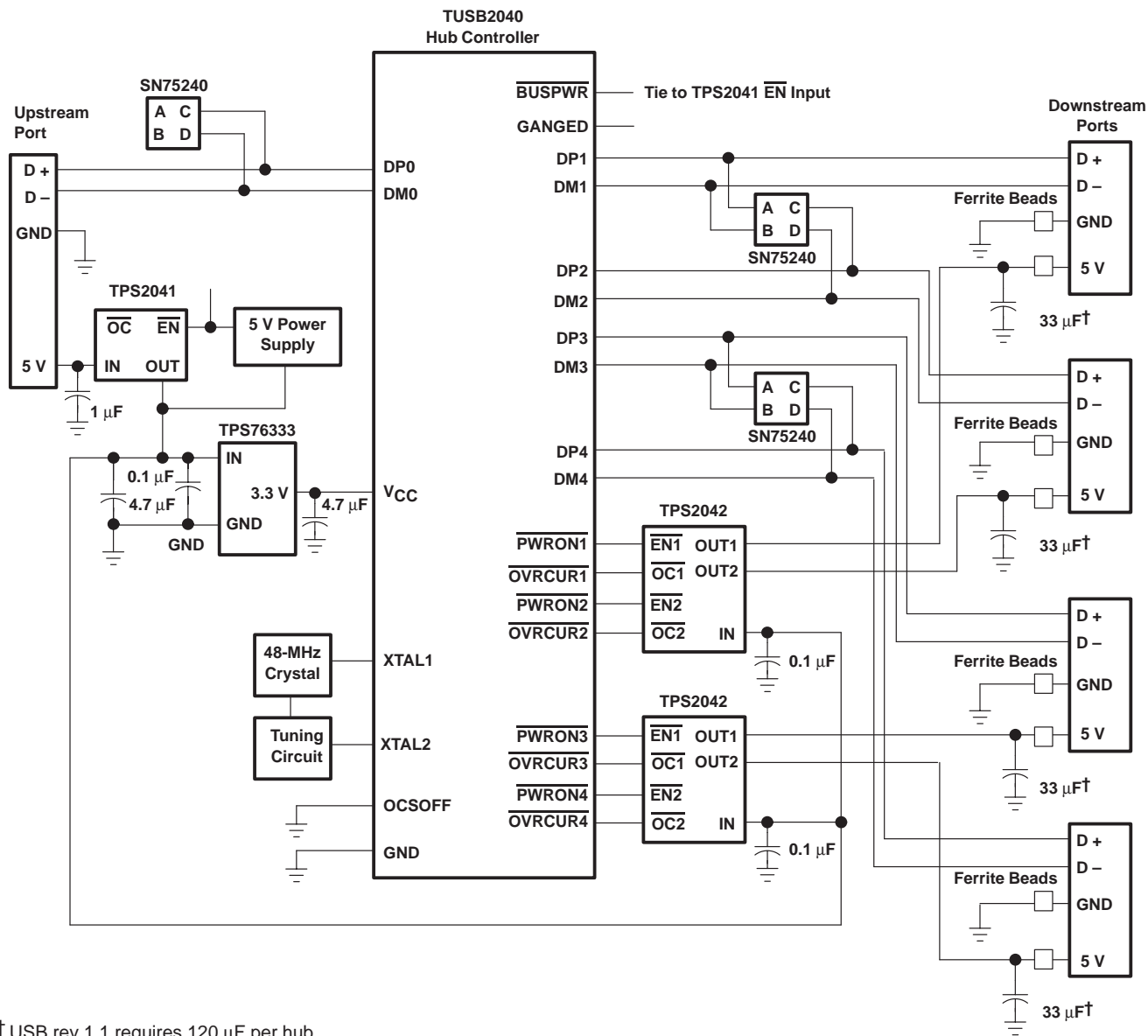
- Hosts/self-powered hubs must:
 - Current-limit downstream ports
 - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
 - Enable/disable power to downstream ports
 - Power up at <100 mA
 - Limit inrush current (<44 Ω and 10 μ F)
- Functions must:
 - Limit inrush currents
 - Power up at <100 mA

The feature set of the TPS2042 and TPS2052 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).

TPS2042, TPS2052 DUAL POWER-DISTRIBUTION SWITCHES

SLVS173A – AUGUST 1998 – REVISED APRIL 1999

APPLICATION INFORMATION



† USB rev 1.1 requires 120 μF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2042 and TPS2052, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2042 and TPS2052 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

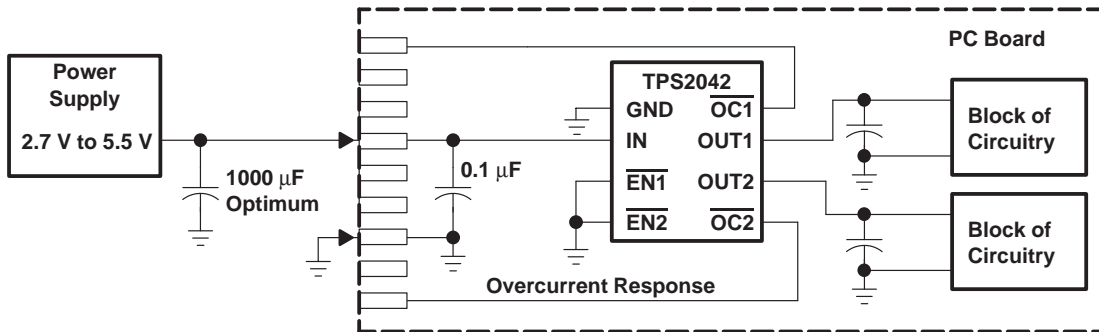


Figure 34. Typical Hot-Plug Implementation

By placing the TPS2042 and TPS2052 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2042D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2042 | Samples |
| TPS2042DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2042 | Samples |
| TPS2042P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS2042P | Samples |
| TPS2052D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2052 | Samples |
| TPS2052DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2052 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2042DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2052DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2042DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2052DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS2042D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS2042P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS2052D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |

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