



**THE DATASHEET OF
SN74LVC2G53YEPR**



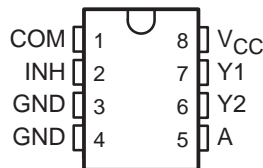
SN74LVC2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

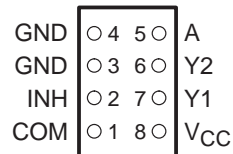
SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- 1.65-V to 5.5-V V_{CC} Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low On-State Resistance, Typically ≈6.5 Ω (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING‡ |
|----------------|--|-----------------|-----------------------|-------------------|
| -40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA | Reel of 3000 | SN74LVC2G53YEAR | ___C4_ |
| | NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free) | | SN74LVC2G53YZAR | |
| | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | | SN74LVC2G53YEPR | |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | | SN74LVC2G53YZPR | |
| | SSOP – DCT | Reel of 3000 | SN74LVC2G53DCTR | C53___ |
| | VSSOP – DCU | Reel of 3000 | SN74LVC2G53DCUR | C53_ |
| | Reel of 250 | SN74LVC2G53DCUT | | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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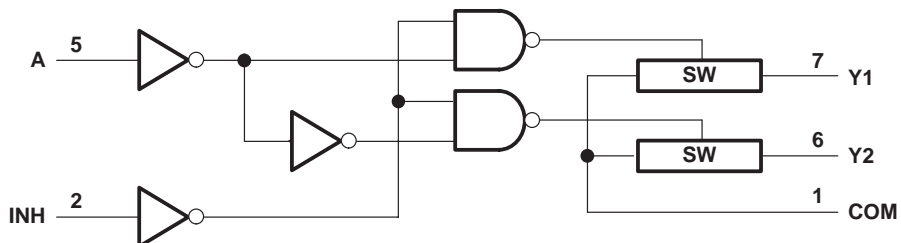
SN74LVC2G53 SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

FUNCTION TABLE

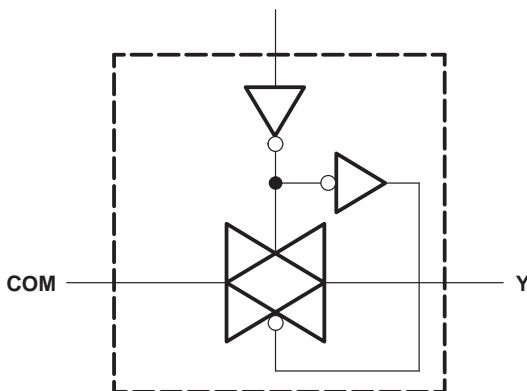
| CONTROL INPUTS | | ON CHANNEL |
|----------------|---|------------|
| INH | A | |
| L | L | Y1 |
| L | H | Y2 |
| H | X | None |

logic diagram (positive logic)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

simplified schematic, each switch (SW)



SN74LVC2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.5 V to 6.5 V |
| Input voltage range, V_I (see Notes 1 and 2) | –0.5 V to 6.5 V |
| Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) | –0.5 V to $V_{CC} + 0.5$ V |
| Control input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$) | ±50 mA |
| On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 4): DCT package | 220°C/W |
| DCU package | 227°C/W |
| YEA/YZA package | 140°C/W |
| YEP/YZP package | 102°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. This value is limited to 5.5 V maximum.
 4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

| | | MIN | MAX | UNIT |
|---------------------|---|-----------------------------|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 5.5 | V |
| $V_{I/O}$ | I/O port voltage | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage, control input | $V_{CC} = 1.65$ V to 1.95 V | $V_{CC} \times 0.65$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | $V_{CC} \times 0.7$ | |
| | | $V_{CC} = 3$ V to 3.6 V | $V_{CC} \times 0.7$ | |
| | | $V_{CC} = 4.5$ V to 5.5 V | $V_{CC} \times 0.7$ | |
| V_{IL} | Low-level input voltage, control input | $V_{CC} = 1.65$ V to 1.95 V | $V_{CC} \times 0.35$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 3$ V to 3.6 V | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 4.5$ V to 5.5 V | $V_{CC} \times 0.3$ | |
| V_I | Control input voltage | 0 | 5.5 | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 1.65$ V to 1.95 V | 20 | ns/V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 20 | |
| | | $V_{CC} = 3$ V to 3.6 V | 10 | |
| | | $V_{CC} = 4.5$ V to 5.5 V | 10 | |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74LVC2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|----------------------|--|--|------------------------|--------|------|-------------|------|
| r _{on} | On-state switch resistance | V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figures 1 and 2) | I _S = 4 mA | 1.65 V | 13 | 30 | Ω |
| | | | I _S = 8 mA | 2.3 V | 10 | 20 | |
| | | | I _S = 24 mA | 3 V | 8.5 | 17 | |
| | | | I _S = 32 mA | 4.5 V | 6.5 | 13 | |
| r _{on(p)} | Peak on-state resistance | V _I = V _{CC} to GND, V _{INH} = V _{IL} (see Figures 1 and 2) | I _S = 4 mA | 1.65 V | 86.5 | 120 | Ω |
| | | | I _S = 8 mA | 2.3 V | 23 | 30 | |
| | | | I _S = 24 mA | 3 V | 13 | 20 | |
| | | | I _S = 32 mA | 4.5 V | 8 | 15 | |
| Δr _{on} | Difference of on-state resistance between switches | V _I = V _{CC} to GND, V _C = V _{IH} (see Figures 1 and 2) | I _S = 4 mA | 1.65 V | | 7 | Ω |
| | | | I _S = 8 mA | 2.3 V | | 5 | |
| | | | I _S = 24 mA | 3 V | | 3 | |
| | | | I _S = 32 mA | 4.5 V | | 2 | |
| I _{S(off)} | Off-state switch leakage current | V _I = V _{CC} and V _O = GND or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 3) | 5.5 V | | | ±1 ±0.1† | μA |
| I _{S(on)} | On-state switch leakage current | V _I = V _{CC} or GND, V _{INH} = V _{IL} , V _O = Open (see Figure 4) | 5.5 V | | | ±1 ±0.1† | μA |
| I _I | Control input current | V _C = V _{CC} or GND | 5.5 V | | | ±1 | μA |
| | | | | | | ±0.1† | μA |
| I _{CC} | Supply current | V _C = V _{CC} or GND | 5.5 V | | | 1 | μA |
| ΔI _{CC} | Supply-current change | V _C = V _{CC} – 0.6 V | 5.5 V | | | 500 | μA |
| C _{ic} | Control input capacitance | | 5 V | | | 3.5 | pF |
| C _{io(off)} | Switch input/output capacitance | Y | 5 V | | | 6.5 | pF |
| | | COM | | | | 10 | |
| C _{io(on)} | Switch input/output capacitance | | 5 V | | | 19.5 | pF |

† T_A = 25°C

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|--------------------|--------------|-------------|----------------------------------|------|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} ‡ | COM or Y | Y or COM | | 2 | | 1.2 | | 0.8 | | 0.6 | ns |
| t _{en} § | INH | COM or Y | 3.3 | 9 | 2.5 | 6.1 | 2.2 | 5.4 | 1.8 | 4.5 | ns |
| t _{dis} ¶ | | | 3.2 | 10.9 | 2.3 | 8.3 | 2.3 | 8.1 | 1.6 | 8 | |
| t _{en} § | A | COM or Y | 2.9 | 10.3 | 2.1 | 7.2 | 1.9 | 5.8 | 1.3 | 5.4 | ns |
| t _{dis} ¶ | | | 2.1 | 9.4 | 1.4 | 7.9 | 1.1 | 7.2 | 1 | 5 | |

‡ t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

§ t_{PZL} and t_{PZH} are the same as t_{en}.

¶ t_{PLZ} and t_{PHZ} are the same as t_{dis}.



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SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

analog switch characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--------------|-------------|---|-----------------|-------|------|
| Frequency response [†] (switch on) | COM or Y | Y or COM | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | 35 | MHz |
| | | | | 2.3 V | 120 | |
| | | | | 3 V | 190 | |
| | | | | 4.5 V | 215 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | >300 | |
| | | | | 2.3 V | >300 | |
| | | | | 3 V | >300 | |
| | | | | 4.5 V | >300 | |
| Crosstalk [‡] (between switches) | COM or Y | Y or COM | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7) | 1.65 V | -58 | dB |
| | | | | 2.3 V | -58 | |
| | | | | 3 V | -58 | |
| | | | | 4.5 V | -58 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7) | 1.65 V | -42 | |
| | | | | 2.3 V | -42 | |
| | | | | 3 V | -42 | |
| | | | | 4.5 V | -42 | |
| Crosstalk (control input to signal output) | INH | COM or Y | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8) | 1.65 V | 35 | mV |
| | | | | 2.3 V | 50 | |
| | | | | 3 V | 70 | |
| | | | | 4.5 V | 100 | |
| Feed-through attenuation [‡] (switch off) | COM or Y | Y or COM | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9) | 1.65 V | -60 | dB |
| | | | | 2.3 V | -60 | |
| | | | | 3 V | -60 | |
| | | | | 4.5 V | -60 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9) | 1.65 V | -50 | |
| | | | | 2.3 V | -50 | |
| | | | | 3 V | -50 | |
| | | | | 4.5 V | -50 | |
| Sine-wave distortion | COM or Y | Y or COM | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10) | 1.65 V | 0.1 | % |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |
| | | | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 10) | 1.65 V | 0.15 | |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |

[†] Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

[‡] Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT |
|---|--|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C _{pd} Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 9 | 10 | 10 | 12 | pF |



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2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

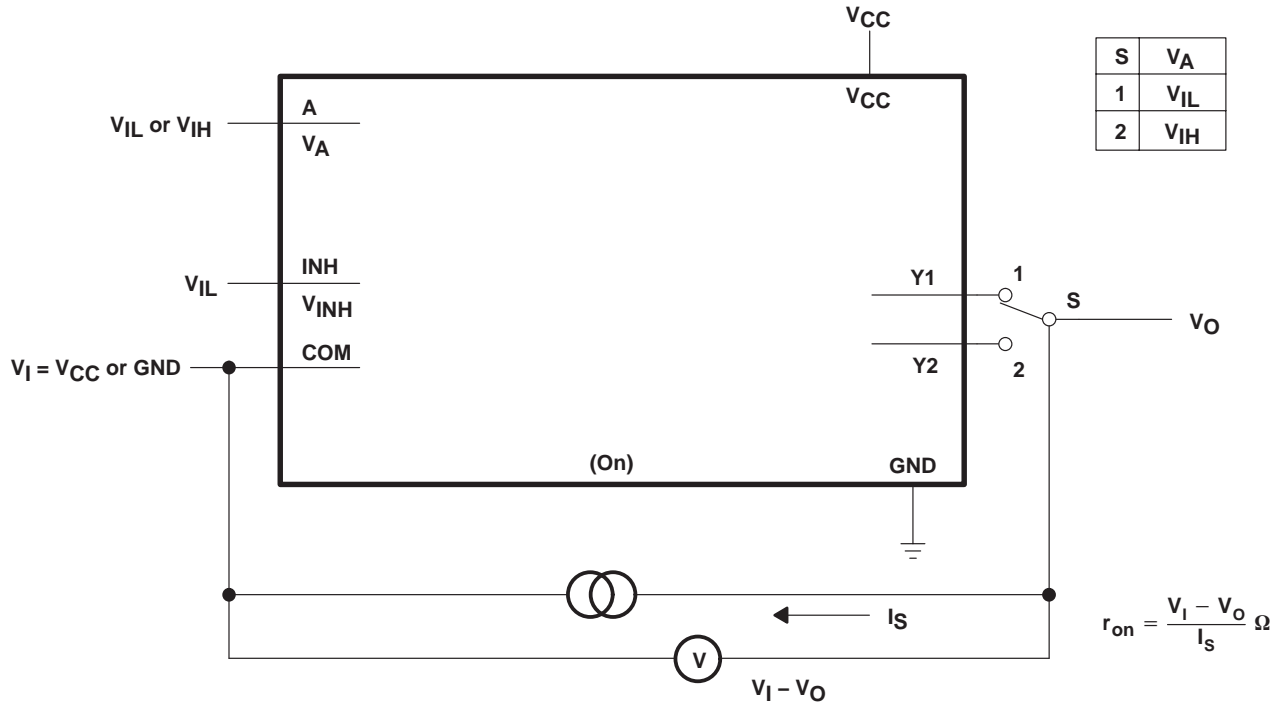


Figure 1. On-State Resistance Test Circuit

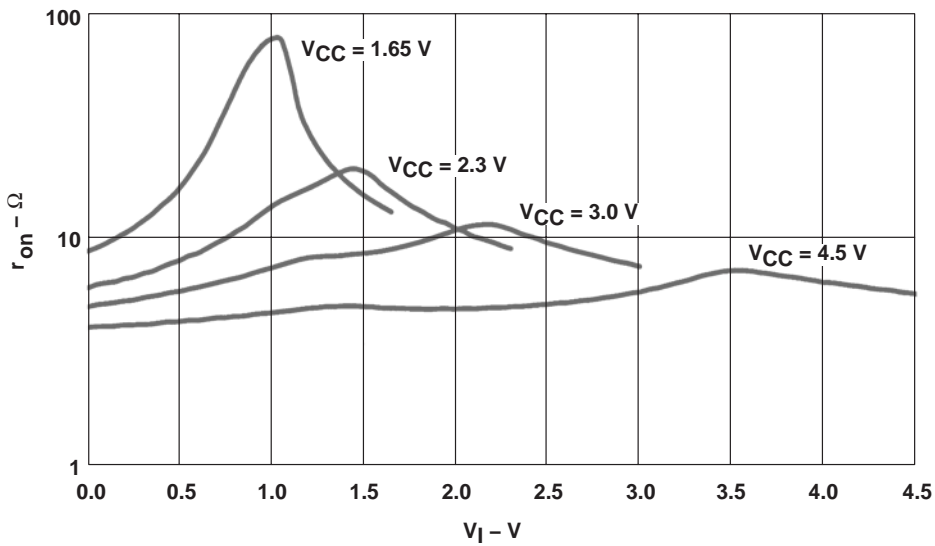


Figure 2. Typical r_{on} as a Function of Input Voltage (V_1) for $V_1 = 0$ to V_{CC}

SN74LVC2G53
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2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

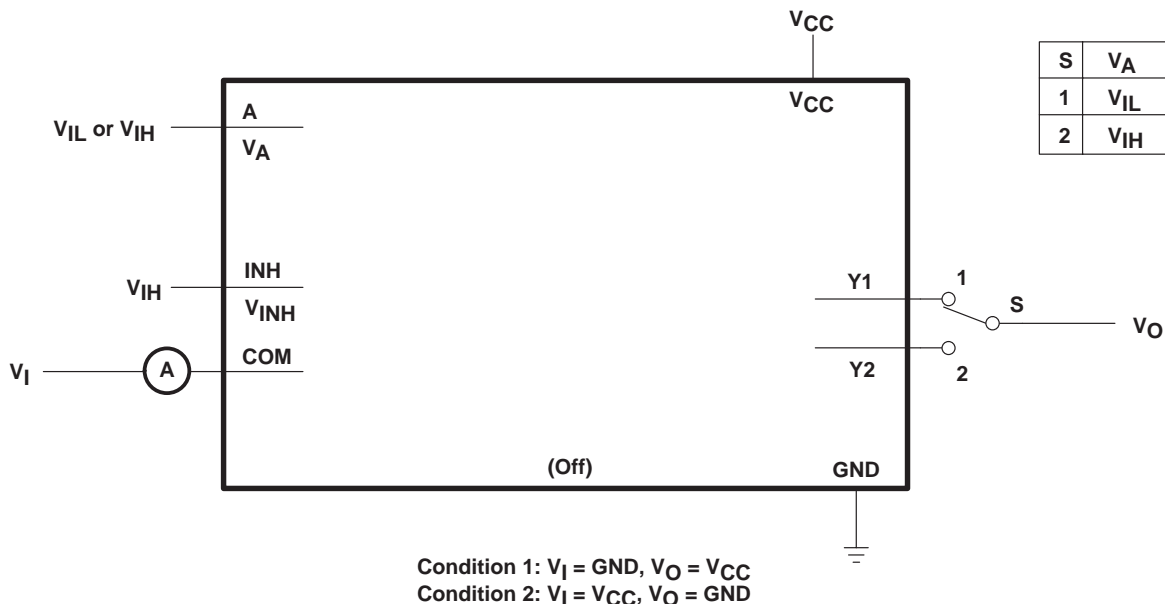


Figure 3. Off-State Switch Leakage-Current Test Circuit

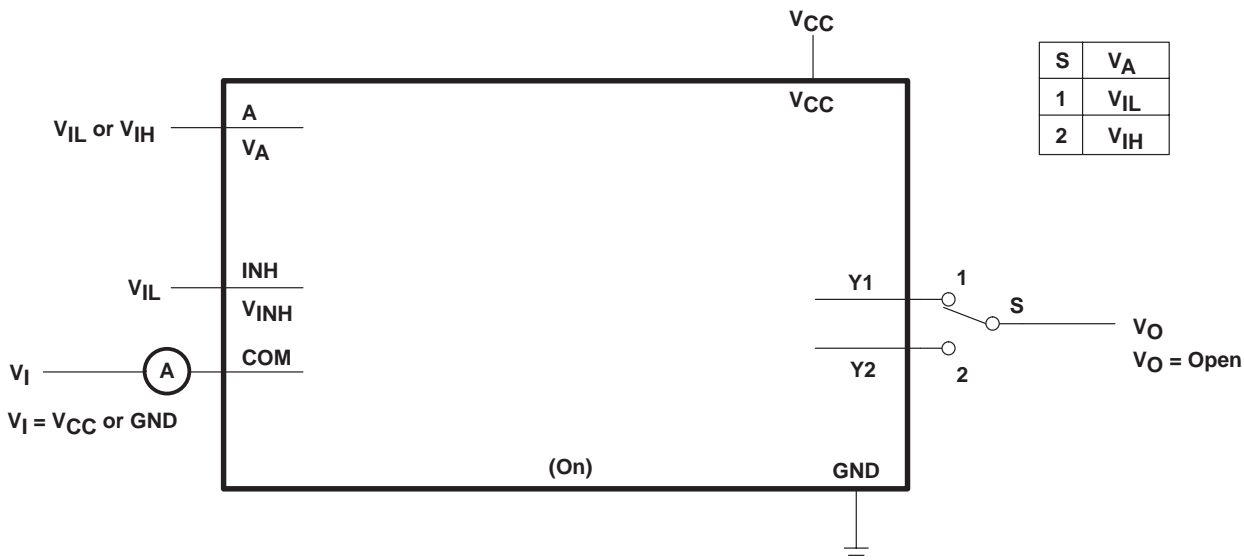
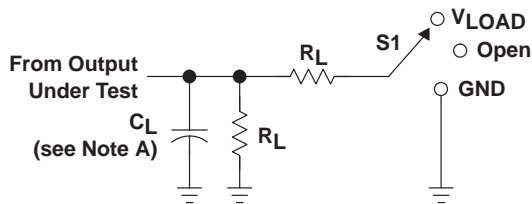


Figure 4. On-State Switch Leakage-Current Test Circuit

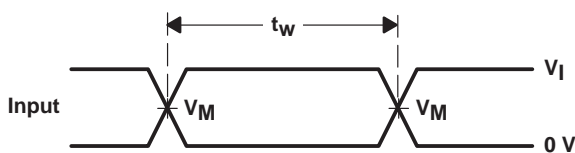
PARAMETER MEASUREMENT INFORMATION



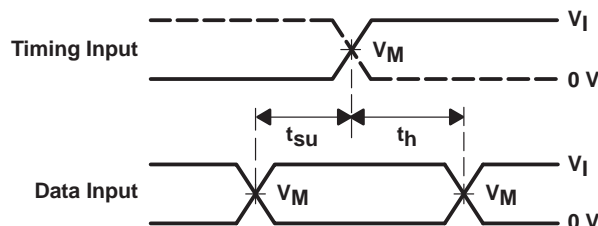
LOAD CIRCUIT

| TEST | S1 |
|------------------------------------|-------------------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | V _{LOAD} |
| t _{PHZ} /t _{PZH} | GND |

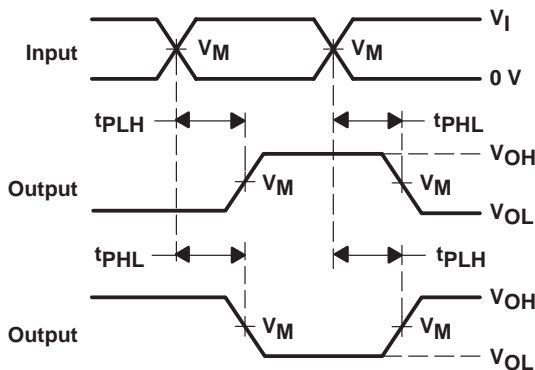
| V _{CC} | INPUTS | | V _M | V _{LOAD} | C _L | R _L | V _Δ |
|-----------------|-----------------|--------------------------------|--------------------|---------------------|----------------|----------------|----------------|
| | V _I | t _r /t _f | | | | | |
| 1.8 V ± 0.15 V | V _{CC} | ≤ 2 ns | V _{CC} /2 | 2 × V _{CC} | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | V _{CC} | ≤ 2 ns | V _{CC} /2 | 2 × V _{CC} | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | V _{CC} | ≤ 2.5 ns | V _{CC} /2 | 2 × V _{CC} | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | V _{CC} | ≤ 2.5 ns | V _{CC} /2 | 2 × V _{CC} | 50 pF | 500 Ω | 0.3 V |



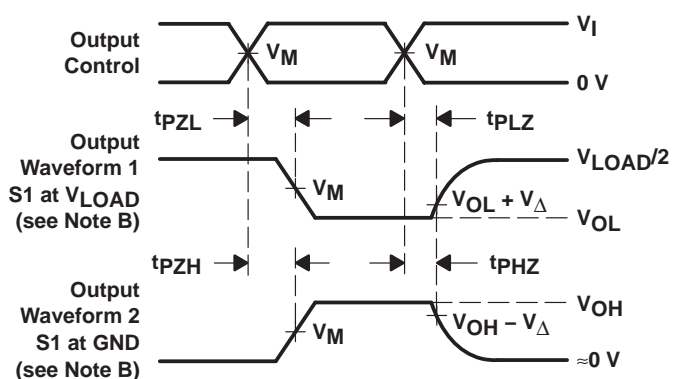
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PZL} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

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SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

PARAMETER MEASUREMENT INFORMATION

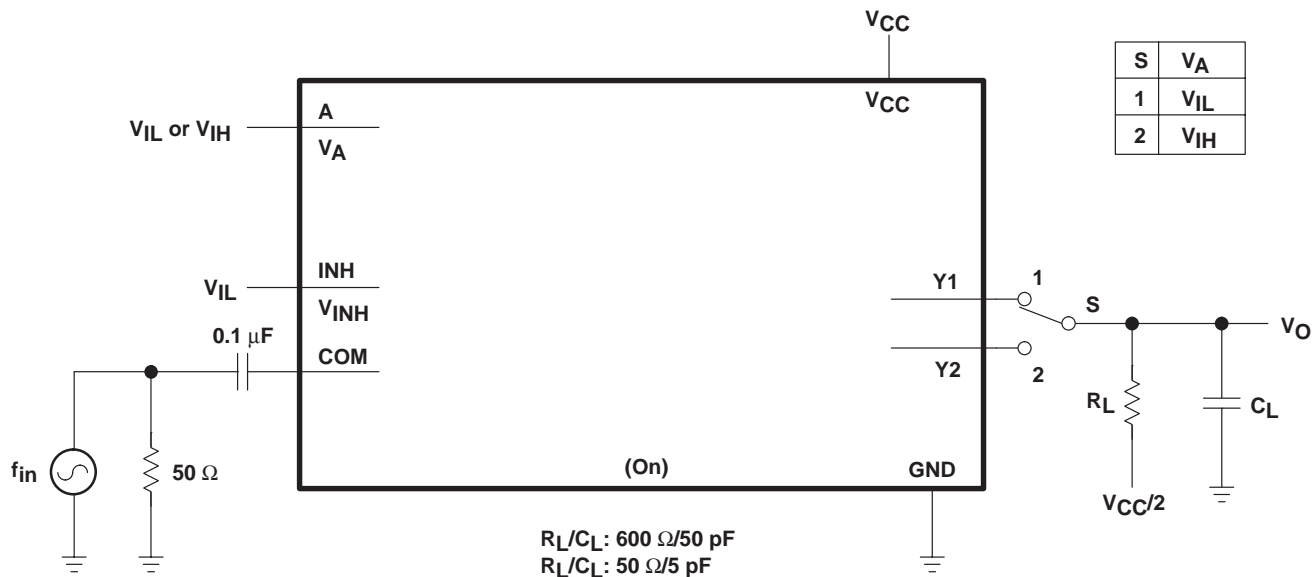


Figure 6. Frequency Response (Switch On)

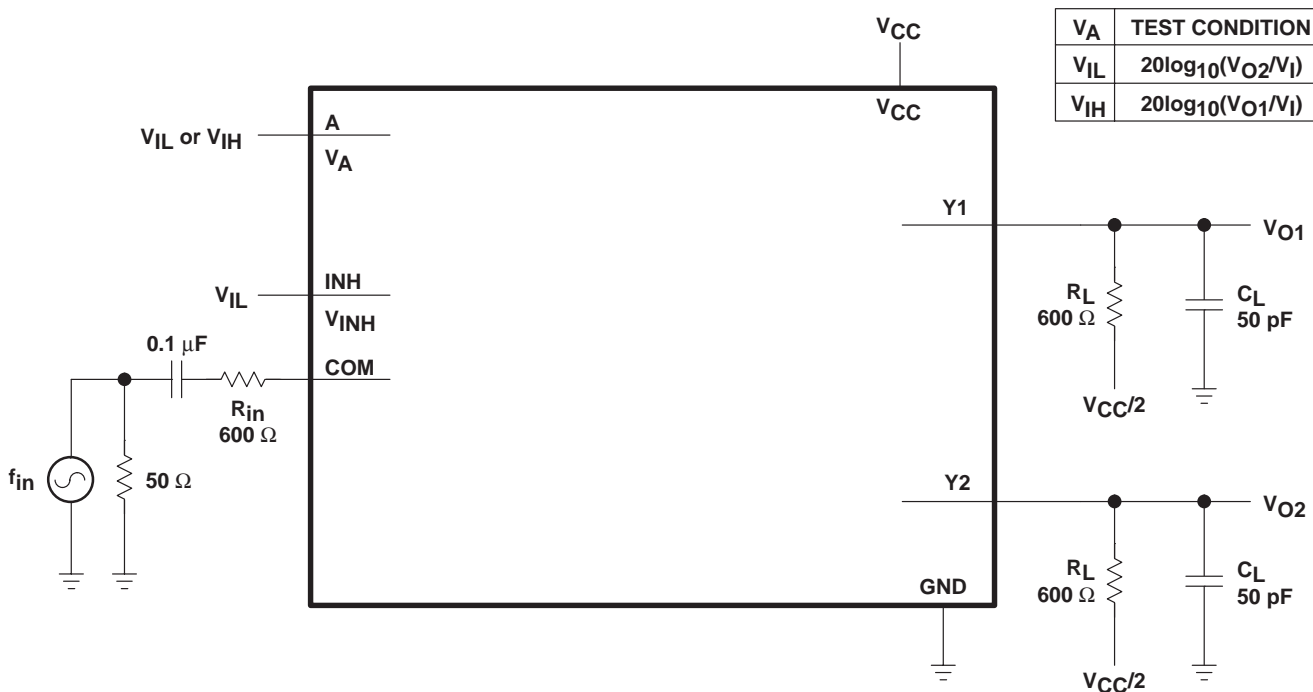


Figure 7. Crosstalk (Between Switches)

SN74LVC2G53
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR
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SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

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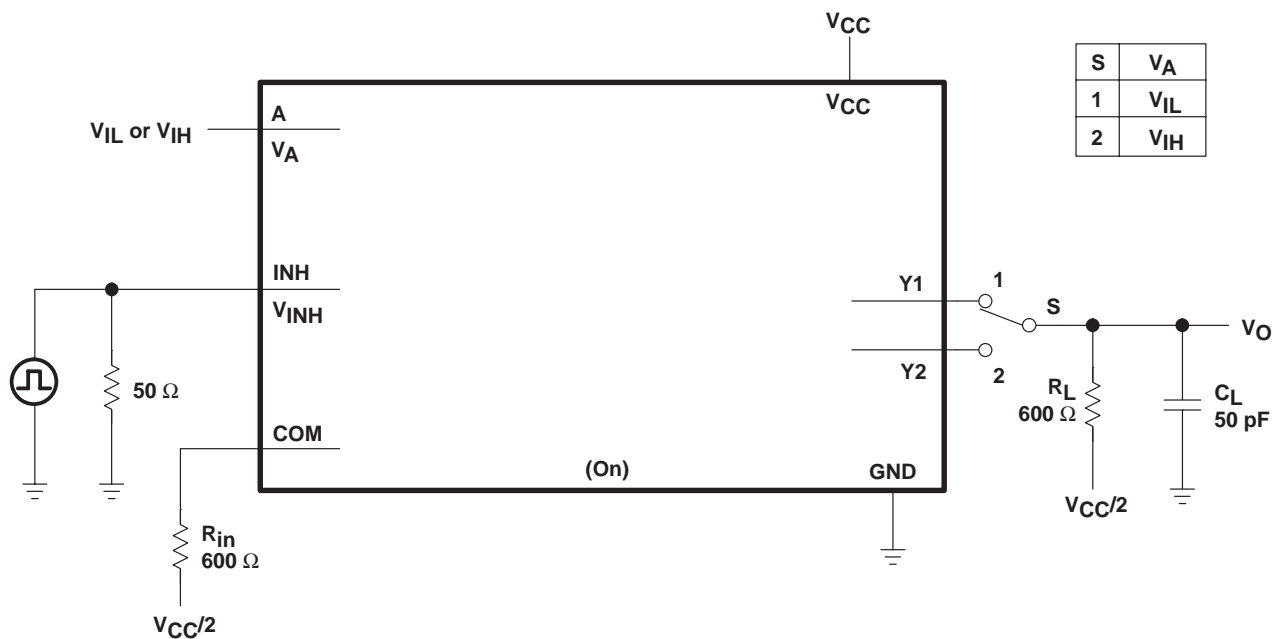


Figure 8. Crosstalk (Control Input, Switch Output)

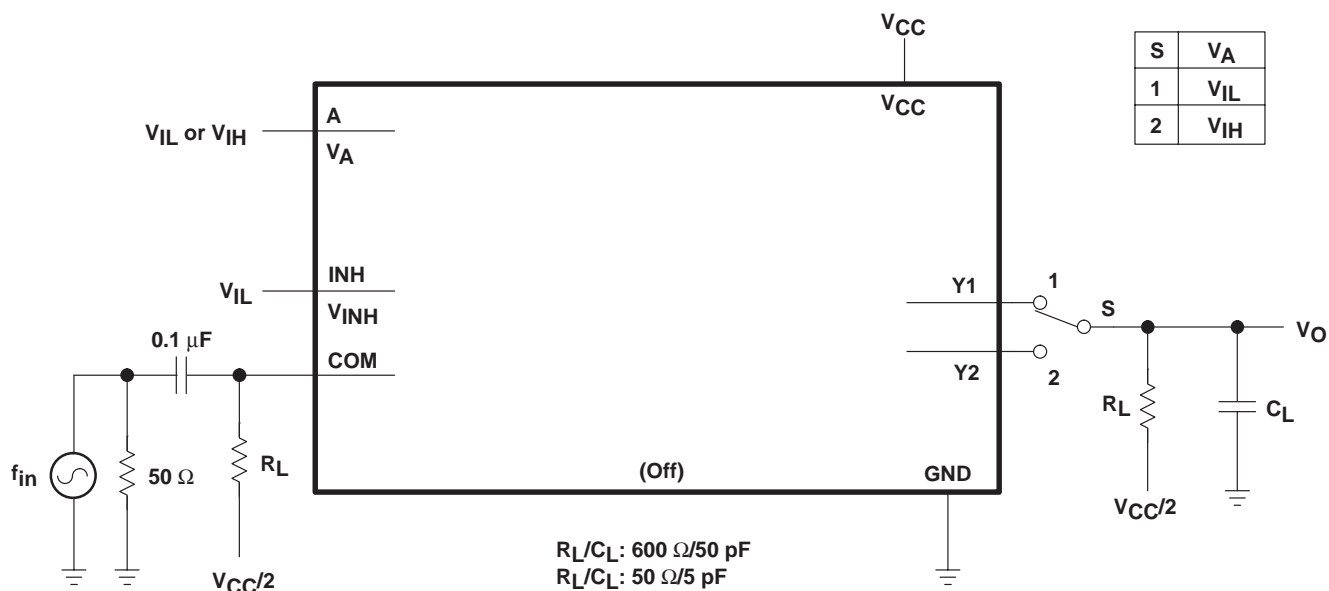


Figure 9. Feed Through (Switch Off)

SN74LVC2G53
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SCES324K – JULY 2001 – REVISED SEPTEMBER 2003

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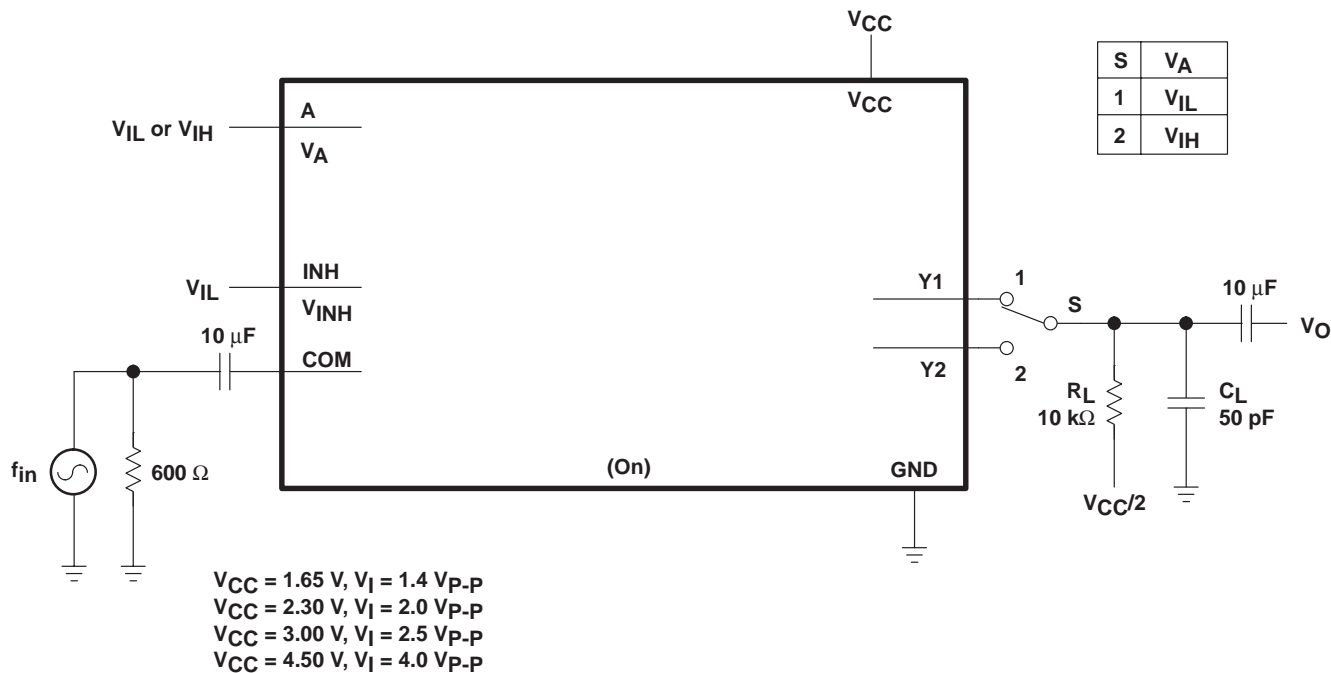
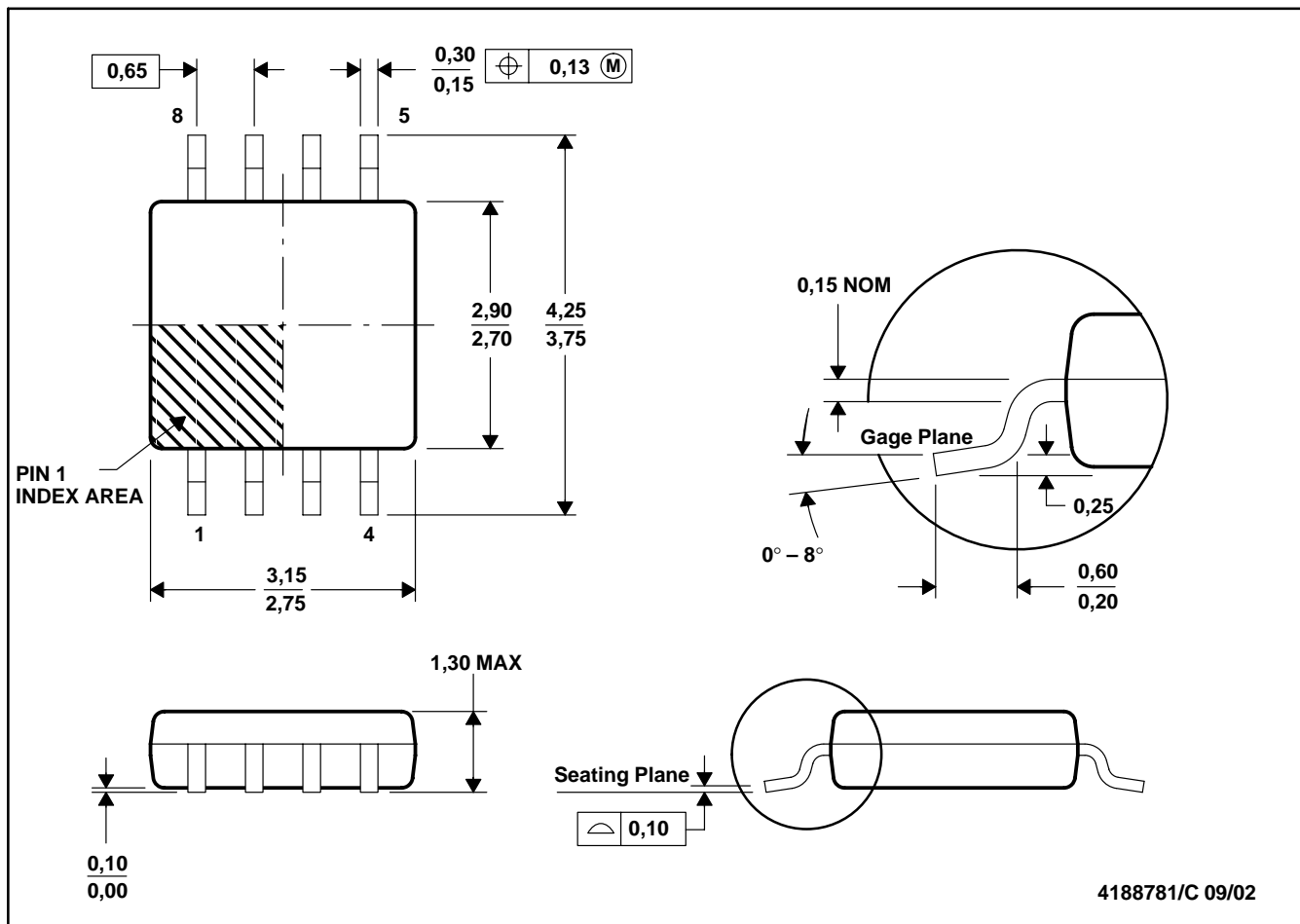


Figure 10. Sine-Wave Distortion

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

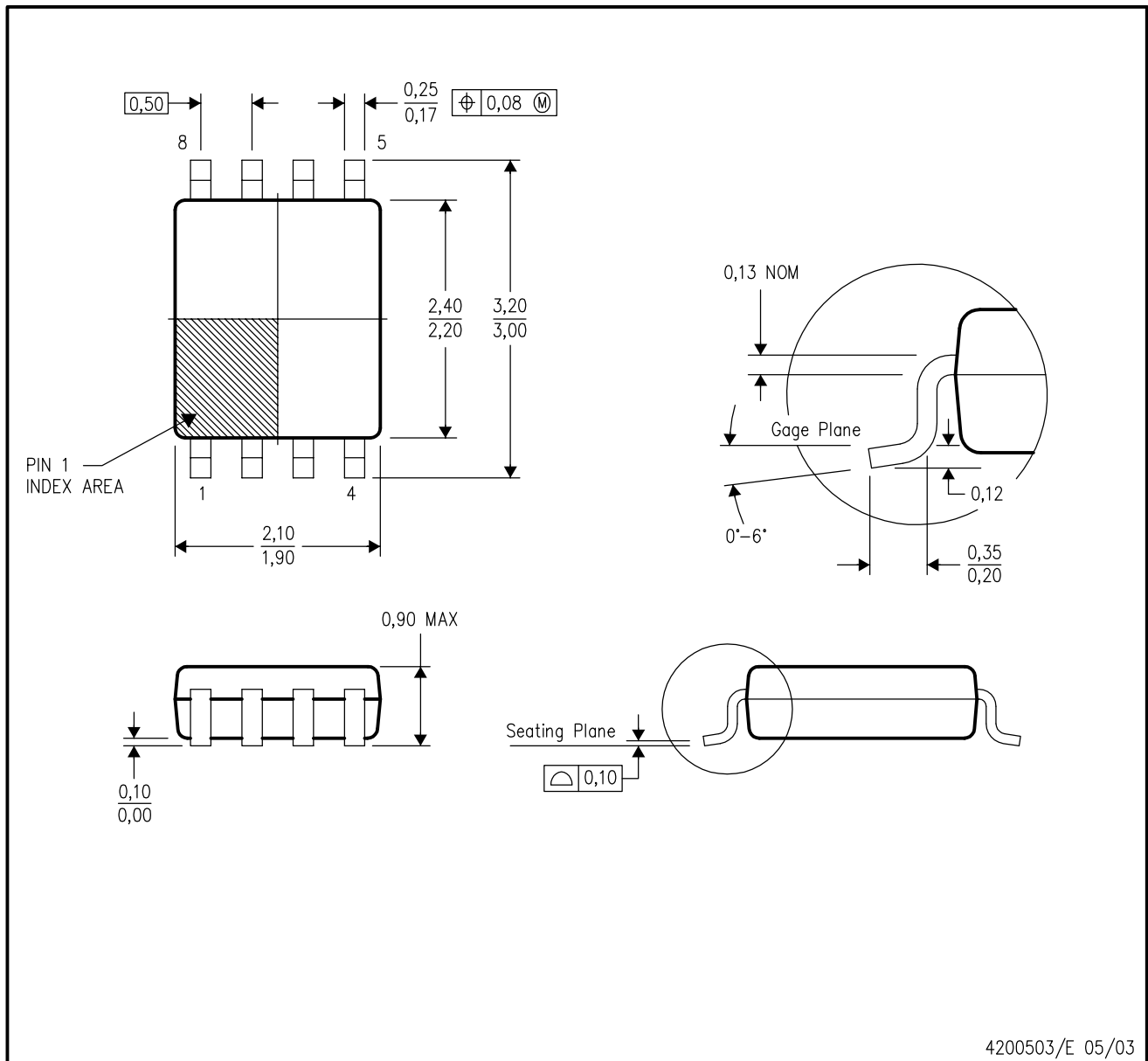


4188781/C 09/02

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8)

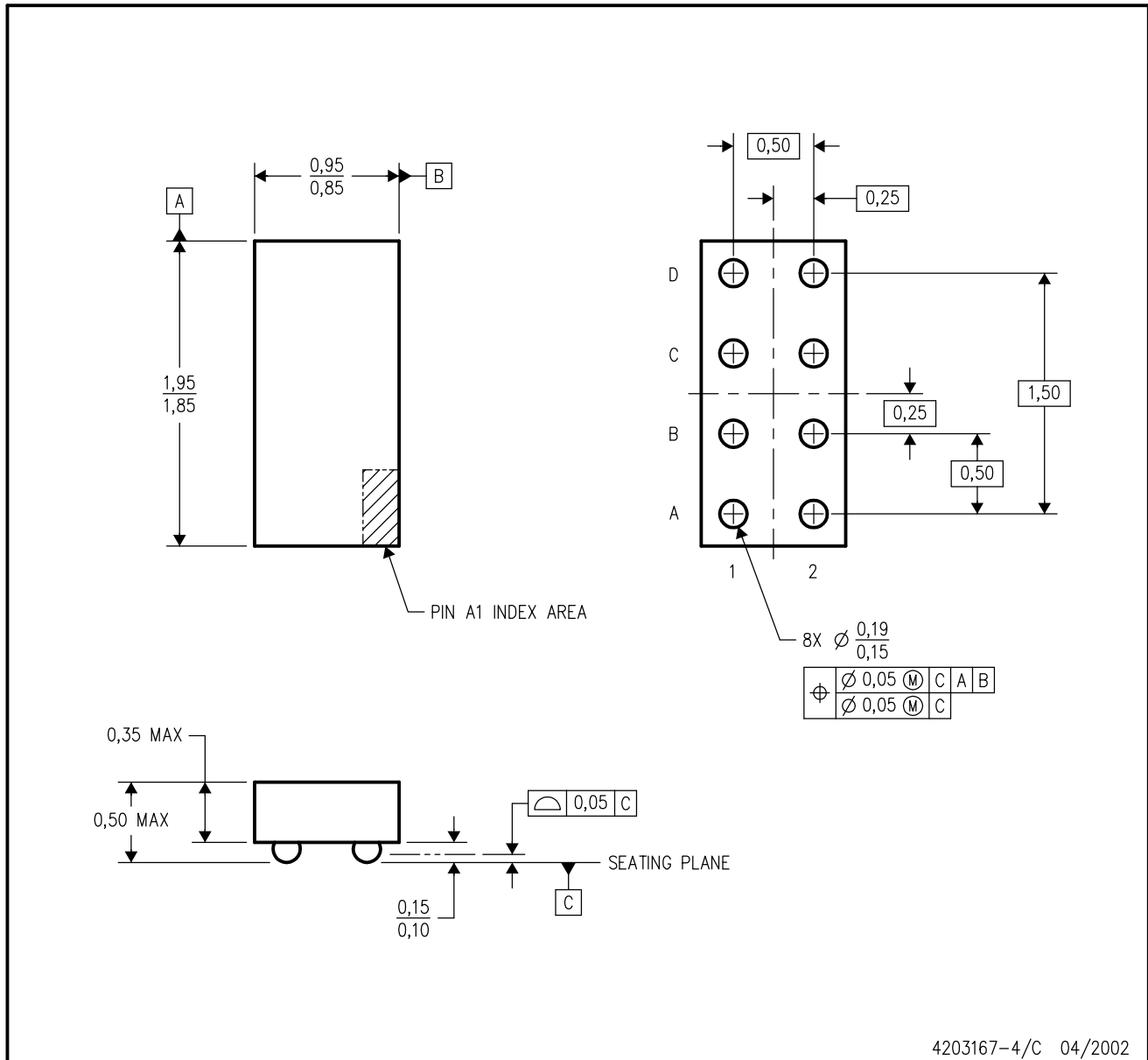
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation CA.

YEA (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY

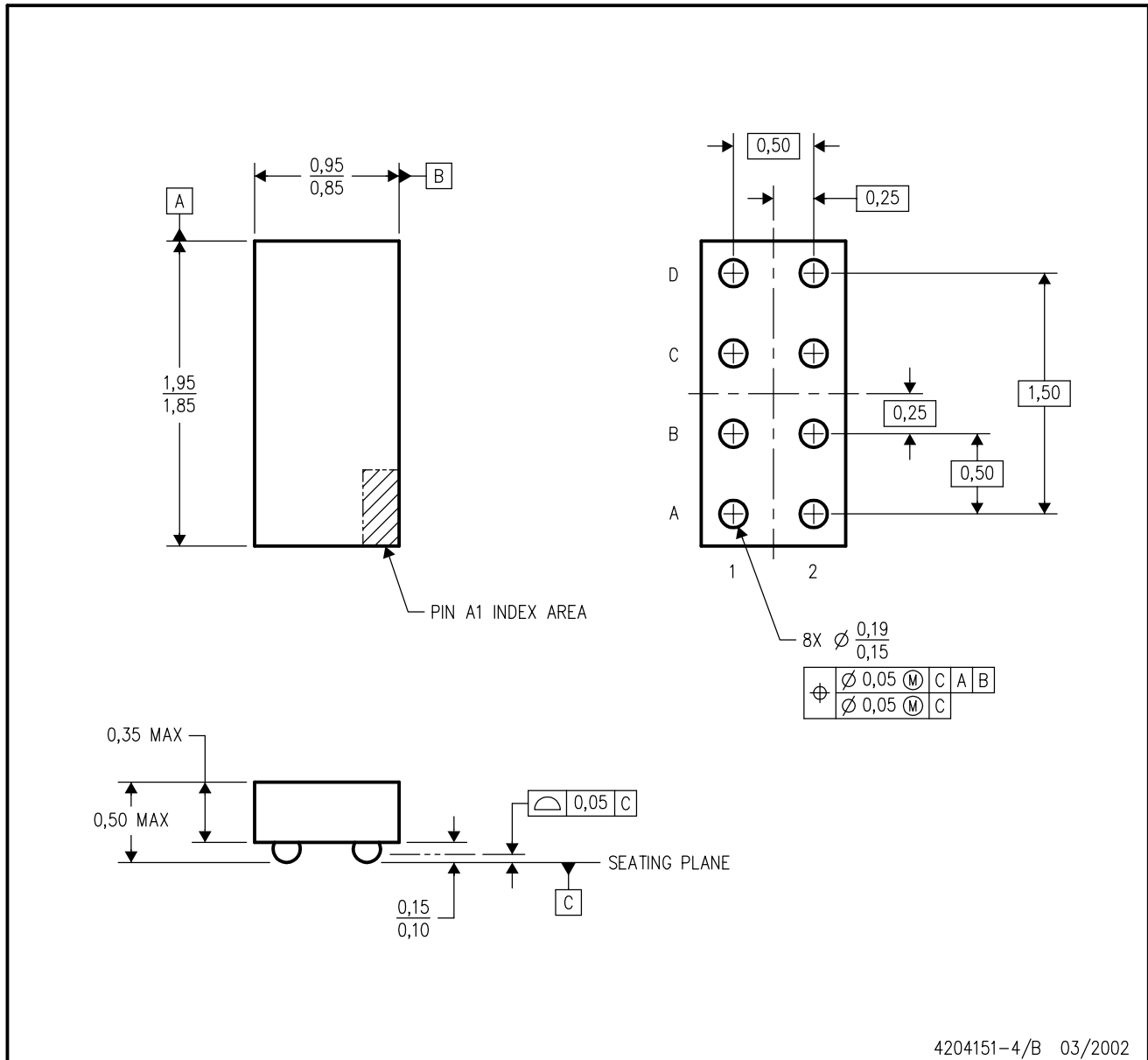


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EB.
 - E. This package is tin-lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead-free.

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YZA (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY

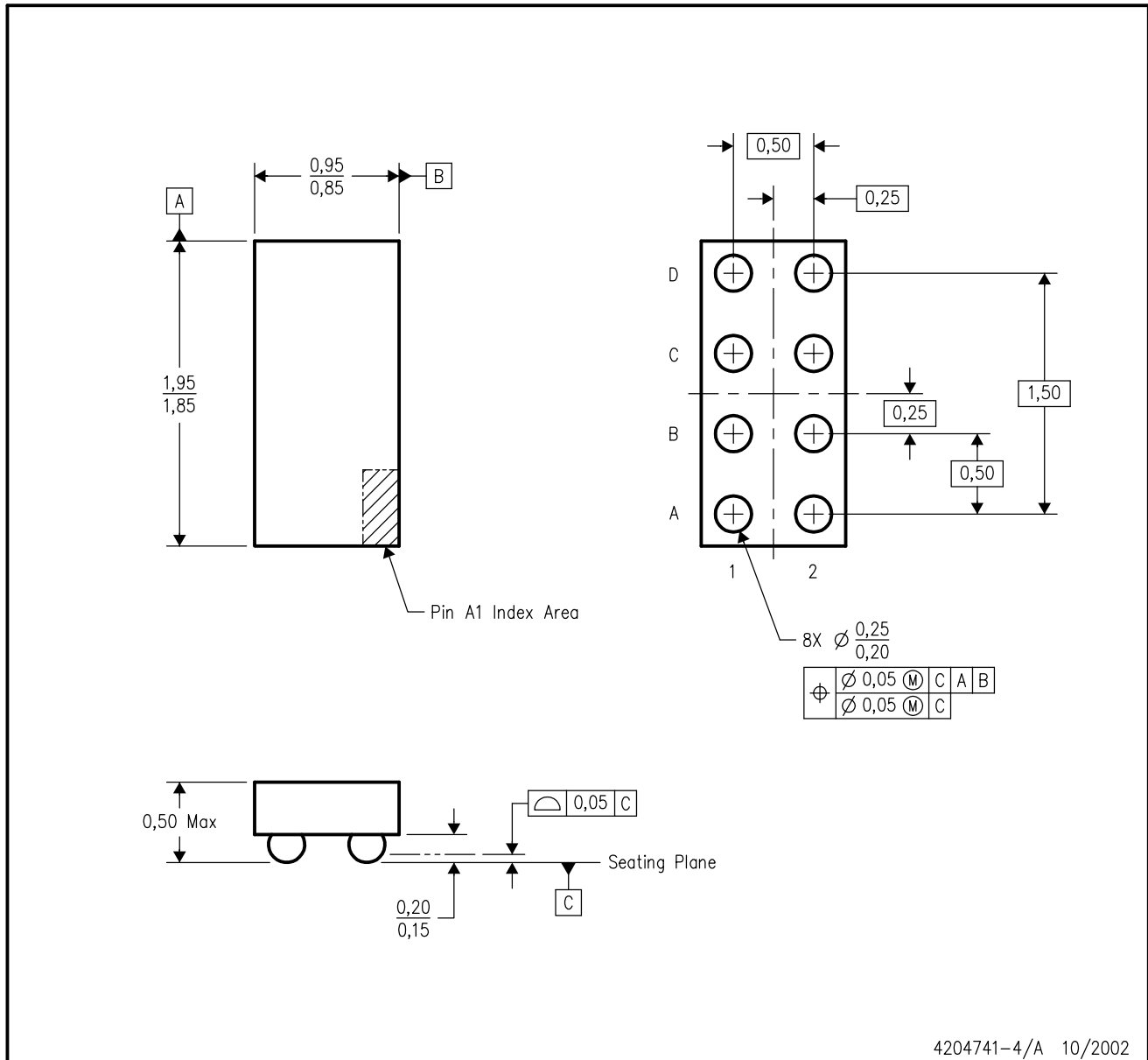


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EB.
 - E. This package is lead-free. Refer to the 8 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY

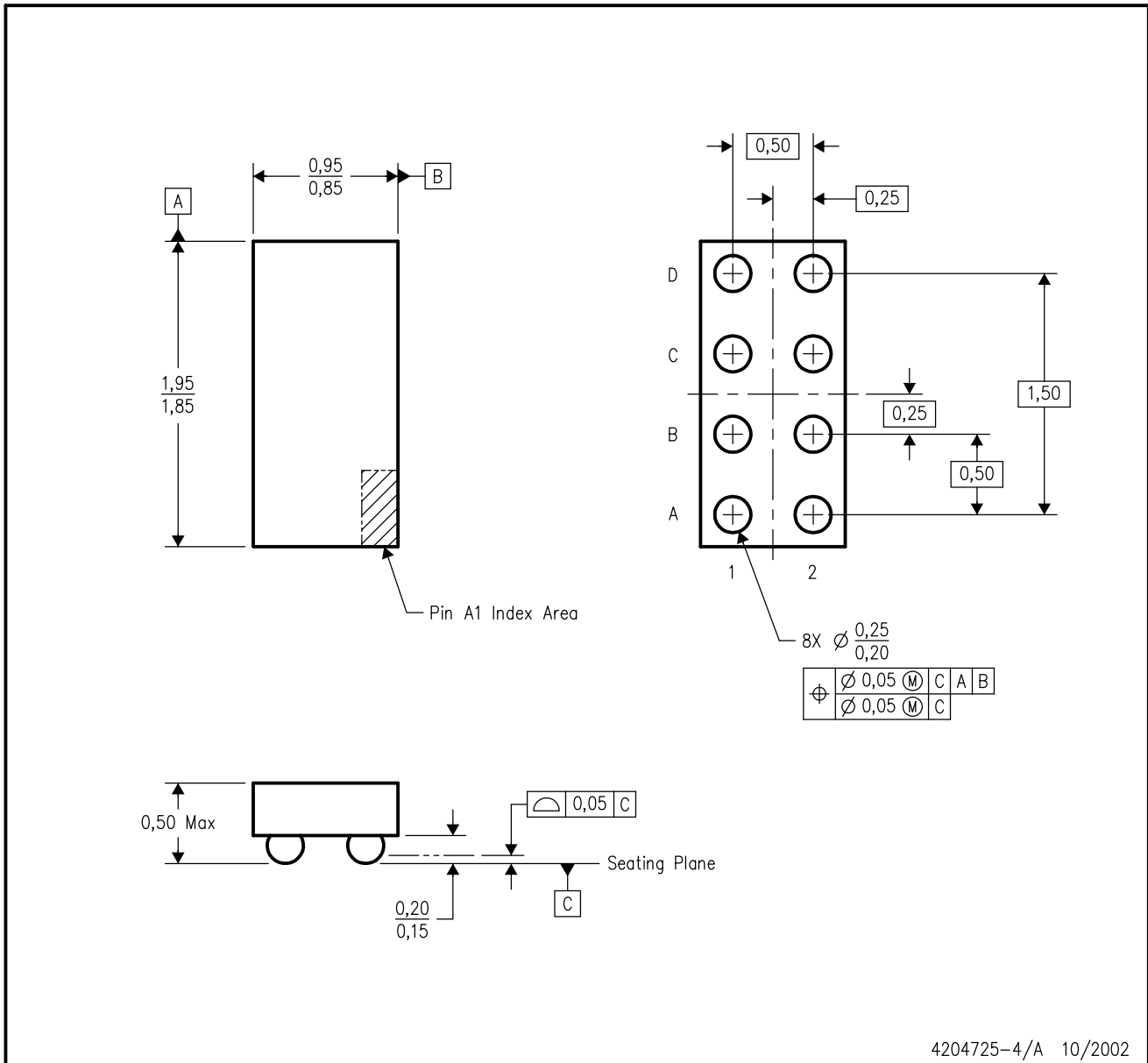


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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