THE DATASHEET OF

STA2058EX

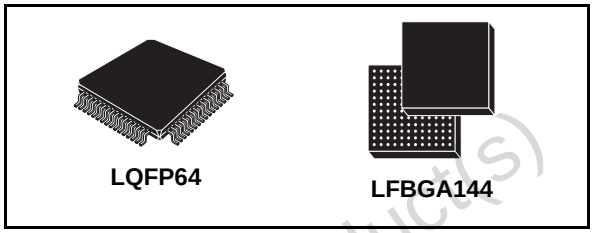
STA2058

TESEO™
GPS platform high-sensitivity baseband

Data Brief

Features

- Single chip baseband with embedded Flash
- Complete embedded memory system:
  - Flash 256 KB +16 Kbytes
  - RAM 64 Kbytes
- 66 MHz ARM7TDMI 32 bit processor
- High performance GPS engine (HPGPS)
- SBAS (WAAS and EGNOS) supported
- Sensitivity (-146 dBm acquisition, -159 dBm tracking)
- Time to first fix (1s reacquisition, 2.5 s hot start, 34 s warm start, 39 s cold start)
- Accuracy (2 m autonomous)
- External memory interface (EMI) supporting up to 64 Mbite of external SRAM, Flash and ROM
- Extensive GPS receiver interfaces:
  48 GPIOs, 4 UARTs, 2 SPIs, 2 I2Cs,
  2 CANs 2.0, 1 USB 1.1,1 HDLC and 4 channels ADC
- ST proprietary Flash embedded technology
- LFBGA144 and LQFP64 lead-free package
- -40 °C to 85 °C operating temperature range



Evaluation kits

- STA2058 module reference design (25x25mm)
- Evaluation board hosting STA2058 module
- SDK board (for application SW development)

Description

STA2058 is the high-sensitivity baseband of TESEO GPS platform which include the STA5620 RF Front-End.

The embedded Flash memory enables the equipment manufacturer to load the entire GPS software (including tracking, acquisition, navigation and data output) after customizing its interfaces to his needs. A standard GPS library is available from ST.

TESEO is the ideal solution for consumer, handheld, PND (portable navigation), in vehicle navigation and telematics systems.

SBAS (WAAS and EGNOS) feature is also supported.

Table 1. Device summary

Order code	Package	EMI (External Memory Interface)	Packing	Automotive grade
STA2058	LQFP64 (10x10x1.4mm)	No	Tray	No
STA2058TR	LQFP64 (10x10x1.4mm)	No	Tape and reel	No
STA2058EX	LFBGA144 (10x10x1.7mm)	Yes	Tray	No
STA2058EXTR	LFBGA144 (10x10x1.7mm)	Yes	Tape and reel	No
STA2058EXA	LFBGA144 (10x10x1.7mm)	Yes	Tray	Yes
STA2058EXATR	LFBGA144 (10x10x1.7mm)	Yes	Tape and reel	Yes

Contents

1 Features summary

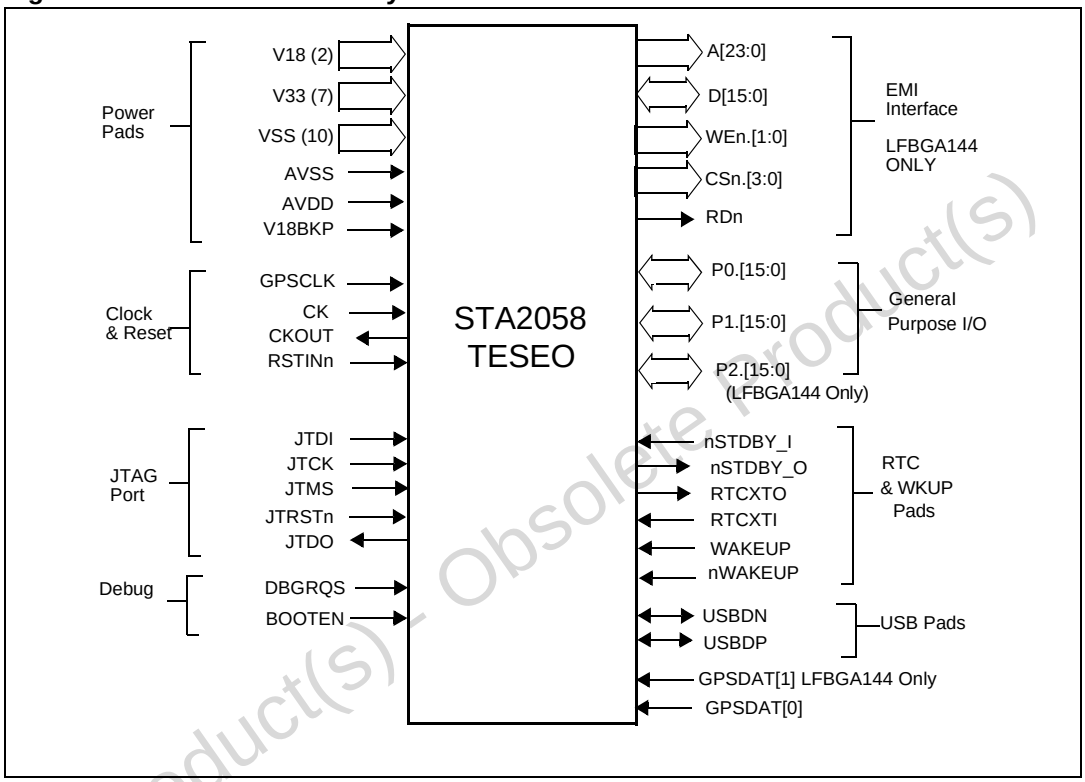
- ARM7TDMI 16/32 bit RISC CPU based host microcontroller running at a frequency up to 66 MHz.
- Complete embedded memory system:
  - Flash 256 Kbytes + 16 Kbytes (100 KB erasing/programming cycles)
  - RAM 64 Kbytes.
- External memory interface provides glueless support for up to four banks of external SRAM, Flash, ROM.
- High performance GPS engine (HPGPS).
- ST Proprietary CMOS (0.18 µm) Flash embedded technology.
- SBAS (WAAS and EGNOS) supported
- -40 °C to 85 °C operating temperature range.
- 144-pin LFBGA package and 64-pin LQFP package
- Power supply:
  - 3.0 V to 3.6 V operating supply range for Input/Output periphery
  - 3.0 V to 3.6 V operating supply range for A/D Converter reference
  - 1.8 V operating supply range for core supply provided either by internal voltage regulator (with external stabilization capacitor) or by external supply voltage.
- Reset and clock control unit able to provide low power modes (WAIT, SLOW, STOP, STANDBY) and to generate the internal clock from the external reference through integrated PLL.
- 48 programmable general purpose I/O, each pin programmable independently as digital input or digital output; 40 (30 in LQFP64) are multiplexed with peripheral functions; 16 can generate an interrupt on input level/transition.
- Real time clock module with 32 kHz low power oscillator and separate power supply to continue running during standby mode.
- 16-bit Watchdog timer with 8 bits prescaler for system reliability and integrity.
- 2 CAN modules compliant with the CAN specification V2.0 part B (active) and bit rate can be programmed up to 1 MBaud. One additional CAN at 1 Mbps (for STA2058 EM SIP version)
- Four 16-bit programmable timers with 7 bit prescaler, up to two input capture/output compare, one pulse counter function, one PWM channel with selectable frequency each.
- 4 channels 12-bit sigma-delta analog to digital converter, single channel or multi channel conversion modes, single-shot or continuous conversion modes, sample rate 1 kHz, conversion range 0-2.5 V .
- Three serial communication interfaces (UART) allow full duplex, asynchronous, communications with external devices, independently programmable TX and RX baud rates up to 625 Kbaud.
- One UART adapted to suit smart card interface needs, for asynchronous SC as defined by ISO 7816-3. It includes SC clock generation.
- Two serial peripheral interfaces (SPI) allow full duplex, synchronous communications with external devices, master or slave operation, max baud rate of 5.5 Mb/s. One SPI may be used as multimedia card interface.

- Two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 KHz), 7/10 bit addressing modes. One I^2C Interface is multiplexed with one SPI, so either 2 x SPI + 1 x I^2C or 1 x SPI + 2 x I^2C may be used at a time.
- Enhanced interrupt controller supports 32 interrupt vectors, independently maskable, with interrupt vector table for faster response and 16 priority levels, software programmable for each source. Up to 2 maskable interrupts may be mapped on FIQ.
- Wakeup unit allows exiting from power down modes by detection of an event on two external pins (one is active high and other is active low) or on internal real time clock alarm.
- USB unit V1.1 compliant, software configurable endpoint setting, USB suspend/resume support
- High level data link controller (HDLC) unit supports full duplex operating mode, NRZ, NRZI, FM0 and MANCHESTER modes, and internal 8-bit baud rate generator.

2 Pin description

2.1 Logic symbol

Figure 1. STA2058 TESEO symbol



3 System block diagram

Figure 2. STA2058 TESEO block diagram

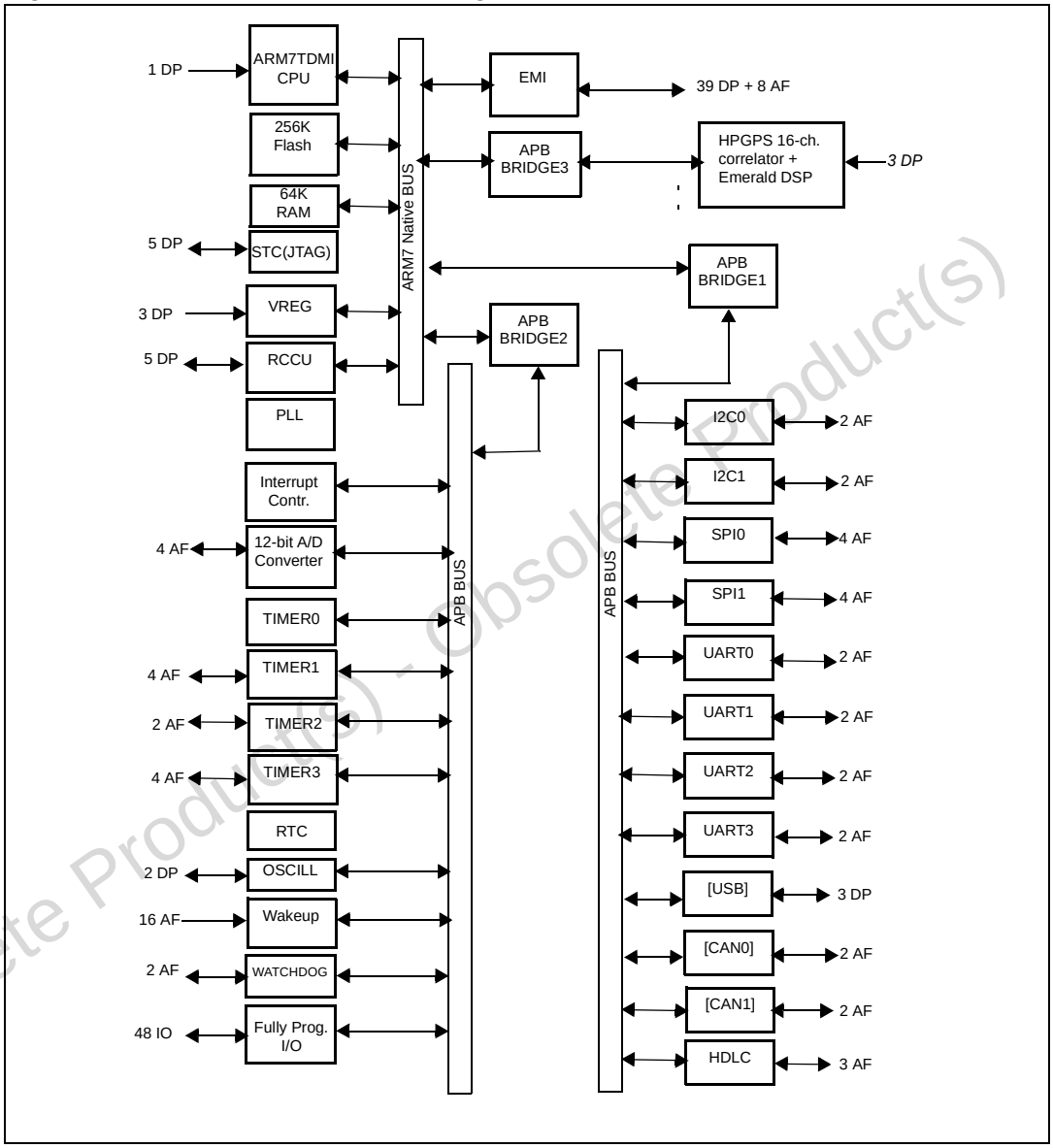
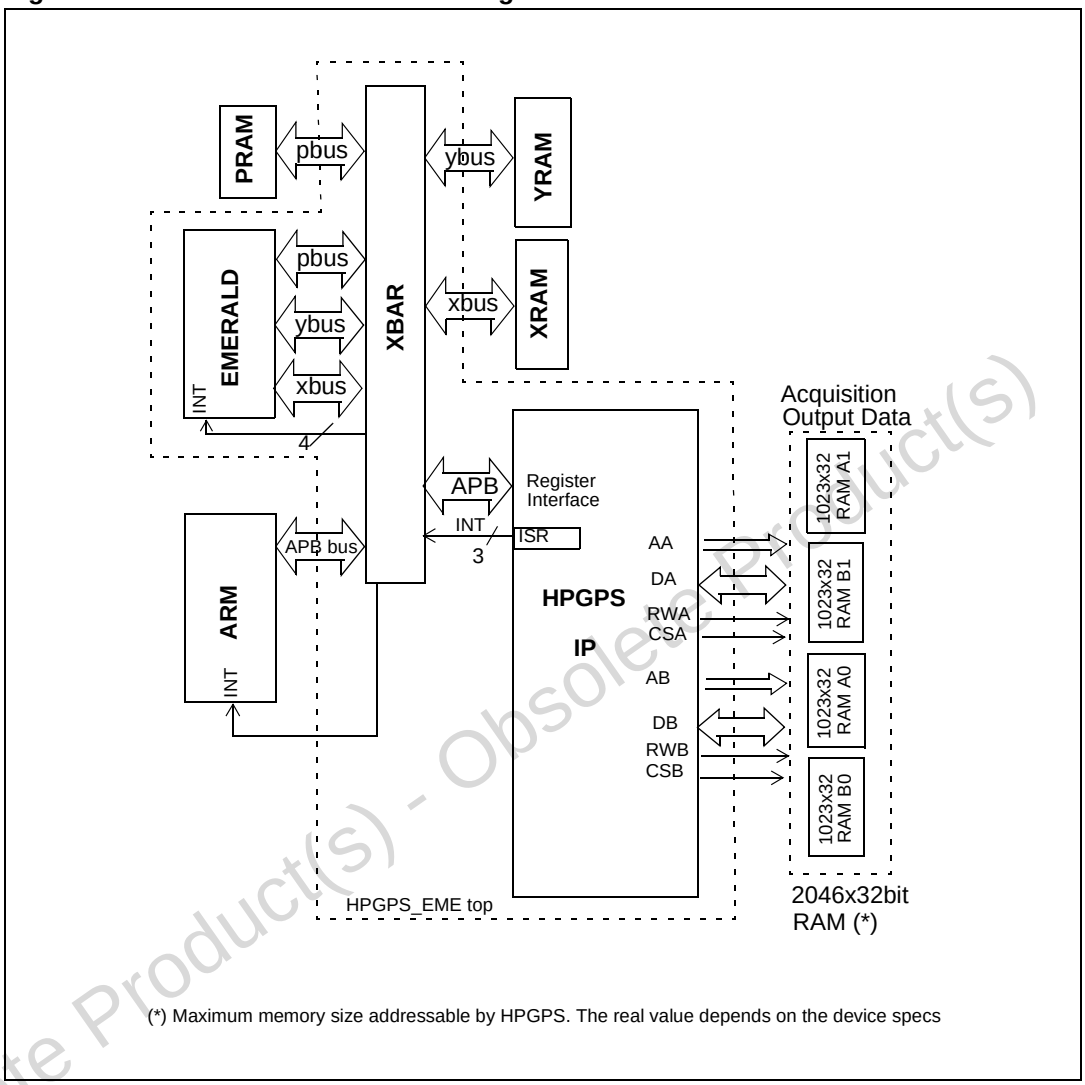


Figure 3. New HPGPS 16-ch including Emerald DSP 16-bit



(*) Maximum memory size addressable by HPGPS. The real value depends on the device specs

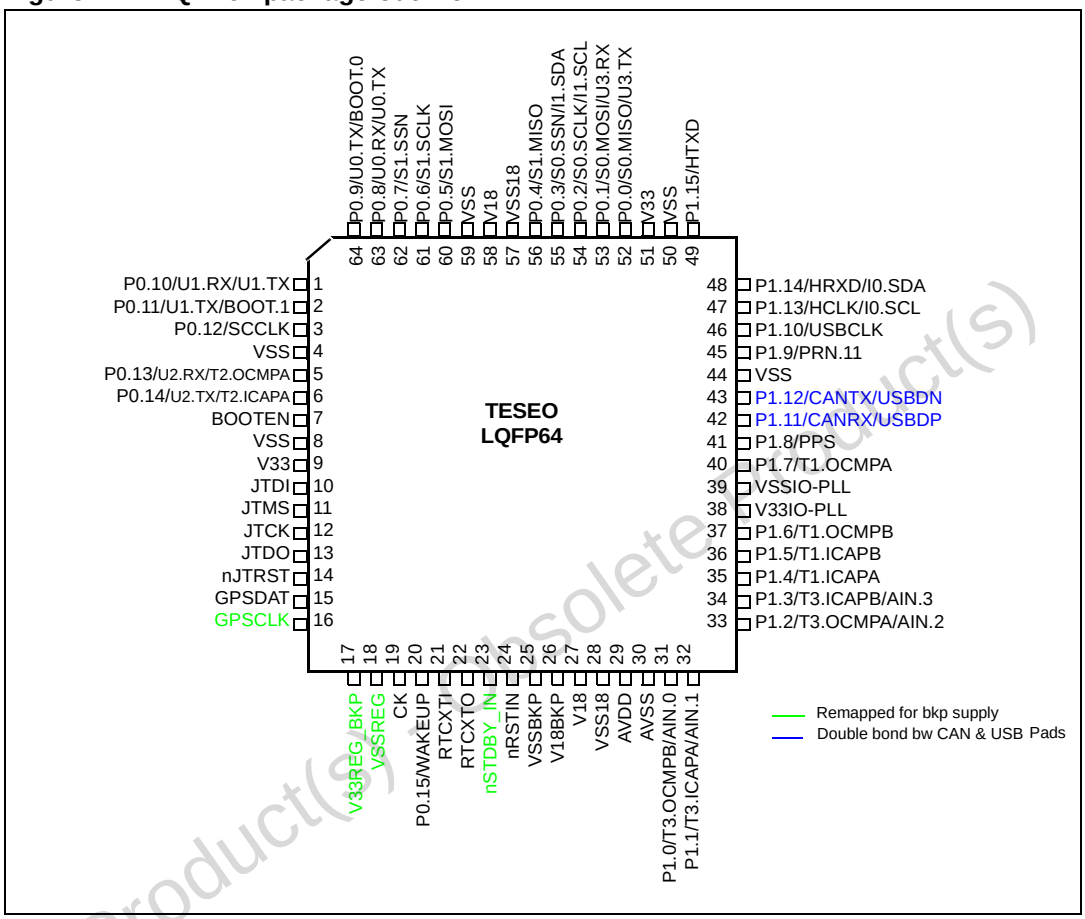
3.1 Package LFBGA144

Table 2. Ball out for LFBGA144 package

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10/ U1.RX/ U1.TX	P2.0/ CSn.0	P2.1/ CSn.1	VSS	P2.2/ CSn.2	P2.6/ A.22	BOOTEN	P2.12	P2.13	P2.15	JTDI	NC
2	VSS	RDN	P0.11/ U1.TX/ BOOT.1	V33	P2.3/ CSn.3	P2.8	P2.9/ CAN1_TX	JTMS	JTRSTn	GPSCLK	GPSDAT1	V33REG_BKP
3	V33	P0.9/ U0.TX/ BOOT.0	P0.12/ SCCLK	P0.13/ U2.RX/ T2.OCMPA	P2.4/ A.20	NC	P2.10/ CAN1_RX	JTCK	GPSDAT0	V33	VSSREG	DBGRQS
4	P0.6/ S1.SCLK	P0.7/ S1.SSN	P0.8/ U0.RX/U0.TX	P0.14/ U2.TX/ T2.ICAPA	P2.5/ A.21	VSS	P2.11	JTDO	CK	CKOUT	VSS	VSS
5	A.19	WEn.1	WEn.0	P0.5/ S1.MOSI	P2.7/ A.23	VSS	P2.14	NC	RTCXTO	RTCXTI	WAKEUP_PA	P0.15/ WAKEUP
6	P0.3/ S0.SSN/ I1.SDA	A.15	A.16	A.17	A.18	V33	V18	V18	V18BKP	V18BKP	VSSBKP	nSTDBY_IN
7	P0.2/ S0.SCLK/ I1.SCL	P0.1/ S0.MOSI/ U3.RX	P0.4/ S1.MISO	VSS	V18	A.14	D.12	D.1	D.0	nSTDBY_O	VSS18	RSTINn
8	A.9	A.10	A.11	A.13	P0.0/ S0.MISO/ U3.TX	A.0	D.11	P1.12/ CANTX	AVSS	AVSS	D.3	D.2
9	VSS18	V33	A.5	A.6	V33	D.15	D.10	P1.8/ PPS	D.9	P1.0/ T3.OCMPB/ AIN.0	NC	AVDD
10	A.8	V33	P1.15/ HTXD	P1.13/ HCLK/ I0.SCL	VSS	D.14	USBDN	P1.7/ T1.OCMPB	D.8	P1.5/ T1.ICAPB	P1.1/ T3.ICAPA/ AIN.1	D.4
11	A.7	NC	P1.14/ HRXD/ I0.SDA	P1.10/ USBCLK	A.2	D.13	USBDP	VSSIO-PLL	D.5	P1.4/ T1.ICAPA	P1.3/ T3.ICAPB/ AIN.3	AVDD
12	A.12	A.4	A.3	P1.9/ PRN.11	A.1	P1.11/ CANRX	NC	V33IO-PLL	P1.6/ T1.OCMPA	D.7	D.6	P1.2/ T3.OCMPA/ AIN.2

3.2 Package LQFP64

Figure 4. LQFP64 package outline



3.3 Power supply pins

Table 3. Power supply pins

Symbol	I/O	Function	LQFP 64	LFBGA144
V_{33}	-	Digital supply voltage for I/O circuitry (3.3 Volt)	9, 51	D2,A3,K3,F6,B9, E9,B10
V_{SS}	-	Digital ground for I/O circuitry	4, 8, 44, 50, 59	D1,A2,F4,L4,M4, F5, D7,E10
$V_{33IO-PLL}$	-	Digital supply voltage for I/O circuitry and for PLL reference (3.3V)	38	H12
$V_{SSIO-PLL}$	-	Digital ground for I/O circuitry and for PLL reference	39	H11
V_{33REG_BKP}	-	Digital supply voltage for backup block I/O circuitry and for ballast I/O (3.3V)	17	M2
V_{SSREG}	-	Digital ground for ballast I/O	18	L3
V_{18}	-	Digital supply voltage for core circuitry (1.8 Volt): when using the internal voltage regulator, this pin shall not be driven by an external voltage supply, but a capacitance of at least 10µF (tantalum, low series resistance) + 33nF (ceramic) shall be connected between these pins and V_{SS18} to guarantee on-chip voltage stability.	27, 58	G6, H6,E7
V_{SS18}	-	Digital Ground for core circuitry	28, 57	A9,L7
V_{18BKP}	-	Digital supply voltage for backup block (RTC, oscillator, Wake-up controller - 1.8 Volt): when using the internal voltage regulator, this pin shall not be driven by an external voltage supply, but a capacitance of at least 1µF shall be connected between this pin and V_{SSBKP} to guarantee on-chip voltage stability.	26	J6,K6
V_{SSBKP}	-	Digital Ground for backup logic	25	L6
AV_{DD}	-	Analog supply voltage for the A/D converter	29	M9, M11
AV_{SS}	-	Analog supply Ground for the A/D converter	30	J8,K8

Note: V_{33} and $V_{33IO-PLL}$ are all internally connected. Same for V_{SS} and $V_{SSIO-PLL}$.

All V_{SS}, V_{SS18}, V_{SSBKP}, AV_{ss} pins must be tied together to the common ground plane, taking care of noise filtering, especially on AV_{SS}

4 Electrical characteristic

4.1 DC electrical characteristic

V_{33} = 3.3 V ± 10 %, T_A = -40 / 85 °C unless otherwise specified.

Table 4. DC electrical characteristic

Symbol	Parameter	Test conditions	Value			
			Min.	Typ.	Max.	Unit
V_{IH}	Input high level CMOS	With or w/o hysteresis	$0.7V_{33}$			V
	Input high level	P0.15 (WAKEUP) only	1.8			V
V_{IL}	Input low level CMOS	With or w/o hysteresis			$0.3V_{33}$	V
	Input low level	P0.15 (WAKEUP) only			0.7	V
V_{HYS}	Input hysteresis CMOS Schmitt trigger		0.4	0.8	1.2	V
	Input hysteresis Schmitt trigger	P0.15 (WAKEUP) only	0.3	0.5		V
V_{OH}	Output high level high current pins	Push Pull, I_{OH}= 8mA	V_{33}-0.8			
	Output high level standard current pins	Push Pull, I_{OH}= 4mA	V_{33}-0.8			
V_{OL}	Output low level standard current pins	Push Pull, I_{OH}= 8mA			0.4	V
		Push Pull, I_{OH}= 4mA			0.4	V
R_{WPU}	Weak pull-up resistor	Measured at $0.5V_{33}$		100		kΩ
R_{WPD}	Weak pull-down resistor	Measured at $0.5V_{33}$		100		kΩ

4.2 AC electrical characteristics

Table 5. AC electrical characteristics

V_{33} = 3.3 V ± 10 %, T_A = 27 °C unless otherwise specified.

Symbol	Mode	System clock	Value			Unit
			Min.	Typ.	Max.	
I_{DDRUN}	RUN mode	33 MHz system clock		60		mA
I_{DDWFI}	WFI mode	1 MHz system clock		5		mA
I_{DDLP}	LPWFI mode	32 kHz system clock		300		µA
I_{DDSTP}	STOP mode	Main VReg off, Flash in power-down		200		µA
I_{DDSB1}	STANDBY_1 mode	LP VReg and 32kHz Osc on		15	30	µA
I_{DDSB0}	STANDBY_0 mode	LP VReg, LVD, 32kHz Osc bypassed		3	10	µA

Note: IDDRUN is the consumption in applications exploiting the full performances of the core. A typical GPS application would run at 33MHz, at the maximum frequency (66MHz) the power consumption is IDDRUN = 150 mA (typ).

In WFI mode the VReg and Flash are ON to guarantees the minimum interrupt response time.

Table 6. AC electrical characteristics

V_{33} = 3.3 V ± 10%, T_A = -40 / 85 °C unless otherwise specified.

Symbol	Mode	System clock	Value			Unit
			Min.	Typ.	Max.	
F_{CPU}	CPU max frequency	Executing from RAM or EMI			66	MHz
F_{MAX}	Flash max frequency	Executing from Flash			60	MHz

4.3 nRSTIN input filter characteristics

V_{33} = 3.3 V ± 10 %, T_A = -40 / 85 °C unless otherwise specified.

Table 7. nRSTIN input filter characteristics

Symbol	Mode	System clock	Value			Unit
			Min.	Typ.	Max.	
t_{FR}	nRSTIN input filtered pulse				100	ns
t_{NFR}	nRSTIN input not filtered pulse		1.2			µs

4.4 Flash electrical characteristics

V_{33} = 3.3 ± 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 8. Flash program/erase characteristics 1

Symbol	Parameter	Test conditions	Value			Unit
			Typ	Max (C_0)	Max (C_{max})	
t_{PW}	Word program		40			µs
t_{PDW}	Double word program		60			µs
t_{PB0}	Bank 0 program (256K)	Double word program	1.6	2.1	4.3	s
t_{PB1}	Bank 1 program (16K)	Double word program	130	170	300	ms
t_{ES}	Sector erase (64K)	Not preprogrammed Preprogrammed	2.3 1.9	4.0 3.3	4.9 4.1	s
t_{ES}	Sector erase (8K)	Not preprogrammed Preprogrammed	0.7 0.6	1.1 1.0	1.36 1.26	s
t_{ES}	Bank 0 erase (256K)	Not preprogrammed Preprogrammed	8.0 6.6	13.7 11.2	17.2 14.0	s
t_{ES}	Bank 1 erase (16K)	Not preprogrammed Preprogrammed	0.9 0.8	1.5 1.3	1.87 1.66	s
t_{RPD}	Recovery from power-down				20	µs
t_{PSL}	Program suspend latency				10	µs
t_{ESL}	Erase suspend latency				300	µs

Note: *C_0: T_A = 85 °C after 0 cycles*
C_{max}: T_A = 85 °C after max number of cycles

Table 9. Flash program/erase characteristics 2

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
	Endurance		10			Kcycles
	Endurance (Bank1 sectors)		100			Kcycles
	Data retention		20			Years
t_{ESR}	Erase suspend rate	Min time from erase resume to next erase suspend	20			ms

4.5 Oscillator electrical characteristics

V_{33} = 3.3 ± 10 %, T_A = -40 / 85 °C unless otherwise specified.

Figure 5. Crystal oscillator and resonator

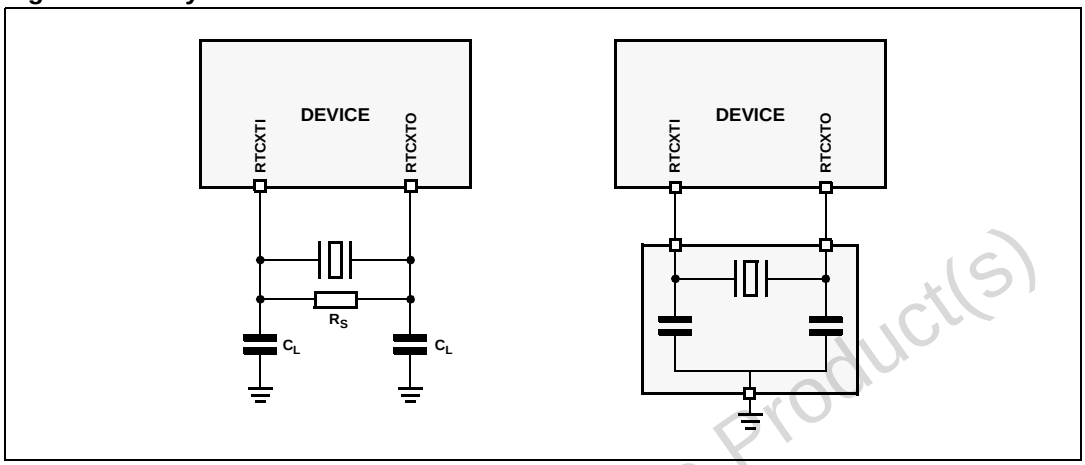


Table 10. Oscillator electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
g_m	Oscillator transconductance			8		µA/V
t_{STUP}	Oscillator startup time	Stable V_{DD}			2.5	s

4.6 ADC electrical characteristics

V_{33} = 3.3 ± 10%, A_{VDD} = 3.3V ± 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 11. ADC electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
RES	Resolution	Sinewave with ΔV_{IN} amplitude		12		bits
ΔV_{IN}	Input voltage range		0		2.5	V
F_{Mod}	Modulator oversampling frequency				2.1	MHz
IBW	Input bandwidth				$F_{Mod}/4096$	kHz
N_{ch}	Number of input channels				4	n
PBR	Passband ripple				0.1	dB
SINAD	S/N and distortion		56	63		dB
THD	Total harmonic distortion		60	74		dB

Table 11. ADC electrical characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
Z_{IN}	Input impedance	F_{Mod} = 2 MHz	1			MΩ
C_{IN}	Input capacitance				5	pF
I_{ADC}	Power consumption	T_A=27 °C		2.5	3.0	mA
I_{STBY}	Standby power consumption	T_A=27 °C			1	µA

4.7 PLL electrical characteristics

V_{33} = 3.3 ± 10 %, $V_{33IOPLL}$= 3.3 ± 10 %, T_A = -40 / 85 °C unless otherwise specified.

Table 12. PLL electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
T_{PLL1}	PLL reference clock	FREF_RANGE=0	1.5		3.0	MHz
T_{PLL2}	PLL reference clock	FREF_RANGE=1 MX[1:0]='00' or '01'	3.0		8.25	MHz
T_{PLL3}	PLL reference clock	FREF_RANGE=1 MX[1:0]='10' or '11'	3.0		6	MHz
T_{LOCK}	PLL lock time	FREF_RANGE=0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
T_{LOCK}	PLL lock time	FREF_RANGE=1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
ΔT_{JITTER}	PLL jitter (peak to peak)	T_{PLL} = 4 MHz, MX[1:0]='11' Global Output division=32 (Output Clock=2 MHz)		0.7	2	ns

4.8 LVD electrical characteristics

V_{33} = 3.3 ± 10 %, T_A = -40 / 85 °C unless otherwise specified.

Table 13. LVD electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
T_{LVD}	LVD Threshold	Main and LP LVD's		1.3		V
ΔV	VLPREG - T_{LVD}	Main regulator off	50			mV

4.9 GPS performances

V_{33} = 3.3 ± 10 %, T_A = 27 °C, unless otherwise specified

Table 14. GPS performances

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
TTFF	Reacquisition	50%, -130dBm, Fu 2ppm, Tu ± 2, Pu 30km		<1		s
	HOt start			<2.5		s
	Warm start			<34		s
	Cold start			<39		s
Accuracy	Autonomous	CEP 50%, 24hr static at -130dBm		2		m
Sensitivity	Acquisition (Warm start)	With external LNA		-146		dBm
	Tracking			-159		dBm

5 Package information

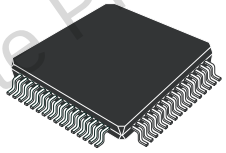
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 6. LQFP64 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7° (max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)

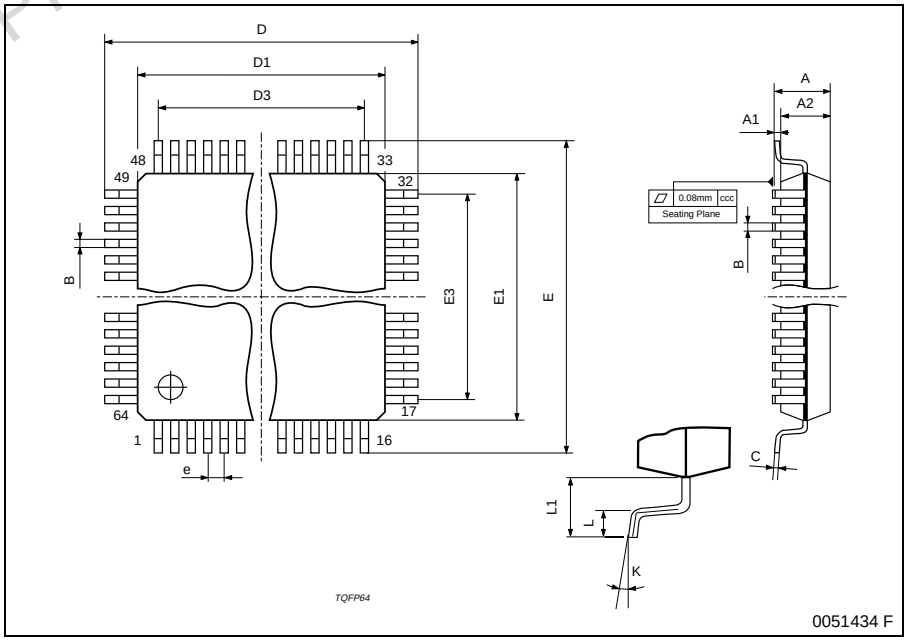
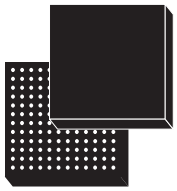


Figure 7. LFBG144 mechanical data and package dimensions

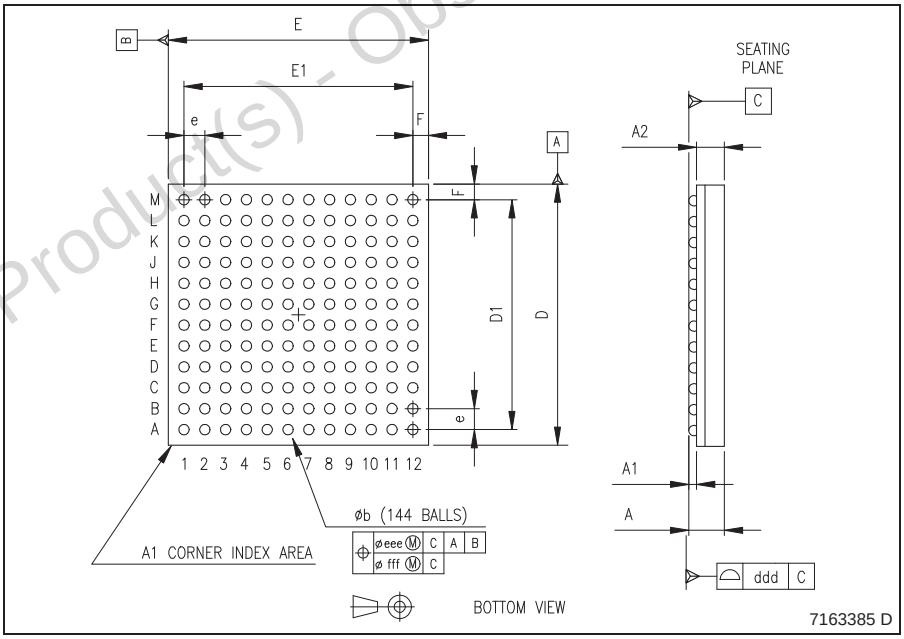
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.12			0.0441	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.0	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.0	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 10 x 10 x 1.7mm

LFBGA144
Low Profile **F**ine Pitch **B**all **G**rid **A**rray



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
23-Apr-2007	1	Initial release.
25-Jun-2007	2	Added features summary, pin description, electrical characteristics and packages information.
19-Mar-2009	3	Updated *Table 1: Device summary on page 1*. Updated ECOPACK description in *Section 5: Package information on page 17*.
22-Sep-2013	4	Updated Disclaimer.

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