# THE DATASHEET OF

# SN761681DBTG4

## FEATURES

- **Single-Chip Mixer/Oscillator and PLL Synthesizer**
- **Three-Band Local Oscillator**
- **I²C Bus Protocol (Bidirectional Data Transmission)**
- **30-V Tuning Voltage Output**
- **Four NPN-Type Band-Switch Drivers**
- **Programmable Reference Divider Ratio (512, 640, or 1024 )**
- **5-V Power Supply**
- **30-Pin TSSOP Package**

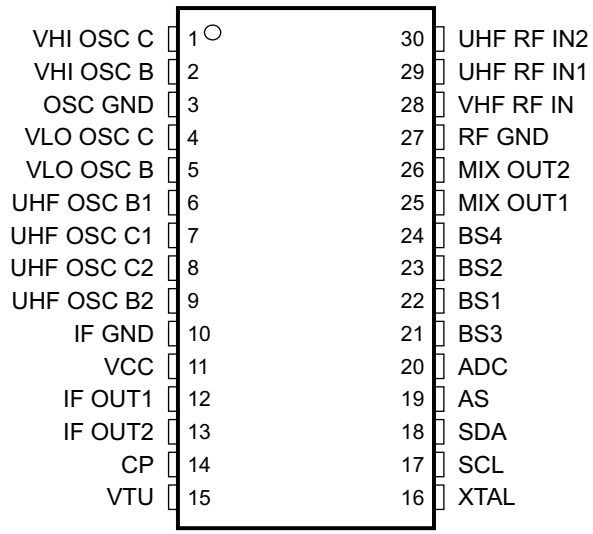
## APPLICATIONS

- **TV**
- **VCR/DVD Recorder**
- **Set-Top Box**

## DESCRIPTION

The SN761681 is a synthesized tuner IC designed for TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, 30-V output tuning amplifier, four NPN band-switch drivers, and is available in a small-outline package. A 15-bit programmable counter and reference divider are controlled by I²C bus protocol. Tuning step frequency is selectable by this reference divider ratio for a crystal oscillator.

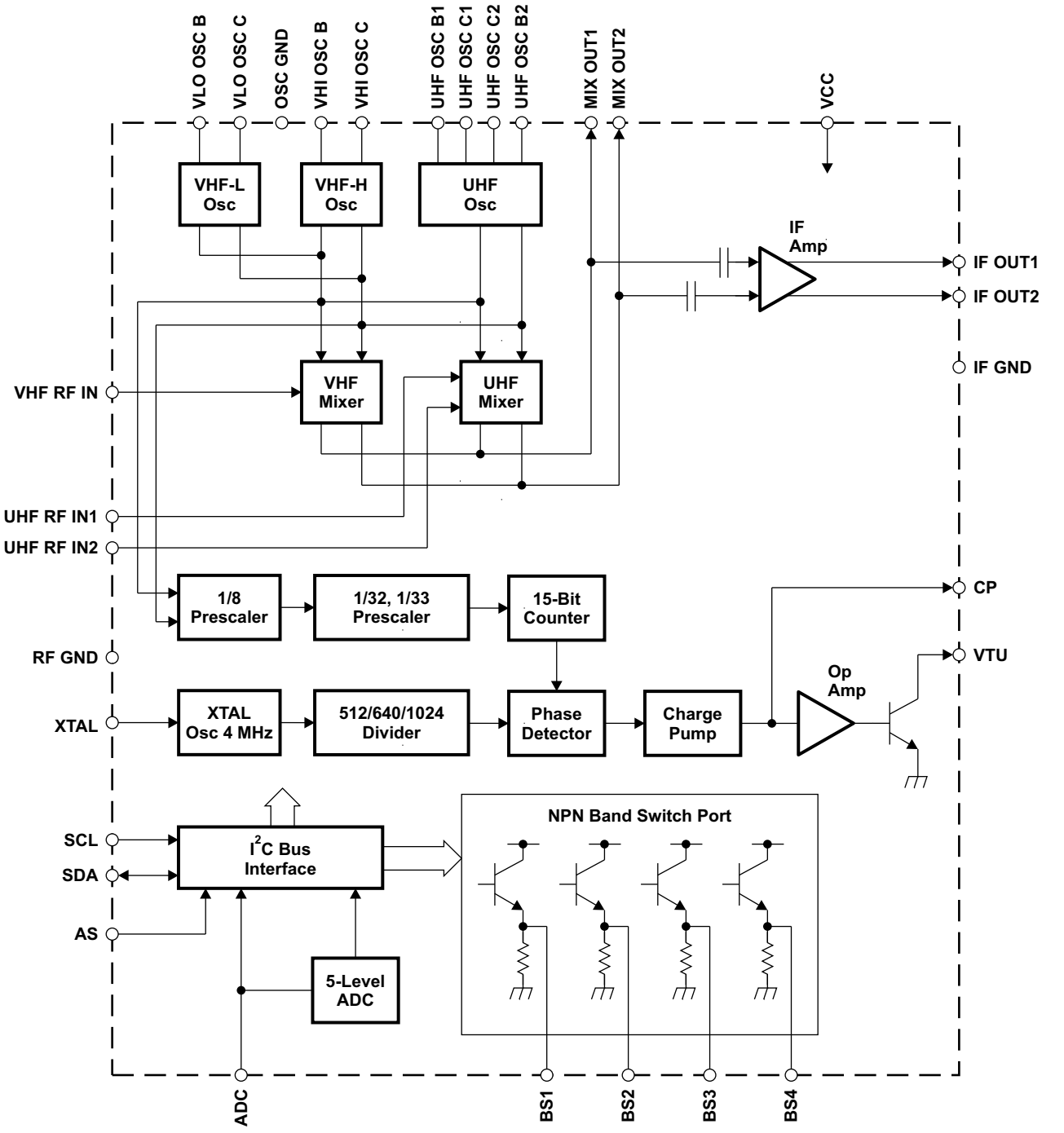
**DBT PACKAGE**
**(TOP VIEW)**




P0038-01

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

## Functional Block Diagram




B0089-02

## Pin Assignments

### Pin Description

| TERMINAL NAME | TERMINAL NO. | DESCRIPTION | SCHEMATIC |
|---|---|---|---|
| ADC | 20 | ADC input | Figure 1 |
| AS | 19 | Address selection input | Figure 2 |
| BS1 | 22 | Band switch1 output (NPN emitter follower) | Figure 3 |
| BS2 | 23 | Band switch2 output (NPN emitter follower) | Figure 3 |
| BS3 | 21 | Band switch3 output (NPN emitter follower) | Figure 3 |
| BS4 | 24 | Band switch4 output (NPN emitter follower) | Figure 3 |
| CP | 14 | Charge pump output | Figure 4 |
| IF GND | 10 | IF ground | |
| IF OUT1 | 12 | IF output | Figure 5 |
| IF OUT2 | 13 | IF output | Figure 5 |
| MIX OUT1 | 25 | Mixer output | Figure 6 |
| MIX OUT2 | 26 | Mixer output | Figure 6 |
| OSC GND | 3 | Oscillator ground | |
| RF GND | 27 | RF ground | |
| SCL | 17 | Serial clock input | Figure 7 |
| SDA | 18 | Serial data input/output | Figure 8 |
| UHF OSC B1 | 6 | UHF oscillator base1 | Figure 9 |
| UHF OSC B2 | 9 | UHF oscillator base2 | Figure 9 |
| UHF OSC C1 | 7 | UHF oscillator collector1 | Figure 9 |
| UHF OSC C2 | 8 | UHF oscillator collector2 | Figure 9 |
| UHF RF IN1 | 29 | UHF RF input | Figure 10 |
| UHF RF IN2 | 30 | UHF RF input | Figure 10 |
| VCC | 11 | Supply voltage for mixer/oscillator/PLL: 5-V | |
| VHF RF IN | 28 | VHF RF input | Figure 11 |
| VHI OSC B | 2 | VHF HIGH oscillator base | Figure 12 |
| VHI OSC C | 1 | VHF HIGH oscillator collector | Figure 12 |
| VLO OSC B | 5 | VHF LOW oscillator base | Figure 13 |
| VLO OSC C | 4 | VHF LOW oscillator collector | Figure 13 |
| VTU | 15 | Tuning voltage amplifier output | Figure 14 |
| XTAL | 16 | 4-MHz crystal oscillator input | Figure 15 |

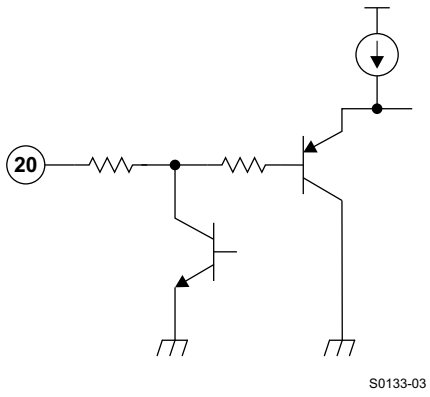



Figure 1.

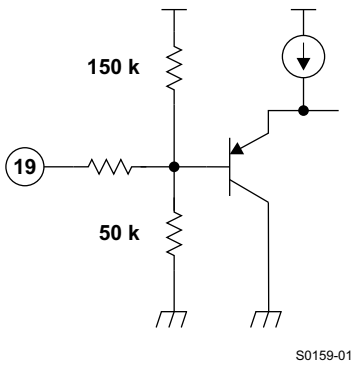



Figure 2.

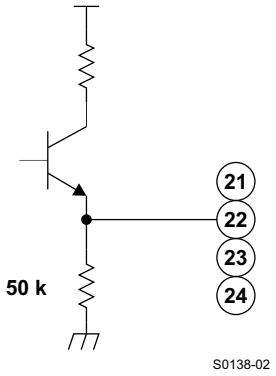



Figure 3.

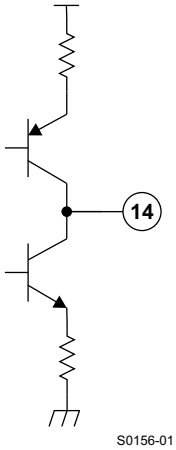



Figure 4.

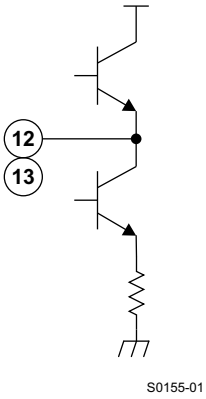



Figure 5.

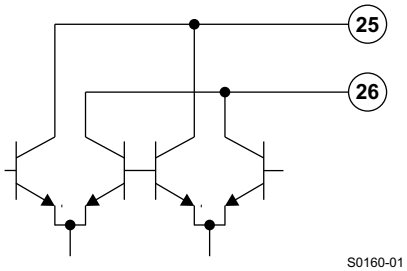



Figure 6.

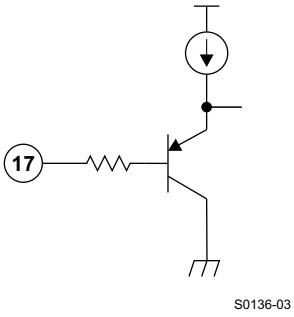



Figure 7.

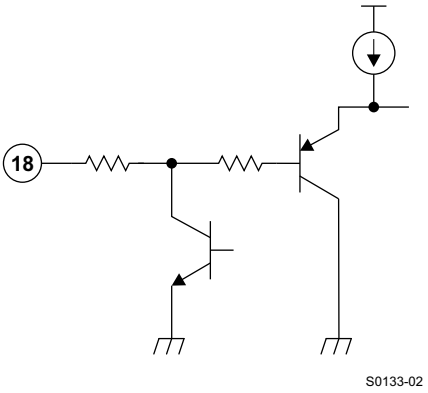



Figure 8.

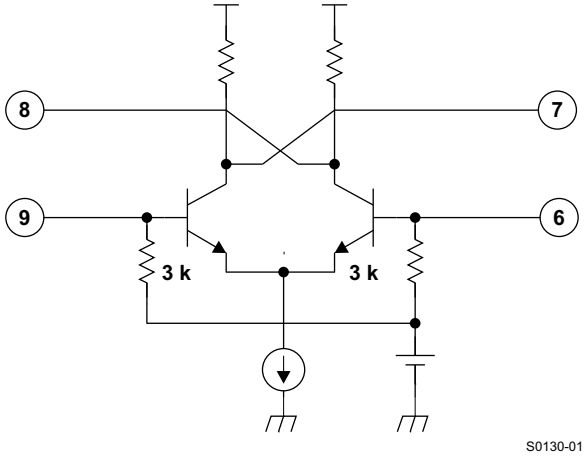



Figure 9.

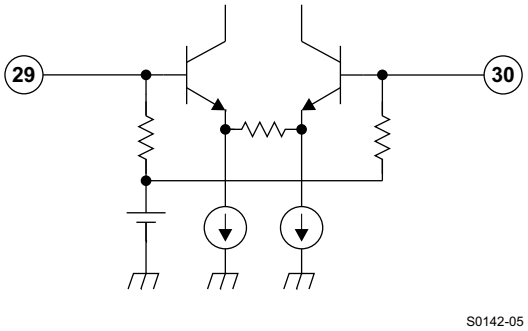



Figure 10.

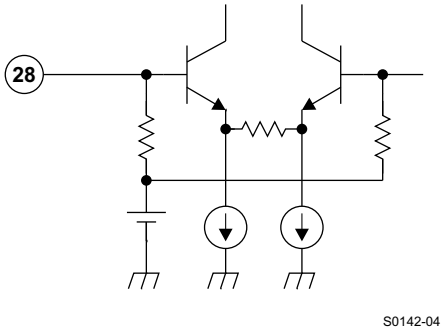



Figure 11.

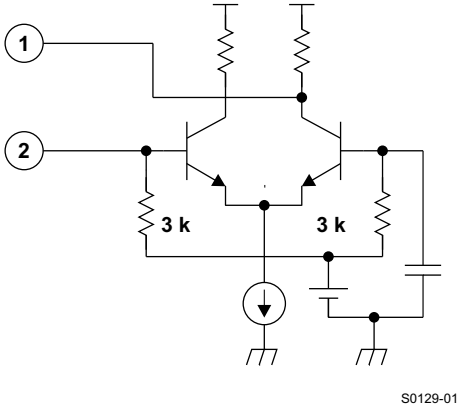



Figure 12.

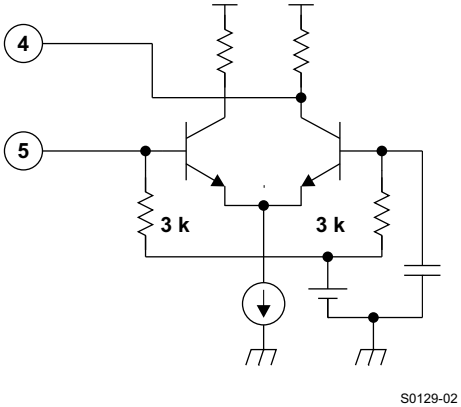



Figure 13.

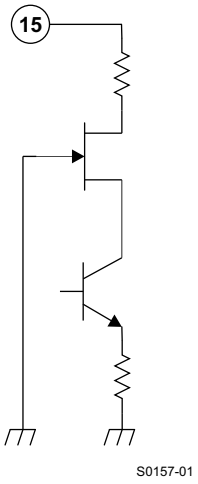



Figure 14.

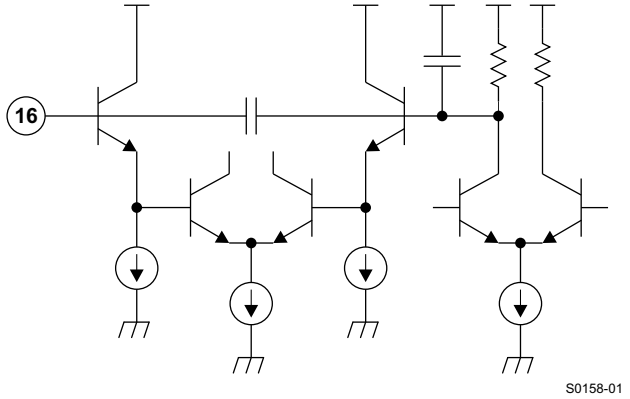



**Figure 15.**

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | |
|---|---|---|
| Supply voltage, $V_{CC}$ (2) | VCC (Pin 11) | –0.4 V to 6.5 V |
| Input voltage 1, $V_{GND}$ (2) | RF GND, OSC GND (Pins 3, 27) | –0.4 V to 0.4 V |
| Input voltage 2, $V_{VTU}$ (2) | VTU | –0.4 V to 35 V |
| Input voltage 3, $V_{IN}$ (2) | Other pins (Pins 1, 2, 4–9, 12–14, 16–26, 28–30) | –0.4 V to 6.5 V |
| Continuous total dissipation, $P_D$ (3) | $T_A \leq 25°C$ | 1071 mW |
| Operating free-air temperature, $T_A$ | | –20°C to 85°C |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |
| Maximum junction temperature, $T_J$ | | 150°C |
| Maximum short-circuit time, $t_{SC(max)}$ | Each pin to $V_{CC}$ or to GND | 10 s |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 8.57 mW/°C for $T_A \geq 25°C$.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| Tuning supply voltage, $V_{TU}$ | | | 30 | 33 | V |
| Output current of band switch, $I_{BS}$ | One port on | | | 10 | mA |
| Operating free-air temperature, $T_A$ | | –20 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS, Total Device and Serial Interface

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –20°C to 85°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}1$ | Supply current 1 | | | 60 | | mA |
| $I_{CC}2$ | Supply current 2 | One band switch on ($I_{BS}$ = 10 mA) | | 70 | | mA |
| $V_{IH}$ | High-level input voltage (SCL, SDA) | | 2.8 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (SCL, SDA) | | | | 1.4 | V |
| $I_{IH}$ | High-level input current (SCL, SDA) | | | | 10 | µA |
| $I_{IL}$ | Low-level input current (SCL, SDA) | | –10 | | | µA |
| $V_{POR}$ | Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode) | | 2.1 | 2.8 | 3.5 | V |
| **I²C INTERFACE** | | | | | | |
| $V_{ASH}$ | Address-select high-input voltage (AS) | $V_{CC}$ = 5 V | 4.5 | | 5 | V |
| $V_{ASM1}$ | Address-select mid1-input voltage (AS) | $V_{CC}$ = 5 V | 2 | | 3 | V |
| $V_{ASM2}$ | Address-select mid2-input voltage (AS) | $V_{CC}$ = 5 V | 1 | | 1.5 | V |
| $V_{ASL}$ | Address-select low-input voltage (AS) | $V_{CC}$ = 5 V | | | 0.5 | V |
| $I_{ASH}$ | Address-select high-input current (AS) | | | | 140 | µA |
| $I_{ASL}$ | Address-select low-input current (AS) | | –50 | | | µA |
| $V_{ADC}$ | ADC input voltage | See Table 8 | 0 | | $V_{CC}$ | V |
| $I_{ADH}$ | ADC high-level input current | $V_{ADC}$ = $V_{CC}$ | | | 10 | µA |
| $I_{ADL}$ | ADC low-level input current | $V_{ADC}$ = 0 V | –50 | | | µA |
| $V_{OL}$ | Low-level output voltage (SDA) | $V_{CC}$ = 5 V, $I_{OL}$ = 3 mA | | | 0.4 | V |
| $I_{SDAH}$ | High-level output leakage current (SDA) | $V_{SDA}$ = 5.5 V | | | 10 | µA |
| $f_{SCL}$ | Clock frequency (SCL) | | | 100 | 400 | kHz |
| | **I²C Timing (see timing chart, Figure 16)** | | | | | |
| $t_{hd(DAT)}$ | Data hold time | | 0 | | | µs |
| $t_{(BUF)}$ | Bus free time | | 1.3 | | | µs |
| $t_{hd(STA)}$ | Start hold time | | 0.6 | | | µs |
| $t_{(Low)}$ | SCL-low hold time | | 1.3 | | | µs |
| $t_{(High)}$ | SCL-high hold time | | 0.6 | | | µs |
| $t_{su(STA)}$ | Start setup time | | 0.6 | | | µs |
| $t_{su(DAT)}$ | Data setup time | | 0.1 | | | µs |
| $t_r$ | SCL, SDA rise time | | | | 0.3 | µs |
| $t_f$ | SCL, SDA fall time | | | | 0.3 | µs |
| $t_{su(STO)}$ | Stop setup time | | 0.6 | | | µs |

## ELECTRICAL CHARACTERISTICS, PLL and Band Switch

$V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = –20°C to 85°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| N | Divider ratio | 15-bit frequency word | 256 | | 32767 | |
| $f_{XTAL}$ | Crystal oscillator frequency | $R_{XTAL}$ = 25 Ω to 300 Ω | 3.2 | 4 | 4.48 | MHz |
| $Z_{XTAL}$ | Crystal oscillator input impedance | | | 1.6 | | kΩ |
| $V_{IXTAL2}$ | Minimum reference input sensitivity (XTAL) | 4 MHz, ac coupling with 0.1 µF capacitor | | | 100 | mVp-p |
| $V_{VTUL}$ | Tuning amplifier low-level output voltage | $R_L$ = 22 kΩ, $V_{TU}$ = 33 V | 0.3 | 0.4 | 0.5 | V |
| $I_{VTUOFF}$ | Tuning amplifier leakage current (off) | OS = 1, $V_{TU}$ = 33 V | | | 10 | µA |
| $I_{CPH}$ | Charge-pump high-level input current | CP = 1 | | 280 | | µA |
| $I_{CPL}$ | Charge-pump low-level input current | CP = 0 | | 60 | | µA |
| $V_{CP}$ | Charge-pump output voltage | PLL locked | | 1.95 | | V |
| $I_{CPOFF}$ | Charge-pump leakage current | T2 = 0, T1 = 1, $V_{CP}$ = 2 V, $T_A$ = 25°C | –15 | | 15 | nA |
| $I_{BS}$ | Band-switch driver output current | | | | 10 | mA |
| $V_{BS1}$ | Band-switch driver output voltage | $I_{BS}$ = 10 mA | 3 | | | V |
| $V_{BS2}$ | | $I_{BS}$ = 10 mA, $V_{CC}$ = 5 V, $T_A$ = 25°C | 3.5 | 3.9 | | |
| $I_{BSOFF}$ | Band-switch driver leakage current | $V_{BS}$ = 0 V | | | 3 | µA |

## ELECTRICAL CHARACTERISTICS, Mixer, Oscillator, IF Amplifier

$V_{CC}$ = 5 V, $T_A$ = 25°C, measured in Figure 17 reference measurement circuit at 50-Ω system,
IF filter characteristics: $f_{peak}$ = 43 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $G_{c1}$ | Conversion gain (mixer-IF amplifier), VHF-LOW | $f_{in}$ = 58 MHz (1) | 22 | 25 | 28 | dB |
| $G_{c3}$ | | $f_{in}$ = 130 MHz (1) | 22 | 25 | 28 | |
| $G_{c4}$ | Conversion gain (mixer-IF amplifier), VHF-HIGH | $f_{in}$ = 136 MHz (1) | 22 | 25 | 28 | dB |
| $G_{c6}$ | | $f_{in}$ = 364 MHz (1) | 22 | 25 | 28 | |
| $G_{c7}$ | Conversion gain (mixer-IF amplifier), VHF-UHF | $f_{in}$ = 370 MHz (1) | 26 | 29 | 32 | dB |
| $G_{c9}$ | | $f_{in}$ = 804 MHz (1) | 25 | 28 | 31 | |
| $NF_1$ | Noise figure, VHF-LOW | $f_{in}$ = 55.25 MHz | | 9.5 | | dB |
| $NF_3$ | | $f_{in}$ = 127.25 MHz | | 9.5 | | |
| $NF_4$ | Noise figure, VHF-HIGH | $f_{in}$ = 133.25 MHz | | 10 | | dB |
| $NF_6$ | | $f_{in}$ = 361.25 MHz | | 10 | | |
| $NF_7$ | Noise figure, UHF | $f_{in}$ = 367.25 MHz | | 11 | | dB |
| $NF_9$ | | $f_{in}$ = 801.25 MHz | | 11 | | |
| $CM_1$ | 1% cross-modulation distortion, VHF-LOW | $f_{in}$ = 55.25 MHz (2) | | 89 | | dBµV |
| $CM_3$ | | $f_{in}$ = 127.25 MHz (2) | | 89 | | |
| $CM_4$ | 1% cross-modulation distortion, VHF-HIGH | $f_{in}$ = 133.25 MHz (2) | | 86 | | dBµV |
| $CM_6$ | | $f_{in}$ = 361.25 MHz (2) | | 86 | | |
| $CM_7$ | 1% cross-modulation distortion, UHF | $f_{in}$ = 367.25MHz (2) | | 87 | | dBµV |
| $CM_9$ | | $f_{in}$ = 801.25 MHz (2) | | 87 | | |
| $V_{IFO1}$ | IF output voltage, VHF-LOW | $f_{in}$ = 55.25 MHz (3) | | 117 | | dBµV |
| $V_{IFO3}$ | | $f_{in}$ = 127.25 MHz (3) | | 117 | | |
| $V_{IFO4}$ | IF output voltage, VHF-HIGH | $f_{in}$ = 133.25 MHz (3) | | 117 | | dBµV |
| $V_{IFO6}$ | | $f_{in}$ = 361.25 MHz (3) | | 117 | | |
| $V_{IFO7}$ | IF output voltage, UHF | $f_{in}$ = 367.25MHz (3) | | 117 | | dBµV |
| $V_{IFO9}$ | | $f_{in}$ = 801.25 MHz (3) | | 117 | | |
| $\Phi_{OSC1}$ | Phase noise, VHF-LOW | $f_{in}$ = 55.25 MHz (4) | | 88 | | dBc/Hz |
| $\Phi_{OSC3}$ | | $f_{in}$ = 127.25 MHz (4) | | 88 | | |
| $\Phi_{OSC4}$ | Phase noise, VHF-HIGH | $f_{in}$ = 133.25 MHz (4) | | 86 | | dBc/Hz |
| $\Phi_{OSC6}$ | | $f_{in}$ = 361.25 MHz (4) | | 86 | | |
| $\Phi_{OSC7}$ | Phase noise, UHF | $f_{in}$ = 367.25MHz (4) | | 84 | | dBc/Hz |
| $\Phi_{OSC9}$ | | $f_{in}$ = 801.25 MHz (4) | | 84 | | |
| | Prescaler beat (5) | | | | 25 | dBµV |

(1) IF = 43 MHz, RF input level = 80 dBµV
(2) $f_{undes} = f_{des} \pm 6$ MHz, $P_{in}$ = 80 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) IF = 45.75 MHz
(4) Offset = 10 kHz, RF input level = 70 dBµV
(5) Design parameter, not tested

# Functional Description

## I²C Bus Mode

### I²C Write Mode (R/$\overline{W}$ = 0)

**Table 1. Write Data Format**

| | MSB | | | | | | | LSB | (1) |
|---|---|---|---|---|---|---|---|---|---|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/$\overline{W}$ = 0 | A |
| Divider byte 1 (DB1) | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A |
| Divider byte 2 (DB2) | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A |
| Control byte (CB) | 1 | CP | T2 | T1 | T0 | RSA | RSB | OS | A |
| Band-switch byte (BB) | X | X | X | X | BS4 | BS3 | BS2 | BS1 | A |

(1) A: Acknowledge

**Table 2. Description of Data Symbols**

| SYMBOL | DESCRIPTION | DEFAULT |
|---|---|---|
| MA[1:0] | Address-set bits (see Table 3, *Address Selection*) | |
| N[14:0] | Programmable counter set bits<br>$N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$<br>Oscillation frequency = $f_r \times 8 \times N$<br>$f_r$ = Reference frequency = 4 MHz/Reference divider | N14 = N13 = N12 = ... = N0 = 0 |
| CP | Charge-pump current-set bit<br>60 µA (CP = 0), 280 µA (CP = 1) | CP = 1 |
| T[2:0] | TEST bits (see Table 4, *Test Bits*)<br>Normal mode: T2 = 0, T1 = 0, T0 = 1/0 | T[2:0] = 001 |
| RSA, RSB | Reference divider ratio selection bits<br>See Table 6, Reference Divider Ratio. | RSA = 0, RSB = 1 |
| OS | Tuning amplifier control bit<br>Tuning voltage on (OS = 0)<br>Tuning voltage off, high impedance (OS = 1) | OS = 0 |
| BS[4:1] | Band-switch control bits<br>BSn = 0: Tr = OFF BSn = 1: Tr = ON<br>Band selection by BS1, BS2, BS4<br>**BS1(VL) BS2(VH) BS4(U)**<br>1 0 0 VHF-LO<br>X 1 0 VHF-HI<br>X X 1 UHF | BSn = 0 |
| X | Don't care | |

### Table 3. Address Selection

| MA1 | MA0 | Voltage Applied on AS Input |
|---|---|---|
| 0 | 0 | LOW: 0 V to 0.1 $V_{CC}$ |
| 0 | 1 | MID2: open, or 0.2 $V_{CC}$ to 0.3 $V_{CC}$ |
| 1 | 0 | MID1: 0.4 $V_{CC}$ to 0.6 $V_{CC}$ |
| 1 | 1 | HIGH: 0.9 $V_{CC}$ to $V_{CC}$ |

### Table 4. Test Bits (1)

| T2 | T1 | T0 | Device Operation | Note |
|---|---|---|---|---|
| 0 | 0 | 0 | Normal operation | |
| 0 | 0 | 1 | Normal operation | Default |
| 0 | 1 | X | Charge pump is off. | |
| 1 | 1 | 0 | Charge pump is sink. | |
| 1 | 1 | 1 | Charge pump is source. | |
| 1 | 0 | X | Test mode | ADC not available |

(1) Not used for other bit patterns

### Table 5. Reference Divider Ratio

| RSA | RSB | Reference Divider Ratio |
|---|---|---|
| X | 0 | 640 |
| 0 | 1 | 1024 |
| 1 | 1 | 512 |

## $I^2C$ Read Mode (R/W = 1)

### Table 6. Read Data Format

| | MSB | | | | | | | LSB | (1) |
|---|---|---|---|---|---|---|---|---|---|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/$\overline{W}$ = 1 | A |
| Status byte (SB) | POR | FL | 1 | 1 | 1 | A2 | A1 | A0 | – |

(1) A: Acknowledge

### Table 7. Description of Data Symbols

| SYMBOL | DESCRIPTION | DEFAULT |
|---|---|---|
| MA[1:0] | Address-set bits (see Table 3, *Address Selection*) | |
| POR | Power-on-reset flag<br>POR set: Power on<br>POR reset: End-of-data transmission procedure | POR = 1 |
| FL | In-lock flag<br>PLL locked (FL = 1), PLL unlocked (FL = 0) | |
| A[2:0] | Digital data of ADC (see Table 8, *ADC Level*) | |

**Table 8. ADC Level**

| A2 | A1 | A0 | Voltage Applied on ADC Input(1) |
|---|---|---|---|
| 1 | 0 | 0 | 0.6 $V_{CC}$ to $V_{CC}$ |
| 0 | 1 | 1 | 0.45 $V_{CC}$ to 0.6 $V_{CC}$ |
| 0 | 1 | 0 | 0.3 $V_{CC}$ to 0.45 $V_{CC}$ |
| 0 | 0 | 1 | 0.15 $V_{CC}$ to 0.3 $V_{CC}$ |
| 0 | 0 | 0 | 0 V to 0.15 $V_{CC}$ |

(1) Accuracy is $0.03 \times V_{CC}$.

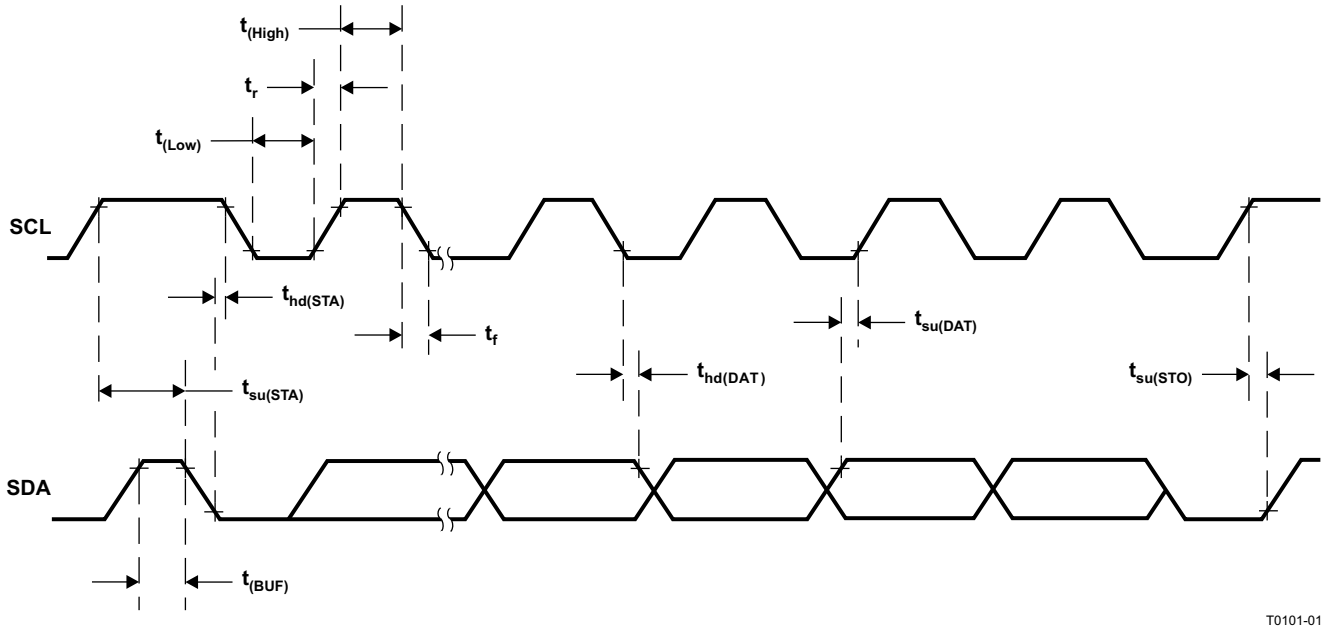
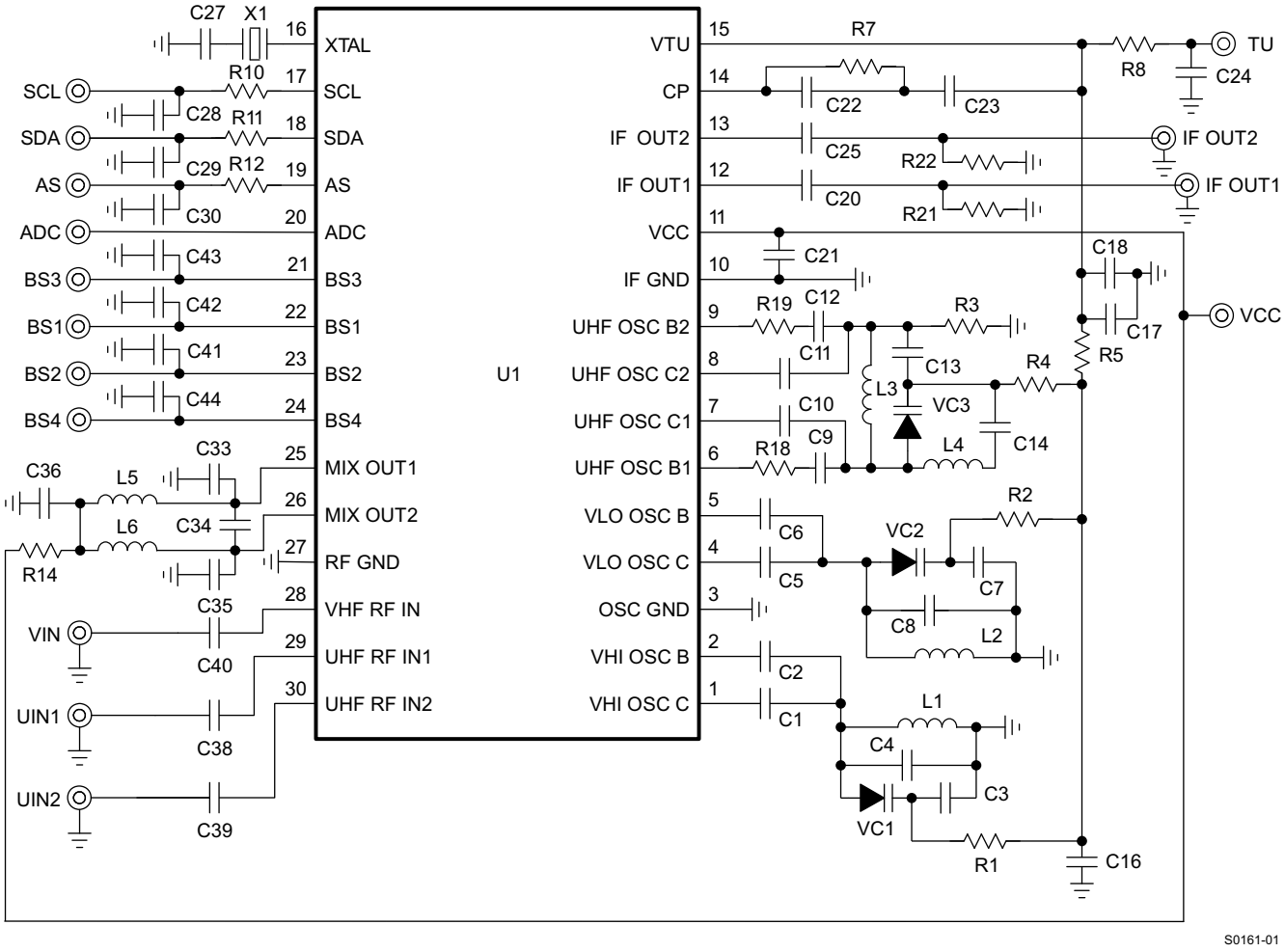



**Figure 16. $I^2C$ Timing Chart**

## APPLICATION INFORMATION

### Reference Measurement Circuit




NOTE: This application information is advisory and a performance check is required for actual application circuits. TI assumes no responsibility for the consequences of the use of this circuit nor for any infringement of patent or patent rights of third parties which may result from its use.

**Figure 17. Reference Measurement Circuit**

## APPLICATION INFORMATION (continued)

### Component Values for Measurement Circuit

| PART NAME | VALUE | PART NAME | VALUE |
|---|---|---|---|
| C1 (VHI OSC C) | 3 pF | C39 (UIN2) | 2.2 nF |
| C2 (VHI OSC B) | 2 pF | C40 (VIN) | 2.2 nF |
| C3 (VHI OSC) | 68 pF | C41 (BS2) | 2.2 nF |
| C4 (VHI OSC) | Open | C42 (BS1) | 2.2 nF |
| C5 (VLO OSC C) | 1 pF | C43 (BS3) | 2.2 nF |
| C6 (VLO OSC B) | 1 pF | C44 (BS4) | 2.2 nF |
| C7 (VLO OSC) | 47 pF | L1 (VHI OSC) | ϕ2,4 mm, 4T, wire 0,4 mm |
| C8 (VLO OSC) | 3 pF | L2 (VLO OSC) | ϕ3 mm, 8T, wire 0,32 mm |
| C9 (UHF OSC B1) | 1.5 pF | L3 (UHF OSC) | ϕ3 mm, 2T, wire 0,4 mm |
| C10 (UHF OSC C1) | 1.5 pF | L4 (UHF OSC) | ϕ2 mm, 3T, wire 0,4 mm |
| C11 (UHF OSC C2) | 1.5 pF | L5 (MIXOUT) | ϕ2,4 mm, 16T, wire 0,26 mm |
| C12 (UHF OSC B2) | 1.5 pF | L6 (MIXOUT) | ϕ2,4 mm, 16T, wire 0,26 mm |
| C13 (UHF OSC) | 12 pF | R1(VHI OSC) | 33 kΩ |
| C14 (UHF OSC) | 100 pF | R2 (VLO OSC) | 33 kΩ |
| C16 (VTU) | 2.2 nF/50 V | R3 (UHF OSC) | 22 kΩ |
| C17 (VTU) | 2.2 nF/50 V | R4 (UHF OSC) | 33 kΩ |
| C18 (VTU) | 2.2 nF/50 V | R5 (VTU) | 22 kΩ |
| C20 (IF OUT1) | 2.2 nF | R7 (CP) | 22 kΩ |
| C21 (VCC) | 4.7 nF | R8 (VTU) | 22 kΩ |
| C22 (CP) | 2.2 nF | R10 (SCL) | 330 Ω |
| C23 (CP) | 0.1 µF/50 V | R11 (SDA) | 330 Ω |
| C24 (VTU) | 2.2 nF/50 V | R12 (AS) | 330 Ω |
| C25 (IF OUT2) | 2.2 nF | R14 (MIXOUT) | 0 |
| C27 (XTAL) | 68 pF | R18 (UHF OSC) | 0 |
| C28 (SCL) | Open | R19 (UHF OSC) | 0 |
| C29 (SDA) | Open | R21 (IF OUT1) | Open |
| C30 (AS) | Open | R22 (IF OUT2) | 51 Ω |
| C33 (MIXOUT) | Open | U1 | SN761681 |
| C34 (MIXOUT) | 22 pF | VC1 (VHI OSC) | 1T363A |
| C35 (MIXOUT) | Open | VC2 (VLO OSC) | 1T363A |
| C36 (MIXOUT) | 4.7 nF | VC3 (UHF OSC) | 1T363A |
| C38 (UIN1) | 2.2 nF | X1 | 4-MHz crystal |

## Test Circuits

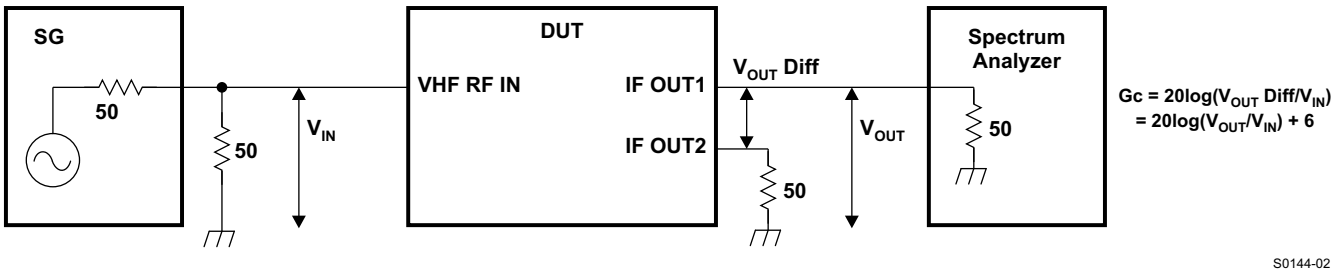



**Figure 18. VHF-Conversion Gain-Measurement Circuit**

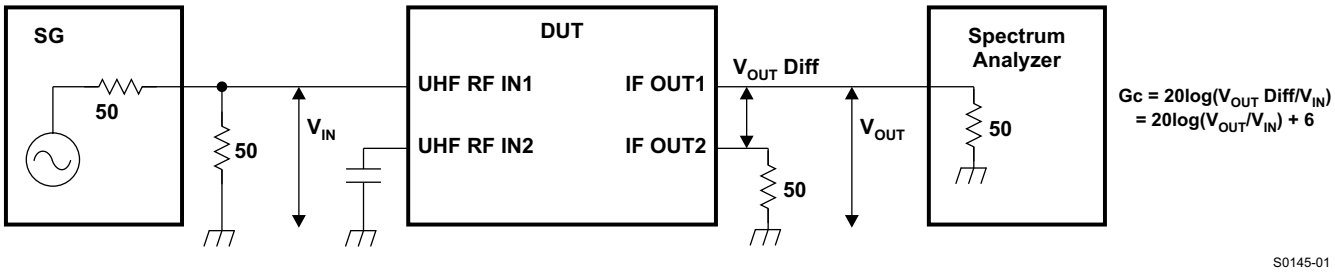



**Figure 19. UHF-Conversion Gain-Measurement Circuit**

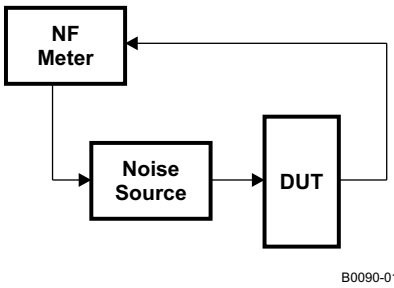



**Figure 20. Noise-Figure Measurement Circuit**

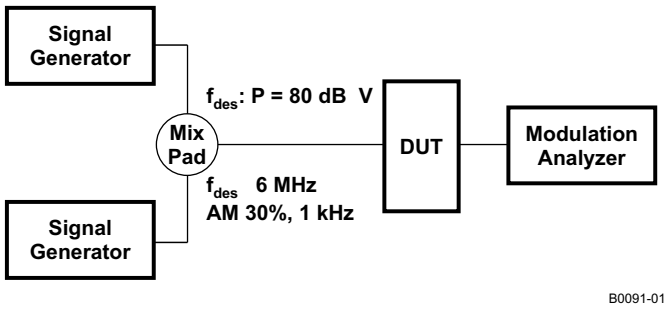



**Figure 21. 1% Cross-Modulation Distortion Measurement Circuit**

## TYPICAL CHARACTERISTICS

### Band-Switch Driver Output Voltage (BS1–BS4)

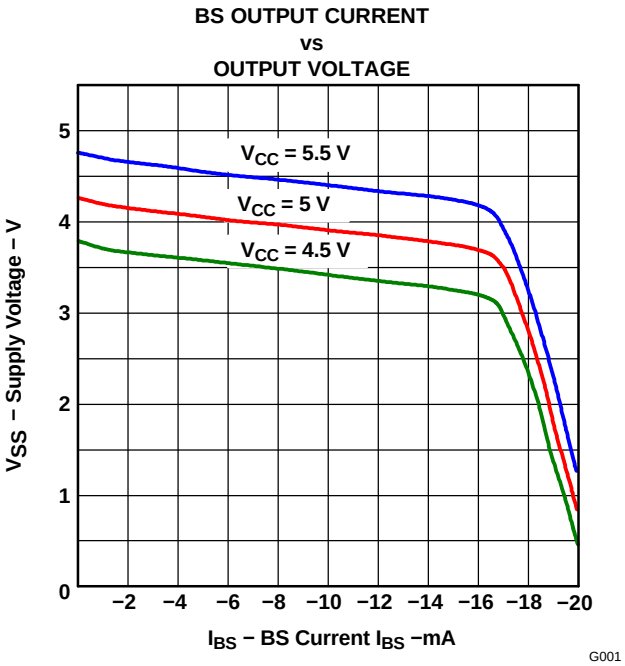



**Figure 22. Band-Switch Driver Output Voltage**

### S-Parameter

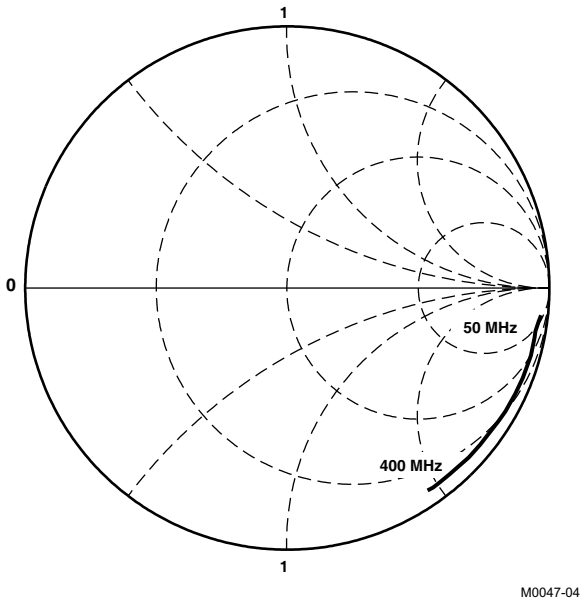



**Figure 23. VHF Input**

## TYPICAL CHARACTERISTICS (continued)

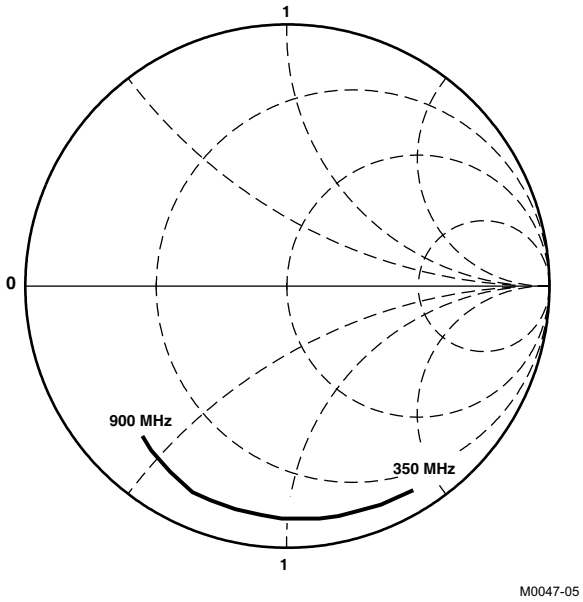



**Figure 24. UHF Input**

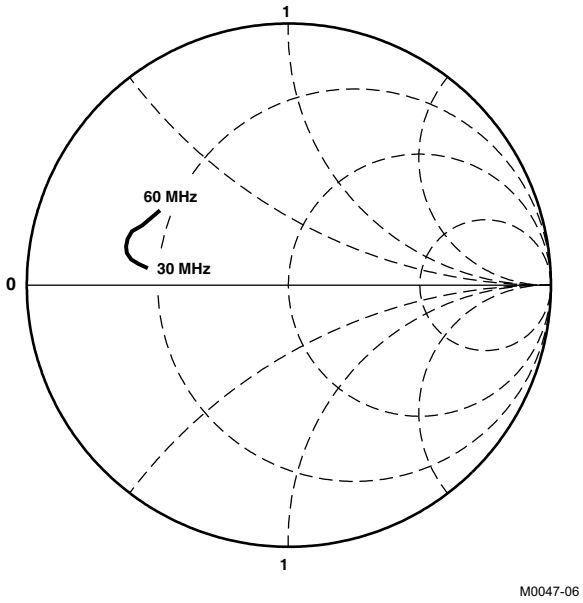



**Figure 25. IF Output**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN761681DBT | ACTIVE | TSSOP | DBT | 30 | | TBD | Call TI | Call TI | |
| SN761681DBTG4 | ACTIVE | TSSOP | DBT | 30 | | TBD | Call TI | Call TI | |
| SN761681DBTR | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| SN761681DBTRG4 | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

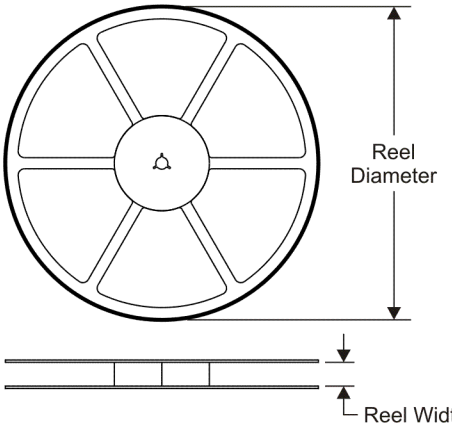
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

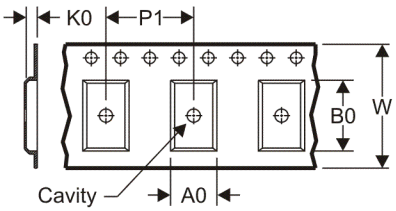
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

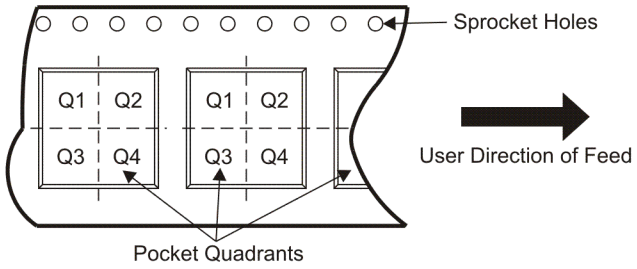



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

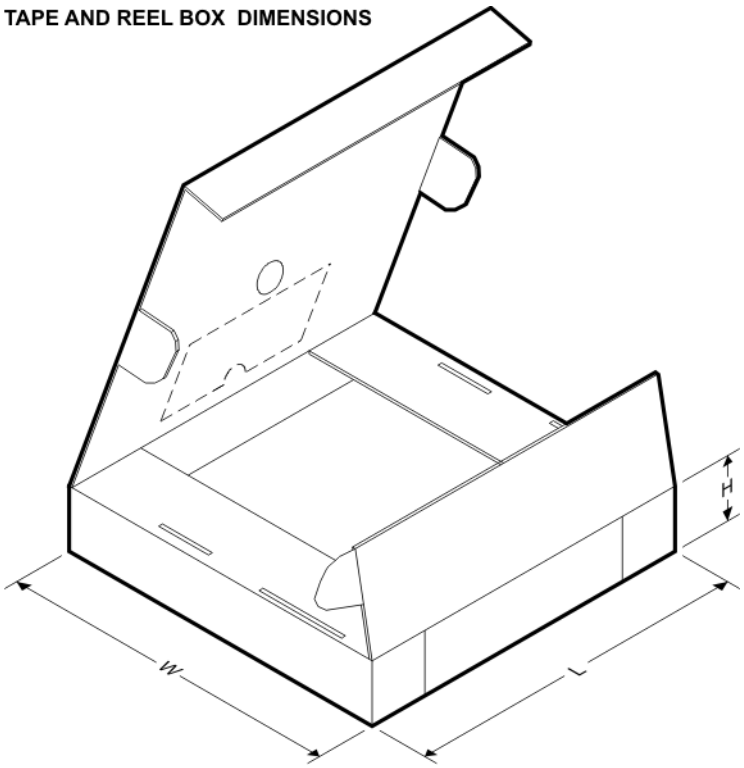
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN761681DBTR | TSSOP | DBT | 30 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

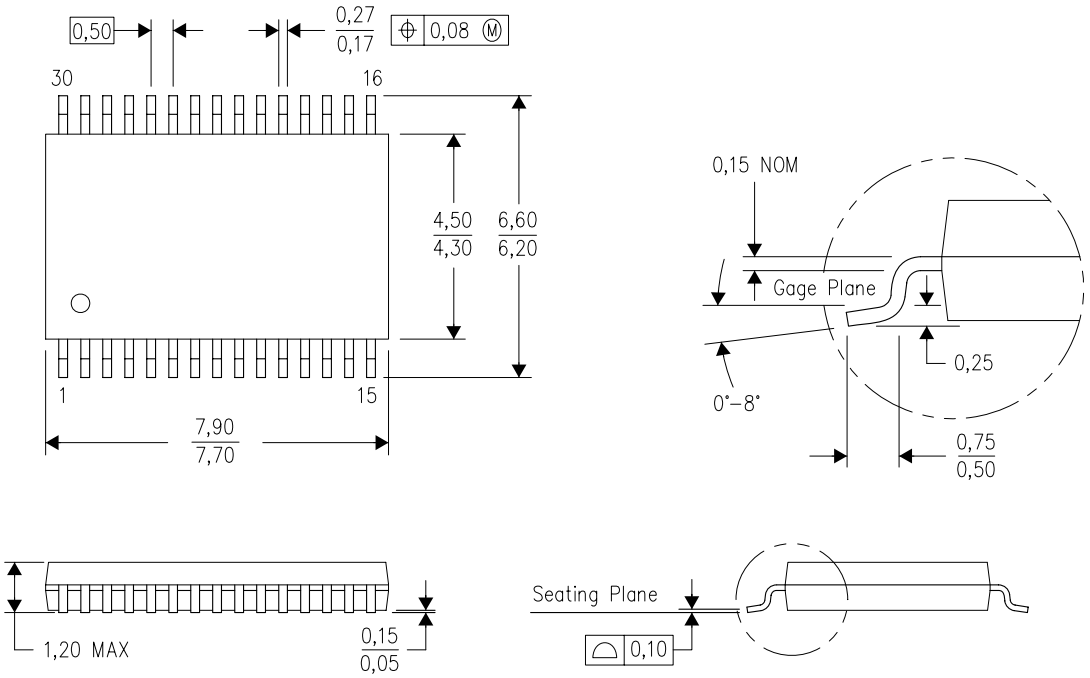
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN761681DBTR | TSSOP | DBT | 30 | 2000 | 346.0 | 346.0 | 33.0 |

DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE




4073252–5/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

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