



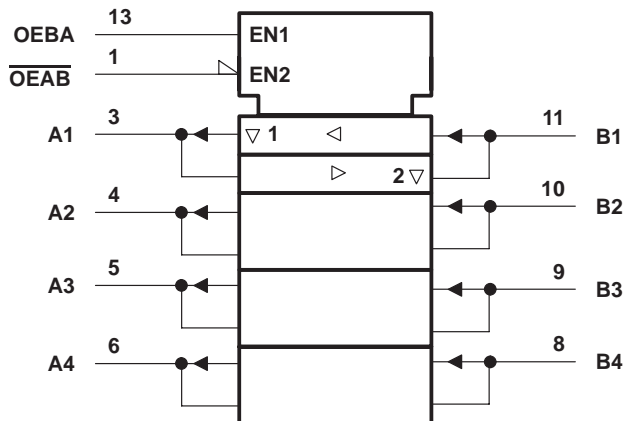
**THE DATASHEET OF
SN74ALS243ANSR**



SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

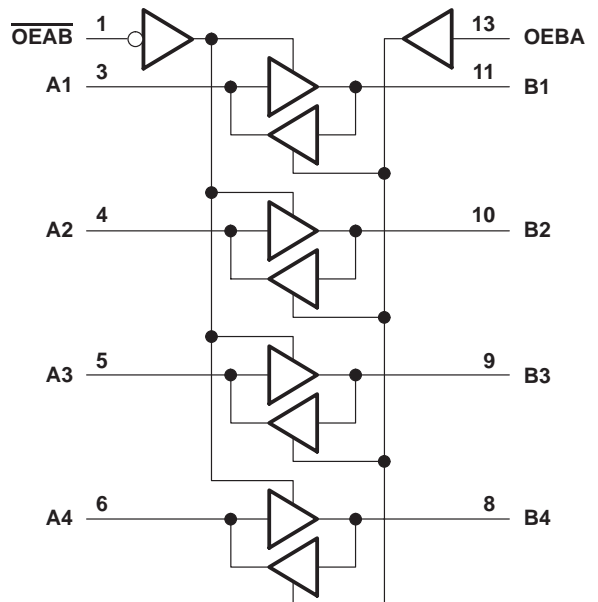
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS243A	-55°C to 125°C
SN74ALS243A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	SN54ALS243A			SN74ALS243A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-12			-15	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	-55		125	0		70	°C

SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS243A		SN74ALS243A		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$		V	
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.4	3.2	2.4	3.2		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$ $I_{OH} = -15\text{ mA}$	2		2			
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V
		$I_{OL} = 24\text{ mA}$			0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		0.1	0.1	mA
	A or B ports		$V_I = 5.5\text{ V}$		0.1	0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$		20		20	μA
	A or B ports‡			20		20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		-0.1		-0.1	mA
	A or B ports‡			-0.1		-0.1	
I_O §	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		-20	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	15	30	15	25	mA
		Outputs low	20	35	20	30	
		Outputs disabled	21	37	21	32	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}^\ddagger$				UNIT
			SN54ALS243A		SN74ALS243A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4	15	4	11	ns
t_{PHL}			4	15	4	11	
t_{PZH}	$\overline{\text{OEAB}}$	B	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	$\overline{\text{OEAB}}$	B	2	16	2	14	ns
t_{PLZ}			3	27	3	22	
t_{PZH}	OEBA	A	7	25	7	20	ns
t_{PZL}			7	25	7	20	
t_{PHZ}	OEBA	A	2	16	2	14	ns
t_{PLZ}			3	27	3	22	

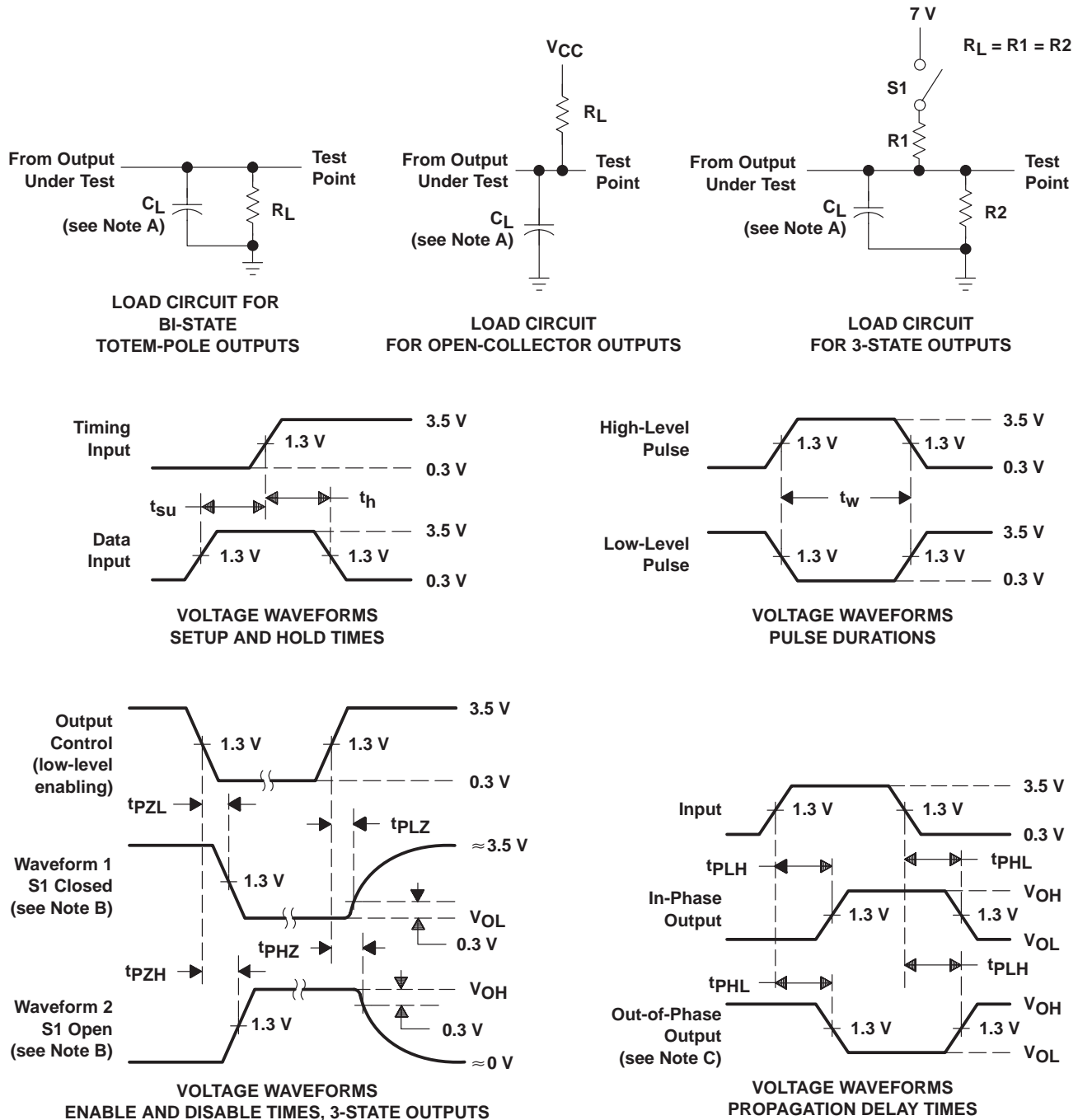
†† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84013022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK	Samples
SN74ALS243A-1N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74ALS243AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	ALS243A	
SN74ALS243AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70	SN74ALS243AN	
SN74ALS243ANSR	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI	0 to 70	ALS243A	
SNJ54ALS243AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Catalog: [SN74ALS243A](#)
- Military: [SN54ALS243A](#)

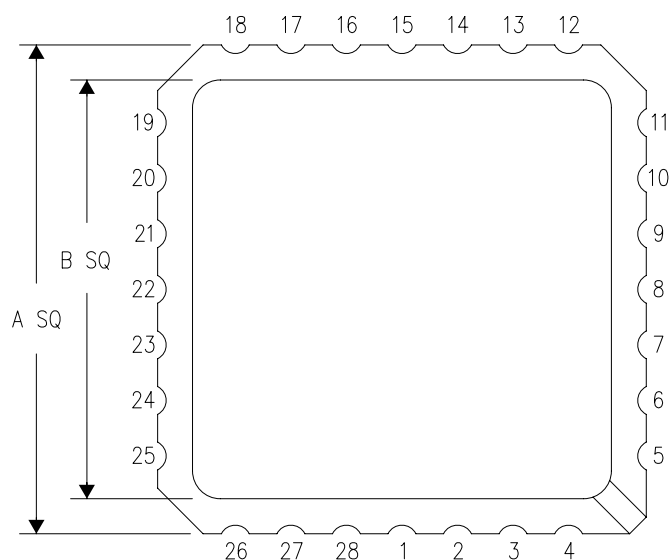
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

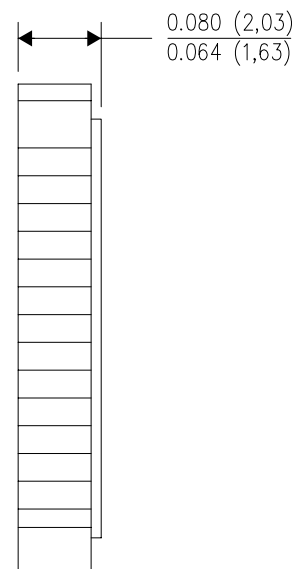
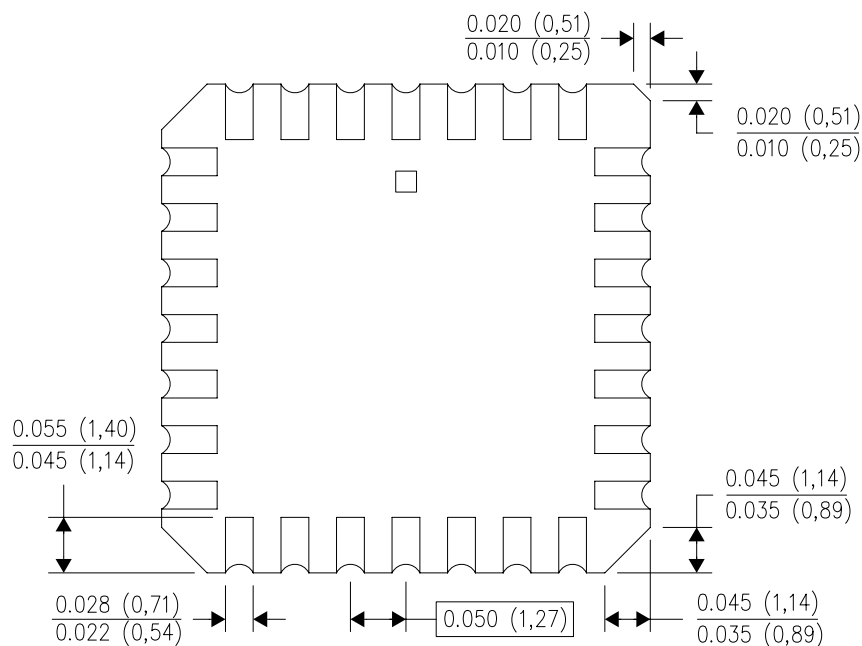
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

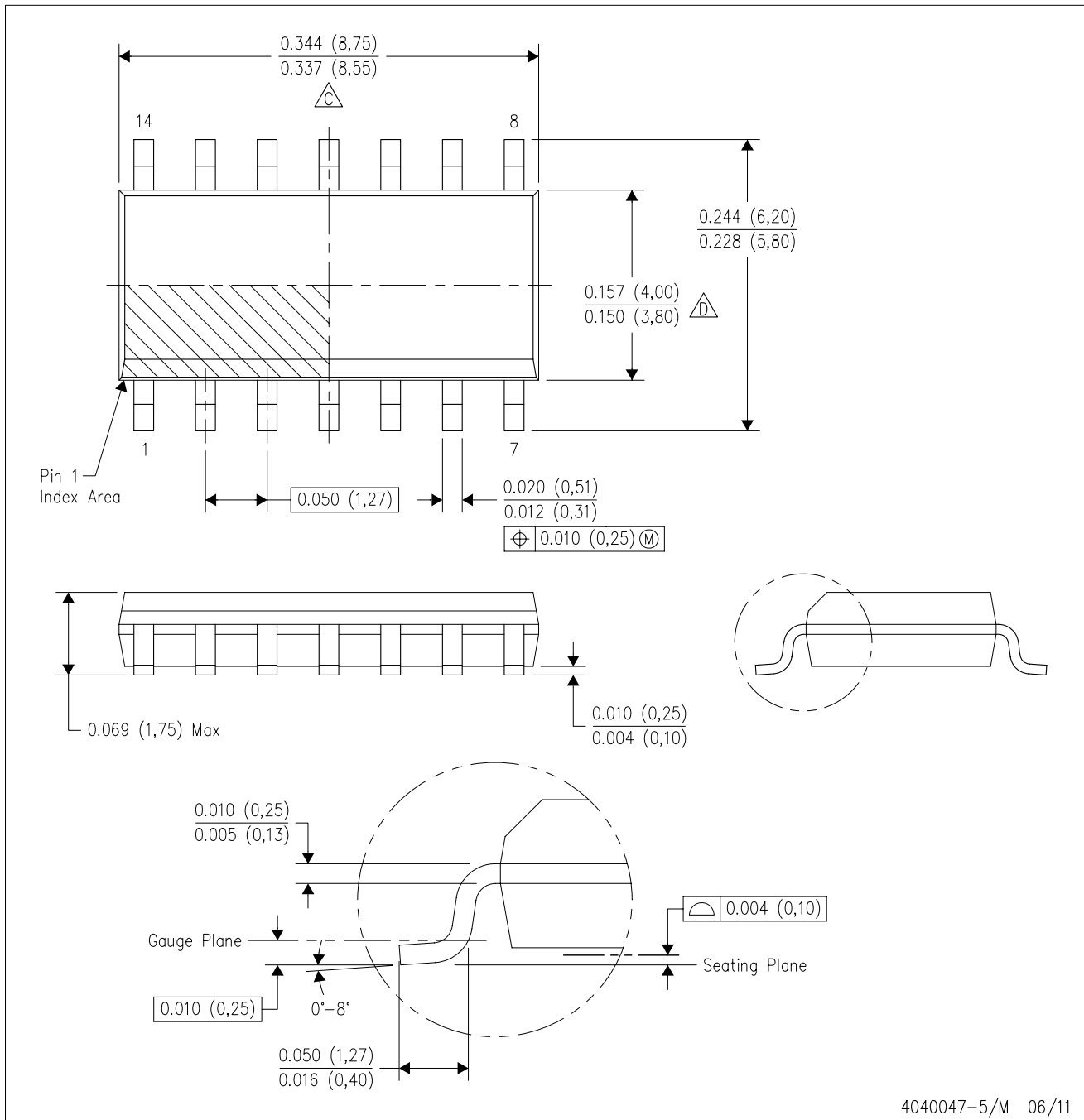
14-PINS SHOWN





- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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