



THE DATASHEET OF SN74ALS642A-1DWRE4

SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DEVICE	LOGIC
SN74ALS641A, SN74AS641	True
SN74ALS642A	Inverting

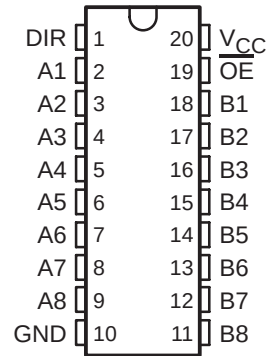
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input disables the device so that the buses are effectively isolated.

The -1 versions of the SN74ALS641A and SN74ALS642A are identical to the standard versions, except that the recommended maximum I_{OL} is increased to 48 mA in the -1 versions.

The SN74ALS641A, SN74ALS642A, and SN74AS641 are characterized for operation from 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION	
$\overline{OE}$	DIR	SN74ALS641A SN74AS641	SN74ALS642A
L	L	B data to A bus	$\overline{B}$ data to A bus
L	H	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

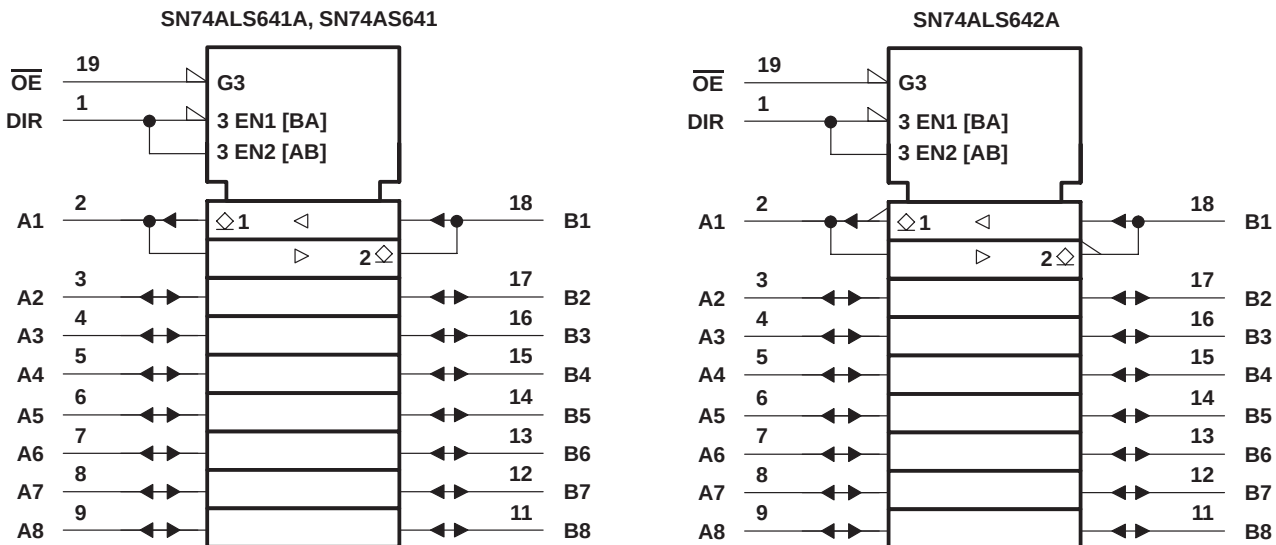
SN74ALS641A, SN74ALS642A, SN74AS641

OCTAL BUS TRANSCEIVERS

WITH OPEN-COLLECTOR OUTPUTS

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logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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The diagram shows the internal logic of the SN74ALS642A. It features four 3-input AND gates. The top two AND gates have inputs from pins 19 ($\overline{OE}$), 1 (DIR), and 2 (A1). The outputs of these two gates are connected to pins 18 (B1) and 17 (B2). The bottom two AND gates have inputs from pins 19 ($\overline{OE}$), 1 (DIR), and 2 (A1). The outputs of these two gates are connected to pins 18 (B1) and 17 (B2). The diagram also shows the connection of the output lines to the other transceivers in the bus.

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SN74ALS641A, SN74ALS642A, SN74AS641

OCTAL BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS641A SN74ALS642A		UNIT
				MIN	TYP [†] MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$		-1.5	V
I_{OH}		$V_{CC} = 4.5\text{ V}$,	$V_{OH} = 5.5\text{ V}$		0.1	mA
V_{OL}		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	V
			$I_{OL} = 24\text{ mA}$	0.35	0.5	
			$I_{OL} = 48\text{ mA}^\ddagger$	0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$		0.1	mA
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$		20	μA
	A or B ports [§]				20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$		-0.1	mA
	A or B ports [§]				-0.1	
I_{CC}	SN74ALS641A	$V_{CC} = 5.5\text{ V}$	Outputs high	25	37	mA
			Outputs low	33	47	
	SN74ALS642A	$V_{CC} = 5.5\text{ V}$	Outputs high	8	15	
			Outputs low	18	28	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX†¶				UNIT
			SN74ALS641A		SN74ALS642A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	5	25	10	30	ns
t _{PHL}			3	18	5	22	
t _{PLH}	$\overline{\text{OE}}$	A or B	8	30	10	30	ns
t _{PHL}			8	30	15	38	
t _{PLH}	DIR	A or B	8	32	10	30	ns
t _{PHL}			8	32	15	38	

[¶] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs and I/O ports	7 V
Operating free-air temperature range, T_A : SN74AS641	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS641			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS641		UNIT
				MIN	TYP [‡]	MAX
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2
I_{OH}		$V_{CC} = 4.5\text{ V}$, $V_{OH} = 5.5\text{ V}$				0.1
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$		0.35	0.55	V
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$			0.1
	A or B ports		$V_I = 5.5\text{ V}$			0.1
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20
	A or B ports [§]					70
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–0.5
	A or B ports [§]					–0.75
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high		50	82
			Outputs low		84	136

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



SN74ALS641A, SN74ALS642A, SN74AS641

OCTAL BUS TRANSCEIVERS

WITH OPEN-COLLECTOR OUTPUTS

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switching characteristics (see Figure 1)

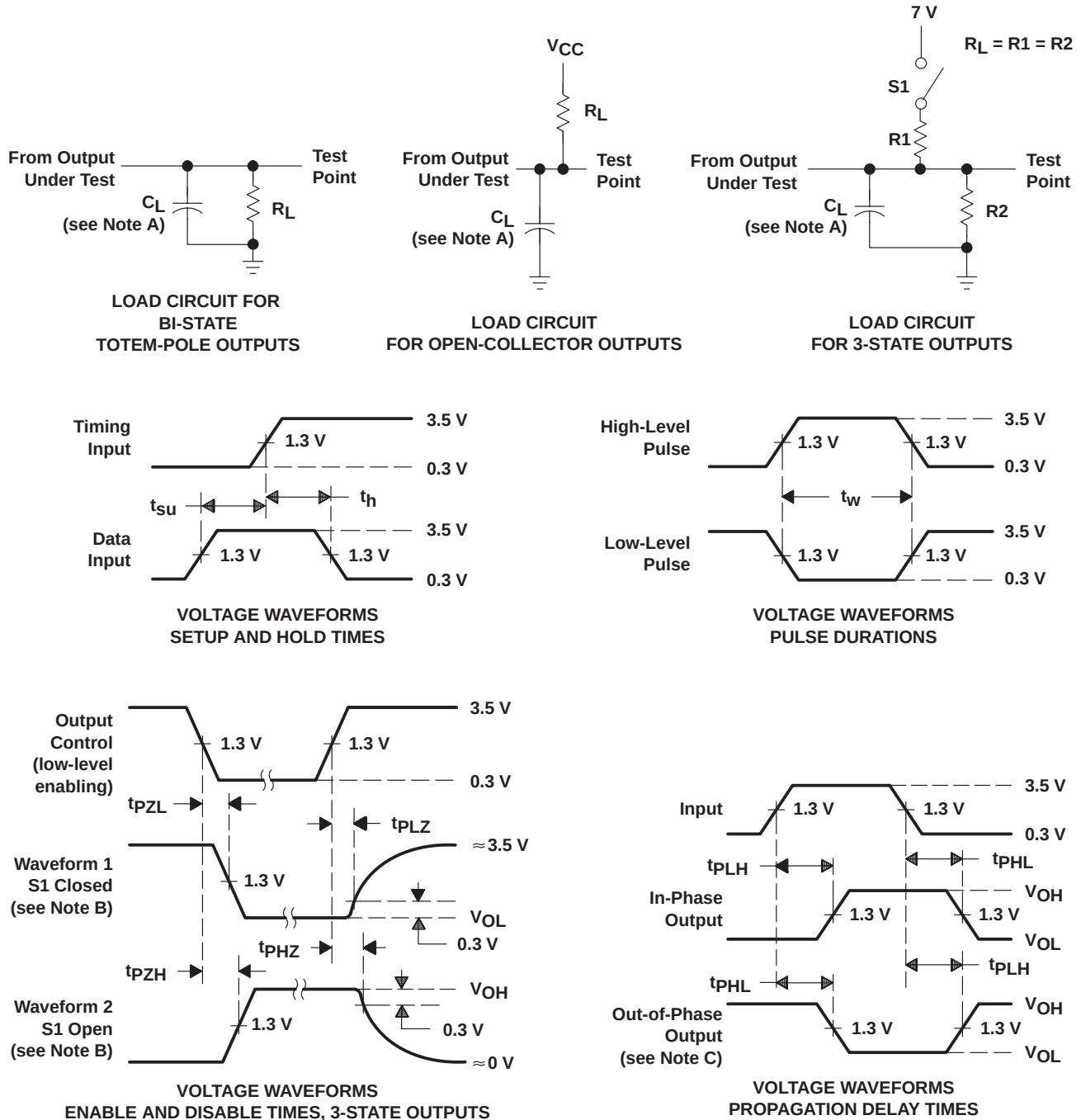
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX†		UNIT
			SN74AS641		
			MIN	MAX	
t _{PLH}	A or B	B or A	5	21	ns
t _{PHL}			1	7.5	
t _{PLH}	$\overline{\text{OE}}$	A or B	5	21	ns
t _{PHL}			1	9	
t _{PLH}	DIR	A or B	5	22	ns
t _{PHL}			1	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS641A-1DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS641A-1	Samples
SN74ALS641A-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS641A-1N	Samples
SN74ALS641A-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS641A-1	Samples
SN74ALS641ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS641A	Samples
SN74ALS641AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS641AN	Samples
SN74ALS641ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS641A	Samples
SN74ALS642A-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS642A-1	Samples
SN74ALS642A-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS642A-1N	Samples
SN74ALS642A-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS642A-1	Samples
SN74AS641DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS641	Samples
SN74AS641N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS641N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

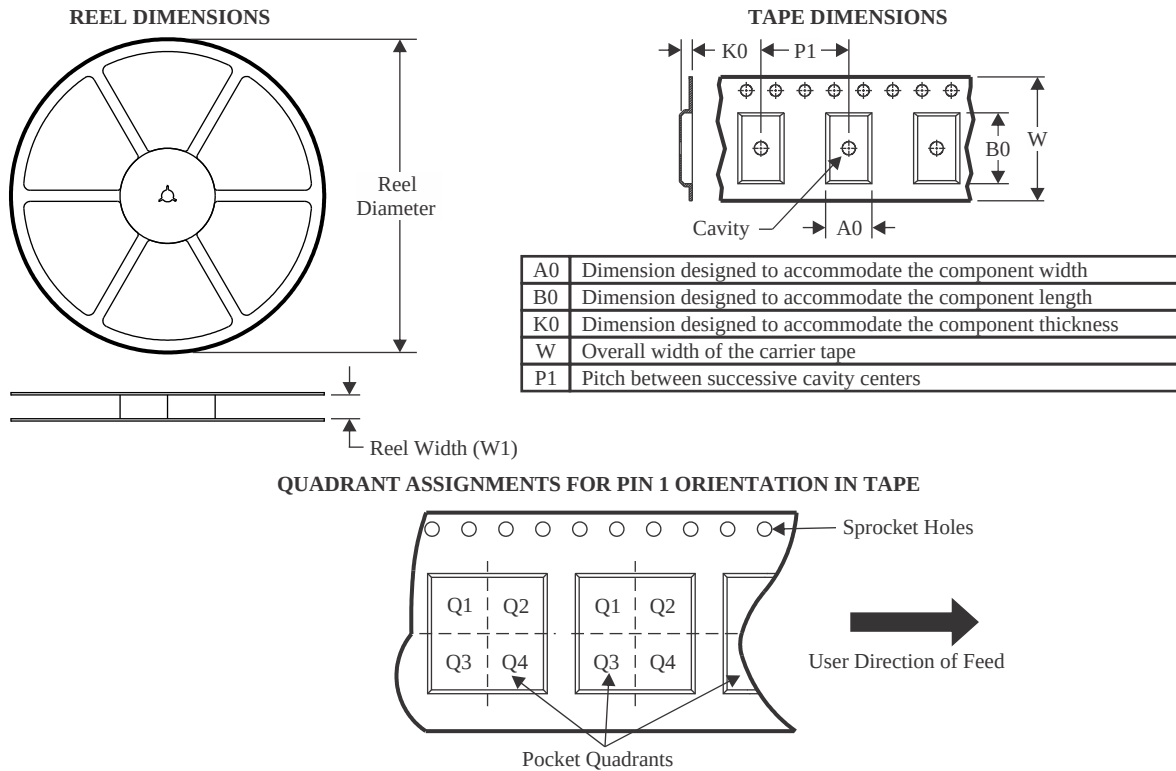
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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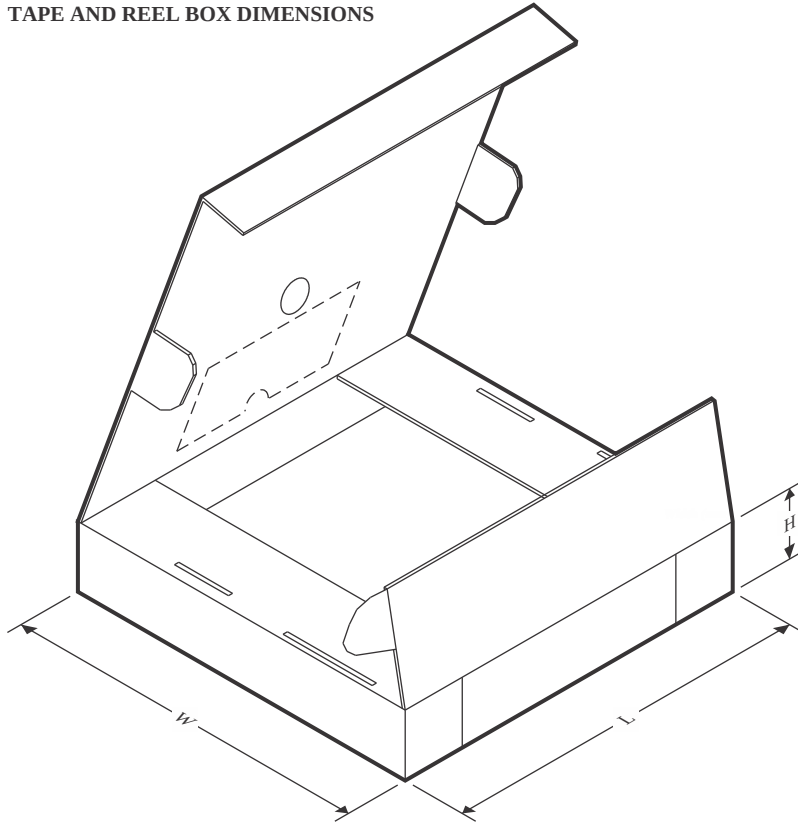
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS641A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS641A-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS641ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS641ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS642A-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

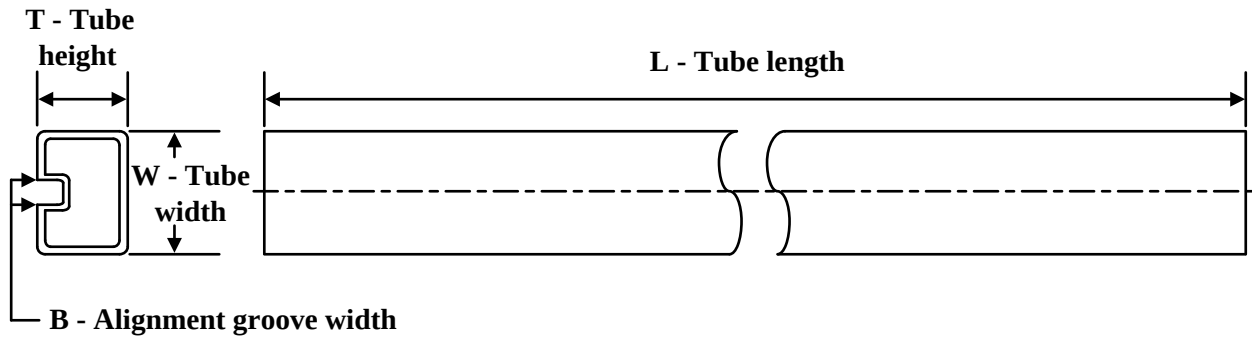
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS641A-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS641A-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS641ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS641ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS642A-1NSR	SO	NS	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

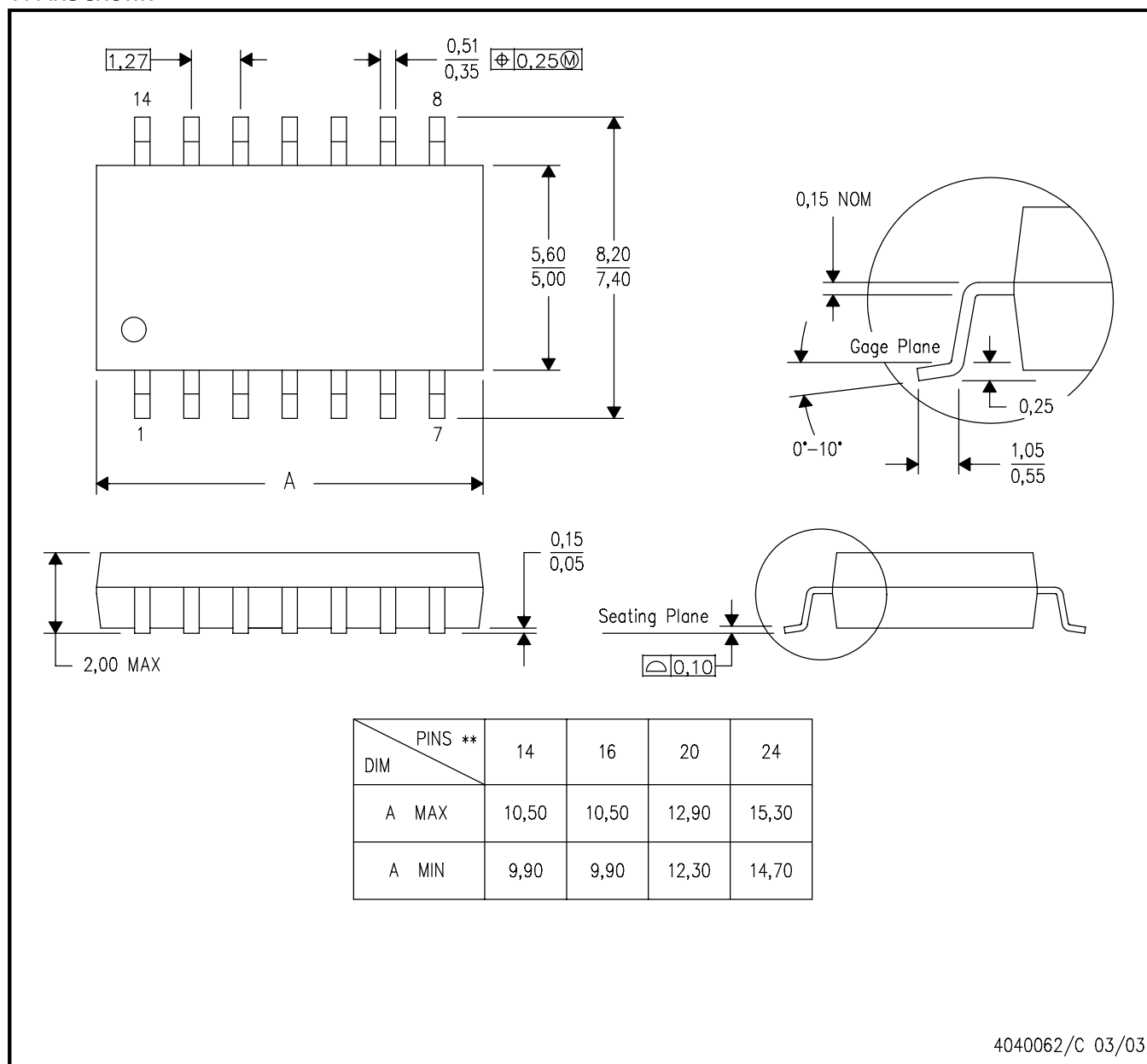
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS641A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS641AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS642A-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS642A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS641DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AS641N	N	PDIP	20	20	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

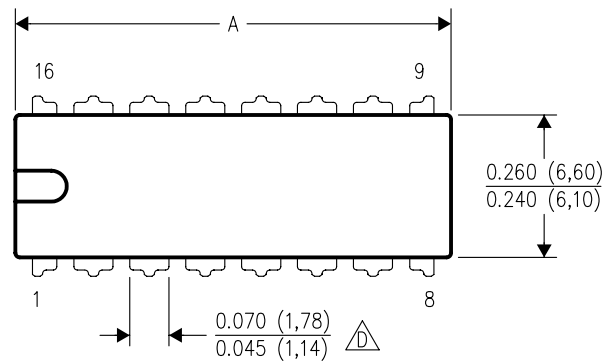


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

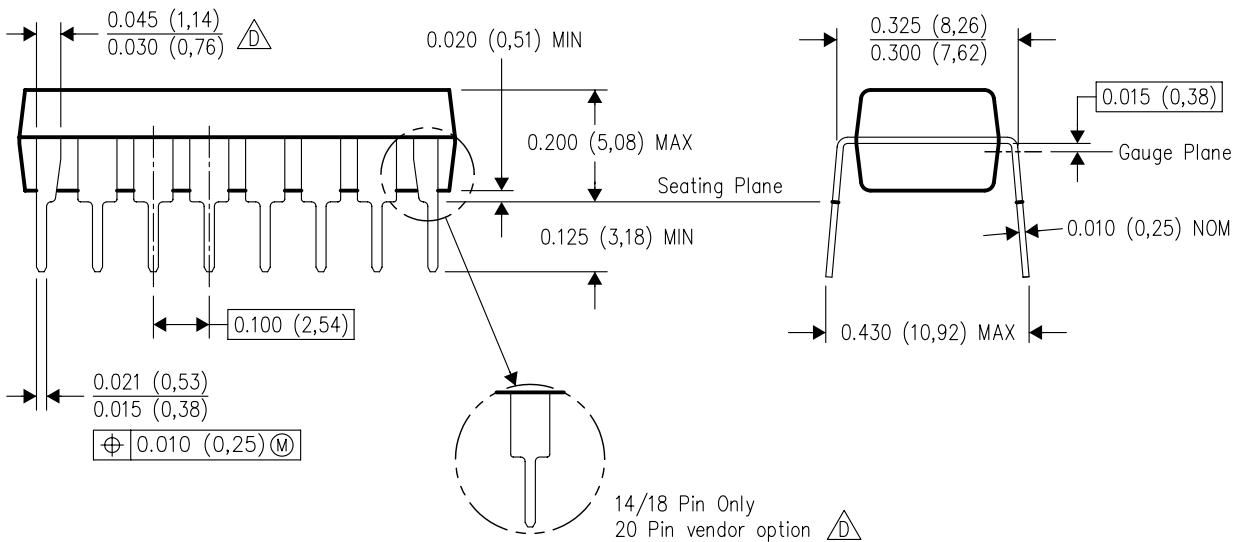
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



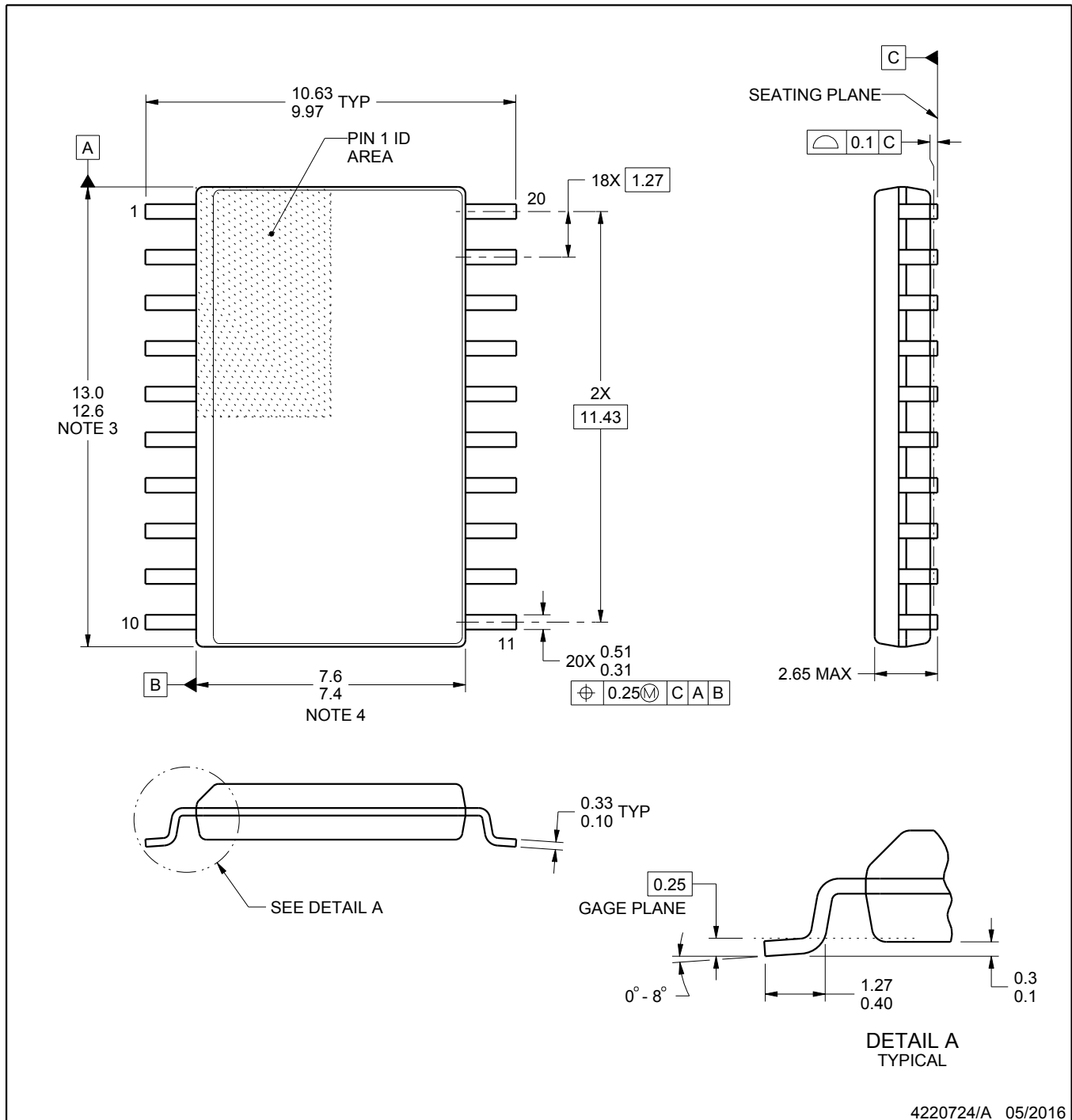
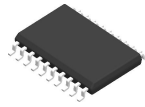
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

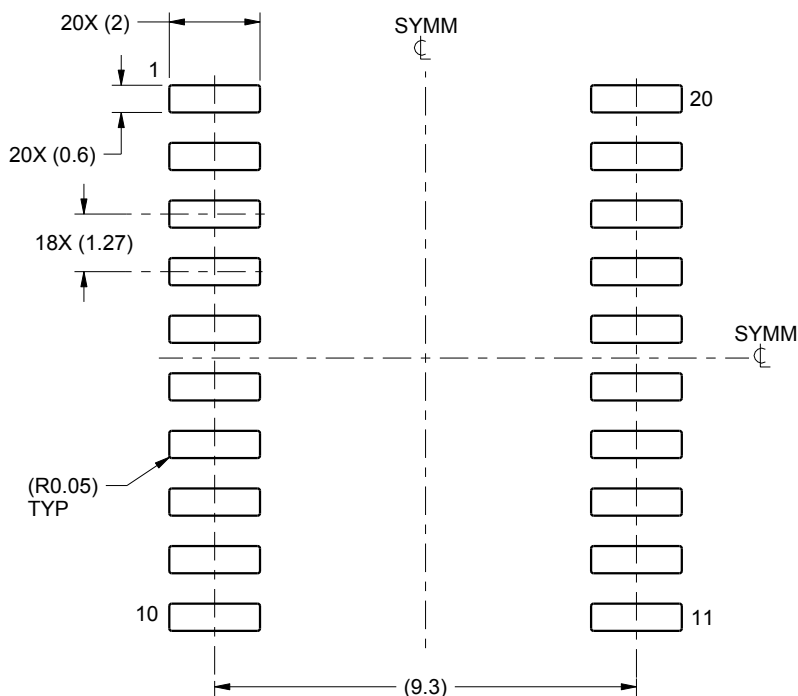
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

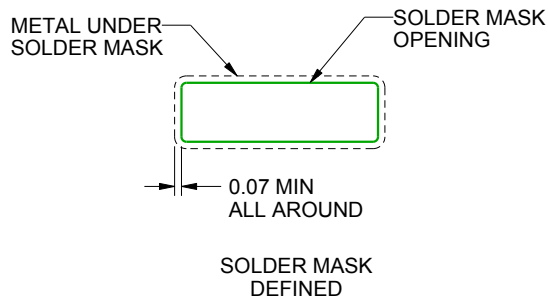
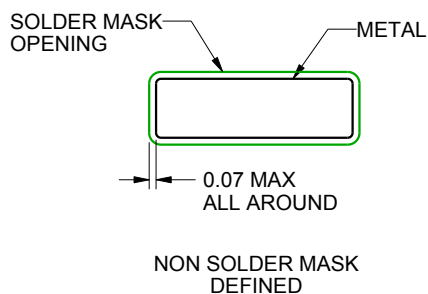
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

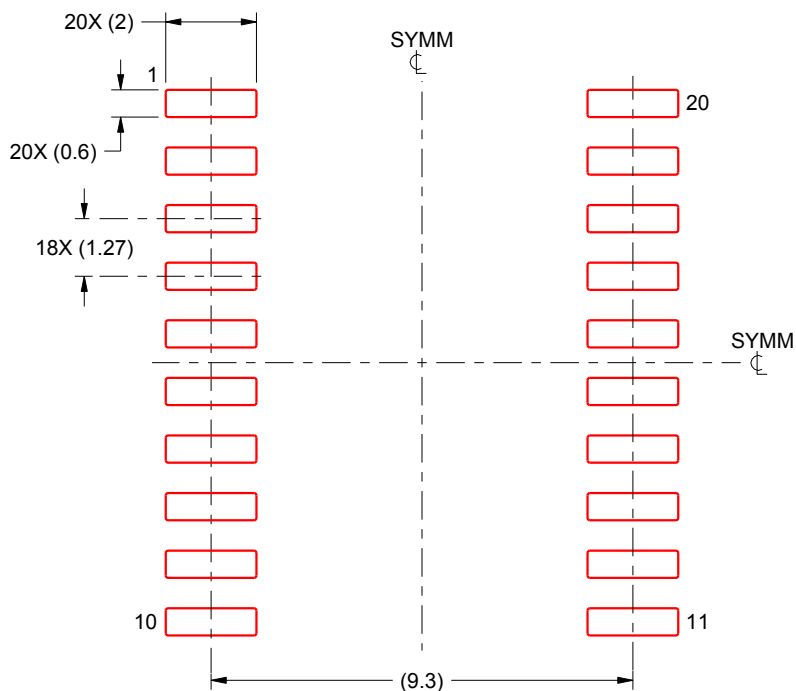
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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