



**THE DATASHEET OF  
SN74AUCH16244ZQLR**

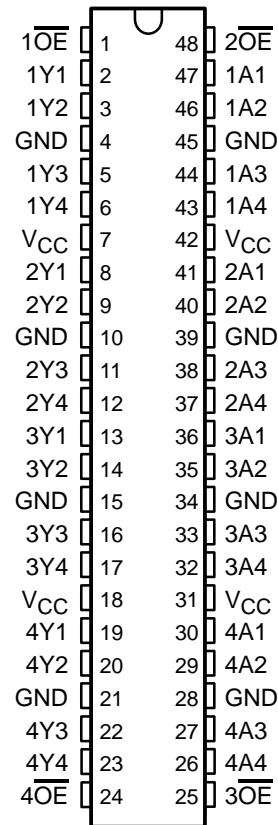


# SN74AUCH16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES391E – MARCH 2002 – REVISED DECEMBER 2002

- Member of the Texas Instruments Widebus™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max  $t_{pd}$  of 1.8 ns at 1.8 V
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE  
(TOP VIEW)



## description/ordering information

This 16-bit buffer/driver is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUCH16244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| TA            | PACKAGE†    |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
|               |             |               |                       |                  |
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74AUCH16244DGGR     | AUCH16244        |
|               | TVSOP – DGV | Tape and reel | SN74AUCH16244DGVR     | MJ244            |
|               | VFBGA – GQL | Tape and reel | SN74AUCH16244GQLR     | MJ244            |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74AUCH16244

## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

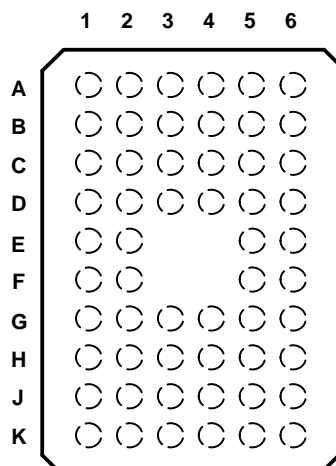
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#### description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**GQL PACKAGE**  
(TOP VIEW)



#### terminal assignments

|   | 1                | 2   | 3               | 4               | 5   | 6                |
|---|------------------|-----|-----------------|-----------------|-----|------------------|
| A | $\overline{1OE}$ | NC  | NC              | NC              | NC  | $\overline{2OE}$ |
| B | 1Y2              | 1Y1 | GND             | GND             | 1A1 | 1A2              |
| C | 1Y4              | 1Y3 | V <sub>CC</sub> | V <sub>CC</sub> | 1A3 | 1A4              |
| D | 2Y2              | 2Y1 | GND             | GND             | 2A1 | 2A2              |
| E | 2Y4              | 2Y3 |                 |                 | 2A3 | 2A4              |
| F | 3Y1              | 3Y2 |                 |                 | 3A2 | 3A1              |
| G | 3Y3              | 3Y4 | GND             | GND             | 3A4 | 3A3              |
| H | 4Y1              | 4Y2 | V <sub>CC</sub> | V <sub>CC</sub> | 4A2 | 4A1              |
| J | 4Y3              | 4Y4 | GND             | GND             | 4A4 | 4A3              |
| K | $\overline{4OE}$ | NC  | NC              | NC              | NC  | $\overline{3OE}$ |

NC – No internal connection

**FUNCTION TABLE**  
(each 4-bit buffer)

| INPUTS          |   | OUTPUT |
|-----------------|---|--------|
| $\overline{OE}$ | A | Y      |
| L               | H | H      |
| L               | L | L      |
| H               | X | Z      |



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**recommended operating conditions (see Note 3)**

|                 |                                    | MIN  | MAX                    | UNIT |
|-----------------|------------------------------------|--|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | 0.8  | 2.7                    | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 0.8 V                    | V <sub>CC</sub>        | V    |
|                 |                                    | V <sub>CC</sub> = 1.1 V to 1.95 V          | 0.65 × V <sub>CC</sub> |      |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V           | 1.7                    |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 0.8 V                    | 0                      | V    |
|                 |                                    | V <sub>CC</sub> = 1.1 V to 1.95 V          | 0.35 × V <sub>CC</sub> |      |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V           | 0.7                    |      |
| V <sub>I</sub>  | Input voltage                      | 0  | 3.6                    | V    |
| V <sub>O</sub>  | Output voltage                     | 0  | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 0.8 V                    | -0.7                   | mA   |
|                 |                                    | V <sub>CC</sub> = 1.1 V                    | -3                     |      |
|                 |                                    | V <sub>CC</sub> = 1.4 V                    | -5                     |      |
|                 |                                    | V <sub>CC</sub> = 1.65 V                   | -8                     |      |
|                 |                                    | V <sub>CC</sub> = 2.3 V                    | -9                     |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 0.8 V                    | 0.7                    | mA   |
|                 |                                    | V <sub>CC</sub> = 1.1 V                    | 3                      |      |
|                 |                                    | V <sub>CC</sub> = 1.4 V                    | 5                      |      |
|                 |                                    | V <sub>CC</sub> = 1.65 V                   | 8                      |      |
|                 |                                    | V <sub>CC</sub> = 2.3 V                    | 9                      |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 0.8 V                    | 20                     | ns/V |
|                 |                                    | V <sub>CC</sub> = 1.3 V                    | 15                     |      |
|                 |                                    | V <sub>CC</sub> = 1.6 V, 1.95 V, and 2.7 V | 10                     |      |
| T <sub>A</sub>  | Operating free-air temperature     | -40  | 85                     | °C   |

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74AUCH16244**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER           | TEST CONDITIONS  | V <sub>CC</sub> | MIN                  | TYP† | MAX  | UNIT |
|---------------------|--|-----------------|----------------------|------|------|------|
| V <sub>OH</sub>     | I <sub>OH</sub> = -100 μA  | 0.8 V to 2.7 V  | V <sub>CC</sub> -0.1 |      |      | V    |
|                     | I <sub>OH</sub> = -0.7 mA  | 0.8 V           | 0.55                 |      |      |      |
|                     | I <sub>OH</sub> = -3 mA  | 1.1 V           | 0.8                  |      |      |      |
|                     | I <sub>OH</sub> = -5 mA  | 1.4 V           | 1                    |      |      |      |
|                     | I <sub>OH</sub> = -8 mA  | 1.65 V          | 1.2                  |      |      |      |
|                     | I <sub>OH</sub> = -9 mA  | 2.3 V           | 1.8                  |      |      |      |
| V <sub>OL</sub>     | I <sub>OL</sub> = 100 μA   | 0.8 V to 2.7 V  |                      |      | 0.2  | V    |
|                     | I <sub>OL</sub> = 0.7 mA   | 0.8 V           | 0.25                 |      |      |      |
|                     | I <sub>OL</sub> = 3 mA   | 1.1 V           |                      |      | 0.3  |      |
|                     | I <sub>OL</sub> = 5 mA   | 1.4 V           |                      |      | 0.4  |      |
|                     | I <sub>OL</sub> = 8 mA   | 1.65 V          |                      |      | 0.45 |      |
|                     | I <sub>OL</sub> = 9 mA   | 2.3 V           |                      |      | 0.6  |      |
| I <sub>I</sub>      | A or $\overline{OE}$ inputs<br>V <sub>I</sub> = V <sub>CC</sub> or GND | 0 to 2.7 V      |                      |      | ±5   | μA   |
| I <sub>BHL</sub> ‡  | V <sub>I</sub> = 0.35 V  | 1.1 V           | 10                   |      |      | μA   |
|                     | V <sub>I</sub> = 0.47 V  | 1.4 V           | 15                   |      |      |      |
|                     | V <sub>I</sub> = 0.57 V  | 1.65 V          | 20                   |      |      |      |
|                     | V <sub>I</sub> = 0.7 V   | 2.3 V           | 40                   |      |      |      |
| I <sub>BHH</sub> §  | V <sub>I</sub> = 0.8 V   | 1.1 V           | -10                  |      |      | μA   |
|                     | V <sub>I</sub> = 0.9 V   | 1.4 V           | -15                  |      |      |      |
|                     | V <sub>I</sub> = 1.07 V  | 1.65 V          | -20                  |      |      |      |
|                     | V <sub>I</sub> = 1.7 V   | 2.3 V           | -40                  |      |      |      |
| I <sub>BHLO</sub> ¶ | V <sub>I</sub> = 0 to V <sub>CC</sub>                                  | 1.3 V           | 75                   |      |      | μA   |
|                     |  | 1.6 V           | 125                  |      |      |      |
|                     |  | 1.95 V          | 175                  |      |      |      |
|                     |  | 2.7 V           | 275                  |      |      |      |
| I <sub>BHHO</sub> # | V <sub>I</sub> = 0 to V <sub>CC</sub>                                  | 1.3 V           | -75                  |      |      | μA   |
|                     |  | 1.6 V           | -125                 |      |      |      |
|                     |  | 1.95 V          | -175                 |      |      |      |
|                     |  | 2.7 V           | -275                 |      |      |      |
| I <sub>off</sub>    | V <sub>I</sub> or V <sub>O</sub> = 2.7 V                               | 0               |                      |      | ±10  | μA   |
| I <sub>OZ</sub>     | V <sub>O</sub> = V <sub>CC</sub> or GND                                | 2.7 V           |                      |      | ±10  | μA   |
| I <sub>CC</sub>     | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0            | 0.8 V to 2.7 V  |                      |      | 20   | μA   |
| C <sub>i</sub>      | V <sub>I</sub> = V <sub>CC</sub> or GND                                | 2.5 V           | 3                    |      | 4.5  | pF   |
| C <sub>o</sub>      | V <sub>O</sub> = V <sub>CC</sub> or GND                                | 2.5 V           | 4                    |      | 7    | pF   |

† All typical values are at T<sub>A</sub> = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

¶ An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

# An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

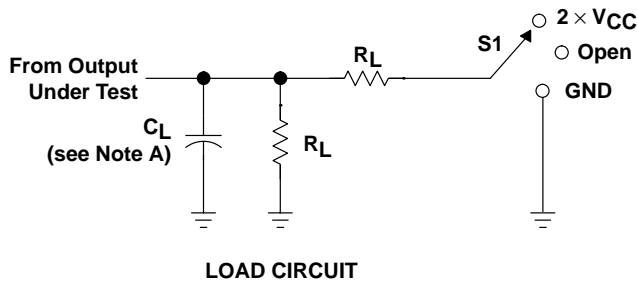
| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> = 0.8 V | V <sub>CC</sub> = 1.2 V ± 0.1 V |     | V <sub>CC</sub> = 1.5 V ± 0.1 V |     | V <sub>CC</sub> = 1.8 V ± 0.15 V |     |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | UNIT |
|------------------|-----------------|-------------|-------------------------|---------------------------------|-----|---------------------------------|-----|----------------------------------|-----|-----|---------------------------------|-----|------|
|                  |                 |             | TYP                     | MIN                             | MAX | MIN                             | MAX | MIN                              | TYP | MAX | MIN                             | MAX |      |
| t <sub>pd</sub>  | A               | Y           | 5.4                     | 0.8                             | 2.8 | 0.6                             | 1.9 | 0.7                              | 1.3 | 1.8 | 0.5                             | 1.8 | ns   |
| t <sub>en</sub>  | $\overline{OE}$ | Y           | 8                       | 1                               | 4.4 | 0.7                             | 2.6 | 0.8                              | 1.4 | 2.5 | 0.6                             | 1.9 | ns   |
| t <sub>dis</sub> | $\overline{OE}$ | Y           | 12                      | 1.9                             | 4.9 | 1                               | 4.6 | 1.5                              | 2.6 | 4   | 0.5                             | 2   | ns   |

operating characteristics, T<sub>A</sub> = 25°C

| PARAMETER       |                   | TEST CONDITIONS | V <sub>CC</sub> = 0.8 V | V <sub>CC</sub> = 1.2 V | V <sub>CC</sub> = 1.5 V | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | UNIT |
|-----------------|-------------------|-----------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
|                 |                   |                 | TYP                     | TYP                     | TYP                     | TYP                     | TYP                     |      |
| C <sub>pd</sub> | Power dissipation | f = 10 MHz      | 21                      | 22                      | 23                      | 25                      | 30                      | pF   |
|                 | capacitance       |                 | 1                       | 1                       | 1                       | 1                       | 1                       |      |

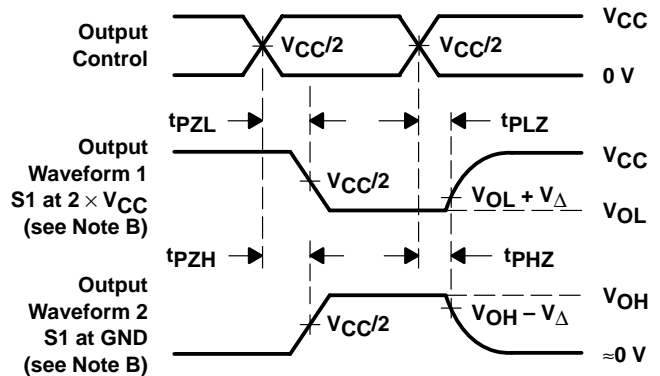
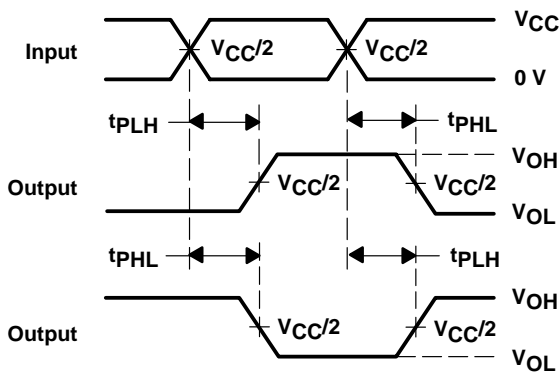
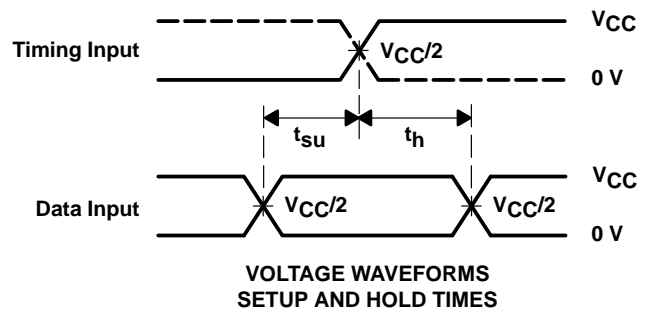
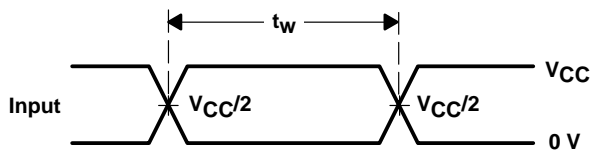


PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$           | $C_L$ | $R_L$        | $V_{\Delta}$ |
|--------------------|-------|--------------|--------------|
| 0.8 V              | 15 pF | 2 k $\Omega$ | 0.1 V        |
| 1.2 V $\pm$ 0.1 V  | 15 pF | 2 k $\Omega$ | 0.1 V        |
| 1.5 V $\pm$ 0.1 V  | 15 pF | 2 k $\Omega$ | 0.1 V        |
| 1.8 V $\pm$ 0.15 V | 30 pF | 1 k $\Omega$ | 0.15 V       |
| 2.5 V $\pm$ 0.2 V  | 30 pF | 500 $\Omega$ | 0.15 V       |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUCH16244DGGR | ACTIVE        | TSSOP        | DGG             | 48   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AUCH16244               | <a href="#">Samples</a> |
| SN74AUCH16244DGVR | ACTIVE        | TVSOP        | DGV             | 48   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | MJ244                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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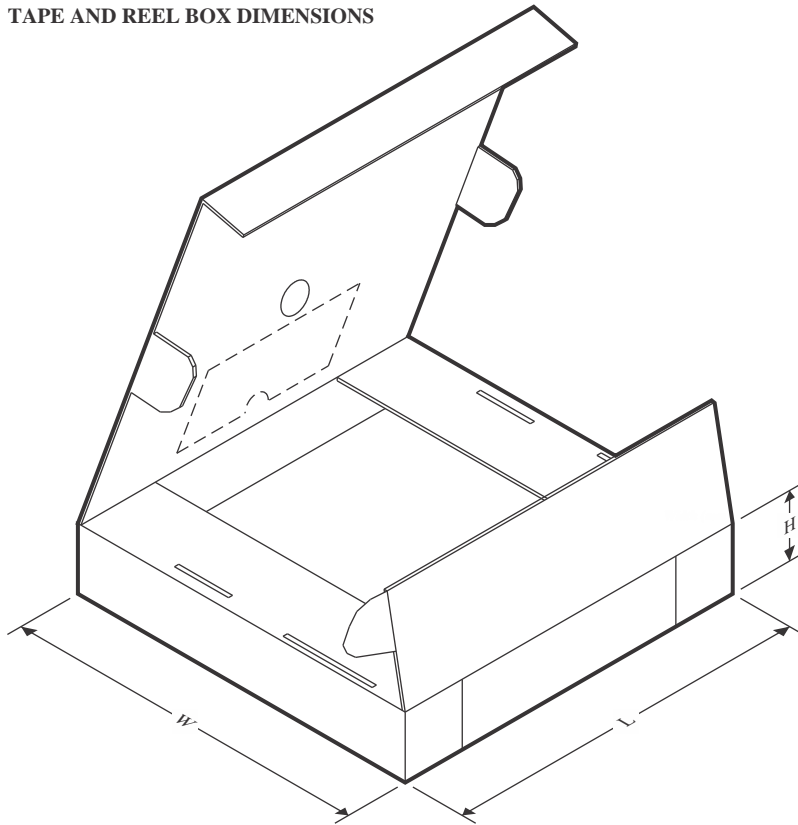


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUCH16244DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74AUCH16244DGVR | TVSOP        | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUCH16244DGGR | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74AUCH16244DGVR | TVSOP        | DGV             | 48   | 2000 | 356.0       | 356.0      | 35.0        |

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

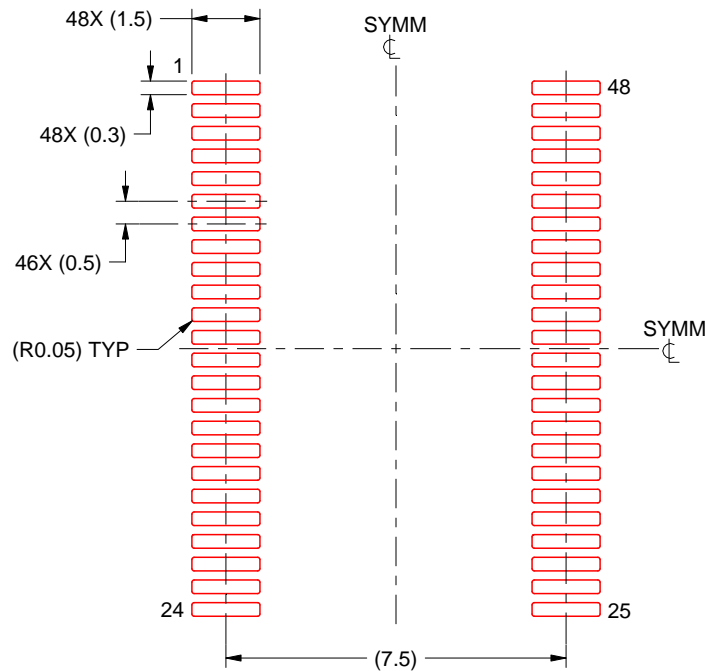
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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