



**THE DATASHEET OF  
SN74LVT245BZQNR**



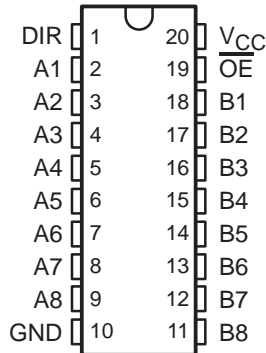
# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

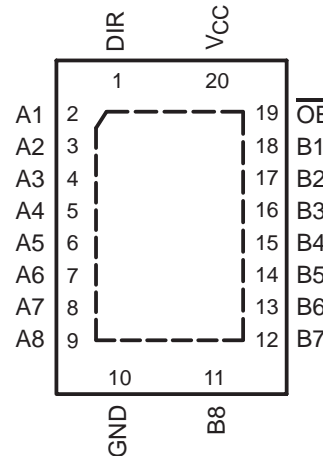
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- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



### description/ordering information

This octal bus transceiver is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT245B is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LVT245BRGYR	LX245B
	SOIC – DW	Tube	SN74LVT245BDW	LVT245B
		Tape and reel	SN74LVT245BDWR	
	SOP – NS	Tape and reel	SN74LVT245BNSR	LVT245B
	SSOP – DB	Tape and reel	SN74LVT245BDBR	LX245B
	TSSOP – PW	Tube	SN74LVT245BPW	LX245B
		Tape and reel	SN74LVT245BPWR	
	VFBGA – GQN	Tape and reel	SN74LVT245BGQNR	LX245B
VFBGA – ZQN (Pb-free)	SN74LVT245BZQNR			

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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**TEXAS  
INSTRUMENTS**

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# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

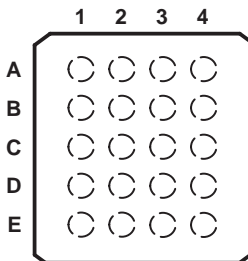
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### description/ordering information (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQN OR ZQN PACKAGE  
(TOP VIEW)



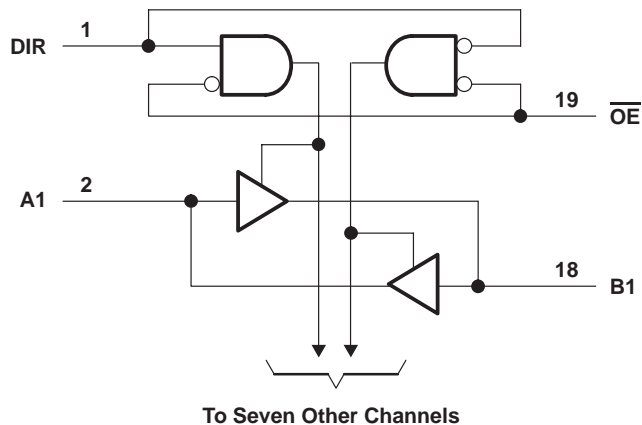
terminal assignments

	1	2	3	4
A	A1	DIR	$V_{CC}$	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### logic diagram (positive logic)



Pin numbers shown are for the DB, DW, NS, PW, and RGY packages.

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## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_{OL}$ .....	128 mA
Current into any output in the high state, $I_{OH}$ (see Note 2) .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): GQN/ZQN package .....	78°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 5)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		5.5	V
$I_{OH}$	High-level output current		–32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
	Outputs enabled			
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		$\mu$ s/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 2.7 V to 3.6 V,	I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.2			V
		V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA	2.4			
		V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA	2			
V <sub>OL</sub>		V <sub>CC</sub> = 2.7 V		I <sub>OL</sub> = 100 μA		0.2	V
				I <sub>OL</sub> = 24 mA		0.5	
		V <sub>CC</sub> = 3 V		I <sub>OL</sub> = 16 mA		0.4	
				I <sub>OL</sub> = 32 mA		0.5	
				I <sub>OL</sub> = 64 mA		0.55	
I <sub>I</sub>		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1	μA
				V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V			
		V <sub>CC</sub> = 3.6 V				V <sub>I</sub> = 5.5 V	
				V <sub>I</sub> = V <sub>CC</sub>		1	
				V <sub>I</sub> = 0		-5	
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V				±100	μA
I <sub>OZH</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V				5	μA
I <sub>OZL</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V				-5	μA
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100	μA
I <sub>OZPD</sub>		V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100	μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs high		0.19	mA
				Outputs low		5	
				Outputs disabled		0.19	
ΔI <sub>CC</sub> §		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2	mA
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0				4	pF
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0				9	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ Unused terminals are at V<sub>CC</sub> or GND.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V<sub>CC</sub> or GND.

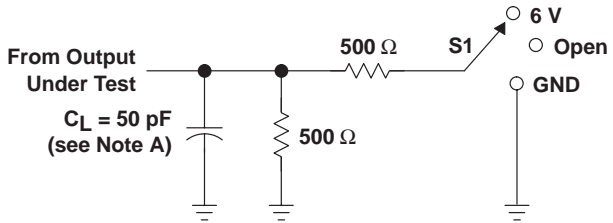
switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1.2	2.3	3.5	4		ns
t <sub>PHL</sub>			1.2	2.1	3.5	4		
t <sub>PZH</sub>	$\overline{OE}$	A or B	1.3	3.2	5.5	7.1		ns
t <sub>PZL</sub>			1.7	3.4	5.5	6.5		
t <sub>PHZ</sub>	$\overline{OE}$	A or B	2.2	3.5	5.9	6.5		ns
t <sub>PLZ</sub>			2.2	3.4	5	5.1		

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

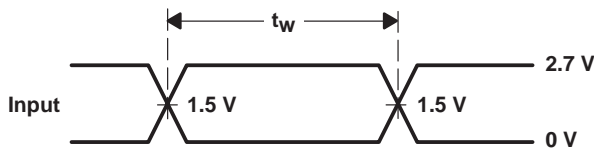


**PARAMETER MEASUREMENT INFORMATION**

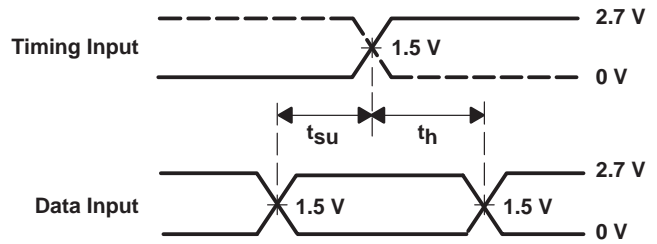


**LOAD CIRCUIT**

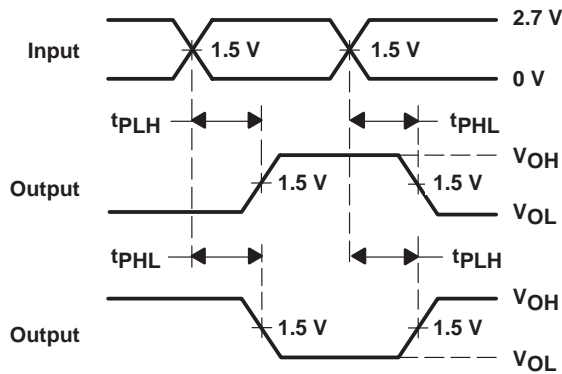
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



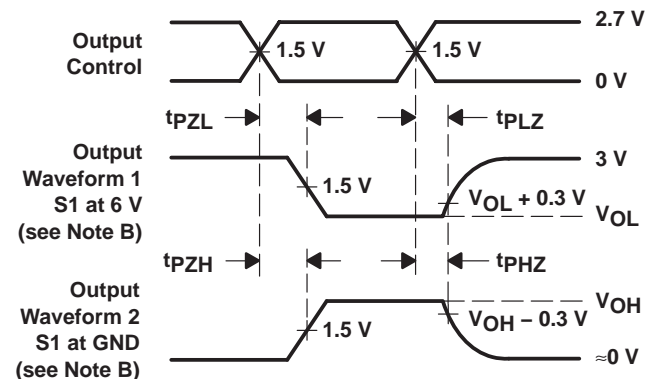
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



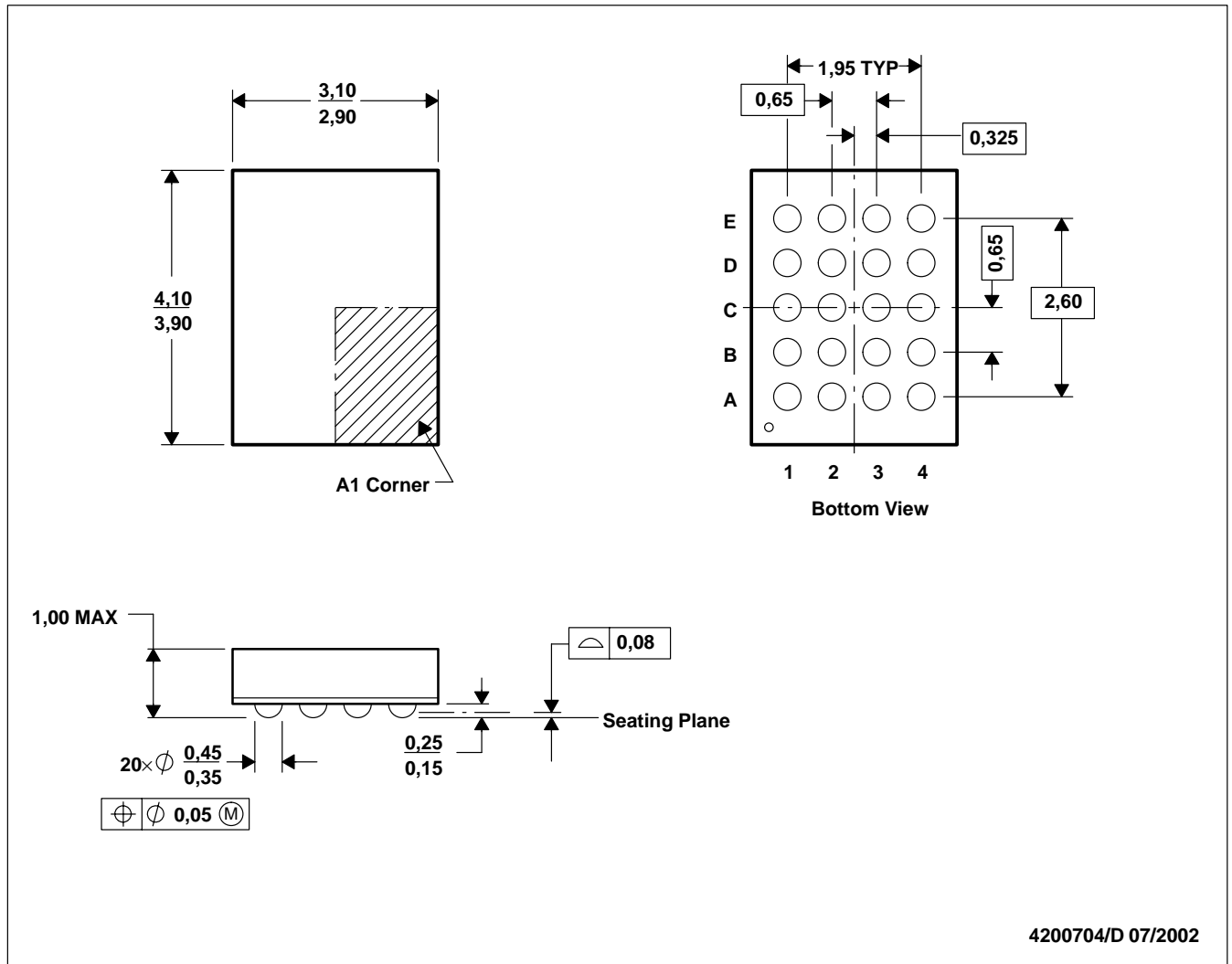
**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



4200704/D 07/2002

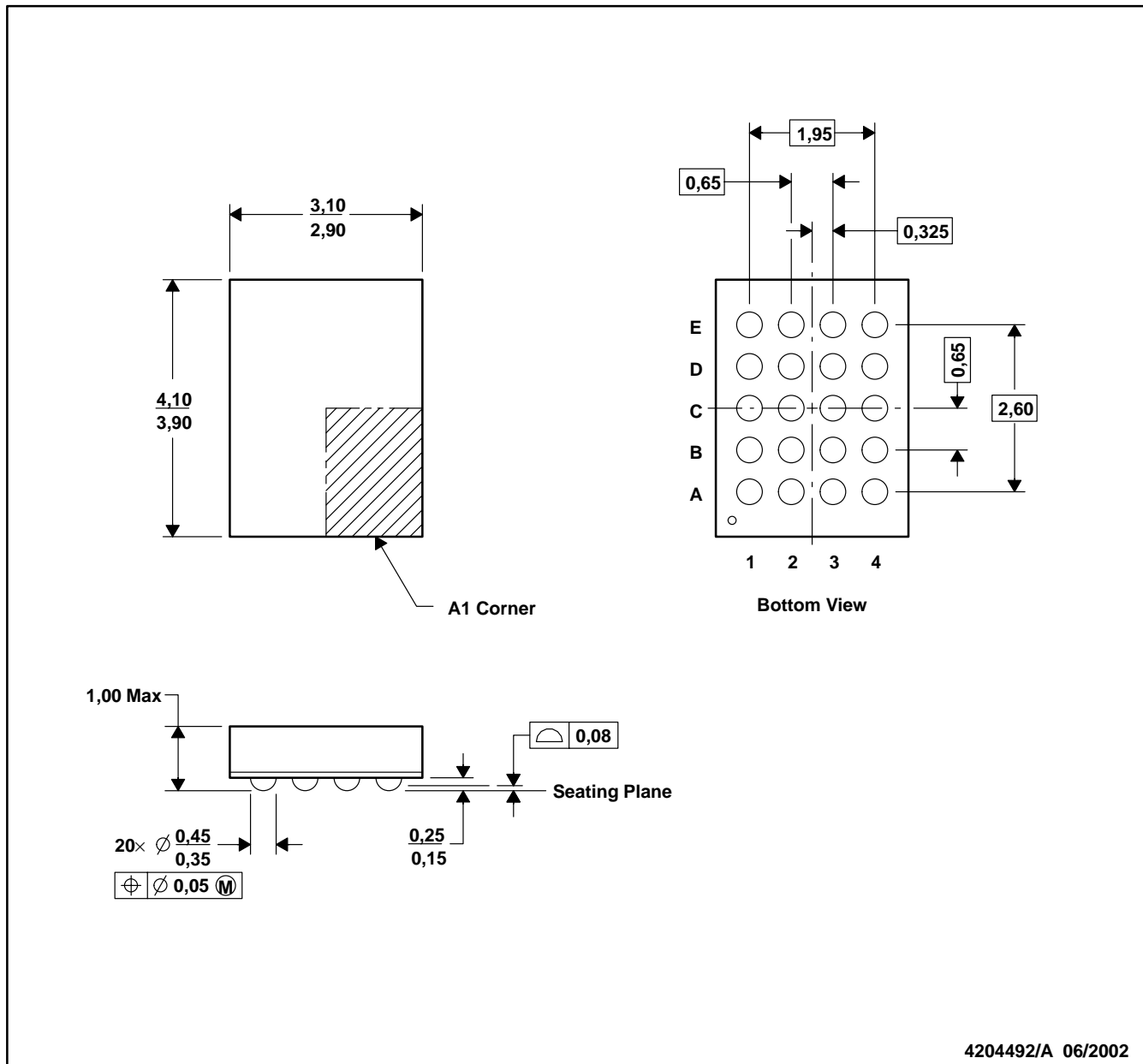
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. MicroStar Junior™ configuration
  - D. Falls within JEDEC MO-225 variation BC.
  - E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.



ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



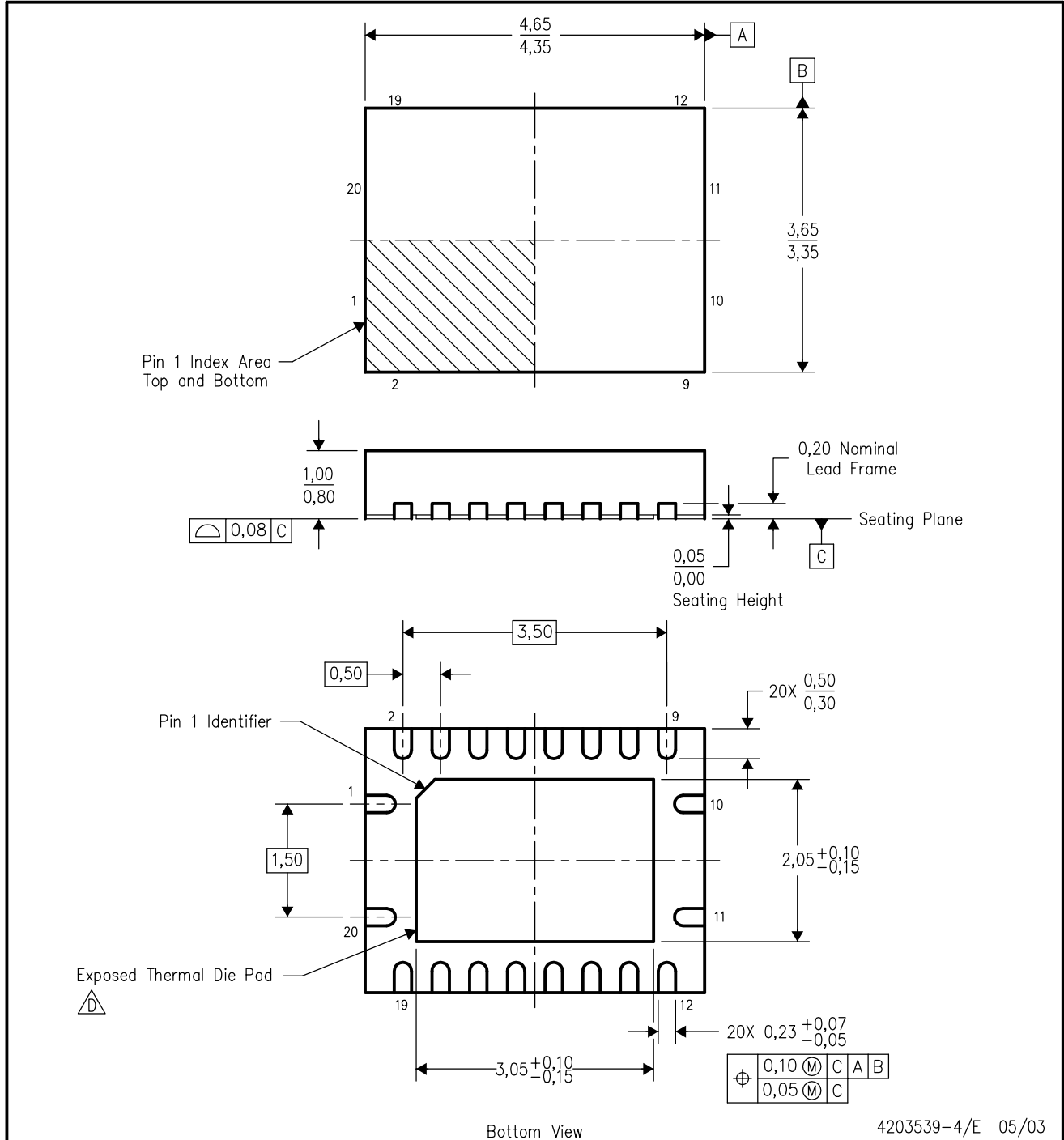
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. MicroStar Junior™ configuration.
  - D. Fall within JEDEC MO-225 variation BC.
  - E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).


MicroStar Junior is a trademark of Texas Instruments.



RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK

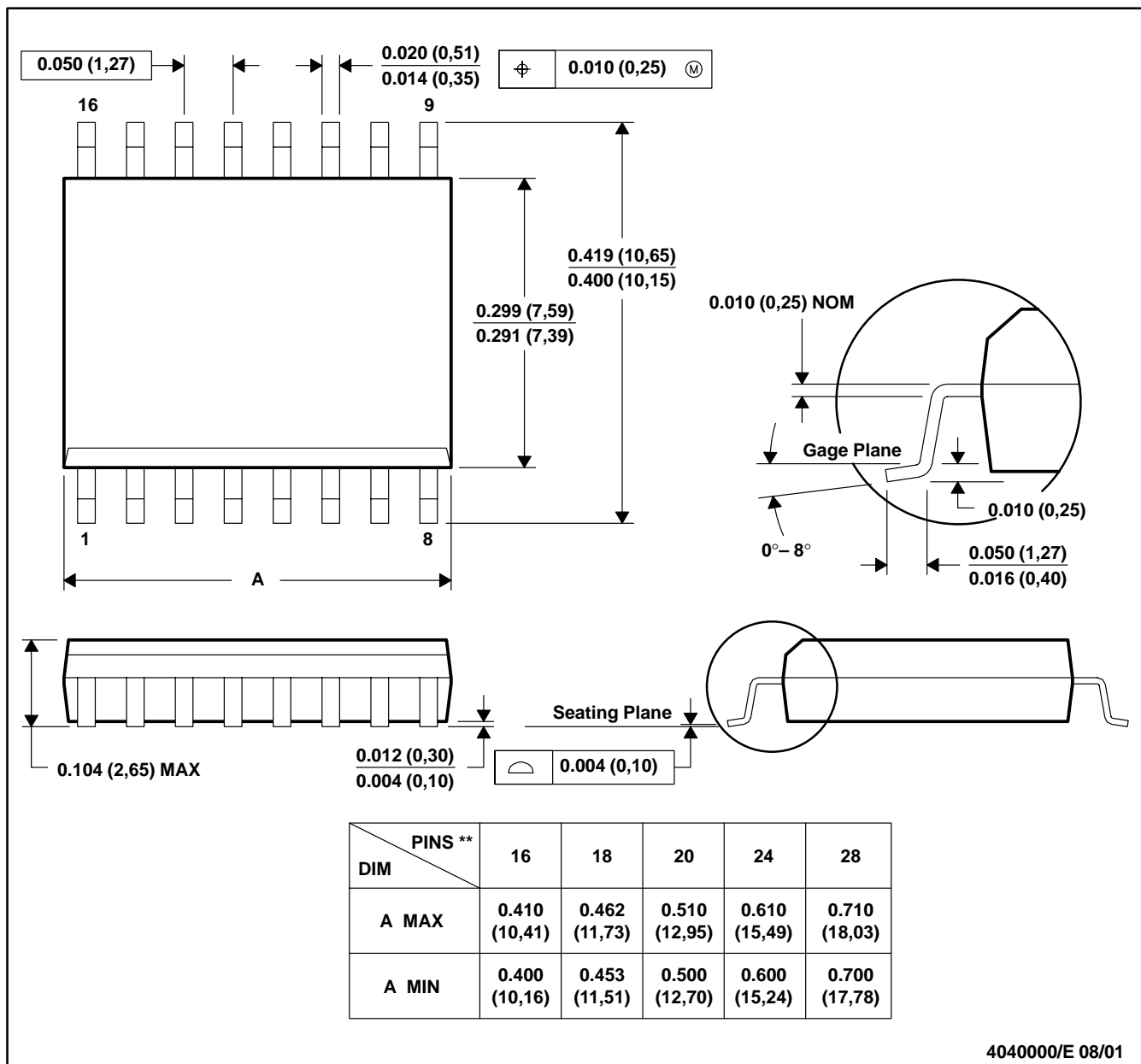


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

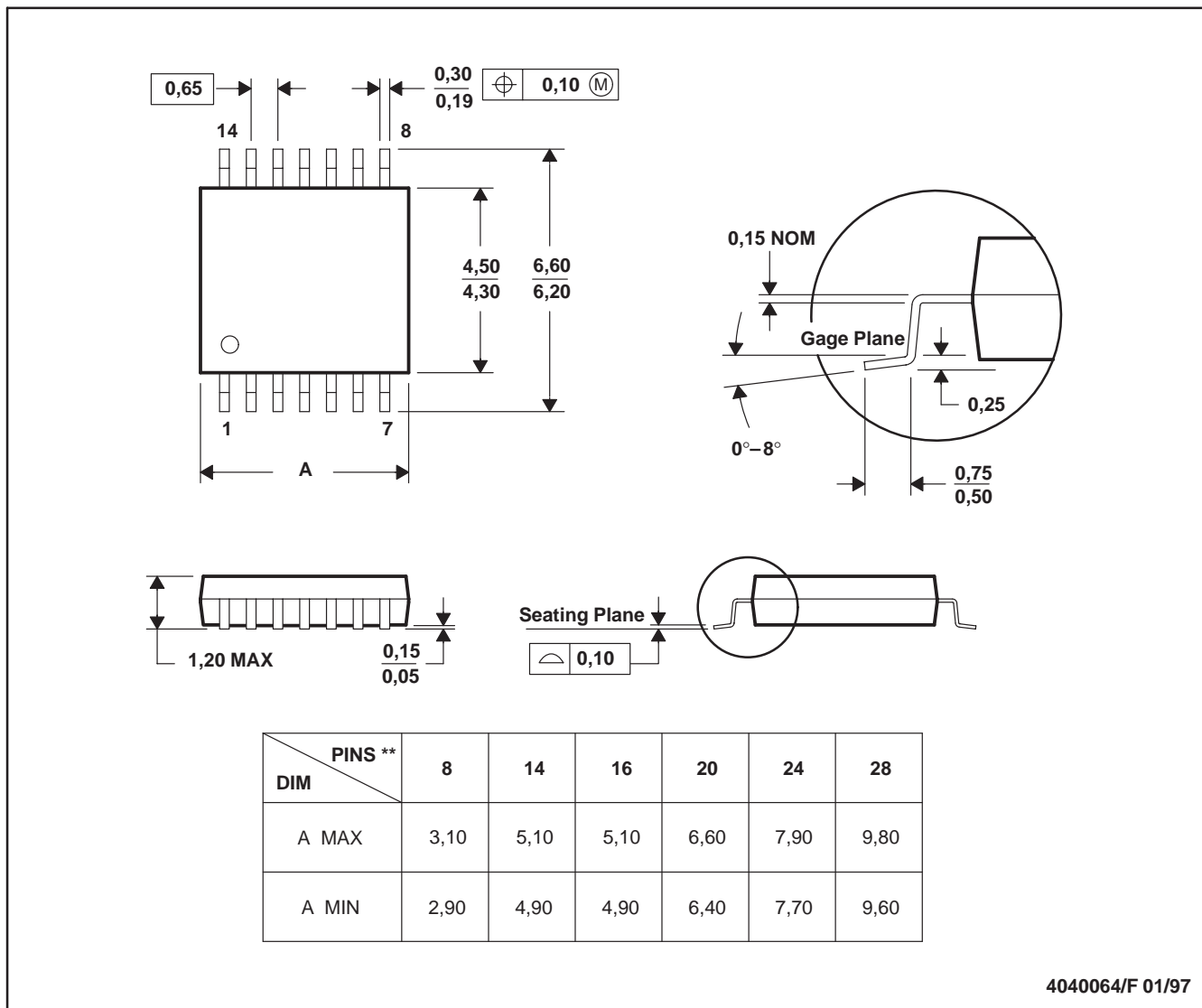


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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