



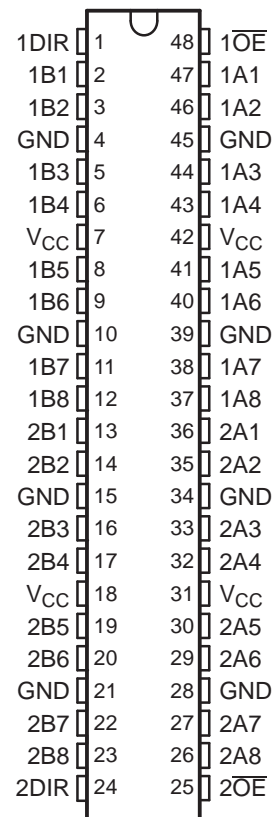
**THE DATASHEET OF
SN74LVT162245AGRDR**



FEATURES

- Members of the Texas Instruments Widebus™ Family
- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVT162245A . . . WD PACKAGE
SN74LVT162245A . . . DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVT162245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

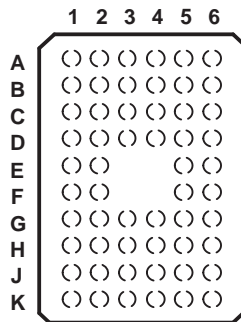
ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT162245AGRDR	LZ245A
	FBGA – ZRD (Pb-free)		SN74LVT162245AZRDR	
	SSOP – DL	Tube of 25	SN74LVT162245ADL	LVT162245A
			SN74LVT162245ADLG4	
		Reel of 1000	SN74LVT162245ADLR	
	74LVT162245ADLRG4			
	TSSOP – DGG	Reel of 2000	SN74LVT162245ADGGR	LVT162245A
		74LVT162245ADGGRE4		
-55°C to 125°C	VFBGA – GQL	Reel of 1000	SN74LVT162245AGQLR	LZ245A
	VFBGA – ZQL (Pb-free)		SN74LVT162245AZQLR	
	CFP – WD	Tube	SNJ54LVT162245AWD ⁽²⁾	SNJ54LVT162245AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) Product preview

GQL OR ZQL PACKAGE (TOP VIEW)

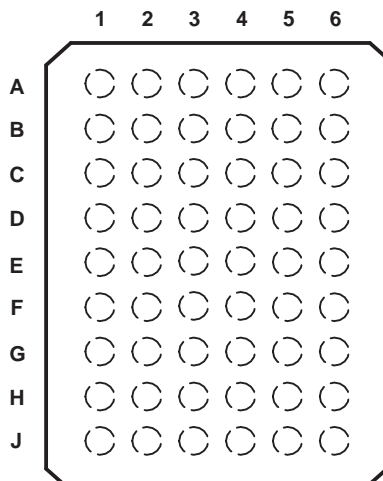


TERMINAL ASSIGNMENTS⁽¹⁾ (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1OE
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V _{CC}	V _{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V _{CC}	V _{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

(1) NC – No internal connection

GRD OR ZRD PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾ (54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
A	1B1	NC	1DIR	1OE	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V _{CC}	V _{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V _{CC}	V _{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2OE	NC	2A8

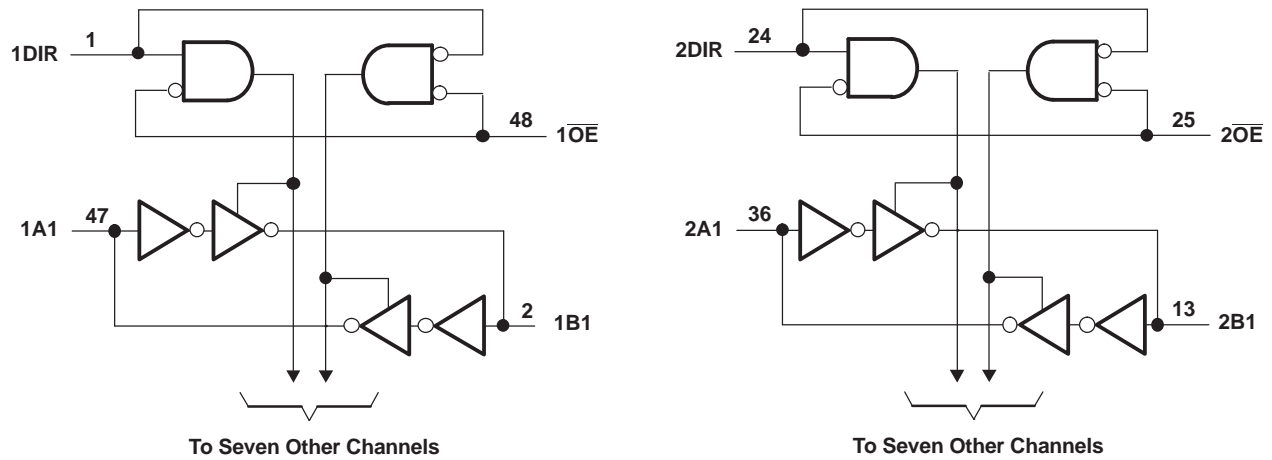
(1) NC – No internal connection

FUNCTION TABLE⁽¹⁾
(EACH 8-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
\overline{OE}	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high state ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _O	Current into any output in the low state	SN54LVT162245A (B port)	96	mA
		SN74LVT162245A (B port)	128	
		A port	30	
I _O	Current into any output in the high state ⁽³⁾	SN54LVT162245A (B port)	48	mA
		SN74LVT162245A (B port)	64	
		A port	30	
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and V_O > V_{CC}.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		SN54LVT162245A ⁽²⁾		SN74LVT162245A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current	A port	-12		-12	mA
		B port		-24		
I _{OL}	Low-level output current	A port		12		mA
		B port		48		
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CC1} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Product preview

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162245A ⁽¹⁾			UNIT	
			MIN	TYP ⁽²⁾	MAX		MIN
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			V	
V_{OH}	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$			V	
		$V_{CC} = 3\text{ V}$, $I_{OH} = -12\text{ mA}$	2				
	B port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$				
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4				
$V_{CC} = 3\text{ V}$		$I_{OH} = -24\text{ mA}$	2				
		$I_{OH} = -32\text{ mA}$					
V_{OL}	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$	0.2			V	
		$V_{CC} = 3\text{ V}$, $I_{OL} = 12\text{ mA}$	0.8				
	B port	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.2			
			$I_{OL} = 24\text{ mA}$	0.5			
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4			
			$I_{OL} = 32\text{ mA}$	0.5			
			$I_{OL} = 48\text{ mA}$	0.55			
		$I_{OL} = 64\text{ mA}$	0.55				
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	± 1			μA	
		$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$	10				
	A or B port ⁽³⁾	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$	20				
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$	5				
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$	-10				
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100		
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^{(4)}$			± 100		
I_{OZPD}	$V_{CC} = 1.5\text{ to }0\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^{(4)}$			± 100		
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19			mA	
		Outputs low	5				
		Outputs disabled	0.19				
$\Delta I_{CC}^{(5)}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	0.3			0.2		
C_i	$V_I = 3\text{ V or }0$	4			pF		
C_{io}	$V_O = 3\text{ V or }0$	10			pF		

(1) Product preview

 (2) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

 (3) Unused pins at $V_{CC}\text{ or GND}$

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

 (5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714D—FEBRUARY 2000—REVISED NOVEMBER 2006

Switching Characteristics

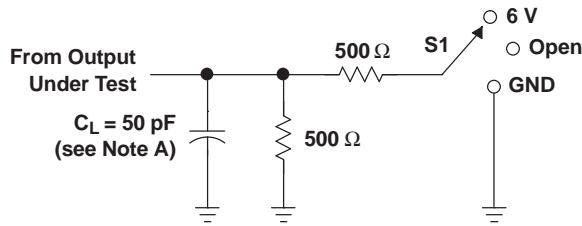
over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162245A ⁽¹⁾				SN74LVT162245A				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP ⁽²⁾	MAX	MIN		MAX
t_{PLH}	A	B	1	3.5	4		1	2.3	3.3	3.7		ns
t_{PHL}			1	3.5	3.9		1	2.2	3.3	3.5		
t_{PLH}	B	A	1	4.3	5.3		1	2.8	4	4.6		ns
t_{PHL}			1	4.2	4.5		1	2.5	3.4	3.6		
t_{PZH}	\overline{OE}	B	1	4.8	5.9		1	2.8	4.6	5.4		ns
t_{PZL}			1	4.8	5.5		1	3	4.6	5.2		
t_{PZH}	\overline{OE}	A	1	5.5	7.2		1	3.3	5.3	6.3		ns
t_{PZL}			1	5.4	6.4		1	3.3	5.1	5.8		
t_{PHZ}	\overline{OE}	B	1.5	5.5	5.8		1.5	3.8	5.2	5.5		ns
t_{PLZ}			1.5	5.5	5.8		1.5	3.5	5.1	5.4		
t_{PHZ}	\overline{OE}	A	1.5	5.8	6.5		1.5	4	5.6	5.9		ns
t_{PLZ}			1.2	6.3	6.3		1.5	3.8	5.5	5.5		
$t_{sk(LH)}$									0.5		ns	
$t_{sk(HL)}$									0.5			

(1) Product preview

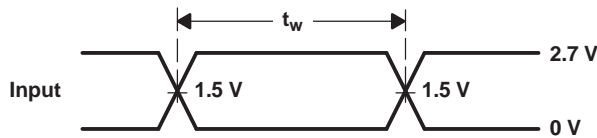
(2) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

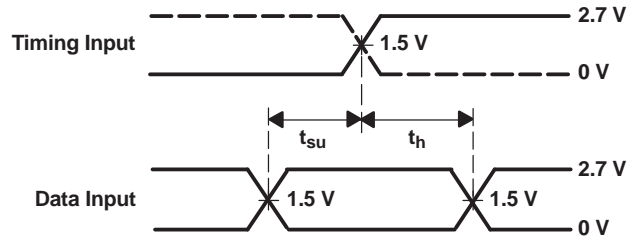


LOAD CIRCUIT

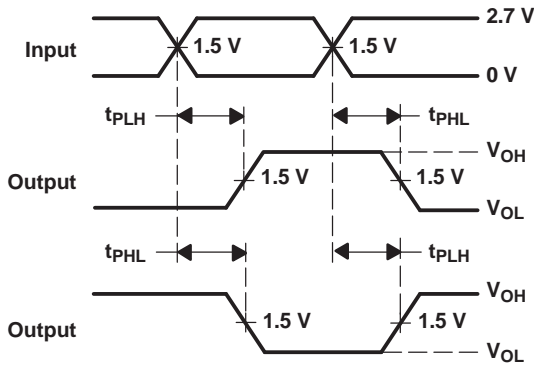
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



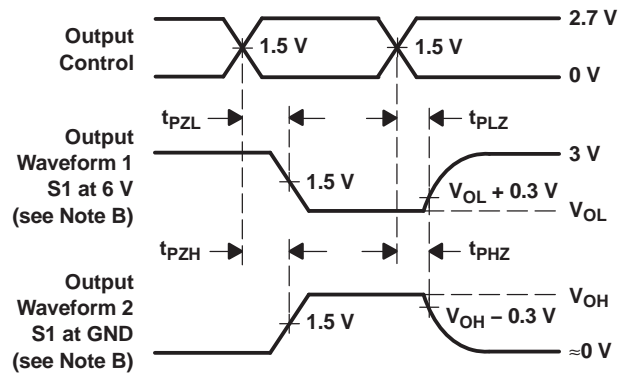
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVT162245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A	Samples
SN74LVT162245ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A	Samples
SN74LVT162245ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162245A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

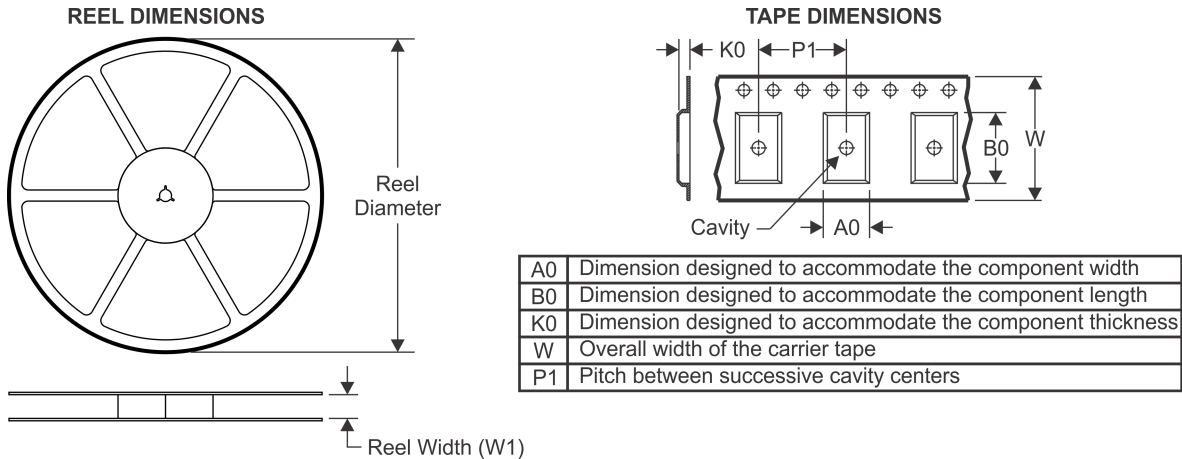
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVT162245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT162245ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVT162245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LVT162245AGRDR on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management